Working Draft

X3T10 2008D

Revision 3
July 26, 1995

Information Technology - AT Attachment-3 Interface (ATA-3)

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Reference number
ISO/IEC ***** : 199x
ANSI X3.*** - 199x
Printed April, 28, 1998 6:53AM

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ATA Anonymous FTP Site
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ATA directory is: "/pub/standards/ata3/ata"

X3T10 Bulletin Board
719-574-0424

Document Distribution
Global Engineering
15 Inverness Way East
Englewood, CO 80112-5704
Tel: 303-792-2181 or 800-854-7179
Fax: 303-792-2192

ABSTRACT

This standard specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers, and suppliers of intelligent storage devices.

This standard maintains a high degree of compatibility with the AT Attachment Interface with Extensions standard (ATA-2), X3.279-199x, which it replaces, and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

PATENT STATEMENT

CAUTION: The developers of this standard have requested that holder's of patents that may be required for the implementation of the standard, disclose such patents to the publisher. However, neither the developers nor the publisher have undertaken a patent search in order to identify which, if any, patents may apply to this standard.

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DOCUMENT STATUS

Revision 0 - 28 February 1995

Initial document. Created from X3T10/948D Revision 2k, the proposed AT Attachment Interface with Extensions (ATA-2) standard, and the following proposed additions:

X3T10/94-053r3	Reset Pulse Duration
X3T10/94-087r3	Security Mode
X3T10/94-154r1	Check Power Mode Enhancement
X3T10/95-144r0	Identify Device DMA
X3T10/95-145r0	Device 1 Only

It is the intent of the editor that any changes that may be made to X3T10/948D by the X3T10 be implemented in this document as well. In addition, the editor has taken the liberty to make improvements as deemed necessary, understanding that the entire document is subject to review and change.

Revision 1 - 21 April 1995

Added changes made to X3T10/948D Revision 3 as a result of letter ballot. Rewrote Abstract, Introduction and Scope. Added the proposals approved at the April 12-13, 1995 meeting as follows:

X3T10/95-125r2	Dynamic Power Selection
X3T10/95-155r0	Delete DASP timing clause 10.6
X3T10/95-198r0	DRDY max set time 30 sec
X3T10/95-198r0	Paragraph merge in READ MULTIPLE command
X3T10/95-199r0	Modify driver current

Revision 2 - 2 June 1995

Added proposal X3T10/95-154r1 and 10K pulldown to DD7 as approved at the 11 May 1995 meeting.

Revision 3 - 26 July 1995

Per the June 21-22 working group meeting:

- Corrected reset timing figures
- Added FFh not specified in revision word.
- Removed word “non-shielded” from Clause 5.1.

Per the July 18-20 working group meeting:

- Added ATAPI bit definition in word 1 of DEVICE ID response.
- Removed DEVICE ID response word 71.
- Moved DEVICE ID response words 72 and 73 to words 73 and 74.
- Added SFF8035i S.M.A.R.T. into the standard.
- Added X3T10/95-294r0, Set Features changes into document.
- Reformatted protocol diagrams.
- Added DD7 pull-down modification.
- Deleted Annex A, reset considerations.
- Moved 40-pin connector definition into new Annex A that includes other connector definitions previously in Annex B and C.
- Deleted the IOCS16- signal.
- Deleted WRITE SAME command.
- Made numerous other minor changes requested during page-by-page review.

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Foreword

This standard encompasses the following:

Clause 1 describes the scope.

Clause 2 lists the normative references.

Clause 3 provides definitions, abbreviations and conventions used within this document.

Clause 4 contains the electrical and mechanical characteristics; covering the interface cabling requirements of the interface and DC cables and connectors.

Clause 5 contains the signal descriptions of the AT Attachment Interface.

Clause 6 contains descriptions of the registers of the AT Attachment Interface.

Clause 7 describes the general operating requirements of the AT Attachment Interface.

Clause 8 contains descriptions of the commands of the AT Attachment Interface.

Clause 9 contains an overview of the protocol of the AT Attachment Interface.

Clause 10 contains the interface timing diagrams.

Annexes A through C are informative.

Introduction

The first IBM PC™ (Personal Computer) introduced had no hard disk storage capability. When the IBM PC AT™ was developed, a hard disk was the key to system performance, and processor to hard disk interface became a de facto industry interface for the inclusion of hard disks in personal computers.

In October 1988, a number of device suppliers formed the Common Access Method Committee to encourage an industry-wide effort to adopt a common software interface to dispatch input/output requests to SCSI devices. Although this was the primary objective, a secondary goal was to specify what was known as the AT Attachment interface. This resulted in the development of the AT Attachment Interface For Disk Drives standard.

As personal computer type systems continued to evolved, there was a need to extend the capabilities of the interface. The lap-top and small computer systems needed to modify the mechanical aspects of the interface. High performance systems needed to have enhanced transfer rates. This evolutionary process has led to today's AT Attachment-3 Interface.

1 Scope

This standard specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers, and suppliers of intelligent storage devices.

The application environment for the AT Attachment Interface is any host system that has storage devices contained within the processor enclosure.

This standard defines the connectors and cables for physical interconnection between host and storage device, as well as, the electrical and logical characteristics of the interconnecting signals. It also defines the operational registers within the storage device, and the commands and protocols for the operation of the storage device.

This standard maintains a high degree of compatibility with the AT Attachment Interface with Extensions (ATA-2) standard, X3.279-199x, which it replaces, and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

2 Normative references

None.

3 Definitions, abbreviations and conventions

3.1 Definitions and abbreviations

For the purposes of this International Standard, the following definitions apply.

ATA (AT Attachment) - ATA defines the physical, electrical, transport, and command protocols for the internal attachment of block storage devices.

ATA-1 device - A device which complies with X3.221-1994, the AT Attachment Interface for Disk Drives.

ATA-2 device - A device which complies with X3T10.279-199x, the AT Attachment Interface with Extensions.

AWG - American Wire Gauge.

Command acceptance - A command is considered accepted whenever the host writes to the Command Register and the device currently selected has its BSY bit equal to zero. An exception exists for the EXECUTE DIAGNOSTIC command (see Clause 8.8).

CHS (Cylinder-head-sector) - This term defines the addressing of the device as being by cylinder number, head number and sector number.

Data block - This term describes a unit of data words transferred using PIO data transfer. A data block is transferred between the host and the device as a complete unit. A data block is a sector, except for data blocks of a READ MULTIPLE, WRITE MULTIPLE, READ LONG and WRITE LONG commands. In the cases of READ MULTIPLE and WRITE MULTIPLE commands, the size of the data block may be changed in multiples of sectors by the SET MULTIPLE MODE command. In the cases of READ LONG and WRITE LONG, the size of the data block is a sector plus a vendor specific number of bytes. The default length of the vendor specific bytes associate with the READ LONG and WRITE LONG commands is four bytes, but may be changed by use of the SET FEATURES command.

Device - Device is a storage peripheral. Traditionally, a device on the ATA interface has been a hard disk drive, but any form of storage device may be placed on the ATA interface provided it adheres to this standard.

Device selection - A device is selected when the DEV bit of the Drive/Head register is equal to the device number assigned to the device by means of a Device 0/Device 1 jumper or switch, or use of the CSEL signal.

DMA (Direct memory access) - A means of data transfer between device and host memory without processor intervention.

LBA (Logical block address) - This term defines the addressing of the device as being by the linear mapping of sectors.

Master - In ATA-1, Device 0 has also been referred to as the master. Throughout this document the term Device 0 is used.

Optional - This term describes features which are not required by the standard. However, if any optional feature defined by the standard is implemented, it shall be done in the way defined by the standard. Describing a feature as optional in the text is done to assist the reader.

PIO (Programmed input/output) - A means of accessing device registers. PIO is also used to describe one form of data transfers. PIO data transfers are performed by the host processor utilizing PIO register accesses to the Data register.

Reserved - Reserved bits, bytes, words, fields and code values are set aside for future standardization. Their use and interpretation may be specified by future extensions to this or other standards. A reserved bit, byte, word or field shall be set to zero, or in accordance with a future extension to this standard. The recipient shall not check reserved bits, bytes, words or fields. Receipt of reserved code values in defined fields shall be treated as an error.

Sector - A uniquely addressable set of 256 words (512 bytes).

Slave - In ATA-1, Device 1 has also been referred to as the slave. Throughout this document the term Device 1 is used.

Unrecoverable error - An unrecoverable error is defined as having occurred at any point when the device sets either the ERR bit or the DF bit to one and the BSY bit to zero in the Status register when processing a command.

VS (Vendor specific) - This term is used to describe bits, bytes, fields and code values which are reserved for vendor specific purposes. These bits, bytes, fields and code values are not described in this standard, and may vary among vendors. This term is also applied to levels of functionality whose definition is left to the vendor.

3.2 Conventions

If there is a conflict between text, figures and tables, the precedence shall be tables, figures, then text.

3.2.1 Keywords

Lower case is used for words having the normal English meaning. Certain words and terms used in this International Standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in Clause 3 or in the text where they first appear.

The names of abbreviations, commands, fields, and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. (See Clause 3.2.4 for the naming convention used for naming bits.)

Names of device registers begin with a capital letter (e.g., Cylinder Low register).

3.2.2 Numbering

Numbers that are not immediately followed by a lower-case "b" or "h" are decimal values. Numbers that are immediately followed by a lower-case "b" (e.g., 01b) are binary values. Numbers that are immediately followed by a lower-case "h" (e.g., 3Ah) are hexadecimal values.

3.2.3 Signal conventions

Signal names are shown in all upper case letters.

All signals are either high active or low active signals. A dash character (-) at the end of a signal name indicates it is a low active signal. A low active signal is true when it is below V_{iL}, and is false when it is above V_{iH}. No dash at the end of a signal name indicates it is a high active signal. A high active signal is true when it is above V_{iH}, and is false when it is below V_{iL}.

Asserted means that the signal is driven by an active circuit to its true state.

Negated means that the signal is driven by an active circuit to its false state.

Released means that the signal is not actively driven to any state. Some signals have bias circuitry that pull the signal to either a true state or false state when no signal driver is actively asserting or negating the signal. These cases are noted under the description of the signal, and their released state is stated.

Control signals that may be used for two mutually exclusive functions are identified with their two names separated by a colon.

3.2.4 Bit conventions

Bit names are shown in all upper case letters except where a lower case n precedes a bit name. If there is no preceding n, then when BIT is equal to one the meaning of the bit is true, and when BIT is equal to zero the meaning of the bit is false. If there is a preceding n, then when nBIT is equal to zero the meaning of the bit is true and when nBIT is equal to one the meaning of the bit is false.

3.2.5 Byte ordering for 8-bit and 16-bit data transfers

Assuming a block of data contains "n" bytes of information, and the bytes are labeled Byte(0) through Byte(n-1), where Byte(0) is first byte of the block, and Byte(n-1) is the last byte of the block. When such a block of data is transferred on the ATA interface in 16-bit wide transfer mode, the bytes shall be presented as shown in Table 1.

Table 1 - Byte Order - 16-bit transfer

	DD 15	DD 14	DD 13	DD 12	DD 11	DD 10	DD 9	DD 8	DD 7	DD 6	DD 5	DD 4	DD 3	DD 2	DD 1	DD 0
First transfer	Byte (1)								Byte (0)							
Second transfer	Byte (3)								Byte (2)							
.....																
Last transfer	Byte (n-1)								Byte (n-2)							

When such a block of data is transferred on the ATA interface in 8-bit wide transfer mode, the bytes shall be presented in Table 2.

Table 2 - Byte Order - 8-bit transfer

	DD 7	DD 6	DD 5	DD 4	DD 3	DD 2	DD 1	DD 0
First transfer	Byte (0)							
Second transfer	Byte (1)							
.....								
Next to last transfer	Byte (n-2)							
Last transfer	Byte (n-1)							

Note: The above description is for data on the ATA Interface. Host systems and/or host adapters may cause the order of data, as seen in the memory of the host, to be different.

4 Interface physical and electrical requirements

Connectors are documented in Annex A.

4.1 Cable Configuration

This standard defines the ATA interface containing a single host or host adapter and one or two devices. If two devices are connected to the interface, they are connected in a daisy chained configuration. One device is configured as Device 0 and the other device as Device 1.

The designation of a device as Device 0 or Device 1 may be made in a number of ways:

- a switch or a jumper on the device
- use of the Cable Select (CSEL) pin

In a two drive configuration, Device 0 shall be at one end of the ATA interface cable and the host shall be placed at one end of the cable.

If only a single device is attached via the ATA interface to a host, the host and the device shall be placed at the two ends of the cable.

Also see Clause 5.2.15.0.

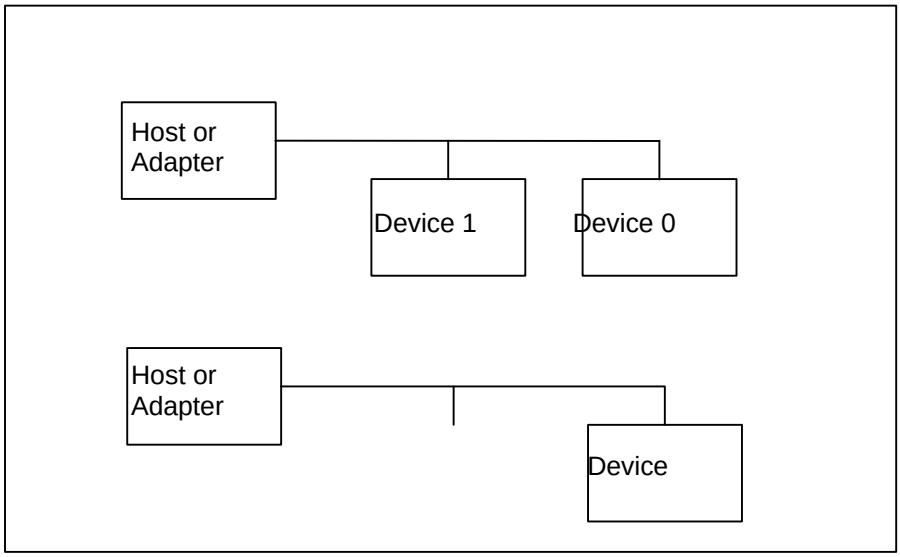


Figure 1- ATA Interface Cabling Diagram

4.2 I/O cable

The cable specification affects system integrity and the maximum length that can be supported in any application.

Cable total length shall not exceed 0,46 m (18 in).

Cable capacitance shall not exceed 35 pf.

4.3 Electrical characteristics

Interface signal are defined in Table 3 and Table 4.

Table 3 - DC Characteristics

Description		Min	Max
I_{oL}	Driver sink current	4 mA (2)	
I_{oH}	Driver source current (1)	400 µA	
V_{iH}	Voltage Input High	2,0 V D.C.	
V_{iL}	Voltage Input Low		0,8 V D.C.
V_{oH}	Voltage Output High (I_{oH} = -400 µA)	2,4 V D.C.	
V_{oL}	Voltage Output Low (I_{oL} = 12 ma)		0,5 V D.C.

Note:
(1) I_{oH} value at 400 µA is insufficient in the case of DMARQ which is typically pulled low by a 5,6 kΩ resistor.
(2) I_{oL} for DASP shall be 12 mA minimum to meet legacy timing and signal integrity.

Table 4 - AC Characteristics

Description		Min	Max
tRISE	Rise time for any signal on AT interface (1)	5 ns	
tFALL	Fall time for any signal on AT interface (1)	5 ns	
Cin	Input Capacitance (each host or Device)		25 pf
Cout	Output Capacitance (each host or Device)		25 pf

Note:
(1) tRISE and tFALL are measured from 10-90% of full signal amplitude with a total capacitive load of 100 pf.

4.3.1 Driver types and required pull-ups

Table 5 - Driver Types and Required Pull-ups

Signal	Source	Driver Type (1)	Pull-up at Host (2)	Pull-up at each Device (2)	Notes
Reset	Host	TP			
DD (15:0)	Bidir	TS			(6)
DMARQ	Device	TS	5,6 kΩ PD		(3)
DIOR- DIOW-	Host	TS			
IORDY	Device	TS	1,0 kΩ		(4)
CSEL	Host		Ground	10 kΩ	(5)
DMACK-	Host	TP			
INTRQ	Device	TS			
DA (2:0)	Host	TP			
PDIAG-	Device	TS		10 kΩ	
CS0- CS1-	Host	TP			
DASP-	Device	OC		10 kΩ	(5)

Notes:
(1) TS=Tri-State; OC=Open Collector; TP=Totem-Pole; PU=Pull-up; PD=Pull-down; VS=Vendor specific
(2) All resistor values are minimum (lowest) allowed.
(3) ATA-3 defines this line to be tri-stated whenever the device is not selected or is not executing a DMA data transfer. When enabled by DMA transfer, it shall be driven high and low by the device.
(4) This signal should only be enabled during DIOR/DIOW cycles to the selected device.
(5) When used as CSEL, this line is grounded at the Host and a 10 kΩ pull-up is required at both devices.

(6) Devices shall not have a pull-up resistor on DD7. It is recommended that a host have a 10 kΩ pull-down resistor and not a pull-up resistor on DD7 to allow a host to recognize the absence of a device at power-up. It is intended that this recommendation become mandatory in a future revision of this standard.

5 Interface signal assignments and descriptions

5.1 Signal summary

The physical interface consists of receivers and drivers communicating through a set of conductors using an asynchronous interface protocol. Signal names are shown in Table 6. Table 24 For connector descriptions see Annex A.

Table 6 - Interface Signal Names Assignments

Description	Source	Acronym
Reset	Host	RESET-
Ground	n/a	Ground
Data bus bit 7	Host/Device	DD7
Data bus bit 8	Host/Device	DD8
Data bus bit 6	Host/Device	DD6
Data bus bit 9	Host/Device	DD9
Data bus bit 5	Host/Device	DD5
Data bus bit 10	Host/Device	DD10
Data bus bit 4	Host/Device	DD4
Data bus bit 11	Host/Device	DD11
Data bus bit 3	Host/Device	DD3
Data bus bit 12	Host/Device	DD12
Data bus bit 2	Host/Device	DD2
Data bus bit 13	Host/Device	DD13
Data bus bit 1	Host/Device	DD1
Data bus bit 14	Host/Device	DD14
Data bus bit 0	Host/Device	DD0
Data bus bit 15	Host/Device	DD15
DMA Request	Device	DMARQ
I/O Write	Host	DIOW-
I/O Read	Host	DIOR-
I/O Ready	Device	IORDY
Cable Select	(1)	CSEL
DMA Acknowledge	Host	DMACK-
Interrupt Request	Device	INTRQ
Device Address Bit 1	Host	DA1
Passed Diagnostics	(1)	PDIAG-
Device Address Bit 0	Host	DA0
Device Address Bit 2	Host	DA2
Chip Select 0	Host	CS0-
Chip Select 1	Host	CS1-
Device Active or Slave (Device 1) Present	(1)	DASP-

Note:
(1) See signal descriptions for information on source of these signals

5.2 Signal descriptions

5.2.1 CS0- (CHIP SELECT 0)

This is the chip select signal from the host used to select the Command Block Registers. See Table 7.

5.2.2 CS1- (CHIP SELECT 1)

This is the chip select signal from the host used to select the Control Block Registers. See Table 7.

5.2.3 DA2, DA1, and DA0 (DEVICE ADDRESS)

This is the 3-bit binary coded address asserted by the host to access a register or data port in the device. See Table 7.

5.2.4 DASP- (Device active, device 1 present)

This is a time-multiplexed signal which indicates that a device is active, or that Device 1 is present. This signal shall be an open collector output and each device shall have a 10 kΩ pull-up resistor.

If the host connects to the DASP- signal for the illumination of an LED or for any other purpose, the host shall ensure that the signal level seen on the ATA interface for DASP- shall maintain V_{oH} and V_{oL} compatibility, given the I_{oH} and I_{oL} requirements of the DASP- device drivers.

5.2.5 DD (15:0) (Device data)

This is an 8- or 16-bit bi-directional data interface between the host and the device. The lower 8 bits are used for 8-bit transfers e.g. registers, vendor specific bytes associated with the READ LONG and WRITE LONG commands and, if the device supports the Features register capability to enable 8-bit data transfers (see Clause 8.32).

5.2.6 DIOR- (Device I/O read)

This is the read strobe signal from the host. The falling edge of DIOR- enables data from the device onto the signals, DD (7:0) or DD (15:0). The rising edge of DIOR- latches data at the host and the host shall not act on the data until it is latched.

5.2.7 DIOW- (Device I/O write)

This is the Write strobe signal from the host. The rising edge of DIOW- latches data from the signals, DD (7:0) or DD (15:0), into the device. The device shall not act on the data until it is latched.

5.2.8 DMACK- (DMA acknowledge)

This signal shall be used by the host in response to DMARQ to initiate DMA transfers.

Figure 14

5.2.9 DMARQ (DMA request)

This signal, used for DMA data transfers between host and device, shall be asserted by the device when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK- i.e. the device shall wait until the host asserts DMACK- before negating DMARQ, and re-asserting DMARQ if there is more data to transfer.

This line shall be released (high impedance state) whenever the device is not selected or is selected and no DMA command is in progress. When enabled by DMA transfer, it shall be driven high and low by the device.

When a DMA operation is enabled, CS0- and CS1- shall not be asserted and transfers shall be 16-bits wide.

5.2.10 INTRQ (Device interrupt)

This signal is used to interrupt the host system. INTRQ is asserted only when the device has a pending interrupt, the device is selected, and the host has cleared the nIEN bit in the Device Control register. If the nIEN bit is equal to one, or the device is not selected, this output is in a high impedance state, regardless of the presence or absence of a pending interrupt.

The interrupt pending condition shall be cleared by:

- assertion of RESET-
- or the setting of the SRST bit of the Device Control register
- or the host writing the Command register
- or the host reading the Status register

On PIO transfers, INTRQ is asserted at the beginning of each data block to be transferred. An exception occurs on FORMAT TRACK, WRITE SECTOR(S), WRITE BUFFER and WRITE LONG commands when INTRQ shall not be asserted at the beginning of the first data block to be transferred.

On DMA transfers, INTRQ is asserted only once, after the command has completed.

5.2.11 IOCS16- (Device 16-bit I/O)

The signal IOCS16- was used in previous versions of the ATA standard.

5.2.12 IORDY (I/O channel ready)

This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the device is not ready to respond to a data transfer request.

If actively asserted, this signal shall only be enabled during DIOR-/DIOW- cycles to the selected device. If open collector, when IORDY is not negated, it shall be in the high-impedance (undriven) state.

The use of IORDY is required for PIO modes 3 and above and otherwise optional.

5.2.13 PDIAG- (Passed diagnostics)

This signal shall be asserted by Device 1 to indicate to Device 0 that it has completed diagnostics. A 10 kΩ pull-up resistor shall be used on this signal by each device.

The host shall not connect to the PDIAG- signal.

5.2.14 RESET- (Device reset)

This signal from the host system shall be asserted beginning with the application of power and held asserted until at least 25 μsec after voltage levels have stabilized within tolerance during power on and negated thereafter unless some event requires that the device(s) be reset following power on.

ATA devices shall not recognize a signal assertion shorter than 20 nsec as a valid reset signal. Devices may respond to any signal assertion greater than 20 nsec, and shall recognize a signal equal to or greater than 25 μsec.

5.2.15 CSEL (Cable select)

This signal shall have a 10 kΩ pull-up resistor at each device.

The device is configured as either Device 0 or Device 1 depending upon the value of CSEL:

- If CSEL is negated then the device address is 0
- If CSEL is asserted then the device address is 1

CSEL shall be maintained at a steady level for at least 31 sec after the negation of RESET-.

> Implementor's Note: Special cabling can be used by the system manufacturer to selectively ground CSEL e.g. CSEL of Device 0 is connected to the CSEL conductor in the cable, and is grounded, thus allowing the device to recognize itself as Device 0. CSEL of Device 1 is not connected to CSEL because the conductor is removed, thus the device can recognize itself as Device 1.

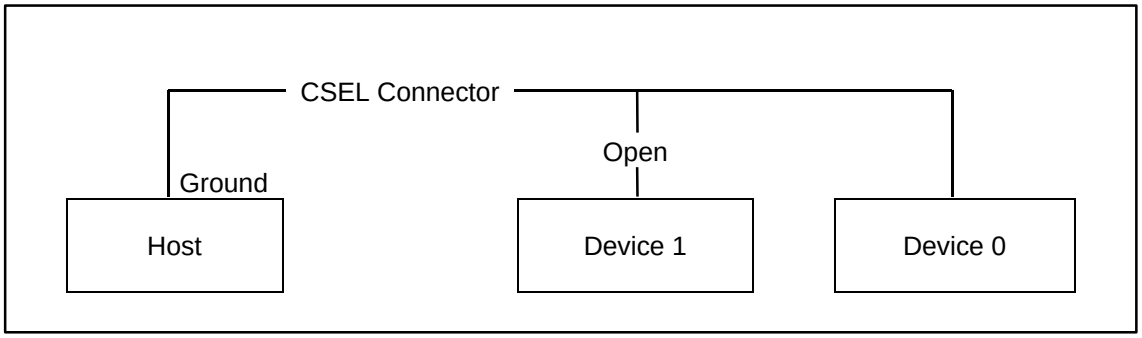


Figure 2 - Cable Select Example

6 Interface register definitions and descriptions

6.1 Device addressing considerations

In traditional controller operation, only the selected device receives commands from the host following selection. In this standard, the register contents go to both devices (and their embedded controllers). The host discriminates between the two by using the DEV bit in the Device/Head register.

Data is transferred in parallel either to or from host memory to the device's buffer under the direction of commands previously transferred from the host. The device performs all of the operations necessary to properly write data to, or read data from, the media. Data read from the media is stored in the device's buffer pending transfer to the host memory and data is transferred from the host memory to the device's buffer to be written to the media.

The devices using this interface shall be programmed by the host computer to perform commands and return status to the host at command completion. When two devices are daisy chained on the interface, commands are written in parallel to both devices, and for all except the EXECUTE DEVICE DIAGNOSTICS command, only the selected device executes the command. On an EXECUTE DEVICE DIAGNOSTICS command addressed to Device 0, both devices shall execute the command, and Device 1 shall post its status to Device 0 via PDIAG-.

Devices are selected by the DEV bit in the Device/Head register (see Clause 6.2.8). When the DEV bit is equal to zero, Device 0 is selected. When the DEV bit is equal to one, Device 1 is selected. When devices are daisy chained, one shall be set as Device 0 and the other as Device 1

6.2 I/O register descriptions

Communication to or from the device is through an I/O Register that routes the input or output data to or from registers addressed by the signals from the host (CS0-, CS1-, DA (2:0), DIOR- and DIOW-).

The Command Block Registers are used for sending commands to the device or posting status from the device. The Control Block Registers are used for device control and to post alternate status.

Table 7 lists these registers and the addresses that select them.

Table 7 - I/O Port Functions and Selection Addresses

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	Read (DIOR-)	Write (DIOW-)
N	N	x	x	x	Data bus high impedence	Not Used
					Control block registers	
N	A	0	x	x	Data bus high impedence	Not Used
N	A	1	0	x	Data bus high impedence	Not Used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	(1)	Not Used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number LBA (7:0) (2)	Sector Number LBA (7:0) (2)
A	N	1	0	0	Cylinder Low LBA (15:8) (2)	Cylinder Low LBA (15:8) (2)
A	N	1	0	1	Cylinder High LBA (23:16) (2)	Cylinder High LBA (23:16) (2)
A	N	1	1	0	Device/Head LBA (27:24) (2)	Device/Head LBA (27:24) (2)
A	N	1	1	1	Status	Command
A	A	x	x	x	Invalid address	Invalid address

Key:
A = signal asserted, N = signal negated, x = don't care
Notes:
(1) This register is obsolete. It is recommended that a device not respond to a read of this address. If a device does respond, it shall not drive the DD7 signal to prevent possible conflict with floppy disk implementations.
(2) Mapping of registers in LBA mode.

Each register description in the following clauses contain the following format:

ADDRESS - the CS and DA address of the register.

DIRECTION - indicates if the register is read/write, read only, or write only from the host.

ACCESS RESTRICTIONS - indicates when the register may be accessed.

EFFECTIVENESS - indicates the effect of accessing the register.

FUNCTIONAL DESCRIPTION - describes the function of the register.

FIELD/BIT DESCRIPTION - describes the content of the register.

6.2.1 Alternate Status register

ADDRESS - CS(1:0)=1h, DA(2:1)=6h

DIRECTION - This register is read only. If this address is written by the host, the Device Control register is written.

ACCESS RESTRICTIONS - When the BSY bit is equal to zero, the other bits in this register shall be valid.

EFFECT - Reading this register shall not perform an interrupt acknowledge or clear a pending interrupt.

FUNCTIONAL DESCRIPTION - This register contains the same information as the Status register in the command block.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

See Clause 6.2.13 for definitions of the bits in this register.

6.2.2 Command register

ADDRESS - CS(1:0)=2h, DA(2:1)=7h

DIRECTION - This register is write-only. If this address is read by the host, the Status register is read.

ACCESS RESTRICTIONS - This register shall only be written when BSY and DRQ are both equal to zero.

EFFECT - Command processing begins when this register is written. The content of the Command Block registers become parameters of the command when this register is written.

FUNCTIONAL DESCRIPTION - This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The executable commands, the command codes, and the necessary parameters for each command are listed in Table 9.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
Command							

6.2.3 Cylinder High register

ADDRESS - CS(1:0)=2h, DA(2:0)=5h

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are zero. The contents of this register are valid only when both BSY and DRQ are zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant.

EFFECT - Information written to this register becomes a command parameter when subsequent commands are written to the Command register.

FUNCTIONAL DESCRIPTION - If the LBA bit is cleared to zero in the Device/Head register, this register contains the high order bits of the starting cylinder address for any media access. If the LBA bit is set to one in the Device/Head register, this register contains Bits 23-16 of the LBA for any media access.

This register shall be updated to reflect the address of the first error when a media access command is unsuccessfully completed.

FIELD/BIT DESCRIPTION -

CHS

7	6	5	4	3	2	1	0
Cylinder(15:8)							

LBA

7	6	5	4	3	2	1	0
LBA(23:16)							

6.2.4 Cylinder Low register

ADDRESS - CS(1:0)=2h, DA(2:0)=4h

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are zero. The contents of this register are valid only when both BSY and DRQ are zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant.

EFFECT - Information written to this register becomes a command parameter when subsequent commands are written to the Command register.

FUNCTIONAL DESCRIPTION -If the LBS bit is cleared to zero in the Device/Head register, this register contains the low order bits of the starting cylinder address for any media access.If the LBA bit is set to one in the Device/Head register, this register contains Bits 15-8 of the LBA for any media access.

This register shall be updated to reflect the address of the first error when a media access command is unsuccessfully completed.

FIELD/BIT DESCRIPTION -

CHS

7	6	5	4	3	2	1	0
Cylinder(7:0)							

LBA

7	6	5	4	3	2	1	0
LBA(15:8)							

6.2.5 Data register

ADDRESS - CS(1:0)=2h, DA(2:0)=0h

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written and the contents shall be valid on read only when DRQ is asserted.

EFFECT -PIO out data transfers are processed by a series of reads to this register, each read transferring the data that follows the previous read. PIO in data transfers are processed by a series of writes to this register, each write transferring the data that follows the previous write. The results of a read during a PIO in or a write during a PIO out is indeterminant.

FUNCTIONAL DESCRIPTION - The data register is either 8-bits or 16-bits depending on the interface width currently selected and/or the type of data being transferred by the current command.

FIELD/BIT DESCRIPTION -

16-bit Interface Width

15	14	13	12	11	10	9	8
Data(15:8)							

7	6	5	4	3	2	1	0
Data(7:0)							

8-bit Interface Width

7	6	5	4	3	2	1	0
Data(7:0)							

6.2.6 Data port

ADDRESS - None

DIRECTION - This port is read/write.

ACCESS RESTRICTIONS - This port shall be written and the contents shall be valid on read only when DMARQ is asserted.

EFFECT - DMA out data transfers are processed by a series of reads to this port, each read transferring the data that follows the previous read. DMA in data transfers are processed by a series of writes to this register, each write transferring the data that follows the previous write. The results of a read during a DMA in or a write during a DMA out is indeterminant.

FUNCTIONAL DESCRIPTION - The data port is 16-bits in width.

FIELD/BIT DESCRIPTION -

15	14	13	12	11	10	9	8
Data(15:8)							

7	6	5	4	3	2	1	0
Data(7:0)							

6.2.7 Device Control register

ADDRESS - CS(1:0)=1h, DA(2:0)=6h

DIRECTION - This register is write. If this address is read by the host, the Alternate Status register is read.

ACCESS RESTRICTIONS - This register shall only be written when both BSY and DRQ equal zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant.

EFFECTIVENESS - the content of this register shall take effect when written.

FUNCTIONAL DESCRIPTION - This register allows a host to software reset attached devices and enable/disable interrupts.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
r	r	r	r	r	SRST	nIEN	0

- Bits 7 through 3 are reserved.
- SRST is the host software reset bit. See Clause 9.2.
- nIEN is the enable bit for the device interrupt to the host. When the nIEN bit is equal to zero, and the device is selected, INTRQ shall be enabled through a tri-state buffer. When the nIEN bit is equal to one, or the device is not selected, the INTRQ signal shall be in a high impedance state.
- Bit 0 shall be written with zero.

6.2.8 Device/Head register

ADDRESS - CS(1:0)=2h, DA(2:0)=6h

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are zero. The contents of this register are valid only when BSY and DRQ equal zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant.

EFFECT - The DRV bit becomes becomes effective when this register is written. All other bits in this register become a command parameter when subsequent commands are written to the Command register.

FUNCTIONAL DESCRIPTION - This register selects the device, defines address translation as CHS or LBA, and provides the head adrress if CHS or LBA (27:24) if LBA.

FIELD/BIT DESCRIPTION -

CHS

7	6	5	4	3	2	1	0
r	LBA	r	DEV	HS3	HS2	HS1	HS0

LBA

7	6	5	4	3	2	1	0
r	LBA	r	DEV	LBA(27:24)			

- Bit 7 is reserved.
- Bit 6 LBA. When this bit is equal to zero, addressing is by CHS. When this bit is equal to one, addressing is by LBA.
- Bit 5 is reserved.
- DEV is the device address. When the DEV bit is equal to zero, Device 0 is selected. When the DEV bit is equal to one, Device 1 is selected.
- Bit 3-0 If bit 6 is equal to zero (CHS), these contain the head address of the starting CHS address. The HS3 bit is the most significant bit. If bit 6 is equal to one (LBA), these bits contain bits 27 through 24 of the LBA. This field shall be updated to reflect the media address of the error when a media access command is unsuccessfully completed. See Clause 7.2.

6.2.9 Error register

ADDRESS - CS(1:0)=2h, DA(2:0)=1h

DIRECTION - This register is read only. If this address is written by the host, the Features register is written.

ACCESS RESTRICTIONS - The contents of this register shall be valid when BSY and DRQ equal zero and ERR equals one. The contents of this register shall be valid upon completion of power on or a reset. The contents of this register shall be valid at the completion of an EXECUTE DEVICE DIAGNOSTIC command.

EFFECT - None.

FUNCTIONAL DESCRIPTION - This register contains status for the current command.

Following a power on, a reset, or completion of an EXECUTE DEVICE DIAGNOSTIC command, this register contains a diagnostic code (see Clause 8.8).

At the completion of any command except EXECUTE DEVICE DIAGNOSTIC, the contents of this register are valid when the ERR bit is equal to one in the Status register.

FIELD/BIT DESCRIPTION -

Table 10

7	6	5	4	3	2	1	0
r	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF

- Bit 7 is reserved.
- UNC (Uncorrectable Data Error) indicates an uncorrectable data error has been encountered.
- MC (Media Changed) is used by removable media devices and indicates that new media is available to the operating system. See Clause 7.4.
- IDNF (ID Not Found) indicates the requested sector's ID field could not be found.
-
- MCR (Media Change Requested) is used by removable media devices and indicates that a request for media removal has been detected by the device. See Clause 7.4.
- ABRT (Aborted Command) indicates the requested command has been aborted because the command code or a command parameter is invalid or some other error has occurred.
- TK0NF (Track 0 Not Found) indicates track 0 has not been found during a RECALIBRATE command.
- AMNF (Address Mark Not Found) indicates the data address mark has not been found after finding the correct ID field.

6.2.10 Features register

ADDRESS - CS(1:0)=2h, DA(2:0)=1h

DIRECTION - This register is write only. If this address is read by the host, the Error register is read.

ACCESS RESTRICTIONS - This register shall be written only when BSY and DRQ equal zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant.

EFFECT - Information written to this register becomes a command parameter when subsequent commands are written to the Command register.

FUNCTIONAL DESCRIPTION - This register is command specific.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
Command Specific							

6.2.11 Sector Count register

ADDRESS - CS(1:0)=2h, DA(2:0)=2h

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are zero. The contents of this register are .valid only when both BSY and DRQ are zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant.

EFFECT - Information written to this register becomes a command parameter when subsequent commanda are written to the Command register.

FUNCTIONAL DESCRIPTION - This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in this register is zero, a count of 256 sectors is specified.

For media access commands that complete with an error indication in the Status register, this register contains the number of sectors which need to be transferred in order to complete the request.

The contents of this register may be redefined on some commands.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
Sector Count							

6.2.12 Sector Number register

ADDRESS - CS(1:0)=2h, DA(2:0)=3h

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are zero. The contents of this register are valid only when both BSY and DRQ are zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant.

EFFECT - Information written to this register becomes a command parameter when subsequent commands are written to the Command register.

FUNCTIONAL DESCRIPTION - If the LBA bit is cleared to zero in the Device/Head register, this register contains the starting sector number for any media access.If the LBA bit is set to one in the Device/Head register, this register contains Bits 7-0 of the LBA for any media access. This register is used by some non-media access commands to pass command specific information from the host to the device, or from the device to the host.

This register shall be updated to reflect the media address of the error when a media access command is unsuccessfully completed.

FIELD/BIT DESCRIPTION -

CHS

7	6	5	4	3	2	1	0
Sector(7:0)							

LBA

7	6	5	4	3	2	1	0
LBA(7:0)							

6.2.13 Status register

ADDRESS - CS(1:0)=2h, DA(2:0)=7h

DIRECTION - This register is read only. If this address is written the Command register is written.

ACCESS RESTRICTIONS -BSY is valid at all times. The remaining contents of this register are valid only when BSY is zero.

EFFECTIVENESS - Reading this register when an interrupt is pending causes the interrupt to be cleared.

FUNCTIONAL DESCRIPTION - This register contains the device status. The contents of this register are updated to reflect the current state of the device and the progress of any command being executed by the device. When the BSY bit is equal to zero, the other bits in this register are valid. When the BSY bit is equal to one, other bits in this register are not valid.

Note: Although host systems might be capable of generating read cycles shorter than the 400 nsec specified for status update following the last command or data cycle, host implementations should wait at least 400 nsec before reading the Status register to insure that the BSY bit is valid.

The contents of the Status register and all other Command Block registers are not valid while a device is in the Sleep mode.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

- BSY (Busy) is set whenever the device has control of the command Block Registers. When the BSY bit is equal to one, a write to a command block register by the host shall be ignored by the device.

  The device shall not change the state of the DRQ bit unless the BSY bit is equal to one. When the last block of a PIO data in command has been transferred by the host, then the DRQ bit is cleared without the BSY bit being set.

  When the BSY bit equals zero, the device may only change the IDX, DRDY, DF, DSC and CORR bits in the Status register and the Data register. None of the other command block registers nor bits within the Status register shall not be changed by the device.

  Note: The assertion of CORR by the device while the BSY bit is cleared to zero might not be recognized by BIOS and drivers which sample status as soon as the BSY bit is equal to zero.

  When writing the Command register either the BSY bit shall be set, or if the BSY bit is cleared, the DRQ bit shall be set, until command completion.

  Implementor's Note: There may be times when the BSY bit is set and then cleared so quickly, that the host may not be able to detect that the BSY bit had been set.

  The BSY bit shall be set by the device under the following circumstances:

  a) within 400 nsec after either the negation of RESET- or the setting of the SRST bit in the Device Control register.

  b) within 400 nsec after writing the Command register if the DRQ bit is not set.

c) between blocks of a data transfer during PIO data in commands if the DRQ bit is not set.

d) after the transfer of a data block during PIO data out commands if the DRQ bit is not set.

e) during the data transfer of DMA commands if the DRQ bit is not set.

The device shall not set the BSY bit at any other time.

- DRDY (Device Ready) is set to indicate that the device is capable of accepting all command codes. This bit shall be cleared at power on. Devices that implement the power management features shall maintain the DRDY bit equal to one when they are in the Idle or Standby power modes. When the state of the DRDY bit changes, it shall not change again until after the host reads the Status register.

  When the DRDY bit is equal to zero, a device responds as follows:

  a) the device shall accept and attempt to execute the EXECUTE DEVICE DIAGNOSTIC and INITIALIZE DEVICE PARAMETERS commands.

  b) If a device accepts commands other than EXECUTE DEVICE DIAGNOSTIC and INITIALIZE DEVICE PARAMETERS during the time the DRDY bit is equal to zero, the results are vendor specific.

- DF (Device Fault) indicates a device fault error has been detected. The internal status or internal conditions that causes this error to be indicated is vendor specific.

- DSC (Device Seek Complete) indicates that the device heads are settled over a track. When an error occurs, this bit shall not be changed until the Status register is read by the host, at which time the bit again indicates the current Seek Complete status.

- DRQ (Data Request) indicates that the device is ready to transfer a word or byte of data between the host and the device.

- CORR (Corrected Data) is used to indicate a correctable data error. The definition of what constitutes a correctable error is vendor specific. This condition does not terminate a data transfer.

- IDX (Index) is vendor specific.

- ERR (Error) indicates that an error occurred during execution of the previous command. The bits in the Error register have additional information regarding the cause of the error. Once the device has set the error bit, the device shall not change the contents of the following items until a new command has been accepted, the SRST bit is set to one or RESET- is asserted:
  the ERR bit in the status register
  Error register
  Cylinder High register
  Cylinder Low register
  Sector Count register
  Sector Number register
  Device/Head register.

7 General operational requirements

7.1 Reset response

There are three types of reset in ATA. The following is a suggested method of classifying reset actions:

- Power On Reset: the device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parametrics, and sets default values. See Clause 9.1.
- Hardware Reset: the device executes a series of electrical circuitry diagnostics, and resets to default values. See Clause 9.1.
- Software Reset: the device resets the interface circuitry. 8.32 See Clause 9.2.

9.19.2

7.2 Sector addressing

All addressing of data sectors recorded on the device's media is by a logical sector address. The mapping of logical sector addresses to the actual physical location of the data sector on the media is vendor specific.

An ATA device shall support at least one logical CHS translation known as the default translation. The device shall enter this translation following a reset. A device may support other logical translations and the host may use the INITIALIZE DEVICE PARAMETERS command to select the default CHS translation or any of the other supported CHS translations. The default translation is described in the Identify Device information. The current translation may also be described in the Identify Device information.

A CHS address is made up of three fields: the sector address, the head number and the cylinder number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation but can not exceed 255. Heads are numbered from 0 to the maximum value allowed by the current CHS translation but can not exceed 15. Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation but cannot exceed 65 535.

When the host selects a CHS translation using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested translation.

Sequential access to logical sectors shall be accomplished by treating the sector number as the least significant portion of the logical sector address, the head number as the middle portion of the logical sector address and the cylinder number as the most significant portion of the logical sector address.

A device that supports LBA addressing indicates this in the Identify Device information. A host shall not use LBA addressing unless the device indicates LBA addressing is supported.

A device shall not change the addressing method and shall return status information utilizing the addressing method specified for the command.

If a device supports LBA addressing, then the following shall be supported by the device:

1) The host may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the LBA bit in the Device/Head register.

2) If LBA addressing is supported, then the device shall supported LBA addressing for all media access commands, except for the FORMAT TRACK command. Implementation of LBA addressing for the FORMAT TRACK command is vendor specific. The LBA bit of the Device/Head register shall be ignored for commands that do not access the media.

3) Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation currently in effect, the LBA address of a given logical sector does not change. The following is always true:

LBA = ((cylinder * heads_per_cylinder + heads) * sectors_per_track) + sector - 1

where heads_per_cylinder and sectors_per_track are the current translation values.

7.3 Power management feature set

The optional Power Management Feature Set permits a host to modify the behavior of a device in a manner which reduces the power required to operate. The Power Management Feature Set provides a set of commands and a timer that enable a device to implement low power consumption modes. A device that implements the Power Management feature shall implement the following minimum set of functions:

1) A Standby timer
2) Idle command
3) Idle Immediate command
4) Sleep command
5) Standby command
6) Standby Immediate command

Additional vendor specific commands and functions are allowed.

7.3.1 Power modes

In Active mode the device is capable of responding to commands and commands complete in the shortest possible time. During the execution of a media access command a device shall be in Active mode. Power consumption is greatest in this mode.

In Idle mode the device is capable of responding to commands but the device may take longer to complete commands than when in the Active mode. Power consumption may be reduced from that of Active mode.

In Standby mode the device is capable of responding to commands but the device may take longer to complete commands than in the Idle mode. Power consumption may be reduced from that of Idle mode.

In Sleep mode the device requires a reset to be activated. Sleep provides the lowest power consumption of any mode.

7.3.2 Power management commands

The CHECK POWER MODE command allows a host to determine if a device is currently in, going to or leaving Standby or Idle mode.

The IDLE and IDLE IMMEDIATE commands move a device to Idle mode immediately from the Active or Standby modes. The Idle command also sets the Standby Timer count and enables or disables the Standby Timer.

The SLEEP command moves a device to Sleep mode. The device's interface becomes inactive at the completion of the SLEEP command. A reset is required to move a device out of Sleep mode. When a device exits Sleep mode it may enter Active, Idle or Standby mode. The mode selected by the device is based on the type of reset received and on vendor specific implementation.

The STANDBY and STANDBY IMMEDIATE commands move a device to Standby mode immediately from the Active or Idle modes. The STANDBY command also sets the Standby Timer count and enables or disables the Standby Timer.

7.3.3 Standby timer

The Standby timer provides a method for the device to automatically enter Standby mode from either Active or Idle mode following a host programmed period of inactivity. If the Standby timer is enabled and if the device is in the Active or Idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the Standby mode.

If the Standby Timer is disabled, the device may not automatically enter Standby mode.

7.3.4 Idle mode transition

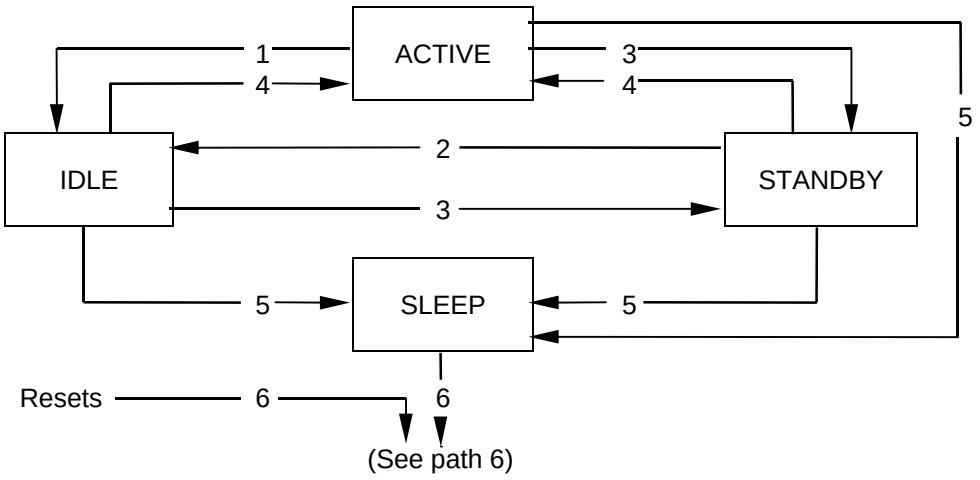
The transition to Idle mode is vendor specific, and may occur as a result of an IDLE or IDLE IMMEDIATE command, or in vendor specific way.

7.3.5 Status

In Sleep mode, the device's interface is not active. A host shall not attempt to read the device's status or issue commands to the device.

7.3.6 Power mode transitions

Figure 3 shows the minimum set of mode transitions that shall be implemented.



Path 1: An IDLE command, IDLE IMMEDIATE command, or vendor specific implementation moves the device to Idle mode.
Path 2: An IDLE command or IDLE IMMEDIATE command moves the device to Idle mode.
Path 3: A STANDBY command, STANDBY IMMEDIATE command, vendor specific implementation, or Standby timerexpiration moves the device to Standby mode.
Path 4: A Media access command moves the device to Active mode.
Path 5: A SLEEP command moves the device to Sleep mode.
Path 6: A reset, either hardware or software, moves the device to Active, Idle or Standby as specified by the device vendor.

Figure 3 - Power Management Modes

7.4 Removable media mode transitions

Figure 4 shows the minimum set of mode transitions that shall be implemented by removable media devices which contain a media change request mechanism (button) and support the DOOR LOCK and DOOR UNLOCK commands, and the MC and MCR bits in the Error register.

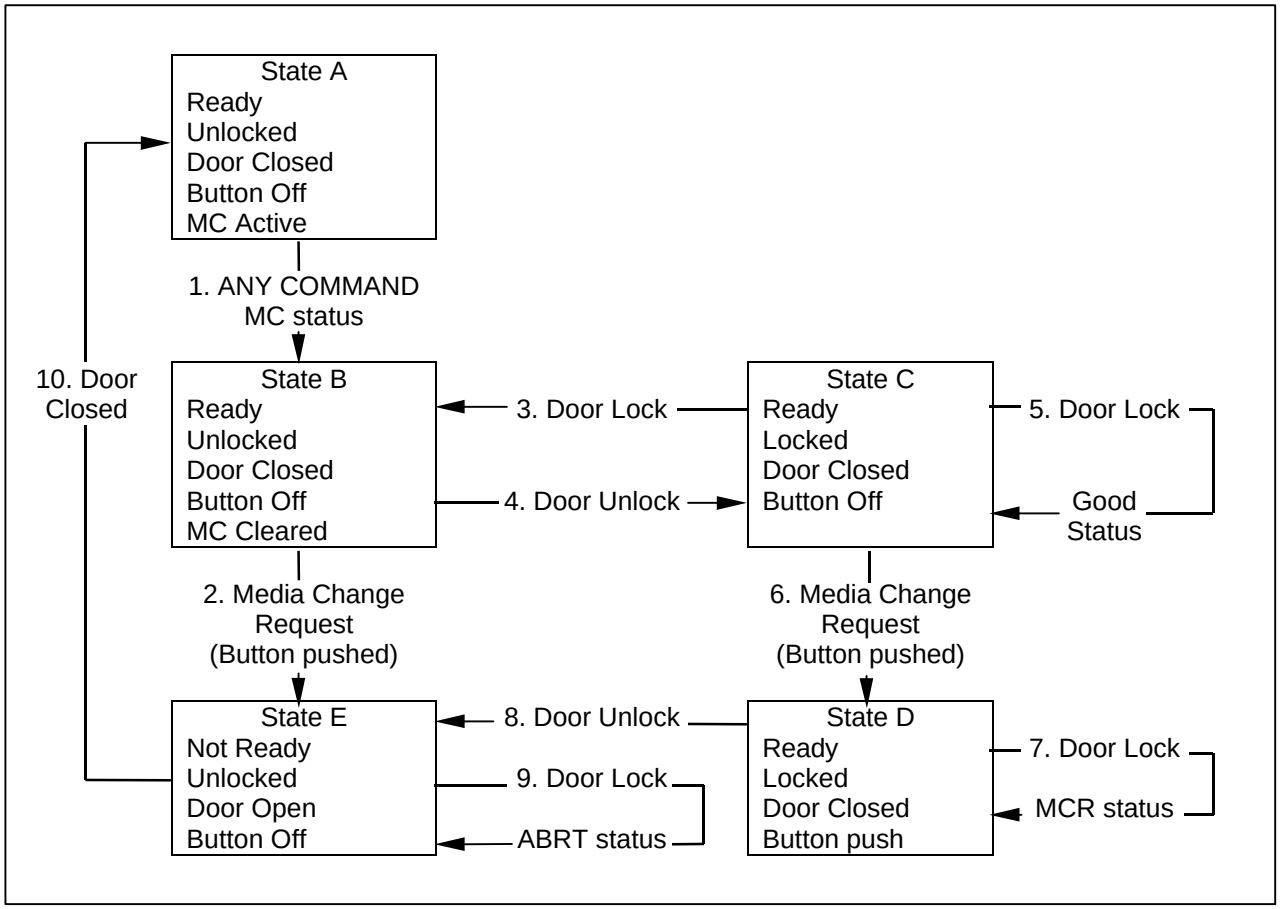


Figure 4 - Removable Modes

State A: Following a media change, the device is ready, the media is not locked, the door is closed, the media change request button is not active and a media change has been detected.
Path 1: The first command following a media change shall be rejected with the MC bit set in the Error register. The device shall then be moved to state B and the MC condition shall be cleared.

State B: In normal operation, the device is ready, the media is not locked, the door is closed, the media change request button is not active and the MC bit is off.
Path 2: Activating the media change request button shall cause the device to complete any pending operations, spin down the device, if needed, and move to state E, allowing media removal.
Path 3: A DOOR LOCK command shall lock the media and move the device to state C.

State C: In normal operation, the device is ready, the media is locked, the door is closed and the media change request button is not active.
Path 4: A DOOR UNLOCK command shall unlock the media and move the device to state B.
Path 5: A DOOR LOCK command shall return good status.
Path 6: Pushing the media change button shall move the device to state D.

State D: The device is ready, the media is locked, the door is closed and the media change button is active.
Path 7: A DOOR LOCK command shall return MCR status.
Path 8: A DOOR UNLOCK command shall move the device to state E, allowing media removal.

State E: The device is not ready, the media is not locked, the door is open and the media change button is not active.
Path 9: A DOOR LOCK command shall return an ABRT error status.
Path 10: Closing the door shall move the device to state A (ready) and shall set the MC bit.

7.5 Status and error posting

The status and errors that are valid for each command are defined in Table 8. It is not a requirement that all valid conditions be implemented. See Clause 6.2.9 and 6.2.13 for the definition of the Error register and Status register bits.

Table 8 - Status and Error Usage

	Status register				Error register					
	DRDY	DF	CORR	ERR	BBK	UNC	IDNF	ABRT	TK0NF	AMNF
ACKNOWLEDGE MEDIA CHANGE	V	V		V				V		
BOOT - POST-BOOT	V	V		V				V		
BOOT - PRE-BOOT	V	V		V				V		
CHECK POWER MODE	V	V		V				V		
DOOR LOCK	V	V		V				V		
DOOR UNLOCK	V	V		V				V		
DOWNLOAD MICROCODE	V	V		V				V		
EXECUTE DEVICE DIAGNOSTIC	V	V		V	See Clause 8.8					
FORMAT TRACK	V	V		V	V	V	V	V	V	V
IDENTIFY DEVICE	V	V		V				V		
IDENTIFY DEVICE DMA	V	V		V				V		
IDLE	V	V		V				V		
IDLE IMMEDIATE	V	V		V				V		
INITIALIZE DEVICE PARAMETERS	V	V								
MEDIA EJECT	V	V		V				V		
NOP	V	V		V				V		
READ BUFFER	V	V		V				V		
READ DMA (w/ retry)	V	V	V	V	V	V	V	V		V
READ DMA (w/o retry)	V	V	V	V	V	V	V	V		V
READ LONG (w/ retry)	V	V		V	V		V	V		V
READ LONG (w/o retry)	V	V		V	V		V	V		V
READ MULTIPLE	V	V	V	V	V	V	V	V		V
READ SECTOR(S) (w/ retry)	V	V	V	V	V	V	V	V		V
READ SECTOR(S) (w/o retry)	V	V	V	V	V	V	V	V		V
READ VERIFY SECTOR(S) (w/ retry)	V	V	V	V	V	V	V	V		V
READ VERIFY SECTOR(S) (w/o retry)	V	V	V	V	V	V	V	V		V
RECALIBRATE	V	V		V				V	V	
SECURE DISABLE	V	V		V				V		
SECURE ENABLE RO	V	V		V				V		
SECURE ENABLE RW	V	V		V				V		
SECURE ENABLE WP	V	V		V				V		
SECURE LOCK	V	V		V				V		
SECURE STATE	V	V		V				V		
SECURE UNLOCK	V	V		V				V		
SEEK	V	V		V			V	V		
SET FEATURES	V	V		V				V		
SET MULTIPLE MODE	V	V		V				V		
SLEEP	V	V		V				V		
SMART DISABLE OPS	V			V				V		
SMART EN/DIS AUTOSAVE	V			V				V		
SMART ENABLE OPS	V			V				V		

SMART READ THRSHOLDS	V			V			V	V		
SMART READ VALUES	V			V			V	V		
SMART RETURN STATUS	V			V				V		
SMART SAVE VALUES	V	V		V			V	V		V
STANDBY	V	V		V				V		
STANDBY IMMEDIATE	V	V		V				V		

Table 8 - Status and Error Usage (cont.)

	Status register				Error register					
	DRDY	DF	CORR	ERR	BBK	UNC	IDNF	ABRT	TK0NF	AMNF
WRITE BUFFER	V	V		V				V		
WRITE DMA (w/ retry)	V	V		V	V		V	V		
WRITE DMA (w/o retry)	V	V		V	V		V	V		
WRITE LONG (w/ retry)	V	V		V	V		V	V		
WRITE LONG (w/o retry)	V	V		V	V		V	V		
WRITE MULTIPLE	V	V		V	V		V	V		
WRITE SECTOR(S) (w/ retry)	V	V		V	V		V	V		
WRITE SECTOR(S) (w/o retry)	V	V		V	V		V	V		
WRITE VERIFY	V	V	V	V	V	V	V	V		V
Invalid command code	V	V		V				V		
Key: V = valid on this command										

7.6 Security mode feature set

The Security Mode Feature Set provides a method for limiting data access to only authorized users or host systems. To accomplish this, the device is placed in secure mode by a user. Having done so, whenever the device is placed in a host, the device must be unlocked before data transfer commands can be executed. Unlocking is accomplished by providing the device with a valid password.

Alternatively, a device may be placed in a write protected mode so that data cannot be accidentally overwritten.

Whether a device supports secure mode can be determined by executing an IDENTIFY DEVICE command. The secure mode state can be determined by issuing a SECURE STATE command (See Clause 8.29).

The device may be set into either Secure Mode Read Only where the device may be read but not written, or Secure Mode Read/Write where no data transfers can be executed. Or, the device may be set into Secure Mode Write Protect where writes are prevented but the device may be removed from this mode without the use of a password.

The device is set into secure mode by a SECURE ENABLE READ ONLY (Clause 8.25) or SECURE ENABLE READ/WRITE (Clause 8.26) command. The user may set up to the maximum number of passwords supported by the device, each password up to 512 bytes in length . The SECURE ENABLE READ ONLY or READ/WRITE command resembles a write command in that the sector count is valid and the command includes the transfer of n sectors of data to the device. Each of the n sectors represents a unique password. If the user defined password contains fewer than 512 bytes, the password is zero filled to complete a full sector by the host, so that a password sent when the device is installed on one system will be exactly the same as a password sent when installed on another system.

When in Secure Mode Read/Write and locked, non-data transfer commands will be executed normally, however, all data transfer commands to the device, i.e., commands that read or modify user data, will be rejected with error. When in Secure Mode Read Only and locked, non-data transfer commands and read commands will be executed normally, however, all write commands to the device, i.e., commands that write or modify user data, will aborted with error. When unlocked, all commands will execute normally.

A device is placed into Secure Mode Write Protect by simply issuing a SECURE ENABLE WRITE PROTECT command (Clause 8.27). This mode requires no password to unlock the device but does prevent writes to the data.

The SECURE DISABLE command will allow the device to be taken out of secure mode (Clause 8.24). If in secure mode and unlocked, a device will accept the SECURE DISABLE command and go out of secure mode and delete all passwords. If the device is in secure mode and has not been unlocked, it will abort the command.

When powered-on, the device will go through the standard startup and the state of secure mode will be noted. If in Secure Mode Read/Write and locked, the device will respond to non-data transfer commands but will abort transfer commands until a SECURE UNLOCK command is received (Clause 8.30). If in Secure Mode Read Only and locked, the device will abort all write commands until a SECURE UNLOCK command is received. The SECURE UNLOCK command again resembles a write command. It must have sector count set at one and will include the transfer of one sector of data to the memory card. When data is received, it will not be written, instead it will be compared to the valid passwords stored. If the received password matches one of the passwords set when secure mode was enabled, the device will unlock and function normally. If no match is found, the command will abort and the extent will remain locked.

When the device is unlocked, a flag tells the device when to relock. It may be set such that the device will automatically lock when powered down or it may require a SECURE LOCK command to lock the device (Clause 8.28). The flag to disable locking at power down is provided for systems that frequently remove power from the device in the course of power management. The passwords remain valid, and normal secure mode locking at power down can be re-enabled by issuing another SECURE UNLOCK command.

When the SECURE UNLOCK command is issued and the device is already in the unlocked state, the command is executed and if the password is not valid, i.e., the command would not have unlocked the extent, the command is aborted. Thus when in unlocked state, passwords can be verified using the SECURE UNLOCK command. The flag for locking the device at power down must be valid when verifying passwords.

The SECURE LOCK command locks the device immediately on receipt.

7.7 Self-monitoring, analysis and reporting technology

The intent of Self-monitoring, analysis and reporting technology (S.M.A.R.T.) is to protect user data and prevent unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, S.M.A.R.T. devices employ sophisticated data analysis algorithms to predict the likelihood of near-term degradation or fault condition. By alerting the host system of a negative reliability status condition, the host system can warn the user of the impending risk of a data loss and advise the user of appropriate action.

Since S.M.A.R.T. utilizes the internal device microprocessor and other device resources, there may be some small overhead associated with its operation. However, special care has been taken in the design of the S.M.A.R.T. algorithms to minimize the impact to host system performance. Actual impact of S.M.A.R.T. overhead is dependent on the specific device design and the usage patterns of the host system. To further ensure minimal impact to the user, S.M.A.R.T. capable devices are shipped from the device manufacturer's factory with the S.M.A.R.T. feature disabled. S.M.A.R.T. capable devices can be enabled by the system OEMs at time of system integration or in the field by aftermarket products.

7.7.1 Attributes

Attributes are the specific performance or calibration parameters that are used in analyzing the status of the device. Attributes are selected by the device manufacturer based on that attribute's ability to contribute to the prediction of degrading or faulty conditions for that particular device. The specific set of attributes being used and the identity of these attributes is vendor specific and proprietary.

7.7.2 Attribute values

Attribute values are used to represent the relative reliability of individual performance or calibration attributes. The valid range of attribute values is from 1 to 253 decimal. Higher attribute values indicate that the analysis algorithms being used by the device are predicting a lower probability of a degrading or faulty condition exisiting. Accordingly, lower attribute values indicate that the analysis algorithms being used by the device are predicting a higher probability of a degrading or faulty condition existing.

7.7.3 Attribute thresholds

Each attribute value has a corresponding attribute threshold limit which is used for direct comparison to the attribute value to indicate the existence of a degrading or faulty condition. The numerical value of the attribute thresholds are determined by the device manufacturer through design and reliability testing and analysis. Each attribute threshold represents the lowest limit to which its corresponding attribute value can be equal while still retaining a positive reliability status. Attribute thresholds are set at the device manufacturer's factory and cannot be changed in the field. The valid range for attribute thresholds is from 1 through 253 decimal.

7.7.4 Threshold exceeded condition

If one or more attribute values are less than or equal to their corresponding attribute thresholds, then the device reliability status is negative, indicating an impending degrading or faulty condition.

7.7.5 S.M.A.R.T. commands

The S.M.A.R.T. commands provide access to attribute values, attribute thresholds and other logging and reproting information. See Clause 8.

7.7.6 S.M.A.R.T. operation with power management modes

It is recomended that, when used in a system that is utilizing the Power Management Feature set, a S.M.A.R.T. enabled device automatically saves its attribute values upon receipt of an IDLE IMMEDIATE, STANDBY IMMEDIATE or SLEEP command. If the device has been set to utilize the Standby timer, it is recommended that the device automatically perform a SAVE ATTRIBUTE VALUES function prior to going from an Idle state to the Standby state.

8 Command descriptions

Commands are issued to the device by loading the pertinent registers in the command block with the needed parameters, and then writing the command code to the Command register.

Upon receipt of a command, the device sets the BSY bit or the DRQ bit within 400 nsec. Following the setting of BSY bit equal to one or BSY bit equal to zero and DRQ bit equal to one, the status presented by the device depends on the type of command: PIO data in, PIO data out, non-data transfer or DMA. See the individual command descriptions and Clause 9 for the protocol followed by each command and command type.

Note: Some older host implementations may require the BSY bit being cleared to zero and the DRQ bit equal to one in the Status register within 700 nsec of receiving some PIO data out commands.

Note: For the power mode related commands, it is recommended that the host utilize E0h through E3h, E5h and E6h command values. While command values 94h through 99h command values are valid, they should be considered obsolete and may be removed in future versions of this standard.

In Table 9, the “proto” column codes represent the command protocol used:

DM - A DMA command.
ND - A non data command.
PI - A PIO data in command.
PO - A PIO data out command.
VS - A Vendor specific command.

In Table 9, the “typ” column codes represent the command type:

O - Optional—the implementation of this command is optional.
M - Mandatory—all ATA devices shall implement this command.
R - Reserved for use in future ATA standards.
V - Vendor specific implementation.

Table 9 - Command Codes and Parameters

proto	Command	typ	Command Code	Parameters Used				
				FR	SC	SN	CY	DH
VS	ACKNOWLEDGE MEDIA CHANGE	O	DBh					D
VS	BOOT - POST-BOOT	O	DCh					D
VS	BOOT - PRE-BOOT	O	DDh					D
ND	CHECK POWER MODE	O	98h E5h		y			D
VS	DOOR LOCK	O	DEh					D
VS	DOOR UNLOCK	O	DFh					D
PO	DOWNLOAD MICROCODE	O	92h	y	y	y	y	D
ND	EXECUTE DEVICE DIAGNOSTIC	M	90h					D*
VS	FORMAT TRACK	V	50h					d
PI	IDENTIFY DEVICE	M	ECh					D
DM	IDENTIFY DEVICE DMA	O	EEh					D
ND	IDLE	O	97h E3h		y			D
ND	IDLE IMMEDIATE	O	95h E1h					D
ND	INITIALIZE DEVICE PARAMETERS	M	91h		y			y
ND	MEDIA EJECT	O	EDh					D
ND	NOP	O	00h					y
PI	READ BUFFER	O	E4h					D
DM	READ DMA (w/ retry)	O	C8h		y	y	y	y

Table 9 - Command Codes and Parameters (cont.)

proto	Command	typ	Command	Parameters Used

			Code	FR	SC	SN	CY	DH
DM	READ DMA (w/o retry)	O	C9h		y	y	y	y
PI	READ LONG (w/ retry)	O	22h		y	y	y	y
PI	READ LONG (w/o retry)	O	23h		y	y	y	y
PI	READ MULTIPLE	O	C4h		y	y	y	y
PI	READ SECTOR(S) (w/ retry)	M	20h		y	y	y	y
PI	READ SECTOR(S) (w/o retry)	M	21h		y	y	y	y
ND	READ VERIFY SECTOR(S) (w/ retry)	M	40h		y	y	y	y
ND	READ VERIFY SECTOR(S) (w/o retry)	M	41h		y	y	y	y
ND	RECALIBRATE	O	1Xh					D
ND	SECURE DISABLE	O	EAh	y				D
PO	SECURE ENABLE RO	O	EBh	y	y			D
PO	SECURE ENABLE RW	O	EBh	y	y			D
ND	SECURE ENABLE WP	O	EAh	y				D
ND	SECURE LOCK	O	EAh	y				D
ND	SECURE STATE	O	EAh	y				D
PO	SECURE UNLOCK	O	EBh	y	y			D
ND	SEEK	M	7Xh			y	y	y
ND	SET FEATURES	O	EFh	y				D
ND	SET MULTIPLE MODE	O	C6h		y			D
ND	SLEEP	O	99h E6h					D
ND	SMART DISABLE OPERATIONS	O	0B0h	y			y	D
ND	SMART ENABLE/DISABLE AUTOSAV	O	0B0h	y	y		y	D
ND	SMART ENABLE OPERATIONS	O	0B0h	y			y	D
PI	SMART READ THRESHOLDS	O	0B0h	y			y	D
PI	SMART READ VALUES	O	0B0h	y			y	D
ND	SMART RETURN STATUS	O	0B0h	y			y	D
ND	SMART SAVE VALUES	O	0B0h	y			y	D
ND	STANDBY	O	96h E2h		y			D
ND	STANDBY IMMEDIATE	O	94h E0h					D
PO	WRITE BUFFER	O	E8h					D
DM	WRITE DMA (w/ retry)	O	CAh		y	y	y	y
DM	WRITE DMA (w/o retry)	O	CBh		y	y	y	y
PO	WRITE LONG (w/ retry)	O	32h	*	y	y	y	y
PO	WRITE LONG (w/o retry)	O	33h	*	y	y	y	y
PO	WRITE MULTIPLE	O	C5h	*	y	y	y	y
PO	WRITE SECTOR(S) (w/ retry)	M	30h	*	y	y	y	y
PO	WRITE SECTOR(S) (w/o retry)	M	31h	*	y	y	y	y
PO	WRITE VERIFY	O	3Ch	*	y	y	y	y
VS	Vendor specific	V	9Ah,C0h-C3h,8xh, F0h-FFh					
-	Reserved: all remaining codes	R						

Key:
CY = Cylinder registers SC = Sector Count register DH = Device/Head register
SN = Sector Number register FR = Features register (see command descriptions for use)
y = the register contains a valid parameter for this command. For the Device/Head register, y means both the device and head parameters are used.
D = only the device parameter is valid and not the head parameter.
d = the device parameter is valid, the usage of the head parameter vendor specific.
D* = Addressed to device 0 but both devices execute it.
* = Maintained for compatibility (see Clause 6.2.10)

Each command description in the following sections contain the following subsections:

OPCODE - Indicates the command code for this command.

TYPE - Indicates if the command is mandatory, optional or vendor specific and, if the command is a member of one or more feature sets, which feature sets it belongs to.

PROTOCOL - Indicates which protocol is used by the command.

INPUTS - Describes the Command Block register data that the host shall supply.

NORMAL OUTPUTS - Describes the Command Block register data that shall be returned by the device at the end of a command. The Status register shall always be valid and, if the ERR bit in the Status register is set to one, then the Error register shall be valid.

ERROR OUTPUTS - Describes the Command Block register data that shall be returned by the device at the end of a command which completes with an unrecoverable error.

PREREQUISITES - Any prerequisite commands or conditions that shall be met before the command can be issued.

DESCRIPTION - The description of the command function(s).

8.1 ACKNOWLEDGE MEDIA CHANGE

OPCODE - DBh

TYPE - Optional - Removable.

PROTOCOL - Vendor specific.

INPUTS - Vendor specific.

NORMAL OUTPUTS - Vendor specific.

ERROR OUTPUTS - Vendor specific or if the device does not support this command, the device shall return a Command Abort error.

PREREQUISITES - Vendor specific.

DESCRIPTION - This command is reserved for use by removable media devices. The implementation of this command is vendor specific.

8.2 BOOT - POST-BOOT

OPCODE - DCh

TYPE - Optional - Removable.

PROTOCOL - Vendor specific.

INPUTS - Vendor specific.

NORMAL OUTPUTS - Vendor specific.

ERROR OUTPUTS - Vendor specific or if the device does not support this command, the device shall return a Command Abort error.

PREREQUISITES - Vendor specific.

DESCRIPTION - This command is reserved for use by removable media devices. The implementation of this command is vendor specific.

8.3 BOOT - PRE-BOOT

OPCODE - DDh

TYPE - Optional - Removable.

PROTOCOL - Vendor specific.

INPUTS - Vendor specific.

NORMAL OUTPUTS - Vendor specific.

ERROR OUTPUTS - Vendor specific or if the device does not support this command, the device shall return a Command Abort error.

PREREQUISITES - Vendor specific.

DESCRIPTION - This command is reserved for use by removable media devices. The implementation of this command is vendor specific.

8.4 CHECK POWER MODE

OPCODE - 98h or E5h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - None.

NORMAL OUTPUTS - The Sector Count register is set to 0 (00h) if the device in Standby mode. The Sector Count register is set to 128 (80h) if the device in Idle Mode. The Sector Count register is set to 255 (FFh) if the device is in Active mode.

ERROR OUTPUTS - Aborted Command if the device does not support the Power Management command set.

PREREQUISITES - None.

DESCRIPTION - If the device is in the Standby Mode the device shall set the BSY bit, set the Sector Count register to 0 (00h), clear the BSY bit, and assert INTRQ.

If the device is in the Idle Mode, the device shall set BSY, set the Sector Count register to 128 (80h), clear BSY, and assert INTRQ.

If the device is in Active Mode, the device shall set the BSY bit, set the Sector Count register to 255 (FFh), clear the BSY bit, and assert INTRQ.

8.5 DOOR LOCK

OPCODE - DEh

TYPE - Optional - Removable.

PROTOCOL - Non-data command.

INPUTS - None.

NORMAL OUTPUTS - None.

ERROR OUTPUTS - If the device is not ready or is not capable of locking the media, the ABRT bit in the Error register and the ERR bit in the Status register shall be returned.

If the device is already locked and the media change request button is active, then a Media Change Requested status shall be returned by setting the MCR bit in the Error register and the ERR bit in the Status register.

PREREQUISITES - None.

DESCRIPTION - This command either locks the device or media, or provides the status of the media change request button.

If the device is not locked, the device shall be set to the locked state and good status returned.

If the device is locked, the status returned shall indicate the state of the media change request button. Good status shall be returned while the media change request button is not active, and the MCR bit in the Error register and the ERR bit in the Status register shall be returned when the media change request button is active.

When a device is in a DOOR LOCKED state, the device shall not respond to the media change request button, except by setting the MCR status, until the DOOR LOCKED condition is cleared. A DOOR LOCK condition shall be cleared by a DOOR UNLOCK or MEDIA EJECT command, or by a hardware device reset.

8.6 DOOR UNLOCK

OPCODE - DFh

TYPE - Optional - Removable.

PROTOCOL - Non-data command.

INPUTS - None.

NORMAL OUTPUTS - None.

ERROR OUTPUTS - If the device does not support this command or is not ready, then the ABRT bit shall be returned in the Error register and the ERR bit shall be returned in the Status register.

PREREQUISITES - None.

DESCRIPTION - This command shall unlock the device, if it is locked, and shall allow the device to respond to the media change request button.

8.7 DOWNLOAD MICROCODE

OPCODE - 92h

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The head bits of the Device/Head register shall always be set to zero. The Cylinder High and Low registers shall be set to zero. The Sector Number and Sector Count registers are used together as a 16-bit sector count value. The Feature register specifies the subcommand code.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the device does not support this command or did not accept the microcode data.

PREREQUISITES - None.

DESCRIPTION - This command enables the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE command is vendor specific.

All transfers shall be an integer multiple of the sector size. The size of the data transfer is determined by the contents of the Sector Number Register and the Sector Count register. The Sector Number Register shall be used to extend the Sector Count register, to create a sixteen bit sector count value. The Sector Number Register shall be the most significant eight bits and the Sector Count register shall be the least significant eight bits. A value of zero in both the Sector Number Register and the Sector Count register shall indicate no data is to be transferred. This allows transfer sizes from 0 bytes to 33 553 920 bytes, in 512 byte increments.

The Features register shall be used to determine the effect of the DOWNLOAD MICROCODE command. The values for the Feature Register are:

01h - download is for immediate, temporary use
07h - save downloaded code for immediate and future use

All other values are reserved.

8.8 EXECUTE DEVICE DIAGNOSTIC

OPCODE - 90h

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - None, except that the device selection bit in the Device/Head register is ignored.

NORMAL OUTPUTS - The diagnostic code written into the Error register is an 8-bit code as shown in Table 10, and not as defined in Clause 6.2.9.

Table 10 - Diagnostic Codes

Code	Description
01h	Device 0 passed, Device 1 passed or not present
00h, 02h-7Fh	Device 0 failed, Device 1 passed or not present
81h	Device 0 passed, Device 1 failed
80h, 82h-FFh	Device 0 failed, Device 1 failed

The meaning of values other than 01h and 81h are vendor specific and should be considered a diagnostic failed condition.

ERROR OUTPUTS - None. All error information is returned as a diagnostic code in the Error register.

PREREQUISITES - None.

DESCRIPTION - This command shall perform the internal diagnostic tests implemented by the device. See also Clause 6.2.9 and 6.2.13. The DEV bit in the Drive/Head register is ignored. Both devices, if present, shall execute this command.

Device 0 performs the following operations for this command:

a) Device 0 sets the BSY bit within 400 nsec after the EXECUTE DEVICE DIAGNOSTIC command is received.

b) Device 0 performs diagnostics.

c) Device 0 resets the Command Block registers to the following:

Cylinder Low	=	00h	Cylinder High	=	00h
Sector Count	=	01h	Device/Head	=	00h
Sector Number	=	01h			

d) Device 0 posts diagnostic results to bits 6-0 of the Error Register.

e) If Device 0 detected that Device 1 is present during the most recent power on or hardware reset sequence, then Device 0 waits up to 6 sec from the time that the EXECUTE DEVICE DIAGNOSTIC command was received for Device 1 to assert PDIAG-. If PDIAG- is asserted within 6 sec, Device 0 clears bit 7 to zero in the Error Register, else Device 0 sets bit 7 equal to 1 in the Error Register.

   If device 1 was not detected during the most recent power up or hardware reset sequence, then Device 0 clears bit 7 to zero in the Error register.

f) Device 0 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1.

NOTE: Device 0 shall clear the BSY bit within 6 sec from the time that the EXECUTE DEVICE DIAGNOSTIC command was received.

g) Device 0 sets the DRDY bit when ready to accept any command.

NOTE: Steps f) and g) may occur at the same time. While no maximum time is specified for the DRDY bit to be set to one to occur, a host is advised to allow up to 30 sec for the DRDY bit to be set to one. See Figure 5.

Device 1 performs the following operations for this command:

a) Device 1 sets the BSY bit within 400 nsec after the EXECUTE DEVICE DIAGNOSTIC command is received.

b) Device 1 negates PDIAG- within 1 msec after the command is received.

c) Device 1 performs diagnostics.

d) Device 1 resets the Command Block registers to the following:

Cylinder Low	=	00h	Cylinder High	=	00h
Sector Count	=	01h	Device/Head	=	00h
Sector Number	=	01h			

e) Device 1 clears bit 7 of the Error register to zero and posts its diagnostic results to bits 6 through 0 of Error register.

f) Device 1 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to one.

g) If Device 1 passed its diagnostics without error in step c), Device 1 asserts PDIAG-. If the diagnostics failed, Device 1 does not assert PDIAG- and continues to the next step.

NOTE: Device 1 shall clear the BSY bit and assert PDIAG- within 5 sec of the time that the EXECUTE DEVICE DIAGNOSTIC command is received.

h) Device 1 sets the DRDY bit when ready to accept any command.

NOTE: Steps f), g) and h) may occur at the same time. While no maximum time is specified for the DRDY bit to set to one, a host is advised to allow up to 30 sec for the DRDY bit to be equal to one. See Figure 5.

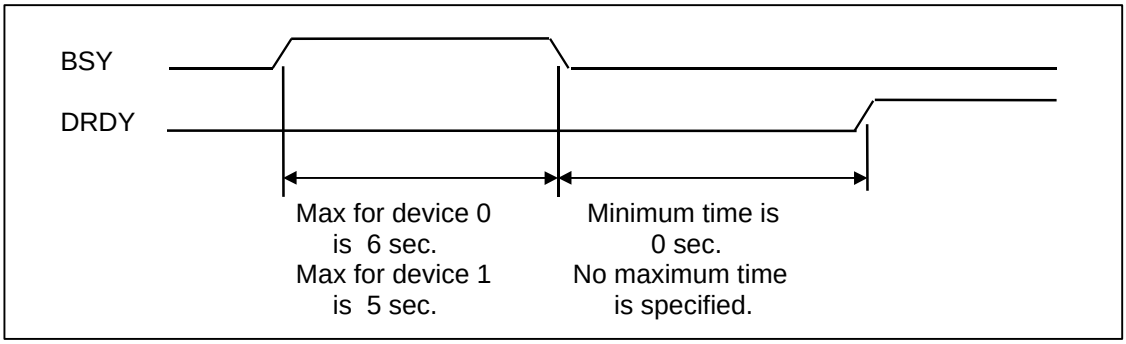


Figure 5 - BSY and DRDY timing for Diagnostic command

8.9 FORMAT TRACK

OPCODE - 50h

TYPE - Vendor specific.

PROTOCOL - Vendor specific.

INPUTS - Vendor specific.

NORMAL OUTPUTS - Vendor specific.

ERROR OUTPUTS - Aborted Command if the device does not support this command. All other errors are vendor specific.

PREREQUISITES - Vendor specific.

DESCRIPTION - The implementation of the FORMAT TRACK command is vendor specific. It is recommend that system implementations not utilize this command.

8.10 IDENTIFY DEVICE

OPCODE - ECh

TYPE - Mandatory

PROTOCOL - PIO data in.

INPUTS - None.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - None.

PREREQUISITES - None.

DESCRIPTION - The IDENTIFY DEVICE command enables the host to receive parameter information from the device.

Some devices may have to read the media in order to complete this command.

When the command is issued, the device sets the BSY bit, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit, clears the BSY bit, and generates an interrupt. The host can then transfer the data by reading the Data register. The parameter words in the buffer have the arrangement and meanings defined in Table 11. All reserved bits or words shall be zero.

The F/V column indicates if the word or part of a word has fixed (F) contents that do not change, variable (V) contents that may change depending on the device state or the commands executed by the device, X for words with vendor specific data which may be fixed or variable, and R for reserved words which shall be zero. For removable media devices, the value of fields indicated as fixed (F) may change when media is removed or changed.

Some parameters are defined as a group of bits. A word which is defined as a set of bits is transmitted with indicated bits on the respective data bus bit (e.g., bit 15 appears on DD15).

Some parameters are defined as a sixteen bit value. A word which is defined as a sixteen bit value places the most significant bit of the value on bit DD15 and the least significant bit on bit DD0.

Some parameters are defined as 32 bit values (e.g., words 57 and 58). Such fields are transferred using two word transfers. The device shall first transfer the least significant bits, bits 15 through 0 of the value, on bits DD (15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits 31 through 16 of the value, shall be transferred on DD (15:0) respectively.

Some parameters are defined as a string of ASCII characters. For the string “Copyright”, the character ‘C’ is the first byte, ‘o’ is the 2nd byte, etc. When such fields are transferred, the order of transmission is:

the 1st character (‘C’) is on bits DD (15:8) of the first word
the 2nd character (‘o’) is on bits DD (7:0) of the first word
the 3rd character (‘p’) is on bits DD (15:8) of the second word
the 4th character (‘y’) is on bits DD (7:0) of the second word
etc.

If the device has been configured for eight bit transfers, then each word as defined in this table is transferred as described in Clause 3.2.5.

Table 11 - Identify Device Information

Word	F/V		
0		General configuration bit-significant information:	
	F	15	0=ATA device 1=ATAPI device
	F	14	Vendor specific (obsolete)
	F	13	Vendor specific (obsolete)
	F	12	Vendor specific (obsolete)
	F	11	Vendor specific (obsolete)
	F	10	Vendor specific (obsolete)
	F	9	Vendor specific (obsolete)
	F	8	Vendor specific (obsolete)
	F	7	1=removable media device
	F	6	1=not removable controller and/or device
	F	5	Vendor specific (obsolete)
	F	4	Vendor specific (obsolete)
	F	3	Vendor specific (obsolete)
	F	2	Vendor specific (obsolete)
	F	1	Vendor specific (obsolete)
	F	0	Reserved
1	F	Number of logical cylinders	
2	R	Reserved	
3	F	Number of logical heads	
4	X	Vendor specific (obsolete)	
5	X	Vendor specific (obsolete)	
6	F	Number of logical sectors per logical track	
7-9	X	Vendor specific	
10-19	F	Serial number	
20	X	Vendor specific (obsolete)	
21	X	Vendor specific (obsolete)	
22	F	Number of vendor specific bytes available on READ/WRITE LONG cmds	
23-26	F	Firmware revision (8 ASCII characters)	
27-46	F	Model number (40 ASCII characters)	
47	X	15-8	Vendor specific
	F	7-0	00h = READ/WRITE MULTIPLE commands not implemented
	F		01h-FFh = Maximum number of sectors that can be transferred per interrupt on READ/WRITE MULTIPLE commands
48	R	Reserved	
49		Capabilities	
	R	15-14	Reserved
	F	13	1=Standby timer values as specified in this standard aresupported 0=Standby timer values are vendor specific
	R	12	Reserved (for advanced transfer mode)
	F	11	1=IORDY supported 0=IORDY may be supported
	F	10	1=IORDY can be disabled
	F	9	1=LBA supported
	F	8	1=DMA supported
	X	7-0	Vendor specific
50	F	15	1=Security Mode Feature Set Supported
		14-8	Maximum number of passwords supported
51	F	15-8	PIO data transfer cycle timing mode
	X	7-0	Vendor specific
52	F	15-8	DMA data transfer cycle timing mode
	X	7-0	Vendor specific

Table 11 - Identify Device Information (cont)

Word	F/V	
53	R	15-2 Reserved
	F	1 1=the fields reported in words 64-70 are valid
	F	0=the fields reported in words 64-70 are not valid
	V	0 1=the fields reported in words 54-58 are valid
	V	0=the fields reported in words 54-58 may be valid
54	V	Number of current logical cylinders
55	V	Number of current logical heads
56	V	Number of current logical sectors per track
57-58	V	Current capacity in sectors
59	R	15-9 Reserved
	V	8 1=Multiple sector setting is valid
	V	7-0 xxh=Current setting for number of sectors that can be transferred per interrupt on R/W Multiple command
60-61	F	Total number of user addressable sectors (LBA mode only)
62	V	15-8 Single word DMA transfer mode active
	F	7-0 Single word DMA transfer modes supported
63	V	15-8 Multiword DMA transfer mode active
	F	7-0 Multiword DMA transfer modes supported
64	R	15-8 Reserved
	F	7-0 Advanced PIO transfer modes supported
65		Minimum Multiword DMA transfer cycle time per word
	F	15-0 Cycle time in nanoseconds
66		Manufacturer's recommended Multiword DMA transfer cycle time
	F	15-0 Cycle time in nanoseconds
67		Minimum PIO transfer cycle time without flow control
	F	15-0 Cycle time in nanoseconds
68		Minimum PIO transfer cycle time with IORDY flow control
	F	15-0 Cycle time in nanoseconds
69-72	R	Reserved (for advanced PIO mode support)
73	F	Major version number
	(1)	0000h or FFFFh = device does not report version
		15 Reserved
		14 Reserved for ATA-14
		13 Reserved for ATA-13
		12 Reserved for ATA-12
		11 Reserved for ATA-11
		10 Reserved for ATA-10
		9 Reserved for ATA-9
		8 Reserved for ATA-8
		7 Reserved for ATA-7
		6 Reserved for ATA-6
		5 Reserved for ATA-5
		4 Reserved for ATA-4
		3 If 15-0 not 0000h 1=supports ATA-3
		2 If 15-0 not 0000h 1=supports ATA-2
		1 If 15-0 not 0000h 1=supports ATA-1

Table 11 - Identify Device Information (cont.)

Word	F/V	
74	F	Minor version number
	(1)	0000h or FFFFh=device does not report version
		0001h-FFFEh=see clause 8.10.37

75-127	R	Reserved
128-159	X	Vendor specific
160-255	R	Reserved

Notes:
(1) Words 73 and 74 are allowed to change between the power on reset condition and the device's first access to vendor specified data stored on the media.

8.10.1 Word 0: General configuration

Devices that conform to this standard shall clear bit 15 to zero. These values are shown to maintain alignment with the X3T10/1120 standard.

8.10.2 Word 1: Number of cylinders

The number of user-addressable logical cylinders in the default translation mode.

8.10.3 Word 2: Reserved.

8.10.4 Word 3: Number of logical heads

The number of user-addressable logical heads per logical cylinder in the default translation mode.

8.10.5 Word 4: Vendor specific data.

8.10.6 Word 5: Vendor specific data.

8.10.7 Word 6: Number of logical sectors per logical track

The number of user-addressable logical sectors per logical track in the default translation mode.

8.10.8 Words 7-9: Vendor specific data.

8.10.9 Words 10-19: Serial number

If word 10 of this field is 0000h, then the serial number is not specified and the definition of the remaining words of this field are vendor specific.

If word 10 of this field is not equal to 0000h, then this field contains the serial number of the device. The contents of this field is an ASCII character string of twenty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

8.10.10 Word 20: Vendor specific data.

8.10.11 Word 21: Vendor specific data.

8.10.12 Word 22: Number of vendor specific bytes on READ/WRITE LONG commands

The contents of this field specifies the number of vendor specific bytes that are appropriate for the device. If the contents of this field are set to a value other than 4, the SET FEATURES command should be used to switch the length of READ LONG and WRITE LONG commands from 512 plus 4 to 512 plus the value specified in this word.

8.10.13 Word 23-26: Firmware revision

If word 23 of this field is 0000h, then the firmware revision is not specified and the definition of the remaining words of this field are vendor specific.

If word 23 of this field is not equal to 0000h, then this field contains the firmware revision of the device. The contents of this field is an ASCII character string of eight bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

8.10.14 Words 27-46: Model number

If word 27 of this field is 0000h, then the model number is not specified and the definition of the remaining words of this field are vendor specific.

If word 27 of this field is not equal to 0000h, then this field contains the model number of the device. The contents of this field is an ASCII character string of forty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

8.10.15 Word 47: READ/WRITE MULTIPLE support.

Bits 7-0 of this word define the maximum number of sectors per block that the device supports for READ/WRITE MULTIPLE commands. If a device supports the READ/WRITE MULTIPLE and SET MULTIPLE MODE commands, these bits contain a non-zero value. If the device does not support the READ/WRITE MULTIPLE and SET MULTIPLE MODE commands, these bits shall be zero.

8.10.16 Word 48: Reserved.

8.10.17 Word 49: Capabilities

8.10.17.1 Standby timer support

Bit 13 of word 49 is used to determine whether a device utilizes the Standby Timer Values as defined in this standard. If bit 13 is set to one, then the device utilizes the Standby Timer values as specified in Table 13 . If bit 13 is cleared to zero, the timer values utilized are vendor specific.

8.10.17.2 IORDY support

Bit 11 of word 49 is used to help determine whether a device supports IORDY. If this bit is set to one, then the device supports IORDY operation. If this bit is zero, the device may support IORDY. This insures backward compatibility. If a device supports PIO Mode 3, then this bit shall be set.

8.10.17.3 IORDY can be disabled

Bit 10 of word 49 is used to indicate a device's ability to enable or disable the use of IORDY. If this bit is set to one, then the device supports the disabling of IORDY. Control of IORDY is accomplished using the SET FEATURES command.

8.10.17.4 LBA supported

Bit 9 of word 49 is used to indicate if the device supports LBA mode addressing. If this bit is set, words 60-61 shall be valid.

8.10.17.5 DMA supported

Bit 8 of word 49 is used to indicate if the device supports the READ/WRITE DMA commands.

8.10.18 Word 50: Security mode

Bit 15 of word 50 is used to indicate the device supports the Security Mode Feature Set. The field, bits 14-8, indicate the maximum number of passwords the device can support including the Emergency password.

8.10.19 Word 51: PIO data transfer cycle timing mode

The PIO transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in Figure 12 with the contents of this field. The value returned in Bits 15-8 should fall into one of the mode 0 through mode 2 categories specified in Figure 12, and if it does not, then Mode 0 shall be used to serve as the default timing.

> Note: For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode (i.e. PIO mode 0, 1, or 2) it can support.

8.10.20 Word 52: Single word DMA data transfer cycle timing mode

The DMA transfer timing for each ATA device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the Cycle Time specified in Figure 13 with the contents of this field. The value returned in Bits 15-8 should fall into one of the categories specified in Figure 13 (i.e. 0, 1, or 2), and if it does not, then Mode 0 shall be used to serve as the default timing.

The contents of this word shall be ignored if Words 62 or 63 are supported.

8.10.21 Word 53: Field validity

If bit 0 of word 53 is set, then the values reported in words 54 through 58 are valid. If this bit is cleared, the values reported in words 54 through 58 may be valid. If bit 1 of word 53 is set, then the values reported in words 64 through 70 are valid. If this bit is cleared, the values reported in words 64-70 are not valid. Any device which supports PIO Mode 3 or above, or supports Multiword DMA Mode 1 or above, shall set bit 1 of word 53 and support the fields contained in words 64 through 70.

8.10.22 Word 54: Number of current logical cylinders

The number of user-addressable logical cylinders in the current translation mode.

> Note: For ATA-1 devices, if the INITIALIZE DEVICE PARAMETERS command has not been issued to the device then the value of this word is vendor specific.

8.10.23 Word 55: Number of current logical heads

The number of user-addressable logical heads per logical cylinder in the current translation mode.

> Note: For ATA-1 devices, if the INITIALIZE DEVICE PARAMETERS command has not been issued to the device then the value of this word is vendor specific.

8.10.24 Word 56: Number of current logical sectors per logical track

The number of user-addressable logical sectors per logical track in the current translation mode.

> Note: For ATA-1 devices, if the INITIALIZE DEVICE PARAMETERS command has not been issued to the device then the value of this word is vendor specific.

8.10.25 Word 57-58: Current capacity in sectors

The current capacity in sectors excludes all sectors used for device-specific purposes. The value reported in this field shall be the product of words 54, 55 and 56.

8.10.26 Word 59: Multiple sector setting

If bit 8 is set, then bits 7-0 reflect the number of sectors currently set to transfer on a READ/WRITE MULTIPLE command. If word 47 bits 7-0 are zero then word 59 bits 8-0 shall also be zero.

8.10.27 Word 60-61: Total number of user addressable sectors

If the device supports LBA Mode, these words reflect the total number of user addressable sectors. This value does not depend on the current device geometry. If the device does not support LBA mode, these words shall be set to 0.

8.10.28 Word 62: Single word DMA transfer

The low order byte identifies by bit all of the Modes which are supported e.g. if Mode 0 is supported, bit 0 is set. The high order byte contains a single bit set to indicate which mode is active.

8.10.29 Word 63: Multiword DMA transfer

The low order byte identifies by bit all of the Modes which are supported e.g. if Mode 0 is supported, bit 0 is set. The high order byte contains a single bit set to indicate which mode is active.

8.10.30 Word 64: Flow control PIO transfer modes supported

Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the Advanced PIO Data Transfer Supported Field. This field is bit significant. Any number of bits may be set in this field by the device to indicate which Advanced PIO Modes that it is capable of supporting.

Of these bits, bits 7 through 2 are Reserved for future Advanced PIO Modes. Bit 0, if set, indicates that the device supports PIO Mode 3. Bit 1, if set, indicates that the device supports PIO Mode 4.

> Note: For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the highest original PIO mode (i.e. PIO mode 0, 1, or 2) it can support.

8.10.31 Word 65: Minimum multiword DMA transfer cycle time per word

Word 65 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum Multiword DMA Transfer Cycle Time Per Word. This field defines, in nanoseconds, the minimum cycle time that the device can support when performing Multiword DMA transfers on a per word basis.

If this field is supported, bit 1 of word 53 shall be set. Any device which supports Multiword DMA Mode 1 or above shall support this field, and the value in word 65 shall not be less than the minimum cycle time reported by the fastest DMA mode supported by the device.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

8.10.32 Word 66: Manufacturer's recommended multiword DMA cycle time

Word 66 of the parameter information of the IDENTIFY DEVICE command is defined as the Manufacturer's Recommended Multiword DMA Transfer Cycle Time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA commands over all locations on the media under nominal conditions. If a host runs at a faster cycle

rate by operating at a cycle time of less than this value, the device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycled rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance MAY result.

If this field is supported, bit 1 of word 53 shall be set. Any device which supports Multiword DMA Mode 1 or above shall support this field, and the value in word 66 shall not be less than the value in word 65.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

8.10.33 Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum PIO Transfer Without Flow Control Cycle Time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of flow control.

Any device may support this field, and if this field is supported, Bit 1 of word 53 shall be set.

Any device which supports PIO Mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

8.10.34 Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the IDENTIFY DEVICE command is defined as the Minimum PIO Transfer With IORDY Flow Control Cycle Time. This field defines, in nanoseconds, the minimum cycle time that the device can support while performing data transfers while utilizing IORDY flow control.

Any device may support this field, and if this field is supported, Bit 1 of word 53 shall be set.

Any device which supports PIO Mode 3 or above shall support this field, and the value in word 68 shall not be less than the fastest PIO mode reported by the device.

If bit 1 of word 53 is set because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

8.10.35 Words 69-72: Reserved for future PIO modes.

Words 69 and 72 are reserved for future advanced PIO modes

8.10.36 Word 73: Major version number

If not 0000h or FFFFh, the device claims compliance with the major version(s) as indicated by bits 1 through 3 being equal to one. Values other than 0000h and FFFFh are bit significant. Since the ATA-3 and ATA-2 standards maintain downward compatibility with ATA-1 (published as ATA), it is allowed for an ATA-3 device to set all of bits 1 through 3 to one.

8.10.37 Word 74: Minor version number

If an implementor claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to this revision of the standard, Word 74 shall be 0000h or FFFFh.

A revision of the standard which guided the implementation may optionally be reported in Word 74 as shown in Table 12.

Table 12 - Minor version number

Value	Minor revision
0001h	ATA (ATA-1) X3T9.2 781D prior to revision 4
0003h	ATA (ATA-1) X3T9.2 781D revision 4
0005h	ATA-2 X3T10 948D prior to revision 2k
0007h	ATA-2 X3T10 948D revision 2k
0009h	ATA-2 X3T10 948D revision 3
0008h	ATA-3 X3T10 2008D revision 0
0006h	ATA-3 X3T10 2008D revision 1
0002h, 0004h, 000Ah-FFFFh	Reserved

8.10.38 Words 75-127: Reserved.

8.10.39 Words 128-159: Vendor specific.

8.10.40 Words 160-255: Reserved.

8.11 IDENTIFY DEVICE DMA

OPCODE - EEh

TYPE - Optional

PROTOCOL - DMA

INPUTS - None.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - None.

PREREQUISITES - None.

DESCRIPTION - The IDENTIFY DEVICE DMA command enables the host to receive parameter information from the device. The command transfers the same 256 words of device identification data as transferred by the IDENTIFY DEVICE command.

8.12 IDLE

OPCODE - 97h or E3h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - The value in the Sector Count register when the IDLE command is issued shall determine the time period programmed into the Standby Timer. See Table 13.

Table 13 - Automatic Standby Timer Periods

Sector Count Register contents		Corresponding Timeout Period
0	(00h)	Timeout Disabled
1-240	(01h-F0h)	(value * 5) sec
241-251	(F1h-FBh)	((value - 240) * 30) min
252	(FCh)	21 min
253	(FDh)	Period between 8 and 12 hrs
254	(FEh)	Reserved
255	(FFh)	21 min 15 sec

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command - The device does not support the Power Management command set.

PREREQUISITES - None.

DESCRIPTION - This command causes the device to set the BSY bit, enter the Idle Mode, clear the BSY bit, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Idle Mode.

If the Sector Count register is non-zero then the Standby Timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby Timer.

If the Sector Count register is zero then the Standby Timer is disabled.

8.13 IDLE IMMEDIATE

OPCODE - 95h or E1h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - None.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command - The device does not support the Power Management command set.

PREREQUISITES - None.

DESCRIPTION - This command causes the device to set the BSY bit, enter the Idle Mode, clear the BSY bit, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Idle Mode.

8.14 INITIALIZE DEVICE PARAMETERS

OPCODE - 91h

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - The Sector Count register specifies the number of logical sectors per logical track, and the Device/Head register which specifies the number of logical heads minus 1.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the device does not support the requested CHS translation.

> Note: Previous ATA specifications were unclear about the error conditions that this command may indicate. Some implementations do not indicate any errors for this command even when the command fails. However, most of these implementations do fail media access commands if a valid CHS translation is not in effect.

PREREQUISITES - None.

DESCRIPTION - This command enables the host to set the number of logical sectors per track and the number of logical heads minus 1, per logical cylinder for the current CHS translation mode.

Upon receipt of the command, the device sets the BSY bit, saves the parameters, clears the BSY bit, and generates an interrupt.

A device shall support the CHS translation described in words 1, 3 and 6 of the IDENTIFY DEVICE information. Support of other CHS translations is optional.

If the requested CHS translation is not supported, the device shall set the Error bit in the Status register and set the Aborted Command bit in the Error register before clearing the BSY bit in the Status register.

If the requested CHS translation is not supported, the device shall fail all media access commands with an ID Not Found error until a valid CHS translation is established.

> Note: Host implementations should use the default CHS translation mode described in words 1, 3 and 6 of the IDENTIFY DEVICE information. Future ATA specifications may restrict the valid input parameters for this command to these values.
>
> Note: Some ATA-1 devices require that this command be issued prior to media access.

8.15 MEDIA EJECT

OPCODE - EDh

TYPE - Optional - Removable.

PROTOCOL - Non-data.

INPUTS - None required.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - If the device does not support this command, the device shall return a Command Abort error.

PREREQUISITES - None.

DESCRIPTION - This command completes any pending operations, spins down the device if needed, unlocks the door or media if locked, and initiates a media eject, if required.

8.16 NOP

OPCODE - 00h

TYPE - Optional.

PROTOCOL - Non-data.

INPUTS - None required.

NORMAL OUTPUTS - The Command Block registers, other than the Error and Status registers, are not changed by this command.

ERROR OUTPUTS - This command always fails with a Aborted Command error.

PREREQUISITES - None.

DESCRIPTION - This command enables a host which can only perform 16-bit register accesses to check device status. The device shall respond as it does to an unrecognized command by setting Aborted Command in the Error register, Error in the Status register, clearing Busy in the Status register, and asserting INTRQ.

NOTE: When a 16-bit host writes to the Device/Head Register, one byte contains the Command register, so the device sees a new command when the intended purpose is only to select a device. Both devices may be Busy but not necessarily Ready, e.g. Device 0 may be ready, but not Device 1. To check this possibility a typical sequence for an 8-bit host would be:

1) Read the Status register (wait until Busy False)
2) Select the device (write to the Device/Head Register)
3) Read the Status register (wait until Busy False and Ready True)
4) Send the command (write to the Command register).

As a 16-bit host executes b) and d) simultaneously, a problem occurs if the device being selected is Not Ready at the time the command is issued.

8.17 READ BUFFER

OPCODE - E4h

TYPE - Optional.

PROTOCOL - PIO data in.

INPUTS - None required.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported.

PREREQUISITES - None.

Note: A WRITE BUFFER command should immediately proceed a READ BUFFER command.

DESCRIPTION - The READ BUFFER command enables the host to read the current contents of the device's sector buffer. When this command is issued, the device sets the BSY bit, sets up the sector buffer for a read operation, sets the DRQ bit, clears the BSY bit, and generates an interrupt. The host then reads the data from the buffer.

The READ BUFFER and WRITE BUFFER commands shall be synchronized such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

8.18 READ DMA (with retries and without retries)

OPCODE - C8h (with retries) or C9h (without retries)

TYPE - Optional.

PROTOCOL - DMA.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number registers specify the starting sector address to be read. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - The host shall initialize the DMA channel.

DESCRIPTION - This command executes in a similar manner to the READ SECTOR(S) command except for the following:

- the host initializes the DMA channel prior to issuing the command
- data transfers are qualified by DMARQ and are performed by the DMA channel
- the device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the DMA transfer phase of a READ DMA command, the device shall provide status of the BSY bit or the DRQ bit until the command is completed.

The with retries and without retries versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

8.19 READ LONG (with retries and without retries)

OPCODE - 22h (with retries) or 23h (without retries)

TYPE - Optional.

PROTOCOL - PIO data in.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be read. The Sector Count register shall not specify a value other than 1.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - The SET FEATURES subcommand to enable more than 4 vendor specific bytes shall be executed prior to the READ LONG command if other than 4 vendor specific bytes are to be transferred.

DESCRIPTION - The READ LONG command performs similarly to the READ SECTOR(S) command except that it returns the data and a number of vendor specific bytes appended to the data field of the desired sector. During a READ LONG command, the device does not check to determine if there has been a data error. Only single sector read long operations are supported.

The transfer of the vendor specific bytes shall be one byte at a time over bits DD (7:0) only (8-bits wide).

The with retries and without retries versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

> Note: Some ATA-1 devices are not capable of delivering the 8-bit ECC immediately after the 16-bit data. BIOS and driver developers should use PIO mode 0 for 8-bit ECC accesses.

8.20 READ MULTIPLE

OPCODE - C4h

TYPE - Optional.

PROTOCOL - PIO data in.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be read. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - A successful SET MULTIPLE MODE command shall proceed a READ MULTIPLE command.

DESCRIPTION - The READ MULTIPLE command performs similarly to the READ SECTOR(S) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a SET MULTIPLE MODE command. Command execution is identical to the READ SECTOR(S) operation except that the number of sectors defined by a SET MULTIPLE MODE command are transferred without intervening interrupts. The DRQ bit qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the SET MULTIPLE MODE command, which shall be executed prior to the READ MULTIPLE command. When the READ MULTIPLE command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer shall be for n sectors, where n = remainder (sector count/ block count)

If the READ MULTIPLE command is attempted before the SET MULTIPLE MODE command has been executed or when READ MULTIPLE commands are disabled, the READ MULTIPLE operation shall be rejected with an Aborted Command error.

Device errors encountered during READ MULTIPLE commands are posted at the beginning of the block or partial block transfer, but the DRQ bit is still set and the data transfer shall take place as it normally would, including transfer of corrupted data, if any. The contents of the Command Block Registers following the transfer of a data block which had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error. Interrupts are generated when the DRQ bit is set at the beginning of each block or partial block.

8.21 READ SECTOR(S) (with retries and without retries)

OPCODE - 20h (with retries) or 21h (without retries)

TYPE - Mandatory.

PROTOCOL - PIO data in.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be read. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - None.

DESCRIPTION - This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

The DRQ bit is always set prior to data transfer regardless of the presence or absence of an error condition.

The with retries and without retries versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

8.22 READ VERIFY SECTOR(S) (with retries and without retries)

OPCODE - 40h (with retries) or 41h (without retries)

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be verified. The Sector Count register specifies the number of sectors to be verified.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - None.

DESCRIPTION - This command is identical to the READ SECTOR(S) command, except that the DRQ bit is never set, and no data is transferred to the host.

When the requested sectors have been verified, the device clears the BSY bit and generates an interrupt.

The with retries and without retries versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

8.23 RECALIBRATE

OPCODE - 10h through 1Fh

TYPE - Optional.

PROTOCOL - Non-data.

INPUTS - None.

NORMAL OUTPUTS - If the command is executed in CHS addressing mode, Cylinder High, Cylinder Low and the head portion of Device/Head shall be zero. The Sector Number register shall be 1. If the command is executed in LBA addressing mode, the Cylinder High, Cylinder Low, the head portion of the Device/Head and the Sector Number register shall be zero.

ERROR OUTPUTS - If the device cannot reach cylinder 0, a Track 0 Not Found error is posted.

PREREQUISITES - None.

DESCRIPTION - The function performed by this command is vendor specific.

8.24 SECURE DISABLE

OPCODE - EAh

TYPE - Optional - Security Mode Feature Set.

PROTOCOL - Non-data command.

INPUTS - The Feature register shall be set to 80h.

NORMAL OUTPUTS - none.

ERROR OUTPUTS - Aborted Command error if:

- the device does not support the Secure Mode Feature Set.
- the device supports the Secure Mode Feature Set and the device is not already in Secure Mode.
- the device supports the Secure Mode Feature Set, is in Secure Mode and Locked.

PREREQUISITES - The device must be in Secure Mode and Unlocked.

DESCRIPTION - When the device is in Secure Mode Read Only or Read/Write, unlocked, with an existing set of valid passwords, this command shall remove the device from Secure Mode. When the device is in Secure Mode Write Protect, this command shall remove the device from Secure Mode.

Upon successful completion of this command, the device shall not be in Secure Mode. All passwords shall be deleted.

If this command is received when not in Secure Mode Read Only or Read/Write and unlocked state, or Secure Mode Write Protect, the command shall be rejected and an Abort error returned.

8.25 SECURE ENABLE READ ONLY

OPCODE - EBh

TYPE - Optional - Security Mode Feature Set.

PROTOCOL - PIO data out.

INPUTS - The Features register shall be set to 81h. The Sector Count register specifies the number of passwords to be set.

NORMAL OUTPUTS - none.

ERROR OUTPUTS - Aborted Command error if:

- the device does not support the Secure Mode Feature Set.
- the device is already in Secure Mode.
- the device supports the Secure Mode Feature Set and the number of passwords indicated in the Sector Count register is less than one or greater than that supported by the device.

PREREQUISITES - The device must not be in Secure Mode.

DESCRIPTION - This command shall set the device into Secure Mode Read Only and define the valid set of passwords.

If the device is not in Secure Mode when the command is received, the value set in the Sector Count register indicates the number of 512 byte passwords that will be passed with this command. If the Sector Count register contains a value less than 1 or greater than the maximum number of passwords supported by the device, the command shall not be executed and Abort error shall be returned.

If the device is in Secure Mode when this command is received, the command shall not be executed and an Abort error shall be returned.

8.26 SECURE ENABLE READ/WRITE

OPCODE - EBh

TYPE - Optional - Security Mode Feature Set.

PROTOCOL - PIO data out.

INPUTS - The Features register shall be set to 82h. The Sector Count register specifies the number of passwords to be set.

NORMAL OUTPUTS - none.

ERROR OUTPUTS - Aborted Command error if:

- the device does not support the Secure Mode Feature Set.
- the device is already in Secure Mode.
- the device supports the Secure Mode Feature Set and the number of passwords indicated in the Sector Count register is less than one or greater than that supported by the device.

PREREQUISITES - The device must not be in Secure Mode.

DESCRIPTION - This command shall set the device into Secure Mode Read/Write and define the valid set of passwords.

If the device is not in Secure Mode when the command is received, the value set in the Sector Count register indicates the number of 512 byte passwords that will be passed with this command. If the Sector Count register contains a value less than 1 or greater than the maximum number of passwords supported by the device, the command shall not be executed and Abort error shall be returned.

If the device is in Secure Mode when this command is received, the command shall not be executed and an Abort error shall be returned.

8.27 SECURE ENABLE WRITE PROTECT

OPCODE - EAh

TYPE - Optional - Security Mode Feature Set.

PROTOCOL - Non-data command.

INPUTS - The Feature register shall be set to 83h.

NORMAL OUTPUTS - none.

ERROR OUTPUTS - Aborted Command error if:

- the device does not support the Secure Mode Feature Set.
- the device supports the Secure Mode Feature Set and is already in secure mode.

PREREQUISITES - The device must not be in Secure Mode.

DESCRIPTION - This command shall set the device into Secure Mode Write Protect. In this mode, the entire device can be read but all write commands shall be rejected.

Once placed in Secure Mode Write Protect state, the device data cannot be written to the device until it is removed from Secure Mode Write Protect by a Disable Secure command.

If the device is in Secure Mode Read Only, Read/Write or Write Protect state when this command is received, it shall be rejected and an Abort error returned.

8.28 SECURE LOCK

OPCODE - EAh

TYPE - Optional - Security Mode Feature Set.

PROTOCOL - Non-data command.

INPUTS - The Features register shall be set to 84h.

NORMAL OUTPUTS - none.

ERROR OUTPUTS - Aborted Command error if:

- the device does not support the Secure Mode Feature Set.
- the device supports the Secure Mode Feature Set and the device is not already in Secure Mode.
- the device supports the Secure Mode Feature Set, is in Secure Mode and Locked.

PREREQUISITES - The device must be in Secure Mode and Unlocked.

DESCRIPTION - This command shall lock the device any time the device is in Secure Mode Read Only or Read/Write, unlocked. If the device was unlocked with the Features register value 87h, this is the only means of locking the device. If the device was unlocked with the Features register value 86h, either this command or powering-down the device shall cause the device to assume the locked state.

Upon successful completion of this command the device shall be in Secure Mode Read Only or Read/Write, locked, state.

If this command is received when the device is not in Secure Mode, or in Secure ModeRead Only or Read/Write, locked, state, the command shall be rejected and an Abort error returned.

8.29 SECURE STATE

OPCODE - EAh

TYPE - Optional - Security Mode Feature Set.

PROTOCOL - Non-data command.

INPUTS - The Features register shall be set to 85h.

NORMAL OUTPUTS - The Sector Count register specifies the Security Mode state as shown in Table 14.

Table 14 - Security Mode State

7	6	5	4	3	2	1	0
Secure Enable RW	Secure Enabled RO	Secure Enabled WP	Unlocked	Lock Flag	Media Not Present	r	r

Bit 7 - Secure Enabled RW - If set, indicates that the device has been set in Secure Mode Read/Write.
Bit 6 - Secure Enabled RO - If set, indicates that the device has been set in Secure Mode Read Only.
Bit 5 - Secure Enabled WP - If set, indicates that the device has been set in Secure Mode Write Protect
Bit 4 - Unlocked - If set, indicates that the device has been unlocked.
Bit 3 - Lock Flag - If the device is in Secure Mode and this bit is cleared, the device will assume the locked state when powered down. If the device is in Secure Mode and this bit is set, the device can only be locked by issuing a Lock command.
Bit 2 - Media Not Present - Set if the device is a removable media device and no media is present.
Bit 1:0 -reserved.

ERROR OUTPUTS - Aborted Command error if the device does not support the Secure Mode Feature Set.

PREREQUISITES - None.

DESCRIPTION - This command shall return the Secure Mode state of a device that implements the Secure Mode Function Set. Upon completion of the command, the Sector Count register shall contain the Secure Mode state as shown in Table 14.

8.30 SECURE UNLOCK

OPCODE - EBh

TYPE - Optional - Security Mode Feature Set.

PROTOCOL - PIO data out.

INPUTS - The Features register shall be set to 86h or 87h. The Sector Count register shall be set to 01h.

NORMAL OUTPUTS - none.

ERROR OUTPUTS - Aborted Command error if:

- the device does not support the Secure Mode Feature Set.
- the device supports the Secure Mode Feature Set and the device is not already in Secure Mode.
- the device supports the Secure Mode Feature Set and the value set in the Sector Count register is not equal to 01h.

PREREQUISITES - The device must be in Secure Mode.

DESCRIPTION - This command unlocks a device in the Secure Mode to allow data transfers.

The device shall match the password received with this command with the existing set of valid passwords. If the unlock password matches a password in the established set of passwords, the device shall unlock.

The Features register indicates the required action to relock the extent. If the Features register contains the value 86h, the device shall assume the lock state when powered-down. If the Features register contains the value 87h, the device shall only assume the locked state when the LOCK command is received, that is, the device may be powered-down and back up without assuming the locked state.

If this command is received when the device is in Secure Mode Read Only or Read/Write, unlocked state, the command shall be executed and if password does not match, an Abort error shall be returned but the device shall remain unlocked. Thus when in the unlocked state, this command can be used to verify passwords. The Features register is used as described above to set or clear the Lock Flag.

Upon successful completion, the secure state shall reflect Secure Mode Read Only or Read/Write set and unlocked. Having been unlocked, the device shall now accept and execute all data transfer commands.

If this command is received when not in Secure Mode, the command shall be rejected and an Abort error returned.

8.31 SEEK

OPCODE - 70h through 7Fh

TYPE - Mandatory.

PROTOCOL - Non-data.

INPUTS - The Cylinder High, Cylinder Low, head portion of the Device/Head register and the Sector Number register contain the sector address to which the device should move the read/write heads.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - None.

DESCRIPTION - The function performed by this command is vendor specific.

8.32 SET FEATURES

OPCODE - EFh

TYPE - The command is optional and if implemented each subcommand is optional.

PROTOCOL - Non-data.

INPUTS - The Feature register contains a subcommand code as described in Table 15. Some subcommands use other registers, such as the Sector Count register to pass additional information to the device.

NORMAL OUTPUTS - See the subcommand descriptions.

ERROR OUTPUTS - If the device does not support the command or if any input value is not supported or is invalid, the device posts an Aborted Command error.

PREREQUISITES - None.

DESCRIPTION - This command is used by the host to establish the following parameters which affect the execution of certain device features as shown in Table 15.

Table 15 - Set Features register Definitions

Value (2)	
01h	Enable 8-bit data transfers (see Clause 6.2.5)
02h	Enable write cache (1)
03h	Set transfer mode based on value in Sector Count register
04h	Enable all automatic defect reassignment (1)
33h	Disable retry (1)
44h	Length of vendor specific bytes on READ LONG/WRITE LONG commands
54h	Set cache segments to Sector Count register value (1)
55h	Disable read look-ahead feature
66h	Disable reverting to power on defaults (see Clause 8.32)
77h	Disable ECC (1)
81h	Disable 8-bit data transfers (see Clause 6.2.5)
82h	Disable write cache (1)
84h	Disable all automatic defect reassignment (1)
88h	Enable ECC (1)
99h	Enable retries (1)
9Ah	Set device maximum average current
AAh	Enable read look-ahead feature
ABh	Set maximum prefetch using Sector Count register value (1)
BBh	4 bytes of vendor specific bytes on READ LONG/WRITE LONG commands
CCh	Enable reverting to power on defaults (see Clause 8.32)

Note:
(1) These feature definitions are vendor specific
(2) All values not shown are reserved for future definition.

At power on, or after a hardware reset, the default setting of the functions specified by the subcommands are vendor specific.

A setting of 66h allows settings of greater than 80h which may have been modified since power on to remain at the same setting after a software reset.

A host can choose the transfer mechanism by Set Transfer Mode and specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

Table 16 - Transfer/Mode Values

PIO Default Transfer Mode	00000	000
PIO Default Transfer Mode, Disable IORDY	00000	001
PIO Flow Control Transfer Mode x	00001	nnn
Single Word DMA Mode x	00010	nnn
Multiword DMA Mode x	00100	nnn
Reserved	01000	nnn
Reserved	10000	nnn
Key: nnn = a valid mode number in binary x = the mode number in decimal for the associated transfer type.		

If a device supports this specification, and receives a SET FEATURES command with a Set Transfer Mode parameter and a Sector Count register value of “00000000b”, it shall set its default PIO transfer mode. If the value is “00000001b” and the device supports disabling of IORDY, then the device shall set its default PIO transfer mode and disable IORDY.

See vendor specification for the default mode of the commands which are vendor specific.

Devices reporting support for Multi Word DMA Transfer Mode 1 shall also support Multi Word DMA Transfer Mode 0. Support of IORDY is mandatory when PIO Mode 3 or above is the current mode of operation.

To adjust the current the device draws, the host issues the Set Features command with the Features register set to 9Ah and the Sector Count register set to a current value which is equal to 4 mA times the value in the Sector Count register. If the device supports this feature, the device will set its average operating current to the nearest supported current that does not exceed the specified current, where average operating current is defined as the maximum current required averaged over a period of one second. For example, if the Sector Count is set to 32 which is equivalent to 128 mA and the nearest possible current less than the selected current that the device can support is 100 mA, the device then will set its average operating current to 100 mA.

A hard reset returns the average operating current to the power default value which is vendor specific. A soft reset does not return the average operating current to the power on default value.

However, if the selected current is less than the minimum value the device can support, the device will still switch to operate at its minimum current. For example, if the Sector count is set to 5 which is equivalent to 20 mA but the minimum device current is 50 mA, the device will still operate at its minimum value at 50 mA. If the host wants to operate at the device’s lowest possible current, the Sector Count value should be set to 1. Similarly the device will use its maximum operating current for any Sector Count value which is greater than the maximum current it can use.

At the completion of this command, the device will update the Cylinder Low register with the minimum valid operating current of the device and the Cylinder High register with the maximum valid operating current. The host can use this minimum valid operating current returned in the Cylinder Low register to verify if the system can run that device.

Sector Count equal to zero is invalid. Therefore, this command allows the host to support current range from 4 mA to 1020 mA.

If the device does not support this feature, it shall post an Aborted Command error.

8.33 SET MULTIPLE MODE

OPCODE - C6h

TYPE - Optional.

PROTOCOL - Non-data.

INPUTS - The Sector Count register contains number of sectors per block to use on all following READ/WRITE MULTIPLE commands.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - If the device does not support the READ/WRITE MULTIPLE and SET MULTIPLE MODE commands or if a block count is not supported, a Aborted Command error is posted, and READ MULTIPLE and WRITE MULTIPLE commands are disabled.

PREREQUISITES - None.

DESCRIPTION - This command enables the device to perform READ AND WRITE MULTIPLE operations and establishes the block count for these commands.

Devices shall support the block size specified in the IDENTIFY DRIVE parameter word 47, bits 7 through 0, and may also support smaller values.

Upon receipt of the command, the device sets the BSY bit equal to one and checks the Sector Count register. If the Sector Count register contains a valid value and the block count is supported, the value is used for all subsequent READ MULTIPLE and WRITE MULTIPLE commands and their execution is enabled.

If the Sector Count register contains 0 when the command is issued, READ AND WRITE MULTIPLE commands are disabled.

At power on, or after a hardware reset, the default mode is READ AND WRITE MULTIPLE disabled. Following a software reset, the READ and WRITE MULTIPLE commands may be enabled or disabled. The SET FEATURES command Disable Reverting To Power on Defaults and Enable Reverting To Power on Defaults subcommands, if supported, can be used to control the results of a software reset.

8.34 SLEEP

OPCODE - 99h or E6h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - None.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command - The device does not support the Power Management command set.

PREREQUISITES - None.

DESCRIPTION - This command is the only way to cause the device to enter Sleep Mode.

This command causes the device to set the BSY bit, prepare to enter Sleep mode, clear the BSY bit and assert INTRQ. The host shall read the Status register in order to clear the interrupt and allow the device to enter Sleep mode. In Sleep mode the interface becomes inactive without affecting the operation of the ATA interface. The host shall not attempt to access the Command Block registers while the device is in Sleep mode.

Because some host systems may not read the Status register and clear the interrupt, a device may automatically deassert INTRQ and enter Sleep mode after a vendor specified time period of not less than 2 sec.

The only way to recover from Sleep Mode is with a software reset or a hardware reset.

A device shall not power on in Sleep Mode nor remain in Sleep Mode following a reset sequence.

8.35 SMART DISABLE OPERATIONS

OPCODE - B0h

TYPE - Optional - SMART Feature set

PROTOCOL - Non-data command

INPUTS - The Features register shall be set to D9h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

NORMAL OUTPUTS - None

ERROR OUTPUTS - If the device does not support the SMART feature set or if the values in the Features, Cylinder low or Cylinder High registers are invalid, an Aborted command error is posted.

PREREQUISITES - None

DESCRIPTION - This command disables all S.M.A.R.T. capabilities within the device including any and all timer functions related exclusively to this feature. After receipt of this command the device will disable all S.M.A.R.T. operations. Attribute values will no longer be monitiored or saved by the device. The state of S.M.A.R.T. (either enabled or disabled) will be preserved by the device across power cycles.

Upon receipt of the SMART DISABLE OPERATIONS command from the host, the device sets BSY, disables S.M.A.R.T. capabilities and functions, clears BSY and asserts INTRQ.

After receipt of this command by the device, all other S.M.A.R.T. commands, with the exception of SMART ENABLE OPERATIONS, are disabled and invalid and shall be aborted by the device (including SMART DISABLE OPERATIONS commands), returning the Aborted command error.

Any attribute values accumulated and saved to non-volitile memory prior to receipt of this command will be preserved in the device's non-volitile memory. If the device is re-enabled, these attribute values will be updated, as needed, upon receipt of a SMART READ ATTRIBUTE VALUES or SMART SAVE ATTRIBUTE VALUES command.

8.36 SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE

OPCODE - B0h

TYPE - Optional - SMART Feature set

PROTOCOL - Non-data command

INPUTS - The Features register shall be set to D2h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h. The Sector Count register is set to 00h to diable attribute autosave and a value of F1h is set to enable attribute autosave.

NORMAL OUTPUTS - None

ERROR OUTPUTS - If the device does not support the SMART feature set or if the values in the Features, Cylinder low or Cylinder High registers are invalid, an Aborted command error is posted.

PREREQUISITES - None

DESCRIPTION - This command enables and disables the optional attribute autosave feature of the device. Depending upon the implementation, this command may either allow the device, after some vendor specified event, to automatically save its updated attribute values to non-volitile memory; or this command may cause the autosave feature to be disabled. The state of the attribute autosave feature (either enabled or disabled) will be preserved by the device across power cycles.

A value of zero written by the host into the device's Sector Count register before issuing this command will cause this feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to non-volitile memory during some other normal operation such as during a power-on or power-off sequence or during an error recovery sequence.

A value of F1h written by the host into the device's Sector Count register before issuing this command will cause this feature to be enabled. Any other meaning of this value or any other non-zero value written by the host into this register before issuing this command is vendor specific. The meaning of any non-zero value written to this register at this time will be preserved by the device across power cycles.

If the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command is supported by the device, upon receipt of the command from the host, the device sets BSY, enables or disables the atuosave feature (depending on the implementation), clears BSY and asserts INTRQ.

If this command is not supported by the device, the device shall abort the command upon receipt from the host, returning the Aborted command error.

During execution of the autosave routine the device shall not assert BSY nor deassert DRDY. If the device receives a command from the host while executing its autosave routine it must respond to the host within two seconds.

Implementation of this feature is optional and vendor specific.

8.37 SMART ENABLE OPERATIONS

OPCODE - B0h

TYPE - Optional - SMART Feature set

PROTOCOL - Non-data command

INPUTS - The Features register shall be set to D8h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

NORMAL OUTPUTS - None

ERROR OUTPUTS - If the device does not support the SMART feature set or if the values in the Features, Cylinder low or Cylinder High registers are invalid, an Aborted command error is posted.

PREREQUISITES - None

DESCRIPTION - This command enables access to all S.M.A.R.T. capabilities within the device. Prior to receipt of this command attribute values are neither monitored nor saved by the device, The state of S.M.A.R.T. (either enabled or disabled) will be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART ENABLE OPERATIONS commands shall not affect any of the attribute values.

Upon receipt of this command from the host, the device sets BSY, enables S.M.A.R.T. capabilities and functions, clears BSY and asserts INTRQ.

8.38 SMART READ ATTRIBUTE THRESHOLDS

OPCODE - B0h

TYPE - Optional - SMART Feature set

PROTOCOL - PIO data in

INPUTS - The Features register shall be set to D1h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

NORMAL OUTPUTS - None

ERROR OUTPUTS - If the device does not support the SMART feature set or if the values in the Features, Cylinder low or Cylinder High registers are invalid, an Aborted command error is posted.

PREREQUISITES - None

DESCRIPTION - This command returns the device's attribute thresholds to the host. Upon receipt of this command form the host, the device sets BSY, reads the attribute thresholdss from non-volitile memory, sets DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of attribute threshold information from the device via the Data register.

The following defines the 512 bytes that make up the attribute threshold information. All multi-byte fields shown in these data structures follow the byte ordering specified in Clause 3.2.5.

The sequence of active attribute thresholds must appear in the same order as their corresponding attribute values (see Clause).

Table 17 - Device attribute thresholds data structure

Description	Bytes	Format	Type
Data structure revision number = 0x0004h for this revision	2	binary	Rd only
1st attribute threshold	12	see below	Rd/Wrt
.....			
.....			
.....			
30th attribute threshold	12	see below	Rd/Wrt
reserved (0x00)	18		Rd/Wrt
Vendor specific	131		Rd only
Data structure checksum	1		Rd only
Total bytes	512		

The data structure revision number shall be the same value used in the device attribute values data structure.

The following defines the twelve bytes that make up the information for each threshold entry in the device attribute thresholds data structure. Attribute entries in the individual threshold data structure must be in the same order and correspond to the entries in the individual attribute data structure.

Table 18 - Individual threshold data structure

Description	Bytes	Format	Type
Attribute ID number	1	binary	Rd only
Attribute threshold (for comparison with attribute values from 0x00 to 0xFFh)	1	binary	Rd only
0x00 “always passing” threshold value to be used for code test purposes			
0x01 minimum value for normal operation			
0xFD maximum value for normal operation			
0xFE invalid for threshold value - not to be used			
0xFF “always failing” threshold value to be used for code test purposes			
Reserved	10		Rd only
Total bytes	12		

The attribute ID numbers are vendor specific. Any non-zero value in the attribute ID number indicates an active attribute.

Attribute threshold values are to be set at the factory and are not meant to be changeable in the field.

The data structure checksum is the two’s compliment of the result of a simple eight-bit addition of the first 511 bytes in the data structure.

8.39 SMART READ ATTRIBUTE VALUES

OPCODE - B0h

TYPE - Optional - SMART Feature set

PROTOCOL - PIO data in

INPUTS - The Features register shall be set to D0h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

NORMAL OUTPUTS - None

ERROR OUTPUTS - If the device does not support the SMART feature set or if the values in the Features, Cylinder low or Cylinder High registers are invalid, an Aborted command error is posted.

PREREQUISITES - None

DESCRIPTION - This command returns the device's attribute values to the host. Upon receipt of this command from the host, the device sets BSY, saves any updated attribute values to non-volitile memory, sets DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of attribute value information from the device via the Data register.

The following defines the 512 bytes that make up the attribute value information. All multi-byte fields shown in these data structures follow the byte ordering described in Clause 3.2.5.

The number of active attributes and, therefore, number of active attribute values is determined independently by the device manufacturer for each individual device. All active attribute entries should be concatenated together directly after the data structure revsion number. If there are fewer than thirty active attributes implemented on a device, the excess locations in the data structure are reserved for future attribute implementations and are designated as blanks containing the value 0x00h. Thus the first reserved byte following the attribute entries shall be the 363rd byte in the structure, the first S.M.A.R.T. capability byte shall be the 369th byte in the structure, etc.

Table 19 - Device attributes data structure

Description	Bytes	Format	Type
Data structure revision number = 0x0004 for this specification revision	2	binary	Rd only
1st device attribute	12	see below	Rd/Wrt
...			
...			
...			
30th device attribute	12	see below	Rd/Wrt
reserved (0x00)	6		Rd only
S.M.A.R.T. capability	2		Rd only
reserved (0x00)	16		Rd/Wrt
Vendor specific	125		Rd only
Data stucture checksum	1		Rd only
Total bytes	512		

The data structure revision number identifies which version of this data structure is implemented by a device. Upon initial release of this specification, the revision number will be set to 0x0004h. Later revisions, if any, will increment the revision number by one for each new revision. The revision number will be the same for both the attribute value and attribute threshold structures.

The following defines the twelve bytes that make up the information for each attribute entry in the device attibutes data stucture.

Table 20 - Individual attribute data structure

Description	Bytes	Format	Type
Attribute ID number (0x01 to 0xFFh)	1	binary	Rd only
Status flags	2	bit flags	Rd only
Pre-failure/advisory bit			
Vendor specific (5 bits)			
reserved (10 bits)			
Attribute value (valid values from 0x01 to 0xFEh)	1	binary	Rd only
0x00 invalid for attribute value - not to be used			
0x01 minimum value			
0x64 initial value for all attributes prior to any data collection			
0xFD maximum value			
0xFE value is not valid			
0xFF invalid for attribute value - not to be used			
Vendor specific	8	binary	Rd only
Total bytes	12		

The attribute ID numbers and their definitions are vendor specific. Any non-zero value in the attribute ID number indicates an active attribute. Valid values for this byte are from 0x01 through 0xFFh.

Status flag

- Bit 0 -Pre-failure/advisory - If the value of this bit equals zero, an attribute value less than or equal to its corresponding attribute threshold indicates an advisory condition where the usage or age of the device has exceeded its intended design life period. If the value of this bit equals one, an atribute value less than or equal to its corresponding attribute threshold indicates a pre-failure condition where imminent loss of data is being predicted.

- Bit 1 Reserved for future use.

- Bits 3-6 - Vendor specific.
- Bits 7-15 - Reserved for future use.

The range and meaning of the attribute values is described in Table 20. Prior to the monitoring and saving of attribute values, all values are set to 0x64h. The attribute values of 0x00h and 0xFFh are reserved and should not be used by the device.

S.M.A.R.T. capability

- Bit 0 - Pre-power mode attribute saving capability - If the value of this bit equals one, the device will save its attribute values prior to going into a power saving mode (Idle, Standby or Sleep modes).

- Bit 1 - Attribute autosave after event capability - If the value of this bit is equal to one, the device supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE comand.

- Bits 2-15 - Reserved for future use.

The data structure checksum is the two’s compliment of the result of a simple eight-bit addition of the first 511 bytes in the data structure.

8.40 SMART RETURN STATUS

OPCODE - B0h

TYPE - Optional - SMART Feature set

PROTOCOL -Non-data command.

INPUTS - The Features register shall be set to DAh. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

NORMAL OUTPUTS - If the device has not detected a thrshold exceeded condition, the device sets the Cylinder Low register to 4Fh and the Cylinder High register to C2h. If the device has detected a threshold exceeded condition, the device sets the Cylinder Low register to F4h and the Cylinder High register to 2Ch.

ERROR OUTPUTS - If the device does not support the SMART feature set or if the values in the Features, Cylinder low or Cylinder High registers are invalid, an Aborted command error is posted.

PREREQUISITES - None

DESCRIPTION - This command is used to communicate the reliability status of the device to the host at the host's request. Upon receipt of this command the device sets BSY, saves any updated attribute values to non-volatile memory and compares the updated attribute values to the attribute thresholds.

If the device does not detect a threshold exceeded condition, the device loads 4Fh into the Cylinder Low register, C2h into the Cylinder High register, clears BSY and asserts INTRQ.

If the device does detect a thrshold exceeded condition, the device loads F4h into the Cylinder Low register, 2Ch into the Cylinder High register, clears BSY and asserts INTRQ.

If this command is not supported by the device, the device wil abort the command upon receipt from the host, returning an Abort command error.

8.41 SMART SAVE ATTRIBUTE VALUES

OPCODE - B0h

TYPE - Optional - SMART Feature set

PROTOCOL -Non-data command

INPUTS - The Features register shall be set to D3h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

NORMAL OUTPUTS - None

ERROR OUTPUTS - If the device does not support the SMART feature set or if the values in the Features, Cylinder low or Cylinder High registers are invalid, an Aborted command error is posted.

PREREQUISITES - None

DESCRIPTION - This command causes the device to immediately save any updated attribute values to the device's non-volatile memory regardless of the state of the attribute autosave timer. Upon receipt of this command from the host, the device sets BSY, writes any updated attribute values to non-volatile memory, clears BSY and asserts INTRQ.

8.42 STANDBY

OPCODE - 96h or E2h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - The value in the Sector Count register when the STANDBY command is issued shall determine the time period programmed into the Standby Timer. See Table 13.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the device does not support the Power Management command set.

PREREQUISITES - None.

DESCRIPTION - This command causes the device to set the BSY bit, enter the Standby Mode, clear the BSY bit, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Standby Mode.

If the Sector Count register is non-zero then the Standby Timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby Timer.

If the Sector Count register is zero then the Standby Timer is disabled.

8.43 STANDBY IMMEDIATE

OPCODE - 94h or E0h

TYPE - Optional - Power Management Feature Set.

PROTOCOL - Non-data command.

INPUTS - None.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command - The device does not support the Power Management command set.

PREREQUISITES - None.

DESCRIPTION - This command causes the device to set the BSY bit, enter the Standby Mode, clear the BSY bit, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Standby Mode.

8.44 WRITE BUFFER

OPCODE - E8h

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - None.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported.

PREREQUISITES - None.

DESCRIPTION - This command enables the host to overwrite the contents of one sector in the device's buffer. When this command is issued, the device sets the BSY bit, sets up the buffer for a write operation, sets the DRQ bit, clears the BSY bit, and waits for the host to write the data. Once the host has written the data, the device sets the BSY bit, clears the BSY bit and generates an interrupt.

The READ BUFFER and WRITE BUFFER commands shall be synchronized within the device such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

8.45 WRITE DMA (with retries and without retries)

OPCODE - CAh (with retries) or CBh (without retries)

TYPE - Optional.

PROTOCOL - DMA.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - The host shall initialize the DMA channel.

DESCRIPTION - This command executes in a similar manner to WRITE SECTOR(S) except for the following:

- the host initializes the DMA channel prior to issuing the command
- data transfers are qualified by DMARQ and are performed by the DMA channel
- the device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the execution of a WRITE DMA command, the device shall provide status of the BSY bit or the DRQ bit until the command is completed.

The with retries and without retries versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

8.46 WRITE LONG (with retries and without retries)

OPCODE - 32h (with retries) or 33h (without retries)

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register shall not specify a value other than 1.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - The SET FEATURES subcommand to enable other than 4 vendor specific bytes shall be executed prior to the WRITE LONG command if other than 4 vendor specific bytes are to be transferred.

DESCRIPTION - This command is similar to the WRITE SECTOR(S) command except that it writes the data and the vendor specific bytes as supplied by the host; the device does not generate the vendor specific bytes itself. Only single sector Write Long operations are supported.

The transfer of the vendor specific bytes shall be one byte at a time over bits DD (7:0) only (8-bits wide).

The with retries and without retries versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

8.47 WRITE MULTIPLE

OPCODE - C5h

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - A successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.

DESCRIPTION - This command is similar to the WRITE SECTOR(S) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by SET MULTIPLE MODE.

Command execution is identical to the WRITE SECTOR(S) operation except that the number of sectors defined by the SET MULTIPLE MODE command are transferred without intervening interrupts. The DRQ bit qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the SET MULTIPLE MODE command, which shall be executed prior to the WRITE MULTIPLE command.

When the WRITE MULTIPLE command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where n = Remainder (sector count/ block count).

If the WRITE MULTIPLE command is attempted before the SET MULTIPLE MODE command has been executed or when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with an Aborted Command error.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The Write command ends with the sector in error, even if it was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block which had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupts are generated when the DRQ bit is set at the beginning of each block or partial block.

8.48 WRITE SECTOR(S) (with retries and without retries)

OPCODE - 30h (with retries) or 31h (without retries)

TYPE - Mandatory.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - None.

DESCRIPTION - This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors.

The with retries and without retries versions of this command differ in operation only in the level of error recovery performed by the device. The level of error recovery performed by the device for either command is vendor specific.

8.49 WRITE VERIFY

OPCODE - 3Ch

TYPE - Optional.

PROTOCOL - PIO data out.

INPUTS - The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

NORMAL OUTPUTS - None required.

ERROR OUTPUTS - Aborted Command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred.

PREREQUISITES - None.

DESCRIPTION - This command is similar to the WRITE SECTOR(S) command, except that each sector is verified from the media after being written and before the command is completed.

9 Protocol

Commands can be grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host first checks if the BSY bit is equal to one, and should proceed no further unless and until the BSY bit is equal to zero. For most commands, the host shall also wait for the DRDY bit to be equal to one before proceeding. The commands shown with DRDY=x can be executed when the DRDY bit is equal to zero.

Data transfers may be accomplished in more ways than are described below, but these sequences should work with all known implementations of ATA devices.

A device shall maintain either the BSY bit equal to one or the DRQ bit equal to one at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from one to zero during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while the BSY bit is equal to one or the DRQ bit is equal to one is unpredictable and may result in data corruption.

9.1 Power on and hardware resets

This clause describes the algorithm and timing relationships for Devices 0 and 1 during the processing of power on and hardware resets.

The timing assumes the following:

a) DASP- is asserted by Device 1 and received by Device 0 at power-on or hardware reset to indicate the presence of Device 1. At all other times it is asserted by Device 0 or Device 1 to indicate when a device is active.
b) PDIAG- is asserted by Device 1 and detected by Device 0. It is used by Device 1 to indicate to Device 0 that it has completed diagnostics without error and is ready to accept commands from the Host (BSY bit is cleared). This does not indicate that the device is ready, only that it can accept commands.

9.1.1 Power on and hardware resets - device 0

a) Host asserts RESET- for a minimum of 25 μsec.
b) Device 0 sets the BSY bit no later than 400 nsec after RESET- is negated.
c) Device 0 negates DASP- no later than 1 msec after RESET- is negated.
d) Device 0 samples for at least 450 msec for DASP- to be asserted from Device 1. This sampling starts 1 ms after RESET- is negated.
e) Device 0 performs hardware initialization and diagnostics.
f) Device 0 may revert to its default condition.
g) If Device 0 detected that DASP- was asserted during step d), then Device 0 waits up to 31 sec for Device 1 to assert PDIAG-. If PDIAG- is asserted within 31 sec, Device 0 clears bit 7 equal to zero in the Error Register, else Device 0 sets bit 7 equal to one in the Error Register. If DASP- assertion was not detected in step d) Device 0 clears bit 7 equal to zero in the Error Register. In either case the device shall set the Sector Count register to 01h, the Sector Number register to 01h, the Cylinder Low register to 00h, the Cylinder High register to 00h, and the Device/Head register to 00h.
   Device 0 shall store whether or not Device 1 was detected in step d) because this information is need in order to process any Software reset or EXECUTE DEVICE DIAGNOSTIC command later.
h) Device 0 posts diagnostic results to bits 6-0 of the Error Register.
i) Device 0 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1. Device 0 shall clear the BSY bit no later than 31 sec from the time that RESET- is negated.

j) Device 0 sets the DRDY bit when ready to accept any command.
NOTE: Steps i) and j) may occur at the same time. While no maximum time is specified for the DRDY bit to be set to one, a host should allow up to 30 sec for the DRDY bit to become 1. See Figure 6.

9.1.2 Power on and hardware resets - device 1

a) Host asserts RESET- for a minimum of 25 μsec.
b) Device 1 sets the BSY bit no later than 400 nsec after RESET- is negated.
c) Device 1 negates DASP- no later than 1 msec after RESET- is negated.
d) Device 1 negates PDIAG- before asserting DASP-.
e) Device 1 asserts DASP- no later than 400 msec after RESET- is negated.
f) Device 1 performs hardware initialization and diagnostics.
g) Device 1 may revert to its default condition.
h) Device 1 posts diagnostic results to the Error Register.
i) Device 1 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1.
j) If Device 1 passed its diagnostics without error in step f), Device 1 asserts PDIAG-. If the diagnostics failed, Device 1 does not assert PDIAG- and continues to the next step. Device 1 shall clear the BSY bit, and optionally assert PDIAG-, no later than 30 sec from the time RESET- is negated. The device shall set the Sector Count register to 01h, the Sector Number register to 01h, the Cylinder Low register to 00h, the Cylinder High register to 00h, and the Device/Head register to 00h.
k) Device 1 sets the DRDY bit when ready to accept any command.
NOTE: Steps i), j) and k) may occur at the same time. While no maximum time is specified for the DRDY bit to be set to one, a host should allow up to 30 sec for the DRDY bit to become 1. See Figure 6.
l) Device 1 negates DASP- after the first command is received or negates DASP- if no command is received within 31 sec after RESET- is asserted.

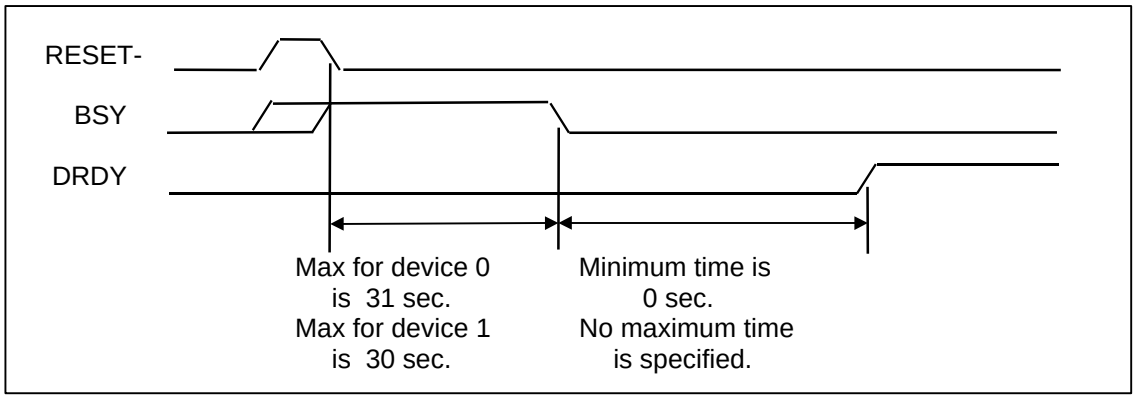


Figure 6 - BSY and DRDY timing for power on and hardware resets

9.2 Software reset

This clause describes the algorithm and timing relationships for Devices 0 and 1 during the processing of software resets.

9.2.1 Software reset - device 0

a) Host sets the SRST bit to one in the Device Control register.
b) Device 0 sets BSY bit no later than 400 nsec after detecting that the SRST bit is equal to one.
c) Device 0 performs hardware initialization and diagnostics.
d) Device 0 may revert to its default condition.
e) Device 0 posts diagnostic results to the Error Register.
f) Device 0 waits for the host to clear the SRST bit to zero.
g) If Device 0 detected that Device 1 is present during the most recent power on or hardware reset sequence, then Device 0 waits up to 31 sec from the time that the SRST bit to become zero for Device 1 to assert PDIAG-. If PDIAG- is asserted within 31 sec, Device 0 clears bit 7 equal to zero in the Error Register,

else Device 0 sets bit 7 equal to one in the Error Register. If device 1 was not detected during the most recent power up or hardware reset sequence, then Device 0 clears bit 7 equal to zero in the Error register. In either case the device shall set the Sector Count register to 01h, the Sector Number register to 01h, the Cylinder Low register to 00h, the Cylinder High register to 00h, and the Device/Head register to 00h.

h) Device 0 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1. Device 0 shall clear the BSY bit no later than 31 sec from the time that the host clears the SRST bit equal to zero.

Note: Steps g) and h) may occur very rapidly.

i) Device 0 sets the DRDY bit when ready to accept any command.

NOTE: Steps h) and i) may occur at the same time. While no maximum time is specified for the DRDY bit to become equal to 1 to occur, a host should allow up to 30 sec for the DRDY bit to be set to one. See Figure 7.

9.2.2 Software reset - device 1

a) Host sets SRST bit to one in the Device Control register.
b) Device 1 set the BSY bit no later than 400 nsec after detecting that the SRST bit to equal to one.
c) Device 1 negates PDIAG- no later than 1 msec after detecting that the SRST bit is one.
d) Device 1 perform hardware initialization and diagnostics.
e) Device 1 may revert to its default condition.
f) Device 1 posts diagnostic results to the Error Register.
g) Device 1 waits for the host to clear the SRST bit equal to zero.
h) Device 1 clears the BSY bit when ready to accept commands that do not require the DRDY bit to be equal to 1.
i) If Device 1 passed its diagnostics without error in step d), Device 1 asserts PDIAG-. If the diagnostics failed, Device 1 does not assert PDIAG- and continues to the next step. Device 1 shall clear the BSY bit, optionally assert PDIAG-, no later than 30 sec from the time the host clears the SRST bit to zero. The device shall set the Sector Count register to 01h, the Sector Number register to 01h, the Cylinder Low register to 00h, the Cylinder High register to 00h, and the Device/Head register to 00h.
j) Device 1 sets the DRDY bit when ready to accept any command.

NOTE: Steps h), i) and j) may occur at the same time. While no maximum time is specified for the DRDY bit to be set to one, a host should allow up to 30 sec for the DRDY bit to become one. See Figure 7.

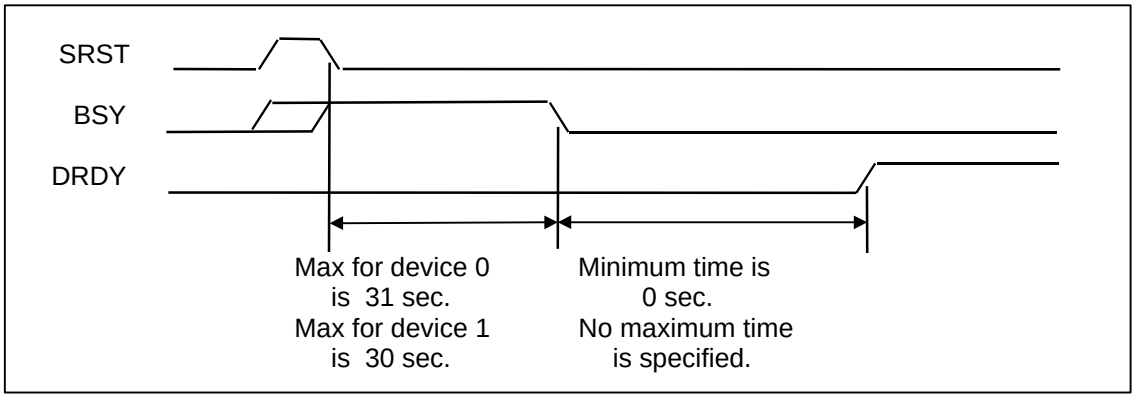


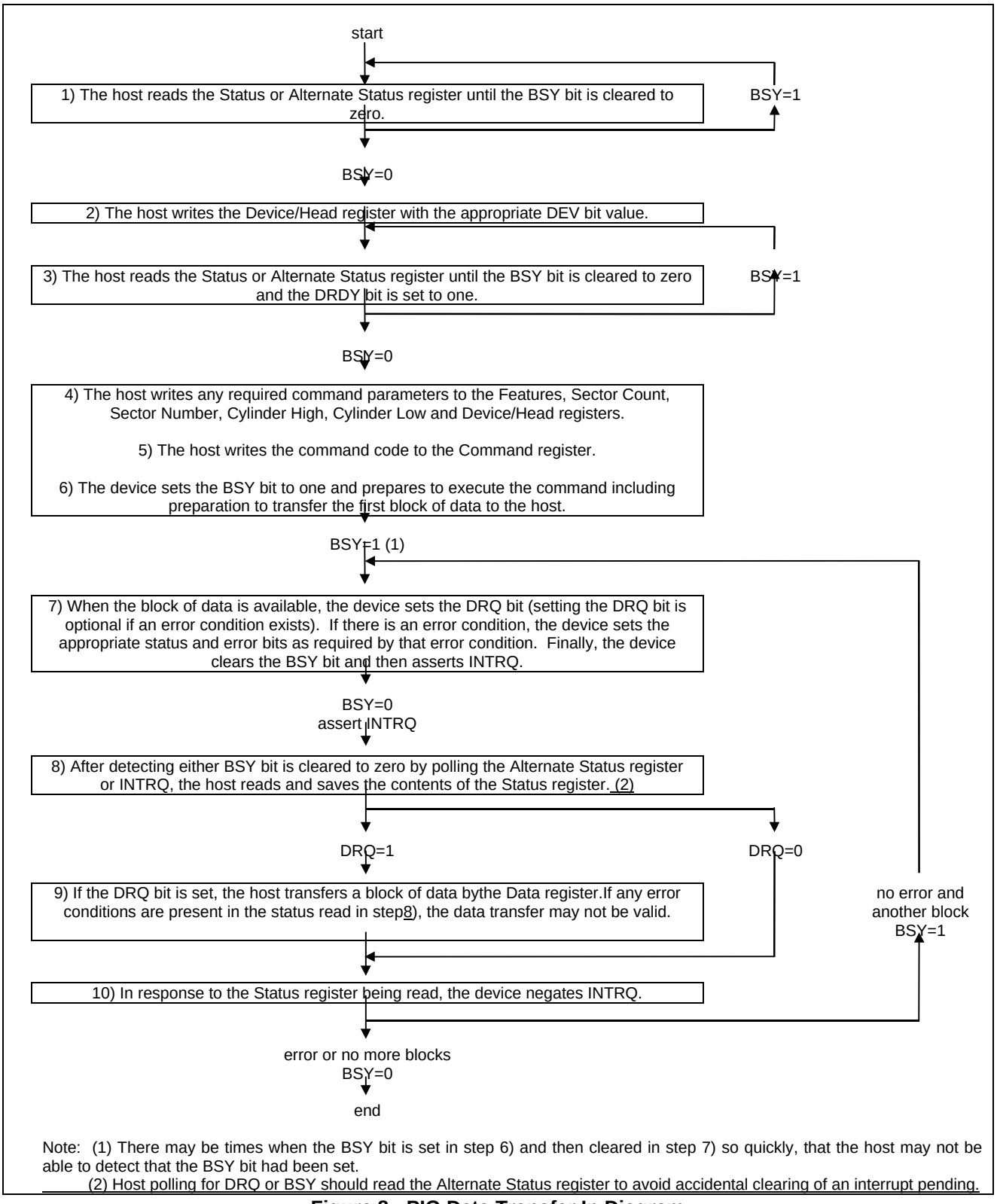
Figure 7 - BSY and DRDY timing for software reset

9.3 PIO data in commands

This class includes:

- IDENTIFY DEVICE
- READ BUFFER
- READ LONG (with and without retry)
- READ SECTOR(S) (with and without retry)
- READ MULTIPLE

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host. The following steps describe the processing of a PIO data in command. This description does not include all possible error conditions. See Figure 8.



Note: (1) There may be times when the BSY bit is set in step 6) and then cleared in step 7) so quickly, that the host may not be able to detect that the BSY bit had been set.

(2) Host polling for DRQ or BSY should read the Alternate Status register to avoid accidental clearing of an interrupt pending.

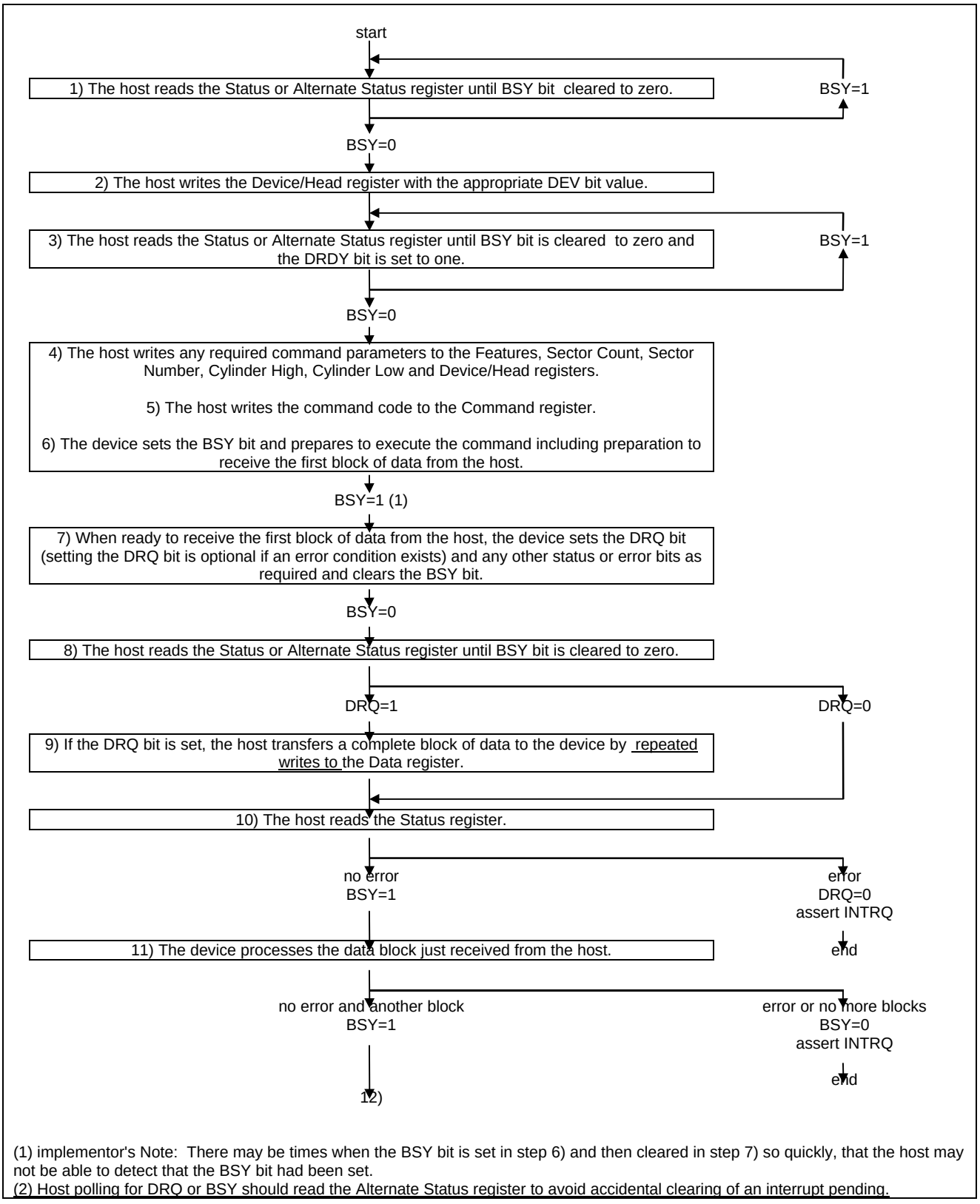
Figure 8 - PIO Data Transfer In Diagram

9.4 PIO data out commands

This class includes:

- DOWNLOAD MICROCODE
- FORMAT TRACK
- SECURE ENABLE RO
- SECURE ENABLE RW
- SECURE UNLOCK
- WRITE BUFFER
- WRITE LONG (with and without retry)
- WRITE MULTIPLE
-
- WRITE SECTOR(S) (with and without retry)
- WRITE VERIFY

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device. The following steps describe the processing of a PIO data out command. This description does not include all possible error conditions. See Figure 9.



(1) implementor's Note: There may be times when the BSY bit is set in step 6) and then cleared in step 7) so quickly, that the host may not be able to detect that the BSY bit had been set.
(2) Host polling for DRQ or BSY should read the Alternate Status register to avoid accidental clearing of an interrupt pending.

Figure 9 - PIO Data Transfer Out Diagram

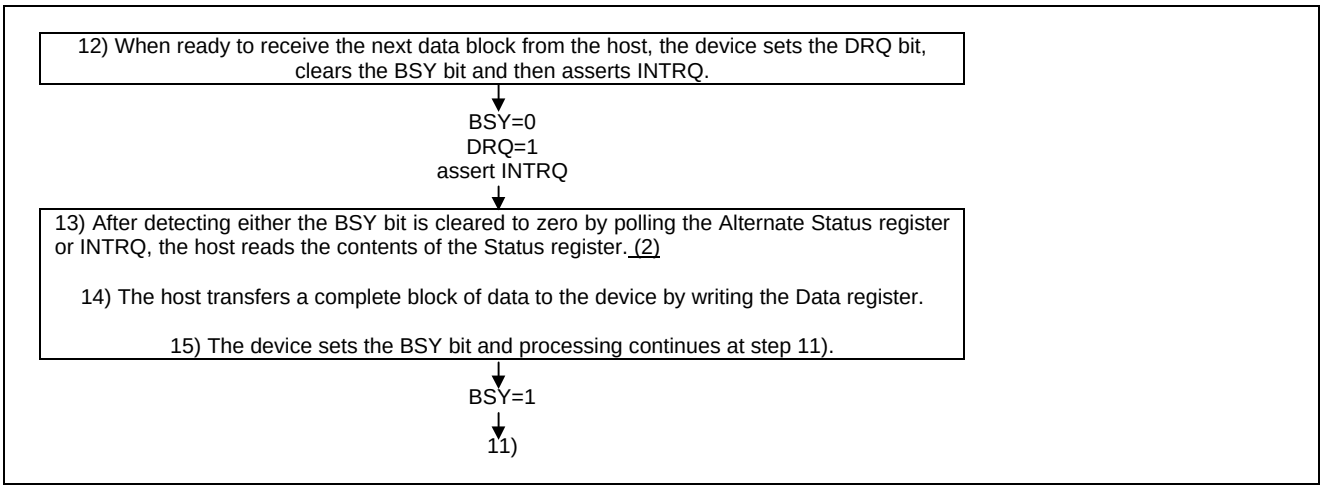


Figure 9 (continued)

9.5 Non-data commands

This class includes:

- CHECK POWER MODE
- DOOR LOCK
- DOOR UNLOCK
- EXECUTE DEVICE DIAGNOSTIC (DRDY=x)
- IDLE
- IDLE IMMEDIATE
- INITIALIZE DEVICE PARAMETERS (DRDY=x)
- MEDIA EJECT
- NOP
- READ VERIFY SECTOR(S)
- RECALIBRATE
- SECURE DISABLE
- SECURE ENABLE WP
- SECURE LOCK
- SECURE STATE
- SEEK
- SET FEATURES
- SET MULTIPLE MODE
- SLEEP
- STANDBY
- STANDBY IMMEDIATE

Execution of these commands involves no data transfer. The following steps describe the processing of a no data transfer command. This description does not include all possible error conditions.

See the EXECUTE DEVICE DIAGNOSTICS command description in Clause 8.8, the NOP command description in Clause 8.16 and the SLEEP command description in Clause 8.34 for additional protocol requirements. See Figure 10.

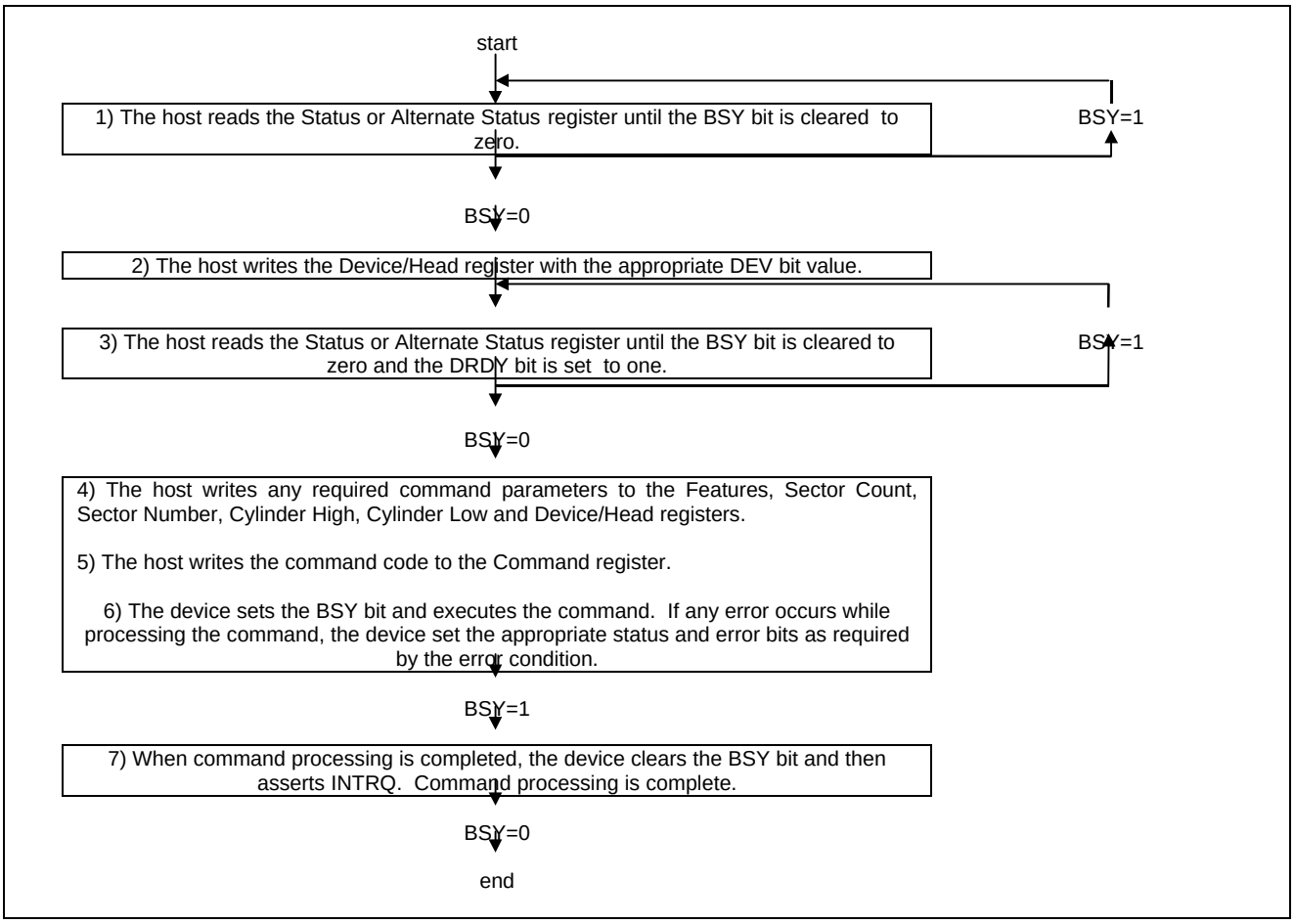


Figure 10 - Non-data Transfer Diagram

9.6 DMA data transfer commands

This optional class comprises:

- READ DMA (with and without retry)
- WRITE DMA (with and without retry)
- IDENTIFY DEVICE DMA

Data transfers using DMA commands differ in two ways from PIO transfers:

- data transfers are performed using the DMA channel
- A Single interrupt is issued at the completion of the command.

Initiation of the DMA transfer commands is identical to the READ SECTOR(S) or WRITE SECTOR(S) commands except that the host initializes the DMA channel prior to issuing the command.

The interrupt handler for DMA transfers is different in that no intermediate sector interrupts are issued on multi-sector commands.

The following steps describe the execution of a DMA command. See Figure 11.

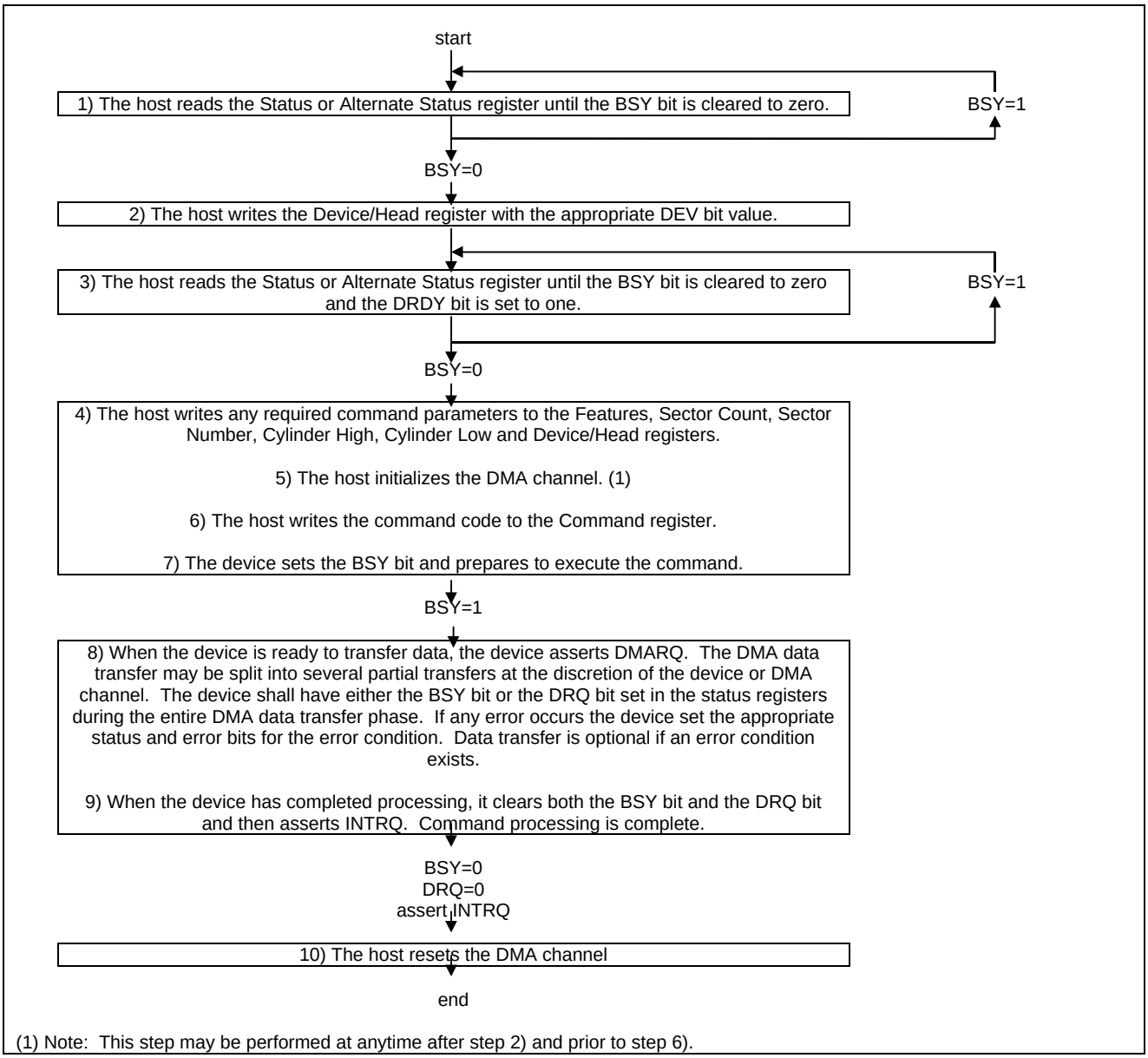


Figure 11 - DMA Data Transfer Diagram

9.7 Single device configurations

9.7.1 Device 0 only configurations

In a single device configuration where Device 0 is the only device and the host selects Device 1, Device 0 may respond to accesses of the Command Block and Control Block registers in one of two methods. These two methods exist because previous versions of the ATA standard did not specify the required behavior for this configuration. The first method is the recommended implementation.

The first method is:

1) A write to the Device Control register shall complete as if Device 0 was the selected device.

2) A write to a Command Block register, other than the Command register, shall complete as if Device 0 was selected.

3) A write to the Command register is ignored.

4) A read of the Control Block or Command Block registers, other than the Status or Alternate Status registers, shall complete as if Device 0 was selected.

5) A read of the Status or Alternate status register returns the value 00h.

> Note: IDX is vendor specific and might change following reset or power mode changes resulting in values for status other than 00h.

The second method requires that Device 0 implement an Error, Status and Alternate Status register that is used whenever Device 1 is selected.

The second method is:

1) The Device 1 Error, Status and Alternate status registers are set to 00h by a reset.

> Note: IDX is vendor specific and might change following reset or power mode changes resulting in values for status other than 00h.

2) A write to the Device Control register shall complete as if Device 0 was the selected device.

3) A write to a Command Block register, other than the Command register, shall complete as if Device 0 was selected.

4) A write to the Command register with a command code other than the INITIALIZE DEVICE PARAMETERS or EXECUTE DEVICE DIAGNOSTICS command causes the Device 1 Error, Status and Alternate Status registers to be used as follows:

a) the BSY bit is set in the Device 1 Status register.

b) the ABRT bit is set in the Device 1 Error register.

c) the ERR bit is set in the Device 1 Status register.

d) the BSY bit is cleared in the Device 1 Status register.

e) if the nIEN bit in the Device Control Register is cleared,
the INTRQ signal is asserted.

5) An EXECUTE DEVICE DIAGNOSTIC command is executed as if it addressed to Device 0.

6) An INITIALIZE DEVICE PARAMETERS command is executed as if Device 1 is present and is actually executing the command. The command shall have no effect of the device parameters of Device 0.

7) A read of the Control Block or Command Block registers, other than the Status or Alternate Status registers, shall complete as if Device 0 was selected.

8) A read of the Error, Status or Alternate status register returns the value in the device 1 copy of these registers. The Device 1 status registers shall contain 00h following a reset and the value 01h following an attempt to execute a command, other than EXECUTE DEVICE DIAGNOSTICS or INITIALIZE DEVICE PARAMETERS, on Device 1.

9.7.2 Device 1 only configurations

Host support of Device 1 only configurations is host specific.

In a single device configuration where Device 1 is the only device and the host selects Device 0, Device 1 shall respond to accesses of the Command Block and Control Block registers in the same way it would if Device 0 was present. This is because Device 1 cannot determine if Device 0 is, or is not, present.

Host implementation of read and write operations to the Command and Control Block registers of non-existent Device 0 are host specific.

Note: The remainder of this section is a host implementation note.

The host implementor should be aware of the following when supporting Device 1 only configurations:

1) Following a hardware reset or software reset, Device 1 will not be selected. The following steps may be used to reselect Device 1:

a) Write to the Device/Head register with DRV bit set to one.
b) Using one or more of the Command Block registers that can be both written and read, such as the Sector Count or Sector Number, write a data pattern other than 00h or FFh to the register(s).
c) Read the register(s) written in step b). If the data read is the same as the data written, proceed to step e).
d) Repeat steps a) to c) until the data matches in step c) or until 31 sec has past. After 31 sec it can probably be assumed that Device 1 is not functioning properly.
e) Read the Status register and Error registers. Check the Status and Error register contents for any error conditions that Device 1 may have posted.

2) Following the execution of an EXECUTE DEVICE DIAGNOSTICS command, Device 1 will not be selected. Also, no interrupt will be generated to signal the completion of the command. After writing the EXECUTE DEVICE DIAGNOSTIC command to the Command register, execute steps a) to e) as described in 1) above.

3) At all other times, do not write zero into the DRV bit of the Device/Head register. All other commands execute normally.

10 Timing

10.1 Deskewing

The host shall provide cable deskewing for all signals originating from the controller. The device shall provide cable deskewing for all signals originating at the host.

All timing values and diagrams are shown and measured at the connector of either device connected to the ATA interface. No values are given for measurement at the host interface.

10.2 Symbols

Certain symbols are used in the timing diagrams. These symbols and their respective definitions are listed below.

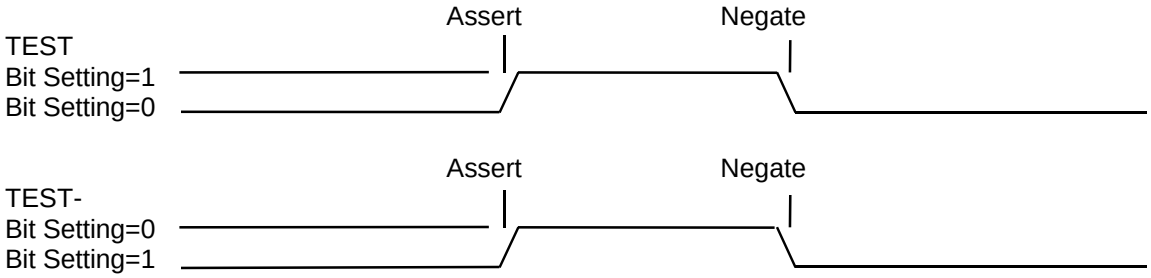
╱ or ╲	-	signal transition (asserted or negated) *
⟨ or ⟩	-	data transition (asserted or negated)
⧖	-	undefined but not necessarily released
- - -	-	the "other" condition if a signal is shown with no change

* All signals are shown with the asserted condition facing to the top of the page. The negated condition is shown towards the bottom of the page relative to the asserted condition.

10.3 Terms

The interface uses a mixture of negative and positive signals for control and data. The terms asserted and negated are used for consistency and are independent of electrical characteristics.

In all timing diagrams, the lower line indicates negated, and the upper line indicates asserted e.g. the following illustrates the representation of a signal named TEST going from negated to asserted and back to negated, based on the polarity of the signal.



10.4 Data transfers

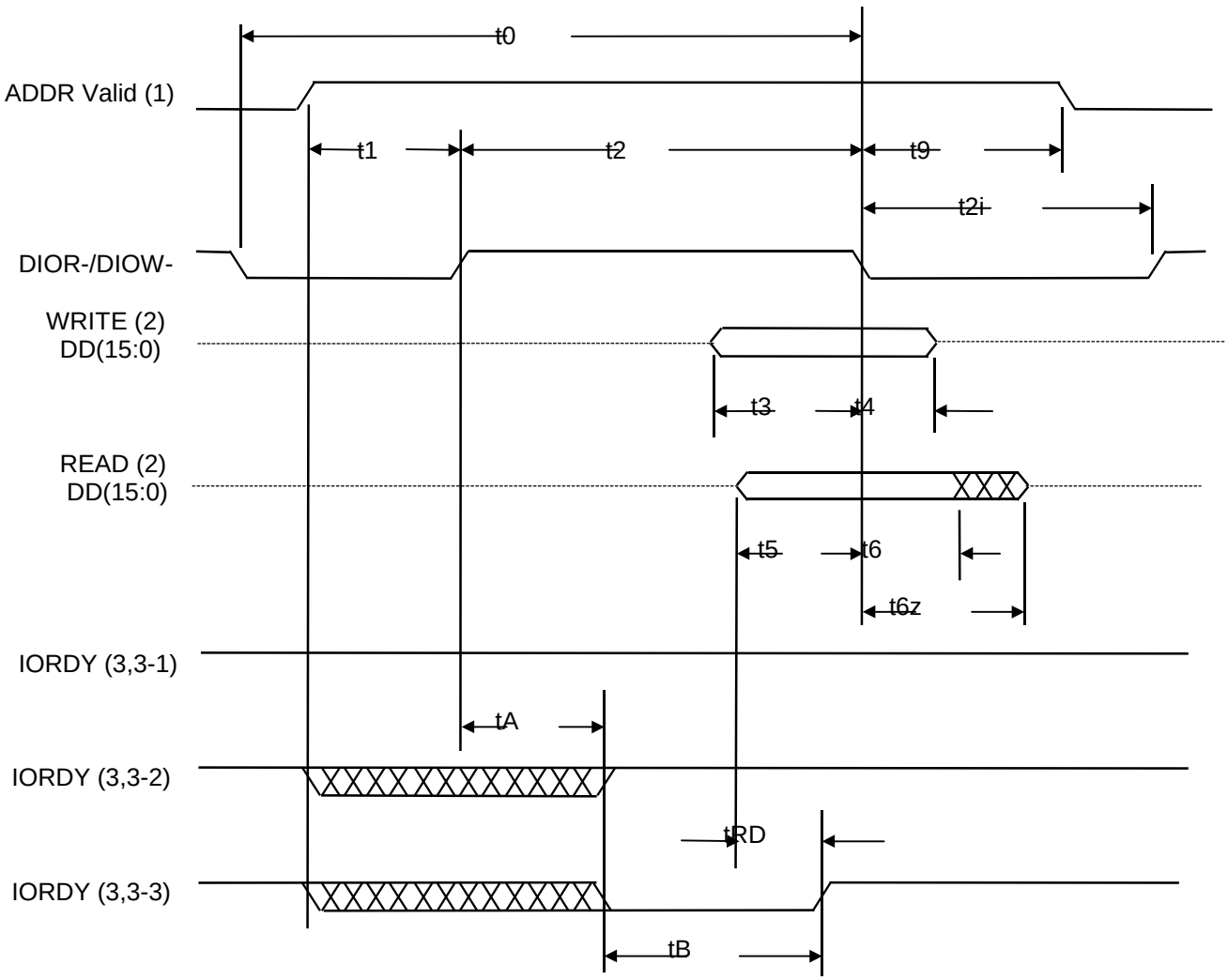
The minimum cycle time supported by the device in PIO Mode 3, 4 and Multiword DMA Mode 1, 2 respectively shall always be greater than or equal to the minimum cycle time defined by the associated Mode e.g. a drive supporting PIO Mode 4 timing shall not report a value less than 120 nsec, the minimum cycle time defined for Mode 4 PIO Timings.

10.4.1 PIO data transfers

Figure 12 defines the relationships between the interface signals for both 16-bit and 8-bit PIO data transfers. Peripherals reporting support for PIO Transfer Mode 3 or 4 shall power up in a PIO Transfer Mode 0, 1 or 2.

For PIO modes 3 and above, the minimum value of t0 is specified by word 68 in the Identify Drive parameter list. The value in word 68 shall not be less than the value shown in Table 21.

IORDY shall be supported when PIO Mode 3 or 4 are the current mode of operation.



Notes:
(1) Device Address consists of signals CS0-, CS1- and DA(2:0)
(2) Data consists of DD(15:0) (16-bit) or DD(7:0) (8-bit)
(3) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:
(3-1) Device never negates IORDY: no wait is generated.
(3-2) Device negates IORDY before tA, but causes IORDY to be asserted before tA: no wait generated.
(3-3) Device negates IORDY before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, device shall place read data on DD(15:0) for tRD before asserting IORDY.

Figure 12 - PIO Data Transfer to/from Device

Table 21 PIO Data Transfer to/from Device

PIO timing parameters			Mode 0 nsec	Mode 1 nsec	Mode 2 nsec	Mode 3 nsec	Mode 4 nsec	Note
t0	Cycle time	(min)	600	383	240	180	120	(1)
t1	Address valid to DIOR-/DIOW- setup	(min)	70	50	30	30	25	
t2	DIOR-/DIOW- 16-bit	(min)	165	125	100	80	70	(1)
	Pulse width 8-bit	(min)	290	290	290	80	70	(1)
t2i	DIOR-/DIOW- recovery time	(min)	-	-	-	70	25	(1)
t3	DIOW- data setup	(min)	60	45	30	30	20	
t4	DIOW- data hold	(min)	30	20	15	10	10	
t5	DIOR- data setup	(min)	50	35	20	20	20	
t6	DIOR- data hold	(min)	5	5	5	5	5	
t6Z	DIOR- data tristate	(max)	30	30	30	30	30	(2)
t9	DIOR-/DIOW- to address valid hold	(min)	20	15	10	10	10	
tRd	Read Data Valid to IORDY active (if IORDY initially low after tA)	(min)	0	0	0	0	0	
tA	IORDY Setup time		35	35	35	35	35	(3)
tB	IORDY Pulse Width	(max)	1250	1250	1250	1250	1250	

Notes:
(1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirements is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the devices identify drive data. A device implementation shall support any legal host implementation.
(2) This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tri-state).
(3) The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the device is not driving IORDY negated at the tA after the activation of DIOR- or DIOW-, then t5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time tA after the activation of DIOR- or DIOW-, then tRD shall be met and t5 is not applicable.5.2.11

10.4.2 Single word DMA data transfer

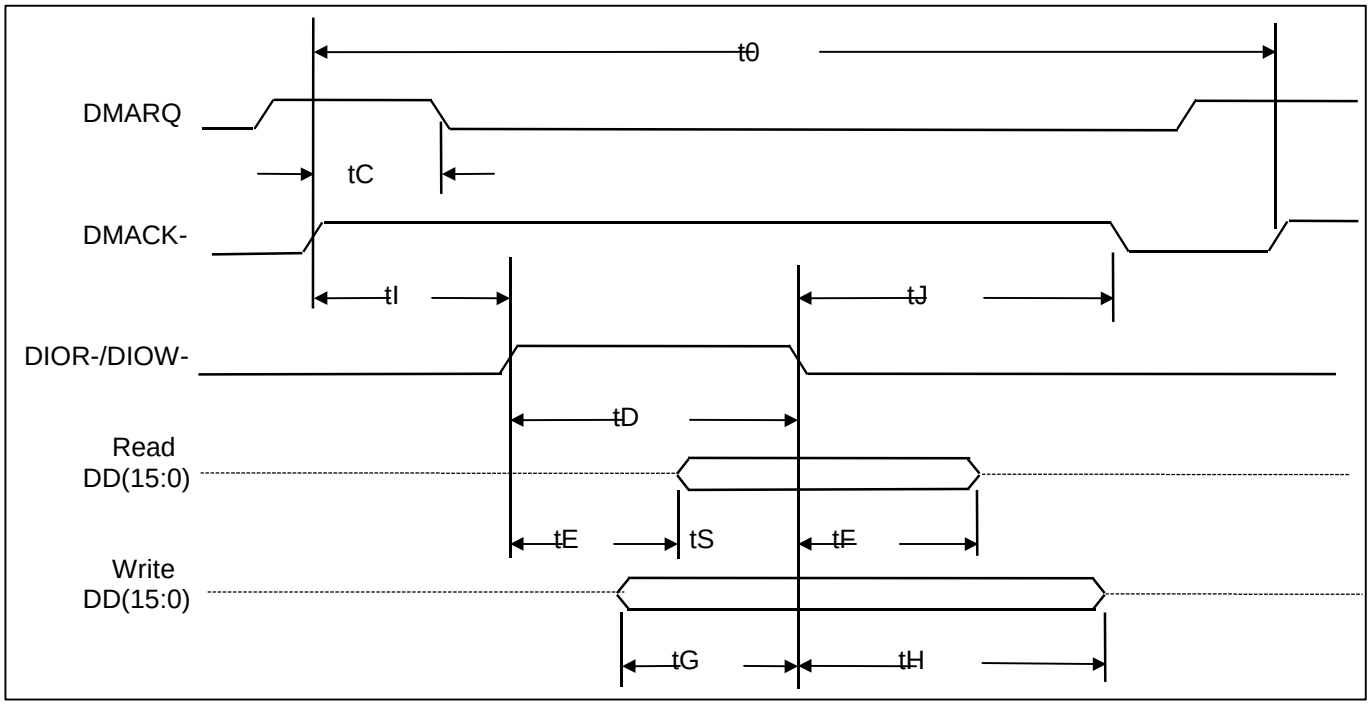


Figure 13 - Single Word DMA Data Transfer

Table 22 - Single Word DMA Data Transfer

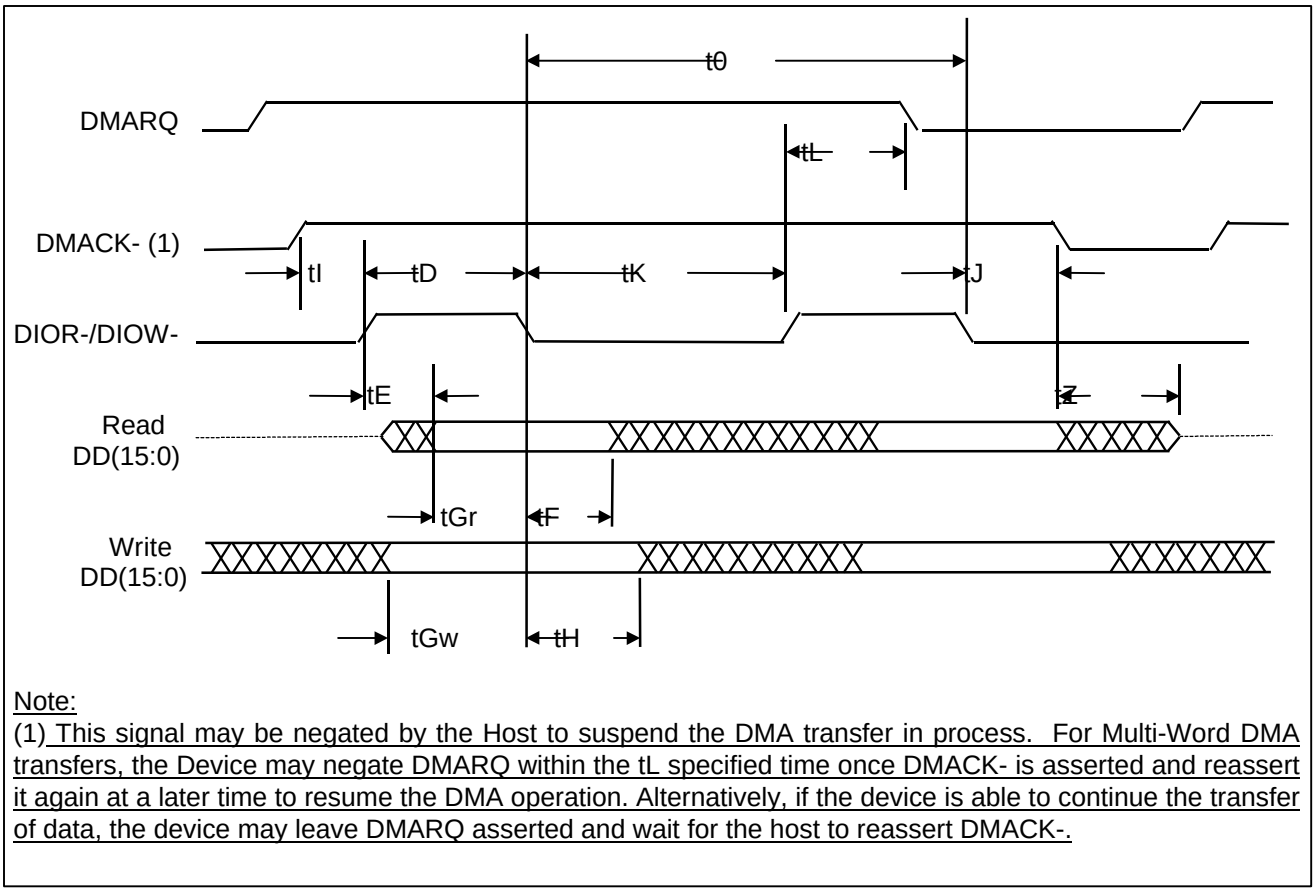
Single word DMA timing parameters			Mode 0 nsec	Mode 1 nsec	Mode 2 nsec
t0	Cycle time	(min)	960	480	240
tC	DMACK to DMARQ delay	(max)	200	100	80
tD	DIOR-/DIOW-	(min)	480	240	120
tE	DIOR- data access	(max)	250	150	60
tF	DIOR- data hold	(min)	5	5	5
tG	DIOW- data setup	(min)	250	100	35
tH	DIOW- data hold	(min)	50	30	20
tI	DMACK to DIOR-/DIOW- setup	(min)	0	0	0
tJ	DIOR-/DIOW- to DMACK hold	(min)	0	0	0
tS	DIOR- setup	(min)	tD-tE	tD-tE	tD-tE

10.4.3 Multiword DMA data transfer

The timings associated with Multiword DMA Transfers are defined in **Figure 14**.

For Multiword DMA modes 1 and above, the minimum value of t0 is specified by word 65 in the Identify Drive parameter list. The value in word 65 shall not be less than the value shown in **Table 23**.

Devices reporting support for Multiword DMA Transfer Mode 2 shall also support Multiword DMA Transfer Mode 0 and 1 and shall power up with Mode 0 as the default Multiword DMA Mode.



Note:
(1) This signal may be negated by the Host to suspend the DMA transfer in process. For Multi-Word DMA transfers, the Device may negate DMARQ within the tL specified time once DMACK- is asserted and reassert it again at a later time to resume the DMA operation. Alternatively, if the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK-.

Figure 14 - Multiword DMA Data Transfer

Table 23 - Multiword DMA Data Transfer

Multiword DMA timing parameters			Mode 0 nsec	Mode 1 nsec	Mode 2 nsec	Note
t0	Cycle time	(min)	480	150	120	(1)
tC	DMACK to DMARQ delay					
tD	DIOR-/DIOW-	(min)	215	80	70	(1)
tE	DIOR- data access	(max)	150	60		
tF	DIOR- data hold	(min)	5	5	5	
tG	DIOW- data setup	(min)	100	30	20	
tH	DIOW- data hold	(min)	20	15	10	
tI	DMACK to DIOR-/DIOW- setup	(min)	0	0	0	
tJ	DIOR-/DIOW- to DMACK hold	(min)	20	5	5	
tKr	DIOR- negated pulse width	(min)	50	50	25	(1)
tKw	DIOW- negated pulse width	(min)	215	50	25	(1)
tLr	DIOR- to DMARQ delay	(max)	120	40	35	
tLw	DIOW- to DMARQ delay	(max)	40	40	35	
tZ	DMACK- to tristate	(max)	20	25	25	

Notes:
(1) t0 is the minimum total cycle time, tD is the minimum command active time, and tK (tKr or tKw, as appropriate) is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, tD, tK shall be met. The minimum total cycle time requirement, t0, is greater than the sum of tD and tK. This means a host implementation can lengthen either or both tD or tK to ensure that t0 is equal to the value reported in the devices identify drive data.. A device implementation shall support any legal host implementation.

Annex A. Connectors

(informative)

A.1 40-pin connector

The I/O connector is a 40-pin connector as shown in Figure 15, with pin assignments as shown in Table 6. The connector should be keyed to prevent the possibility of installing it upside down. A key is provided by the removal of pin 20. The corresponding pin on the cable connector should be plugged.

The pin locations are governed by the cable plug, not the receptacle. The way in which the receptacle is mounted on the printed circuit board affects the pin positions, and pin 1 should remain in the same relative position. This means the pin numbers of the receptacle may not reflect the conductor number of the plug. The header receptacle is not polarized, and all the signals are relative to pin 20, which is keyed.

By using the plug positions as primary, a straight cable can connect devices. As shown in Figure 15, conductor 1 on pin 1 of the plug has to be in the same relative position no matter what the receptacle numbering looks like. If receptacle numbering was followed, the cable would have to twist 180 degrees between a device with top-mounted receptacles, and a device with bottom-mounted receptacles.

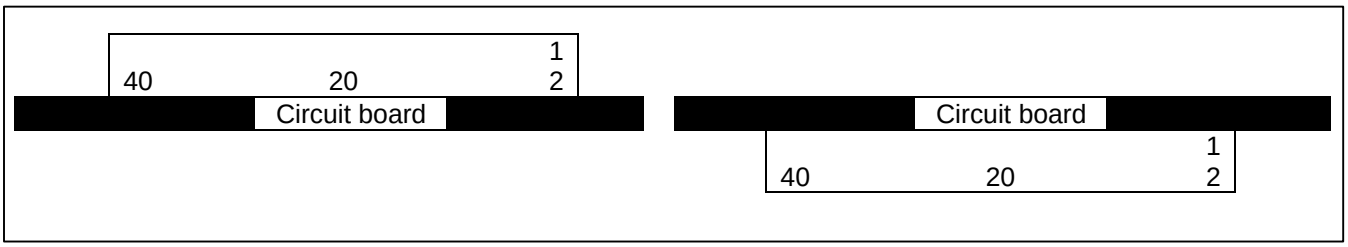


Figure 15 - 40-Pin Connector Mounting

Table 24 - Interface signals - Alphabetical Listing

Signal	Pin
CS0-	37
CS1-	38
CSEL	28
DA0	35
DA1	33
DA2	36
DASP-	39
DD0	17
DD1	15
DD2	13
DD3	11
DD4	9
DD5	7
DD6	5
DD7	3
DD8	4
DD9	6
DD10	8

Signal	Pin
DD11	10
DD12	12
DD13	14
DD14	16
DD15	18
DIOR-	25
DIOW-	23
DMACK-	29
DMARQ	21
ground	2,19,22,24, 26,30,40
INTRQ	31
reserved	32
IORDY	27
keypin	20
PDIAG-	34
RESET-	1

Recommended part numbers for the mating connector and cable are shown below, but equivalent parts may be used.

Connector (40 pin)	3M 3417-7000 or equivalent
Strain relief	3M 3448-2040 or equivalent

Flat cable (stranded 28 AWG)	3M 3365-40 or equivalent
Flat cable (stranded 28 AWG)	3M 3517-40 (shielded) or equivalent

A.1.1 4-pin power connector

When the device uses the 40-pin connector, the device receives DC power through a 4-pin connector. The pin assignments are shown in Table 25. Recommended part numbers for the mating connector to 18 AWG cable are shown below, but compatible parts may be used.

Connector (4 pin)	AMP 1-480424-0 or compatible
Contacts (loose piece)	AMP 60619-4 or compatible
Contacts (strip)	AMP 61117-4 or compatible

Table 25 - DC Interface Using 4 Pin Power Connector

Power line designation	Pin Number
+12 Volts	1
+12 Volt Return	2
+5 Volt Return	3
+5 Volts	4

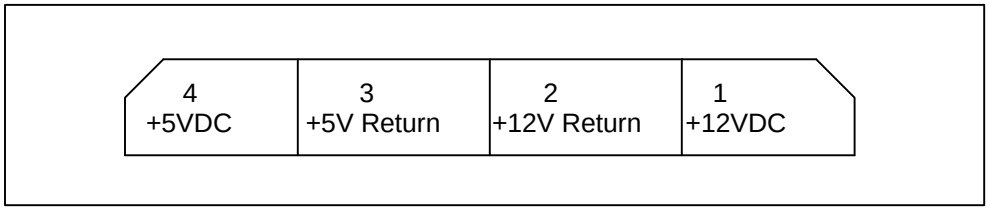


Figure 16 - Drive Side Connector Pin Numbering

A.2 44-pin small form factor connector

This annex describes a connector alternative often used for 2 1/2" or smaller devices. This alternative was developed by the Small Form Factor (SFF) Committee, an industry ad hoc group.

In an effort to broaden the applications for small form factor devices, a group of companies representing system integrators, device suppliers, and component suppliers decided to address the issues involved.

A primary purpose of the SFF Committee was to define the external dimensions of small form factor devices so that products from different vendors could be used in the same mounting configurations.

The restricted area, and the mating of devices directly to a motherboard required that the number of connectors be reduced, which caused the assignment of additional pins for power. Power is provided to the devices on the same connector as used for the signals, and addresses are set by the receptacle into which the devices are plugged.

The 50-pin connector that has been widely adopted across industry for SFF devices is a low density 2mm connector which has no shroud on the plug which is mounted on the device. A number of suppliers provide

intermatable components. The following information has been provided to assist users in specifying components used in an implementation.

Signals Connector Plug	DuPont 86451 or equivalent
Signals Connector Receptacle	DuPont 86455 or equivalent

A.2.1 44-pin signal assignments

The signals assigned for 44-pin applications are described in Table 26. Although there are 50 pins in the plug, a 44-pin mating receptacle may be used(the removal of pins E and F provides room for the wall of the receptacle).

Some devices may utilize pins A, B, C and D for option selection via physical jumpers. Such implementations may require use of the 44-pin receptacles.

The first four pins of the connector plug located on the device are not to be connected to the host, as they are reserved for manufacturer's use. Pins E, F and 20 are keys, and are removed. See Figure 17.

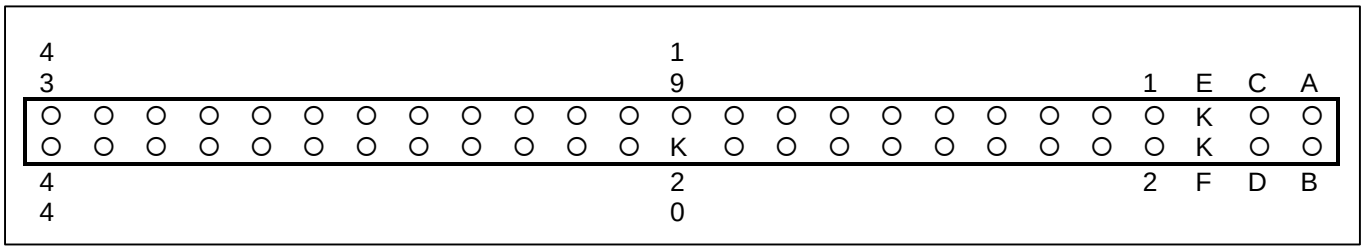


Figure 17 - 44-pin Connector

Table 26 - Signal Assignments for 44-Pin ATA

Signal name	Connector contact	Conductor		Connector contact	Signal name
Vendor specific	A			B	Vendor specific
Vendor specific	C			D	Vendor specific
(keypin)	E			F	(keypin)
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin)
DMARQ	21	21	22	22	Ground
DIOW-	23	23	24	24	Ground
DIOR-	25	25	26	26	Ground
IORDY	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	reserved
DA1	33	33	34	34	PDIAG-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground
+5v (logic) (1)	41	41	42	42	+5v (Motor) (1)
Ground(Return) (1)	43	43	44	44	TYPE- (0=ATA) (1)

Note :
(1) Pins which are additional to those of the 40-pin cable.

A.3 68-pin small form factor connector

This appendix defines the pinouts used for the 68-pin alternative connector for the AT Attachment Interface. This connector is the same as the one defined by PCMCIA. This appendix defines a pinout alternative that allows a device to function as an AT Attachment Interface compliant device, while also allowing the device to be compliant with PC Card ATA mode defined by PCMCIA. The signal protocol allows the device to identify the host interface as being 68-pin ATA or PC Card ATA.

To simplify the implementation of dual-interface devices, the 68-pin AT Attachment Interface maintains commonality with as many PC Card ATA signals as possible, while supporting full command and signal compliance with the ATA standard.

The 68-pin ATA pinout does not cause damage or loss of data if a PCMCIA card is accidentally plugged into a host slot supporting this interface. The inversion of the reset signal between the ATA and PCMCIA interfaces prevents loss of data if the device is unable to reconfigure itself to the appropriate host interface.

A.3.1 Signals

This Specification relies upon the electrical and mechanical characteristics of PCMCIA and unless otherwise noted, all signals and registers with the same names as PCMCIA signals and registers have the same meaning as defined in PCMCIA.

The PC Card-ATA specification is used as a reference to identify the signal protocol used to identify the host interface protocol.

Unless otherwise noted, all signals and registers with the same names as ATA signals and registers have the same meaning as defined in X3.221-1994, which defines the protocol by which commands are directed to the storage device.

A.3.2 Signal descriptions

Any signals not defined below are as described in the ATA, PCMCIA, or the PC Card ATA documents.

Table 27 shows the ATA signals and relationships such as direction, as well as providing the signal name of the PCMCIA equivalent.

Table 27 - Signal Assignments for 68-Pin ATA

Pin	Signal	Hst	Dir	Dev	PCMCIA	Pin	Signal	Hst	Dir	Dev	PCMCIA
1	Ground	x	→	x	Ground	35	Ground	x	→	x	Ground
2	DD3	x	↔	x	D3	36	CD1-	x	←	x	CD1-
3	DD4	x	↔	x	D4	37	DD11	x	↔	x	D11
4	DD5	x	↔	x	D5	38	DD12	x	↔	x	D12
5	DD6	x	↔	x	D6	39	DD13	x	↔	x	D13
6	DD7	x	↔	x	D7	40	DD14	x	↔	x	D14
7	CS0-	x	→	x	CE1-	41	DD15	x	↔	x	D15
8			→	i	A10	42	CS1-	x	→	x(1)	CE2-
9	SELATA-	x	→	x	OE-	43			←	i	VS1-
10						44	DIOR-	x	→	x	IORD-
11	CS1-	x	→	x(1)	A9	45	DIOW-	x	→	x	IOWR-
12			→	i	A8	46					
13						47					
14						48					
15			→	i	WE-	49					
16	INTRQ	x	←	x	READY/ IREQ-	50					
17	Vcc	x	→	x	Vcc	51	Vcc	x	→	x	Vcc
18						52					
19						53					
20						54					
21						55	M/S-	x	→	x(2)	
22			→	i	A7	56	CSEL	x	→	x(2)	
23			→	i	A6	57			←	i	VS2-
24			→	i	A5	58	RESET-	x	→	x	RESET
25			→	i	A4	59	IORDY	o	←	x(3)	WAIT-
26			→	i	A3	60	DMARQ	o	←	x(3)	INPACK-
27	DA2	x	→	x	A2	61	DMACK-	o	→	o	REG-
28	DA1	x	→	x	A1	62	DASP-	x	↔	x	BVD2/ SPKR-
29	DA0	x	→	x	A0	63	PDIAG-	x	↔	x	BVD1/ STSCHG
30	DD0	x	↔	x	D0	64	DD8	x	↔	x	D8
31	DD1	x	↔	x	D1	65	DD9	x	↔	x	D9
32	DD2	x	↔	x	D2	66	DD10	x	↔	x	D10
33		x	←	x	WP/ IOIS16	67	CD2-	x	←	x	CD2-
34	Ground	x	→	x	Ground	68	Ground	x	→	x	Ground

Key:
Dir = the direction of the signal between host and device.
x in the Hst column = this signal shall be supported by the Host.
x in the Dev column = this signal shall be supported by the device.
i in the Dev column = this signal shall be ignored by the device while in 68-pin ATA mode.
o = this signal is Optional.
Nothing in Dev column = no connection should be made to that pin.

Notes:
(1) The device shall support only one CS1- signal pin.
(2) The device shall support either M/S- or CSEL but not both.
(3) The device shall hold this signal negated if it does not support the function.

A.3.2.1 CD1- (Card Detect 1)

This signal shall be grounded by the device. CD1- and CD2- are used by the host to detect the presence of the device.

A.3.2.2 CD2- (Card Detect 2)

This signal shall be grounded by the device. CD1- and CD2- are used by the host to detect the presence of the device.

A.3.2.3 CS1- (Device chip Select 1)

Hosts shall provide CS1- on both the pins identified in Table 27.

Devices are required to recognize only one of the two pins as CS1-.

A.3.2.4 DMACK- (DMA Acknowledge)

This signal is optional for hosts.

This signal is optional for devices.

If this signal is supported by the host or the device, the function of DMARQ shall also be supported.

A.3.2.5 DMARQ (DMA Request)

This signal is optional for hosts.

If this signal is supported by the host or the device, the function of DMACK- shall also be supported.

A.3.2.6 IORDY (I/O Channel Ready)

This signal is optional for hosts.

A.3.2.7 M/S- (Master/Slave)

This signal is the inverted form of CSEL. Hosts shall support both M/S- and CSEL though devices need only support one or the other.

Hosts shall assert CSEL and M/S- prior to applying VCC to the connector.

A.3.2.8 SELATA- (Select 68-pin ATA)

This pin is used by the host to select which mode to use, PC Card-ATA mode or the 68-pin ATA mode. To select 68-pin ATA mode, the host shall assert SELATA- prior to applying power to the connector, and shall hold SELATA- asserted.

The device shall not re-sample SELATA- as a result of either a Hard or Soft Reset. The device shall ignore all interface signals for 19 msec after the host supplies Vcc within the device's voltage tolerance. If SELATA- is negated following this time, the device shall either configure itself for PC Card-ATA mode or not respond to further inputs from the host.

A.3.3 Removability considerations

This Specification supports the removability of devices which use the ATA protocol. As removability is a new consideration for ATA devices, several issues need to be considered with regard to the insertion or removal of devices.

A.3.3.1 Device recommendations

The following are recommendations to device implementors:

- CS0-, CS1-, RESET- and SELATA- should be negated on the device to prevent false selection during hot insertion.

- Ignore all interface signals except SELATA- until 19 msec after the host supplies VCC within the device's voltage tolerance. This time is necessary to de-bounce the device's power on reset sequence. Once in the 68-pin ATA mode, if SELATA- is ever negated following the 19 msec de-bounce delay time, the device should disable itself until VCC is removed.

- The DOOR LOCK and DOOR UNLOCK commands and the MC and MCR bits in the Error register should be used to prevent unexpected removal of the device or media.

A.3.3.2 Host recommendations

The following are recommendations to host implementors:

- Connector pin sequencing should protect the device by making contact to ground before any other signal in the system.

- SELATA- should be asserted at all times.

- All devices should be reset and reconfigured to the same base address each time a device at that address is inserted or removed.

- The removal or insertion of a device at the same address should be detected so as to prevent the corruption of a command.

- The DOOR LOCK and DOOR UNLOCK commands and the MC and MCR bits in the Error register should be used to prevent unexpected removal of the device or media.

Annex B. Identify device data for ATA devices below 8 GB

(informative)

B.1 Definitions and background information

The following abbreviations are used in this annex:

- 528 MB is used to describe a drive that has 1 032 192 sectors or 528 482 304 bytes.
- 8 GB is used to describe a drive that has 16 515 072 sectors or 8 455 716 864 bytes.

The original IBM PC BIOS (Basic Input/Output System) imposed several restrictions on the support of disk drives, and these have been incorporated into many higher level software products. One such restriction limits the capacity of a hard disk drive. Most BIOS software cannot support a disk drive with more than 1,024 cylinders, 16 heads and 63 sectors per track. The maximum addressable capacity of an ATA disk drive under this scheme is 528 MB.

There is growing support of auto-configuration for disk drives on PC systems. The auto-configuration capability usually resides in the BIOS and uses the IDENTIFY DEVICE command data to configure an ATA disk drive.

This annex defines rules for the IDENTIFY DEVICE data of all capacity ATA disk drives and allows BIOS support of ATA drives up to 8 GB using Cylinder/Head/Sector (CHS) addressing.

This specification defines information that newer BIOSs and system software can use to determine the true size of a disk drive and access the full capacity of the drive.

B.2 Cylinder, Head and Sector Addressing

BIOSs and other software that operate an ATA disk drive in CHS (Cylinder, Head and Sector) addressing mode use IDENTIFY DEVICE data words 1, 3, 6 and words 53-58 to ascertain the appropriate translation mode to use and determine the capacity of an ATA disk drive.

Maximum compatibility is achieved if the following rules are obeyed. These rules limit the values placed into words 1, 3, 6, and 53-58. The rules specified here for CHS addressing apply to drives up to 8 GB.

B.2.1 Word 1

For drives less than or equal to 528 MB, IDENTIFY DEVICE data word 1 (Default Cylinders) does not specify a value greater than 1 024.

If a drive is greater than 528 MB but less than or equal to 8 GB, the maximum value that is placed into this word is determined by the value in Word 3 as shown in Table 28.

Table 28 - Word 1 Value

Value in Word 3	Maximum value in Word 1
1 1h	65 535 FFFFh
2 2h	65 535 FFFFh
3 3h	65 535 FFFFh
4 4h	65 535 FFFFh
5 5h	32 767 7FFFh
6 6h	32 767 7FFFh
7 7h	32 767 7FFFh
8 8h	32 767 7FFFh
9 9h	16 383 3FFFh
10 Ah	16 383 3FFFh
11 Bh	16 383 3FFFh
12 Ch	16 383 3FFFh
13 Dh	16 383 3FFFh
14 Eh	16 383 3FFFh
15 Fh	16 383 3FFFh
16 10h	16 383 3FFFh

The value in this word does not change.

B.2.2 Word 3

IDENTIFY DEVICE data word 3 (Default Heads) does not specify a value greater than 16.

The value in this word does not change.

B.2.3 Word 6

For drives of 8 GB or less, IDENTIFY DEVICE data word 6 (Default Sectors) does not specify a value greater than 63.

The value in this word does not change.

B.2.4 Use of words 53 through 58

ATA drives that are over 528 MB does implement words 53-58. Drives not over 528 MB may also implement these words. These words define the addressing for all sectors accessible in CHS mode.

B.2.5 Word 53

IDENTIFY DEVICE data word 53 bit 0 is set to one at all times that the drive is in a valid translation mode. Some drives may have translation modes that cannot be supported. An attempt to put a drive into one of these unsupported modes shall cause word 53 bit 0 to be cleared to zero with words 54-58 cleared to zero until a valid translation mode is established.

B.2.6 Word 54

IDENTIFY DEVICE data word 54 (Current Cylinders) does specify the number of full logical cylinders that can be accessed in the current translation mode. If an INITIALIZE DEVICE PARAMETERS command has not been executed, the contents of this word is the same as word 1. If an INITIALIZE DEVICE PARAMETERS command has been executed, this word is the integer result of dividing the total number of user sectors (this value may be in words 60-61) by the number of sectors per logical cylinder ([word55] x [word56]), but is not a value greater than 65 535.

B.2.7 Word 55

IDENTIFY DEVICE data word 55 (Current Heads) is the number of heads specified by the last INITIALIZE DEVICE PARAMETERS command. This word may contain a value of between 1 and 16. If an INITIALIZE DEVICE PARAMETERS command has not been executed, the contents of this word is the same as word 3.

B.2.8 Word 56

IDENTIFY DEVICE data word 56 (Current Sectors) is the number of sectors specified by the last INITIALIZE DEVICE PARAMETERS command. This word may contain a value of between 1 and 255. If an INITIALIZE DEVICE PARAMETERS command has not been executed, the contents of this word is the same as word 6.

B.2.9 Words 57-58

IDENTIFY DEVICE data words 57-58 contain a 32-bit value that is equal to [word54] x [word55] x [word56]. If words 60-61, LBA sectors, are not zero, words 57-58 are less than or equal to the value in words 60-61 at all times.

B.3 Logical Block Addressing

It is recommended that ATA drives over 528 MB support Logical Block Addressing (LBA).

B.3.1 Words 60-61

IDENTIFY DEVICE data words 60-61 specify the total number of user sectors available in LBA mode at all times. This value is equal to or greater than the value in words 57-58 at all times. The contents of these words do not change.

B.3.2 Orphan sectors

The sectors, if any, between the last sector addressable in CHS mode and the last sector addressable in LBA mode are known as "orphan" sectors. A drive may or may not allow access to these sectors in CHS addressing mode.

The values in words 1, 3 and 6 should be selected such that the number of orphan sectors is minimized. Normally, the number of orphan sectors should not exceed ([word55] x [word56] - 1). However, the host system can create conditions where there are a larger number of orphans sectors by issuing the INITIALIZE DEVICE PARAMETERS command with values other than the values in words 3 and 6.

Annex C. ATA command set summary

(informative)

The following two tables are provided to facilitate the understanding of the ATA command set. Table 29 provides information on which command codes are currently defined. Table 30 provides a list of all of the ATA commands in order of command code.

Table 29 - Command Matrix

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	C	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
1x	C	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
2x	C	C	C	C	R	R	R	R	R	R	R	R	R	R	R	R
3x	C	C	C	C	R	R	R	R	R	R	R	R	C	R	R	R
4x	C	C	R	R	R	R	R	R	R	R	R	R	R	R	R	R
5x	C	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
6x	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
7x	C	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
8x	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
9x	C	C	C	R	C	C	C	C	C	C	V	R	R	R	R	R
Ax	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bx	C	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Cx	V	V	V	V	C	C	C	R	C	C	C	C	R	R	R	R
Dx	R	R	R	R	R	R	R	R	R	R	R	C	C	C	C	C
Ex	C	C	C	C	C	C	C	R	C	R	C	C	C	C	C	C
Fx	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

Key:
C = a unique command
R = Reserved, undefined in current specifications
V = Vender Unique commands
* = Values 11h through 1Fh are identical to command 10h; values 71h through 7Fh are identical to command 70h

Table 30 - Commands Sorted By Command Value

Command Name	Command Code
NOP	00h
Reserved	01h-0Fh
RECALIBRATE	1xh
READ SECTOR(S) (w/ retry)	20h
READ SECTOR(S) (w/o retry)	21h
READ LONG (w/ retry)	22h
READ LONG (w/o retry)	23h
Reserved	24h-2Fh
WRITE SECTOR(S) (w/ retry)	30h
WRITE SECTOR(S) (w/o retry)	31h
WRITE LONG (w/ retry)	32h
WRITE LONG (w/o retry)	33h
Reserved	34h-3Bh
WRITE VERIFY	3Ch
Reserved	3Dh-3Fh
READ VERIFY SECTOR(S) (w/ retry)	40h
READ VERIFY SECTOR(S) (w/o retry)	41h
Reserved	42h-4Fh
FORMAT TRACK	50h
Reserved	51h-5Fh
Reserved	60h-6Fh
SEEK	7xh

Table 30 - Commands Sorted By Command Value (cont.)

Command Name	Command Code
Vendor specific	8xh
EXECUTE DEVICE DIAGNOSTIC	90h
INITIALIZE DEVICE PARAMETERS	91h
DOWNLOAD MICROCODE	92h
Reserved	93h
STANDBY IMMEDIATE (1)	94h E0h
IDLE IMMEDIATE (1)	95h E1h
STANDBY (1)	96h E2h
IDLE (1)	97h E3h
CHECK POWER MODE (1)	98h E5h
SLEEP (1)	99h E6h
Vendor specific	9Ah
Reserved	9Bh-9Fh
Reserved	A0h-AFh
S.M.A.R.T.	B0h
Reserved	B1h-BFh
Vendor specific	C0h-C3h
READ MULTIPLE	C4h
WRITE MULTIPLE	C5h
SET MULTIPLE MODE	C6h
Reserved	C7h
READ DMA (w/ retry)	C8h
READ DMA (w/o retry)	C9h
WRITE DMA (w/ retry)	CAh
WRITE DMA (w/o retry)	CBh
Reserved	CCh-CFh
Reserved	D0h-DAh
ACKNOWLEDGE MEDIA CHANGE	DBh
BOOT - POST-BOOT	DCh
BOOT - PRE-BOOT	DDh
DOOR LOCK	DEh
DOOR UNLOCK	DFh
STANDBY IMMEDIATE (1)	E0h 94h
IDLE IMMEDIATE (1)	E1h 95h
STANDBY (1)	E2h 96h
IDLE (1)	E3h 97h
READ BUFFER	E4h
CHECK POWER MODE (1)	E5h 98h
SLEEP (1)	E6h 99h
Reserved	E7h
WRITE BUFFER	E8h
SECURE MODE	EAh-EBh
IDENTIFY DEVICE	ECh
MEDIA EJECT	EDh
IDENTIFY DEVICE DMA	EEh
SET FEATURES	EFh
Vendor specific	F0h-FFh

Note:
(1) These commands have two command codes and appear in this table twice, once for each command code.