Thick Film Hybrid IC



Features

- Pin compatible with the STK4102II and STK4101V series (high-grade type) over the output range 6 to 50W for easy interchangability
- Small-sized package with the same pin assignment as the STK4101II series
- · Built-in muting circuit to cut off spurious shock noise
- 125°C guaranteed high temperature operation allows greatly reduced heat sink size
- · Excellent low-cost performance

Package Dimensions

unit: mm

4083



Specifications

Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		±34.5	. V
Thermal resistance	Өј-с		3.0	°C/W
Junction temperature	Тј		150	°C
Operating substrate temperature	Tc		125	°C
Storage temperature	Tstg		-30 to +125	°C
Available time for load short-circuit	ts	$V_{CC} = \pm 23V, R_L = 8\Omega, f = 50Hz, P_O = 20W$	2	s

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC}		+23	V
Load Impedance	RL		8	Ω

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Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	I _{CCO}	V _{CC} = ±28V	20	40	100	mA
	P ₀ (1)	THD = 0.4%, f = 20Hz to 20kHz	20	-	-	w
Output power	P ₀ (2)	$\label{eq:V_CC} \begin{array}{l} V_{CC} = \pm 20 \text{V}, \mbox{THD} = 1.0\%, \\ R_L = 4 \Omega, \mbox{ f} = 1 \mbox{Hz} \end{array}$	20	-	-	w
Total harmonic distortion	ТНО	$P_0 = 1.0W$, f = 1kHz	-	-	0.3	%
Frequency response	fL, fH	$P_0 = 1.0W, \frac{+0}{-3} dB$	_	20 to 50k	_	Hz
Input impedance	ri ri	P ₀ = 1.0W, f = 1kHz	_	55	_	kΩ
Neutral voltage	V _N	V _{CC} = ±50.5V	70	0	+70	mV
Output noise voltage	V _{NO}	$V_{CC} = \pm 28V$, Rg = 10k Ω	-	-	1.2	mVrms
Muting voltage	V _M		-2	5	-10	V V

Operating Characteristics at Ta = 25°C, V_{CC} = ±23V, R_L = 8 Ω (noninductive load), Rg = 600 Ω , VG = 40dB

Notes.

All tests are measured using a constant-voltage supply unless otherwise specified. Available time for load short-circuit and output noise voltage are measured using the transformer supply specified below.

The output noise voltage is the peak value of an average-reading meter with an rms value scale (VTVM). A regulated AC supply (50Hz) should be used to eliminate the effects of AC primary line flicker noise.

Specified Transformer Supply (RP-25 or Equivalent)



Equivalent Circuit





Sample Application Circuit (20W min, 2-Channel, AF Power Amplifier)

Sample Application Circuit PCB Layout (Copper Foil Surface)



 $50\times 100 \text{mm}^2$ Unit (resistance: Ω ; capacitance: F)





THD — Po



2 3 5 _{1k} 2 3 Frequency, f — Hz

5 10k 2 3 5 100k

-40

-50 L____ 10

2 3 5 100





C1, C2	Input filter capacitors. These, together with R3 and R4, form filters to reduce high-band noise.
C3, C4	Input coupling capacitors. For DC blocking. Since capacitor reactance becomes larger at lower frequencies, the output noise can be adversely affected by signal sourc resistance-dependent 1/f noise. In this case, a lower reactance value should be chosen. In order to remove pop noise at power-on, larger values of capacitance should be chosen for C3 and C4, which determine the input time constant, and smaller values for C5 and C6 in the N circuit.
C5, C6	NF capacitors. These determine the low-side cut-off frequency. $f_{L} = \frac{1}{2\pi \times C5 \times R5}$ [Hz] A large value should be chosen for C5 to maintain voltage gain at low frequencies. However, because this would tend to increase the shock noise at power-on, a value larger than absolutely necessary should be avoided.
C15	Decoupling capacitors. This removes shock noise and ripple voltage from the supply.
C11, C12	Bootstrap capacitors. If these capacitors are made small, then the total harmonic distortion at low frequencies increases significantly.
C9, C10	Oscillation prevention capacitors. These should be inserted as close as possible to the IC supply pins to reduce supply impedance and hence provide stable IC operation. Electrolytic capacitors are recommended.
C14	Ripple filter capacitor. This forms a ripple filter in combination with internal transistor TR10.
C7	Oscillation prevention capacitor. Mylar capacitors are recommended for their excellent thermal and frequency characteristics.
R3, R4	Input filter resistors.
R1, R2	Input bias resistors. These are used to bias the input pins at zero potential. The input impedance is largely determined by this resistance.
R5, R9 (R6, R10)	Voltage-gain VG setting resistors. VG = 40dB is recommended using R5, R6 = 560 Ω , and R9, R10 = 56k Ω . Gain adjustments are best made using R5 or R6. If gain adjustments are made using R5 or R6, then set R1, R2 = R9, R10 to maintain V _N balance stability.
R11, R13 (R12, R14)	Bootstrap resistors. These resistors determine the quiescent current. Values of 2.2k Ω and 2.2k Ω are recommended.
R21	Ripple filter resistor. This resistor performs as predriver transistor limiting resistor during load short circuits.
R18	Clipping plus/minus balance resistor.
R19, R20	Ripple filter resistors. When muting transistor TR11 is on, current flows from ground through TR11 to $-V_{CC}$. Values of 1k Ω (0.5W) and 1k Ω (0.5W) are recommended.

External Component Description



Sample Application Circuit (Protection and Muting Circuit)

Heatsink Design

The total STK4132II device power dissipation for a continuous sine wave signal is shown in figures 1 and 2. The maximum dissipation is 29.2W for $R_L = 8\Omega$, and 42.8W for $R_L = 4\Omega$ (2-channel simultaneous drive).



When estimating the power dissipation for an actual audio signal input, the rule of thumb is to select Pd corresponding to $(1/10) \times P_0$ max (within safe limits) for a continuous sine wave input. For example,

$$Pd = 18.6W$$
 for 8Ω , and $Pd = 23W$ for 4Ω

The heatsink thermal resistance, θ c-a, required to dissipate the STK4132II device total power dissipation, Pd, is determined as follows:

Condition 1: IC substrate temperature not to exceed 125°C.

where Ta is the guaranteed maximum ambient temperature.

Condition 2: Power transistor junction temperature, Tj, not to exceed 150°C.

$$Tj = Pd \times \theta c \cdot a + Pd/4 \times \theta j \cdot c + Ta \le 150^{\circ}C \dots (2)$$

The STK4132II has 4 power transistors (2 per channel), and the thermal resistance per transistor, θj -c, is 3.0°C/W. Therefore, equation 2 becomes:

 $Pd \times (\theta c - a + 3.0/4) + Ta \le 150^{\circ}C$ (3)

The required heatsink must have a thermal resistance that satisfies both expressions 1 and 3. Figure 3 shows the ambient temperature parameter against Pd and θ c-a calculated from equations 1 and 3.





For example, a stereo amplifier with ambient temperature of $Ta = 50^{\circ}C$ needs a heatsink with thermal resistance given by the following:

For V_{CC} = ± 23 V, R_L = 8Ω: 1/10 P_O max corresponds to Pd1 = 18.6W From figure 3, the STK4132II thermal resistance is θ c-a1 = 4.04°C/W From equation 3, this results in a junction temperature Tj = 139.1°C. For V_{CC} = ± 20 V, R_L = 4Ω:

1/10 P_O max corresponds to Pd2 = 23W From figure 3, the STK4132II thermal resistance is $\theta c-a2 = 3.26^{\circ}C/W$

From equation 3, this results in a junction temperature Tj = 142.3 °C.

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