CCS Technical Documentation
NHL-2NA Series Transceivers

Camera Module

Issue 1 07/02

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Table of Contents

List of Figures

Abbreviations

VGA	Video Graphic Array
CIF	Common intermediate format
CCI	Camera Control Interface
LVDS	Low voltage differential signals
CCP	Compact camera port
CDS	Correlated double sampling
AGC	Automatic gain control
ADC	Analog digital converter
TG	Timing generator
SG	Synchronization generator
PLL	Phase locked loop
VCO	Voltage control oscillator
AWB	Automatic white balance
AES	Automatic electronics shutter

Camera Module

Key specification

The table below shows the key specification of the VGA2 camera module (TCM8002MD).

Table 1: Key specification

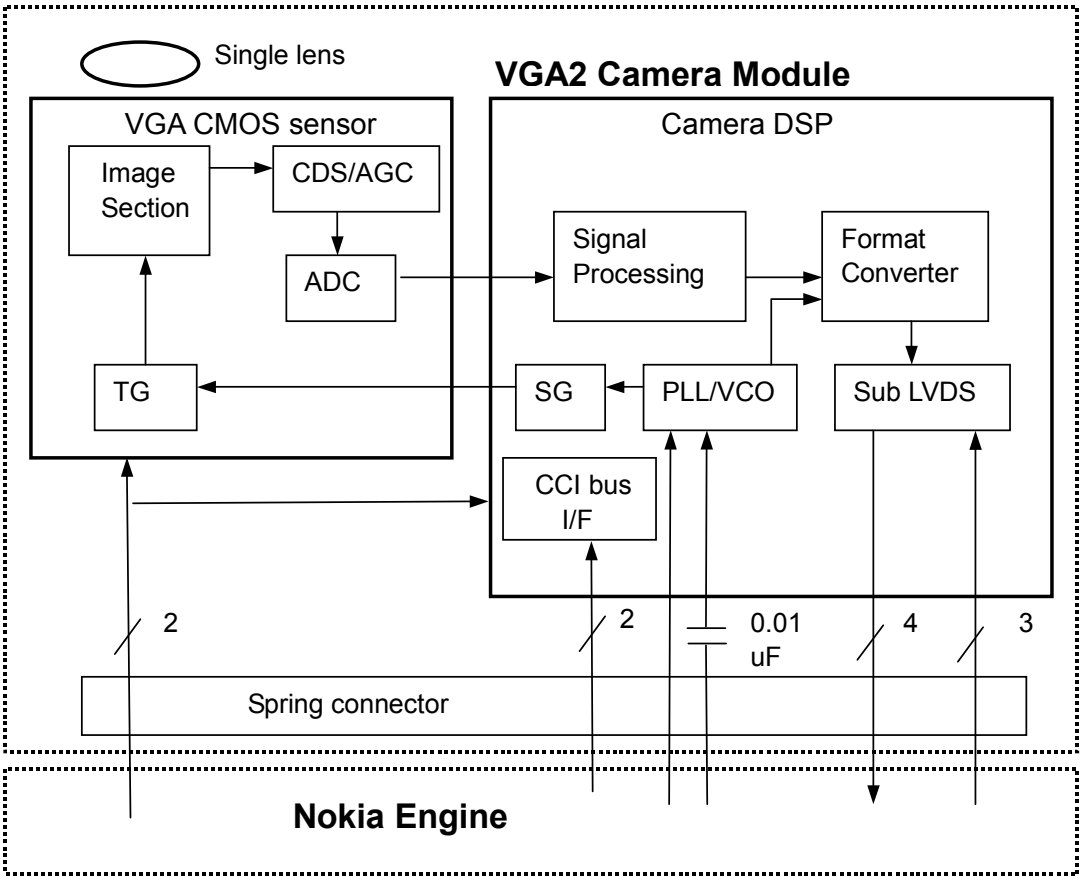
Image sensor	Array format	active: 660 H x 492 V
	color filter	RGB bayer arrangement
	Optical format	1/4 "
	pixel size	5.4 um
lens	F no.	2.8
	H view angle	53 degrees(H) / 39(V) / 65(D)
	focal length	3.5 mm
	focus range	30 cm to infinity
	focus adjustment	Object distance for adjustment is infinity.
Interface	image signal output	CCP (sub LVDS serial output)
	output image format	YUV 4:2:2, RGB 5:6:5, sensor 10 bit raw data
	image size	A variety of size is supported. See table 6
	frame rate	typical : 15 fps
	master clock	External clock is supplied.
	control interface	CCI bus
	mechanics	13-pin spring connector
Power source	VDD=DC 2.78 +/- 0.13 V and VDDI =DC 1.8 +/- 0.1	
Current consumption	VDD on & VDDI	34 mA typical for VDD, 7 mA typical for VDDI
	VDD off & VDDI	1 uA
Dimension	16 mm (H) x 20 mm (W) x 8.9 mm (D) excluding protrusion of connector	
Weight		1.6 gram
Temperature range	operation	-30 to + 70 centigrade
	full quality	-10 to + 40 centigrade
	storage	-40 to + 85 centigrade

Electrical specifications

Block diagram

The figure below shows the block diagram of the VGA2 camera module connected to Nokia Engine.

Figure 1: Block diagram of camera module



Signal description

The following description indicates the meaning of each signal shown in figure above.

(1) VDD	Supply voltage to the main circuits of a camera module
(2) GND2	Ground line corresponding to VDD
(3) D +	Fast serial data out
(4) VDDI	Supply voltage to sub LVDS circuit. This voltage can be always applied, even if the Vctrl is off.
(5) D -	Fast serial data out of which is inverted to D+
(6) SDA	Serial data line of CCI bus
(7) GND1	Ground line corresponding to VDDI
(8) SCL	Serial clock line of CCI bus
(9) Clk +	Fast serial clock
(10) Vctrl	This signal is used for sub LVDS circuit to be shut off in order to reduce stand-by current of a camera module. "High" designates "ON". Please see the operation flow chart.
(11) Clk -	Fast serial data out of which is inverted to Clk+
(12) GND3	Ground line corresponding to Extclk.
(13) Extclk	System clock from Nokia engine to the camera module. This signal is sinusoidal by RC filtering on Nokia engine. Extclk is AC coupled to the camera module through a capacitor of which capacitance is more than

0.01 uF. Extclk has 4 operating modes depending on the wireless system in which the camera module is used. The Extclk is active before VDD is on. This Extclk shall be exclusively used for generating any other clocks

DC characteristics

(1) Maximum ratings

VDD	3.6 V
VDDI	2.7 V
Input signals, min	-0.3 V
Input signals, max	VDDI (1.8V) + 0.3 V

Note: Values respect to GND.

(2) DC characteristics of each signal are shown in the table below.

Table 2: DC characteristics of each signal

Signal name	Type		Min	Typ	Max	Unit
VDDI	IN		1.7	1.8	1.9	V
VDDI current consumption *2			--	7	10	mA
D+,D-, Clk+,Clk	OUT		VDDI/2 - 0.1	VDDI/	VDDI/2 + 0.1	V
			1	104	120	MHz
ExtCl	IN		0.5	1	1.2	V peak-peak
	Mode		6.45/12.9	6.5/13.0	6.55/13.1	MHz
	Mode		9.55/19.1	9.6/19.2	9.65/19.3	MHz
	Mode		8.35/16.7	8.4/16.8	8.45/16.9	MHz
	Mode		9.67/19.34	9.72/19.44	9.77/19.54	MHz
	The wave shape is sinusoidal by applying LPF in a host					
SDA, SCL	IN/OUT		0.3*VDDI	-	0.7*VDDI	VIL, VIH
VDD	IN		2.65	2.78	2.91	V
Stand-by Current(*1)	ExtClk open		--	1	5	uA
	ExtClk 500mVpp		--	1	5	uA
VDD current consumption *2			--	34	40	mA
Vctr	IN	High	VDDI x 0.7	--	VDD	V
		Low	0	--	VDDI x 0.3	V

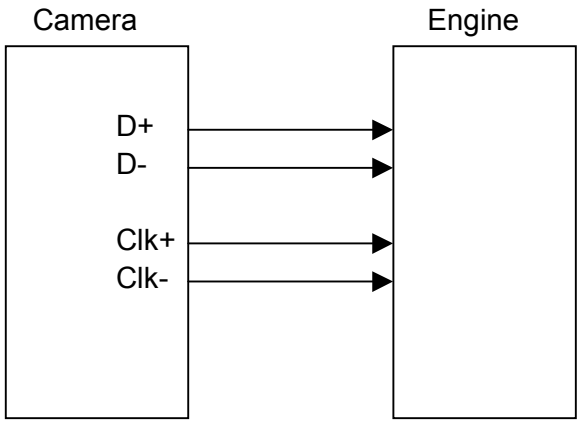
*1 Measuring conditions of typical value
VDD Off, VDDI 1.8V On, VCtrl Off, ExtClk Open or 500mVp-p, Temperature 25C
Lens capped.

Signals specifications

Signals and timing

The fast serial interface of digital image data is employed for the VGA camera module. The fast serial interface described in this document is named CCP (Compact Camera Port). In terms of signaling scheme, CCP is based on the idea of IEEE standard LVDS signaling scheme (current mode differential low voltage signaling method). CCP described in this document utilizes lower voltage than that of standard LVDS. The low voltage LVDS is named in this document sub LVDS. CCP is an one-way differential serial camera connection with clock and integrated line / frame synchronization:

Figure 2: CCP interface between camera and engine



D+ and D- are differential picture data output from the camera module. This data is written on each falling edge of **Clk**. Data format is least significant bit first. When nothing is being transferred, **D** remains high, except in power shut-down.

Clk+ and Clk- are differential pixel clock. Data should be read by the receiving end on rising edge. When nothing is being transferred, **Clk** remains high, except in power shut-down.

The figure below shows the basing timing between D and Clk schematically. In the table below the AC characteristics in D and Clk relation are shown.

Figure 3: Basic bus timing

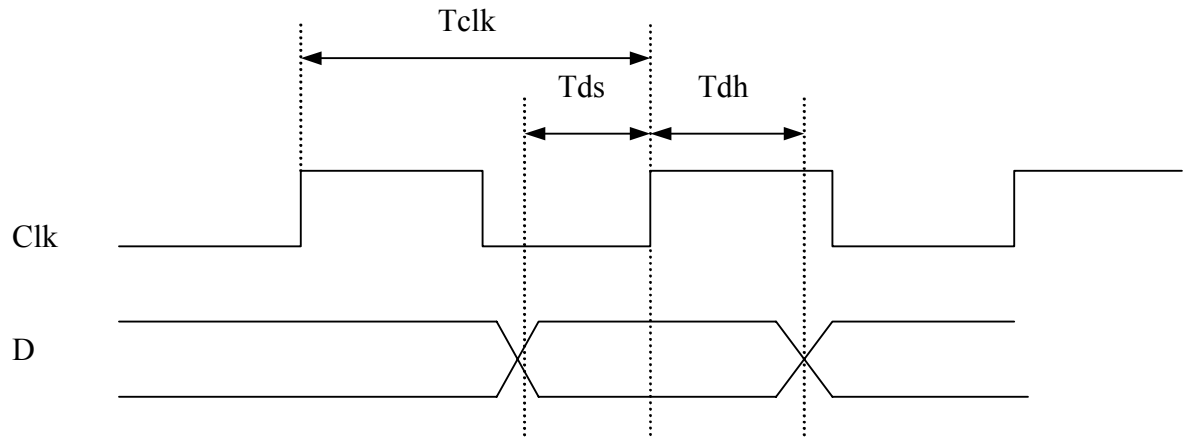


Table 3: AC timing between D and Clk

Parameter	Abbreviation	Min time	Max time
Bus clock cycle	**T**clk	8.3 ns (120MHz)	1000 ns (1 MHz)
Data set-up time before **Clk** rising	**T**ds	1ns	
Data hold time	**T**dh	2 ns	

	Min	Typ	Max	Unit
Clk duty	40/60	50/50	60/40	%

Synchronization

Each image line that is received begins with line synchronization code and ends with line end code. Each frame begins with frame synchronization code and ends with frame end code. At frame start and frame end no line synchronization are added but they are replaced by the frame synchronization.

Image formats and frame rate

The table below shows the relationship between Extclk and CCP frequency to keep the frame rate constant (approximately 15 fps). Each mode on the table below can be selected by CCI bus command setting from Nokia engine.

Table 4: Frequency relationship for each Extclk (VGA image)

Mode	Extclk	CCP frequency	Pixel clock	Number of Pixel clock per H	Frame rate
	MHz	MHz	MHz		fps
1	6.5/13.0	104.0	6.50	828	14.952
2	9.6/19.2	115.2	7.2	916	14.972
3	8.4/16.8	100.8	6.30	802	14.962
4	9.72/19.44	116.6	7.29	928	14.962

The table below shows image size format of the respective image made from the original full VGA. Each CCP frequency shown on the table below designates the ratio to CCP frequency of full VGA at 15 fps.

In case of subsampling QVGA, subsampling QQVGA and subsampling QCIF, 30 fps operation is supported as well as 15 fps. In this case, CCP frequency becomes twice.

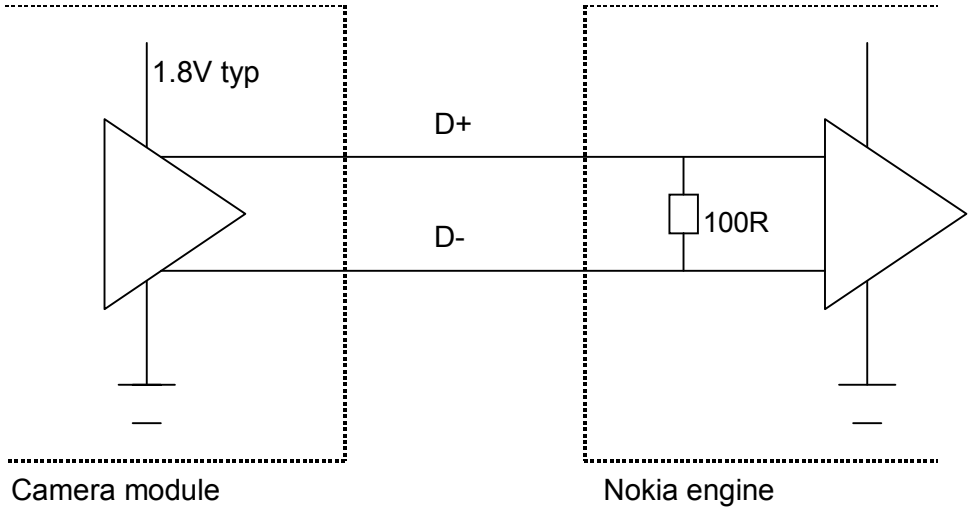
Sub LVDS specification

General

The fast serial transfer of image data from the camera module to Nokia engine is to be

achieved based on 1.8 power supply condition. Accordingly, modified LVDS type current mode transmitters/receivers is used. In this document, the LVDS scheme which is modified corresponding to 1.8 V is named sub LVDS. The figure below shows simplified configuration of sub LVDS

Figure 4: sub LVDS configuration



DC, AC characteristics

DC characteristics, AC characteristics (transmitting end) and (receiving end) are shown in the tables below.

Table 5: DC characteristics

Item	Min	Typ	Max	Unit
Bus operating voltage VDDI	1.7	1.8	1.9	V
Absolute maximum rating	- 0.3		VDDI + 0.3	V

Table 6: AC characteristics of camera module

Parameter	**Signal level**			
	Min	Typical	Max	
Input voltage range	VDDI/2-0.1	VDDI/2	VDDI/2+0.1	V
Differential voltage swing Vod	100	150	200	mV
Output impedance R0	40	100	140	Ohm
Operating frequency	1		120	MHz
Clock duty cycle @ 120 MHz	40	50	60	%
Vod rise time 20% - 80%	300		500	ps
Vod fall time 80% - 20%	300		500	ps

Note: Vod is measured with 100 ohm termination.

Camera control interface

General

The camera control interface configuration is based on fast mode IIC(i.e. I^2C) bus.

Slave address

The Camera Module control interface has got slave address 78h. General call address and start byte are not supported.

Sub address

A sub address for internal register are prepared. Width of sub address is 8 bits, and each address has 8 registers. The camera module has the function of increment addressing, the host can operate continuous addresses by one sequence. After system reset by Power ON (when VDD is applied) subaddress becomes 00'h.

Read & write

Nokia engine can read and write all registers' data except for test registers.

Operating procedure

Mode description

This camera module supports following two operating modes.

1 Normal mode
This mode means continuous image capturing operation.
(Namely every frame is output.)
2 Long storage mode
This mode means intermittent image capture operation (one frame out of every four frame) particularly in case of long time exposure. Nokia engine submits a command to set this mode.

Operation flow chart

(1) For Power-on, the following order is necessary.

VDDI(1.8 V) power ON → Extclk ON → Vctrl ON → VDD(2.8 V) Power ON →
T1 T2 T3 T4
Command for initializing → Image data output start.
T5

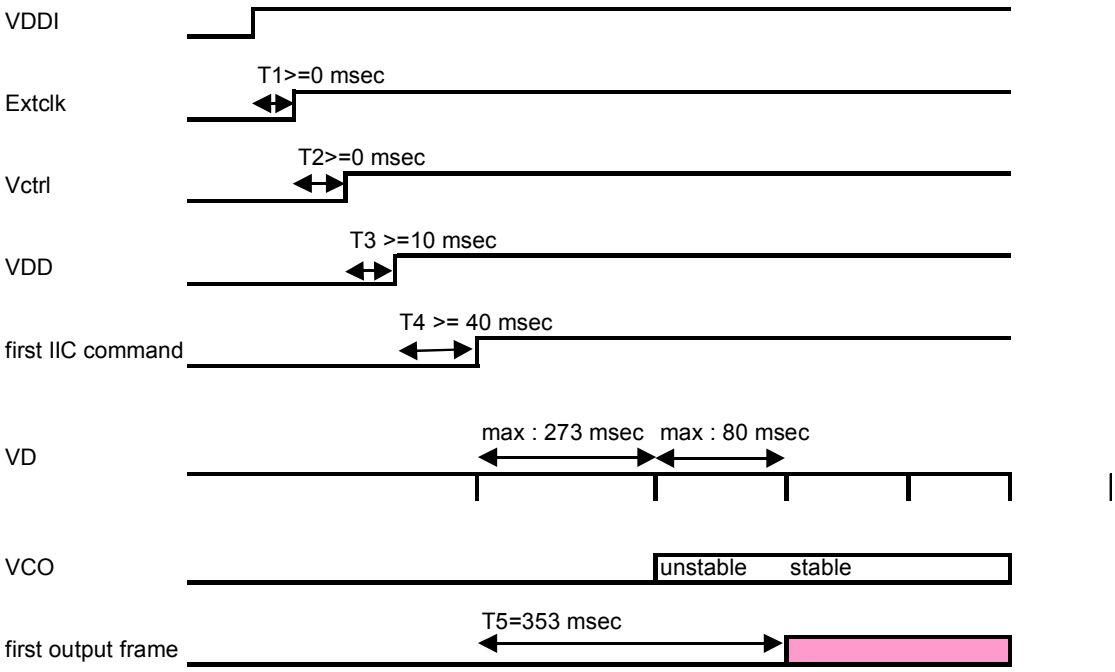
The camera has default values of parameters for start-up action. The host can change

the parameter values by sending the parameter value via CCI bus. In this case these changed values are not memorized in the camera module because no EEPROM is provided inside.

Accordingly. after power-off, the host must send the values again if the same operation is necessary. The necessary time interval for moving to the next operation is listed in Figure 9. For the external clock of 6 MHz (lowest), the pixel clock becomes 1.5 MHz (without VCO). In this case, one vertical scanning period is 273 msec t the maximum value).

In the figure below, "VD" is internal synchronization pulse to show vertical scanning period.

Figure 9. operation sequence in power-on



(2) For Power-off

VDD(VDD2.8 V) → Vctrl OFF → Extclk OFF → OFF VDDI (1.8 V) OFF
T1>=0 T2>=0 T3>=0

Mechanics

Mechanics drawing in the file of "TCM8002MD external view.pdf".

The camera module has got a plastic lens holder with a metallized surface. The lens barrel part does not have metallization. The material of the lens holder plastic is 30% metal coated carbon. The lens barrel material is non-conductive carbon. The lens holder has a curved rib for attaching the module into the mobile phone. The connector is the spring type. The PWB material is FR4.

Pin assignment is shown in **Figure 9** and **Table 9.**

Figure 5: Top view

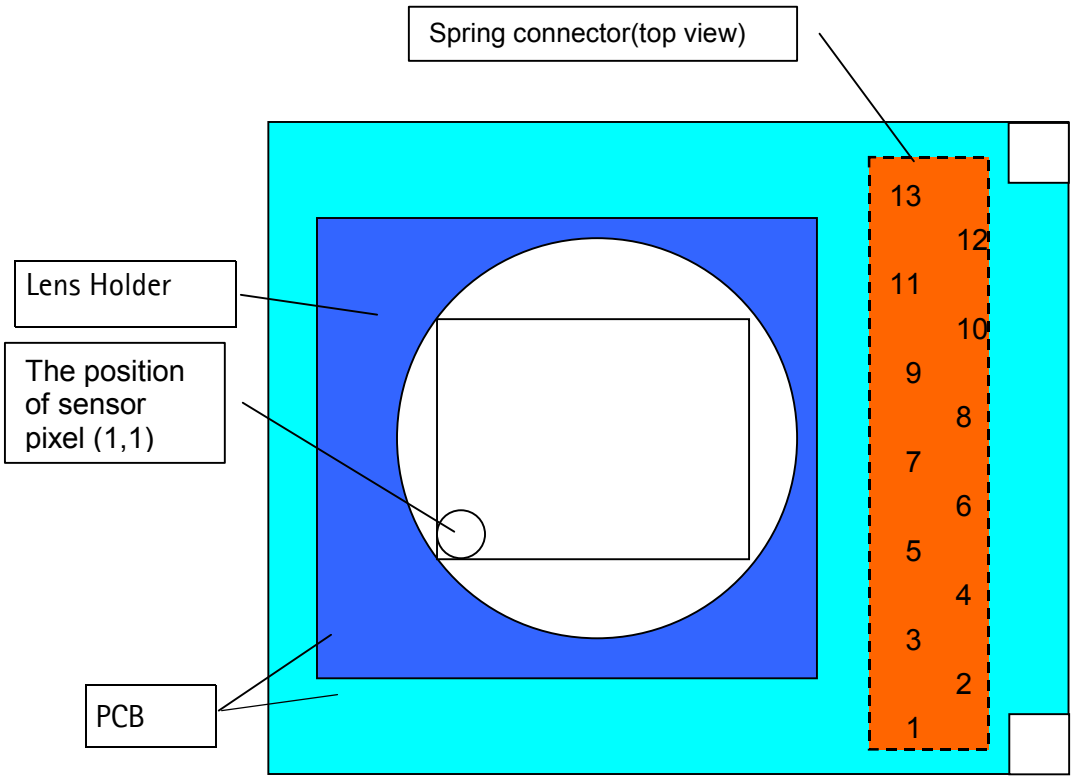


Table 7: Pin assignment

Pin number	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Pin name	VDD	GND2	D+	VDDI	D-	SDA	GND1	SCL
Pin number	9	10	11	12	13			
Pin name	CLK+	Vctrl	CLK-	GND3	EXTCLK			

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