

FDS6298**30V N-Channel Fast Switching PowerTrench® MOSFET****General Description**

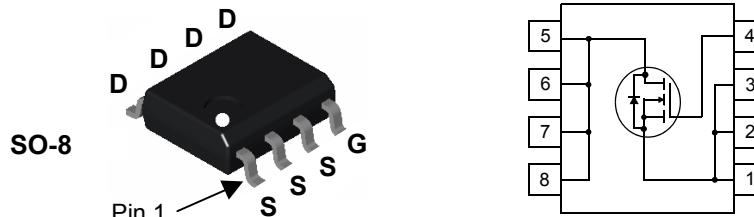
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

Applications

- Control Switch for DC-DC Buck converters
- Notebook Vcore
- Telecom / Networking Point of Load

Features

- 13 A, 30 V $R_{DS(ON)} = 9\text{m}\Omega$ @ $V_{GS} = 10\text{ V}$
 $R_{DS(ON)} = 12\text{m}\Omega$ @ $V_{GS} = 4.5\text{ V}$
- Low gate charge (10nC @ $V_{GS} = 5\text{ V}$)
- Very low Miller Charge (3nC)
- Low R_g (1 Ohm)
- RoHS Compliant

**Absolute Maximum Ratings** $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|----------------|--|-------------|------------------|
| V_{DSS} | Drain-Source Voltage | 30 | V |
| V_{GSS} | Gate-Source Voltage | ± 20 | V |
| I_D | Drain Current -Continuous (Note 1a) | 13 | A |
| | -Pulsed | 50 | |
| P_D | Power Dissipation for Single Operation (Note 1a) | 3.0 | W |
| | Power Dissipation for Single Operation (Note 1b) | 1.2 | |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | $^\circ\text{C}$ |

Thermal Characteristics

| | | | |
|-----------------|---|-----|--------------------|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1a) | 50 | $^\circ\text{C/W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1b) | 125 | $^\circ\text{C/W}$ |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case (Note 1) | 25 | $^\circ\text{C/W}$ |

Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape Width | Quantity |
|----------------|---------|-----------|------------|------------|
| FDS6298 | FDS6298 | 13inch | 12mm | 2500 units |

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|-----------------------------------|---|---|-----|-----|-----------|----------------------------|
| Off Characteristics | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ | 30 | - | - | V |
| ΔBV_{DSS} ΔT_J | Breakdown Voltage Temperature Coefficient | $I_D = 250\mu\text{A},$ Referenced to 25°C | - | 30 | - | $\text{mV}/^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{GS} = 0\text{V}, V_{DS} = 24\text{V}$ | - | - | 1 | μA |
| I_{GSS} | Gate-Body Leakage, | $V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$ | - | - | ± 100 | nA |

On Characteristics (Note 2)

| | | | | | | |
|--|--|---|---|-----|----|----------------------------|
| $V_{GS(\text{th})}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250\mu\text{A}$ | 1 | 1.7 | 3 | V |
| $\Delta V_{GS(\text{th})}$ ΔT_J | Gate Threshold Voltage Temperature Coefficient | $I_D = 250\mu\text{A},$ Referenced to 25°C | - | -5 | - | $\text{mV}/^\circ\text{C}$ |
| $R_{DS(\text{on})}$ | Static Drain-Source On-Resistance | $I_D = 13\text{A}, V_{GS} = 10\text{V}$ | - | 7.4 | 9 | $\text{m}\Omega$ |
| | | $I_D = 12\text{A}, V_{GS} = 4.5\text{V}$ | - | 9.4 | 12 | |
| | | $I_D = 13\text{A}, V_{GS} = 10\text{V},$ $T_J = 125^\circ\text{C}$ | - | 11 | 15 | |
| g_{FS} | Forward Transconductance | $I_D = 13\text{A}, V_{DS} = 10\text{V}$ | - | 58 | - | S |

Dynamic Characteristics

| | | | | | | |
|-----------|------------------------------|---|-----|------|-----|----------|
| C_{iss} | Input Capacitance | $V_{DS} = 15\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$ | - | 1108 | - | pF |
| C_{oss} | Output Capacitance | | - | 310 | - | pF |
| C_{rss} | Reverse Transfer Capacitance | | - | 109 | - | pF |
| R_G | Gate Resistance | $V_{GS} = 15\text{mV}, f = 1\text{MHz},$ | 0.3 | 1 | 1.7 | Ω |

Switching Characteristics (Note 2)

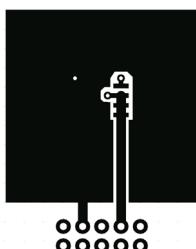
| | | | | | | |
|--------------|---------------------|--|---|----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 15\text{V}, I_D = 1\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$ | - | 11 | 20 | ns |
| t_r | Turn-On Rise Time | | - | 5 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 27 | 43 | ns |
| t_f | Turn-Off Fall Time | | - | 7 | 14 | ns |
| Q_g | Total Gate Charge | $V_{DS} = 15\text{V}, I_D = 13\text{A},$ $V_{GS} = 5\text{V}$ | - | 10 | 14 | nC |
| Q_{gs} | Gate-Source Charge | | - | 3 | - | nC |
| Q_{gd} | Gate-Drain Charge | | - | 3 | - | nC |

Drain-Source Diode Characteristics and Maximum Ratings

| | | | | | | |
|----------|------------------------------------|---|---|------|-----|----|
| V_{SD} | Drain-Source Diode Forward Voltage | $V_{GS} = 0\text{V}, I_S = 2.1\text{ A}$ (Note 2) | - | 0.74 | 1.2 | V |
| t_{rr} | Diode Reverse Recovery Time | $I_F = 13\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$ | - | 27 | - | ns |
| Q_{rr} | Diode Reverse Recovery Charge | | - | 13 | - | - |

Notes:

- R_{0JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0JC} is guaranteed by design while R_{0JA} is determined by the user's board design.



a) $50^\circ\text{C}/\text{W}$ when mounted on a 1in^2 pad of 2 oz copper



b) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad

Scale 1: 1 on letter size paper

- Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

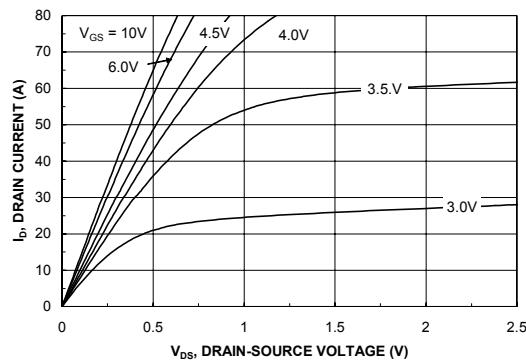


Figure 1. On-Region Characteristics

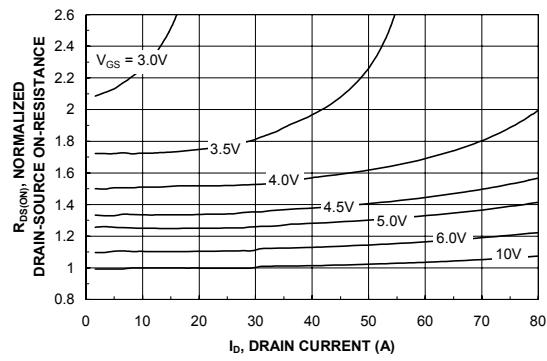


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

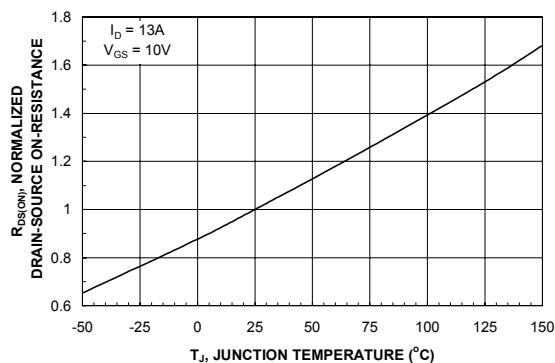


Figure 3. On-Resistance Variation with Temperature

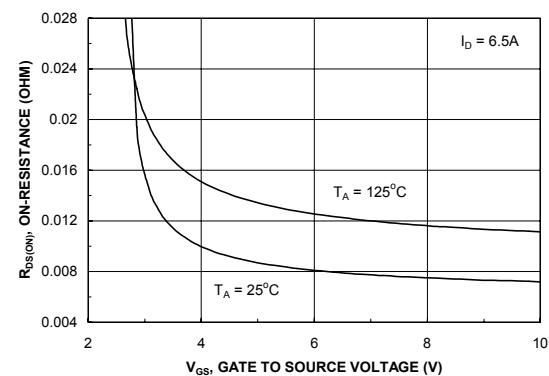


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

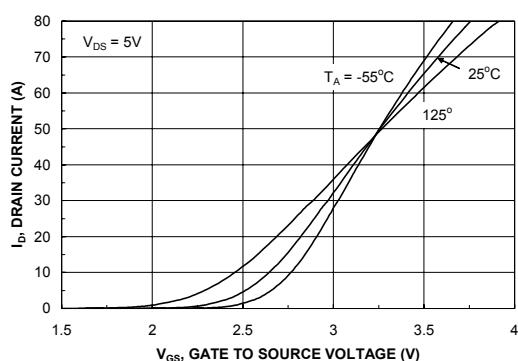


Figure 5. Transfer Characteristics

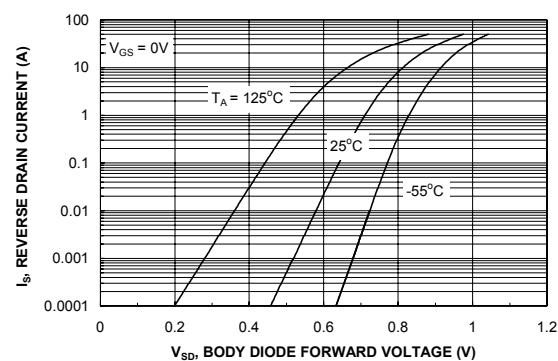


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

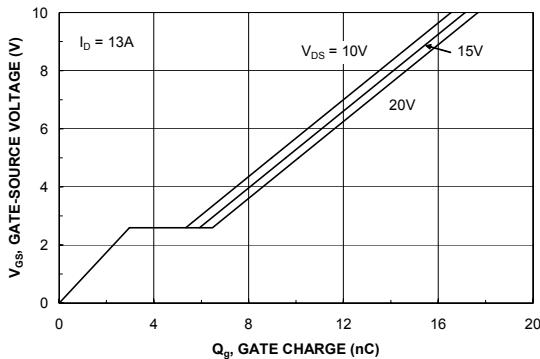


Figure 7. Gate Charge Characteristics

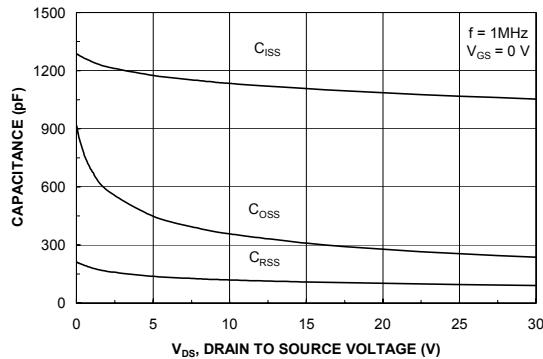


Figure 8. Capacitance Characteristics

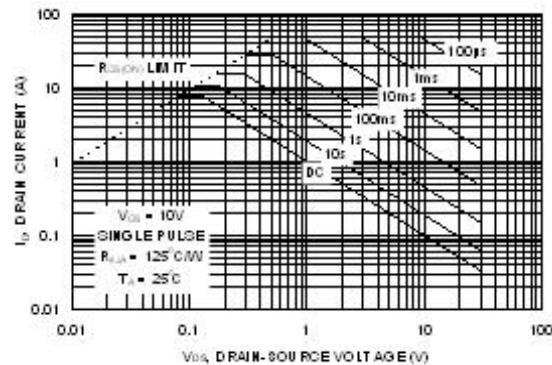


Figure 9. Maximum Safe Operation Area

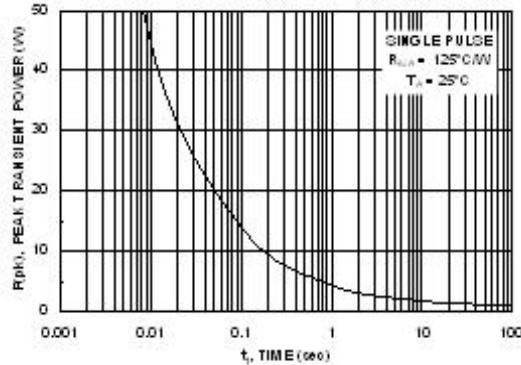


Figure 10. Single Pulse Maximum Power Dissipation

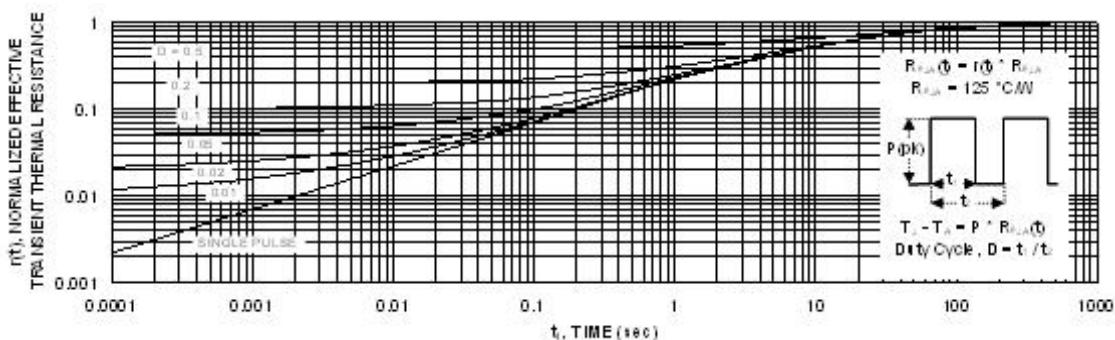


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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