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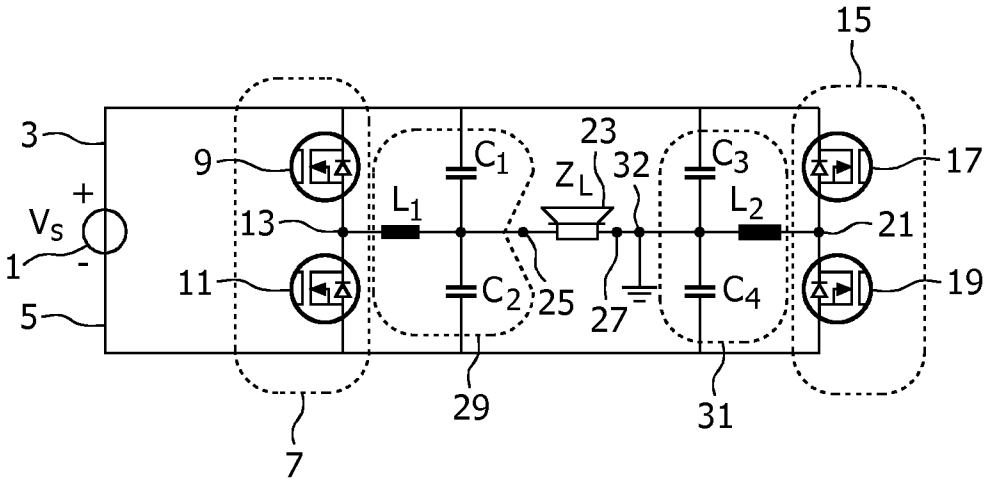
(54) Title: FULL-BRIDGE CLASS-D POWER AMPLIFIER



(57) Abstract: The present invention relates a full bridge class-D amplifier where one of the output terminals (27) is grounded, and which is arranged to be supplied by a floating power supply (1). Each amplifier switching leg (7, 15) is connected to the corresponding load terminal (25, 27) via a low-pass filter (29, 31), at least one of which comprises a capacitor (C1, C2, C3 or C4), connected between the load terminal and the positive or negative output terminal (3, 5) of the floating power supply.

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Full-bridge class-D power amplifier

FIELD OF THE INVENTION

The present invention relates to a full-bridge class-D power amplifier comprising a first switching leg, having a first and a second controllable switch, which are interconnected in a first connection point and connected in series to the positive and negative terminals of a power supply, a second switching leg, having a third and a fourth controllable switch, which are interconnected in a second connection point and connected in series to the positive and negative terminals of the power supply, a first low pass filter being connected between the first connection point and a first load terminal, the second connection point being connected to a second load terminal and the first or the second load terminal being connected to earth by means of an earth connection.

BACKGROUND OF THE INVENTION

Such an amplifier is disclosed in US, 6259317, B1. An advantage with such an amplifier is, since an output terminal is grounded, that the output voltage does not have a common mode voltage component. This makes it possible to use a less complicated feedback arrangement to control the amplifier.

In such a full-bridge amplifier, the positive and negative terminals of the power supply are alternately connected to ground with the switching frequency. This means that no capacitance should be allowed from any load connection to the power supply, not even a parasitic capacitance. In practice however, there is always a parasitic capacitance present. This transmits a switching noise to the load. The signal to noise ratio may thus be low. This is of course undesired e.g. in audio applications where the thus induced interference may be audible.

SUMMARY OF THE INVENTION

An object of the present invention is therefore to provide a class-D amplifier with improved signal to noise ratio.

This object is achieved by means of a full bridge class-D amplifier as defined in claim 1.

More specifically, in an amplifier of the initially mentioned kind the second connection point is then connected to the second load terminal via a second low pass filter, and at least one of the first and second low pass filters comprises a capacitor connected to the positive or negative terminal of the power supply. Such a filter arrangement provides improved noise insulation, since the power supply positive and negative terminals will be balanced around the ground level, and hence improved signal to noise ratio.

Preferably each of the first and second low-pass filters has a capacitor connected to the positive or negative terminal of the power supply. This achieves the inventive effect even if a connected load does not have a substantial capacitive characteristic.

Even more improved properties are achieved when the first low-pass filter has a capacitor connected between the first load terminal and the positive terminal of the power supply and a capacitor connected between the first load terminal and the negative terminal of the power supply, and the second low-pass filter has a capacitor connected between the second load terminal and the positive terminal of the power supply and a capacitor connected between the second load terminal and the negative terminal of the power supply. Such filter arrangement will provide, due to its symmetry, a reconstructed and amplified audio signal by means of averaging and guarantee good balancing of the power supply.

The used switches may be MOSFET switches.

The amplifier may be arranged to be connected in a bridge tied load (BTL) arrangement with a similar auxiliary full-bridge class-D power amplifier.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates schematically an asymmetric full-bridge class-D amplifier according to an embodiment of the invention.

Fig. 2 illustrates the amplifier of Fig. 1 with an arrangement for providing a floating power supply.

Fig. 3 illustrates the amplifier of Fig. 1 with a control arrangement.

Fig. 4 illustrates two amplifiers of the kind shown in Fig. 1 arranged in a bridge-tied load (BTL) configuration.

DESCRIPTION OF PREFERRED EMBODIMENTS

Full-bridge class-D amplifiers are often used in e.g. high power audio applications due to their high power efficiency. In a conventional full-bridge configuration the load is usually floating, at a common mode voltage that equals half the power supply voltage. This causes a problem when designing a feedback arrangement for the amplifier, since the differential voltage over the load must be measured with a very high common-mode rejection ratio (CMRR). This can be done by scaling down each load terminal voltage by means of a precision divider and subtracting the two resulting voltages from each other in order to obtain a differential value used for feedback purposes. The voltage dividers used must then be very well matched in order to achieve low total harmonic distortion and noise, which is of course very important in audio applications.

One way of reducing the common mode influence is to use a full-bridge amplifier with a symmetric dual supply voltage, i.e. a power source providing a positive and a negative voltage, which are symmetrically referenced to ground. However, a drawback with this type of amplifier stage is that it cannot be used in a so-called bridge-tied load (BTL) configuration, where two full-bridge class-D amplifiers are used to supply a load with high power.

An asymmetric full-bridge class-D amplifier according to an embodiment of the invention, can be used in a BTL configuration and does not have a common mode output voltage at all, as will now be described.

Fig. 1 illustrates schematically an asymmetric full-bridge class-D amplifier stage according to an embodiment of the invention. The stage has a floating voltage power supply 1, providing a positive potential V_{s+} at a positive terminal 3 and a negative potential V_{s-} (negative in relation to the positive potential) at a negative terminal 5. The power supply is arranged to provide a substantially constant voltage ($V_s=V_{s+}-V_{s-}$), but the absolute potentials are floating in relation to ground. A power supply arrangement of this kind will be described in more detail later.

The amplifier comprises a first switching leg 7, having a first 9 and a second 11 controllable switch, which may e.g. be MOSFET switches. The first switch 9 and the second switch 11 are interconnected in a first connection point 13 and are connected in series to the positive 3 and negative 5 terminals, respectively, of the power supply 1. A second switching leg 15, has a third 17 and a fourth 19 controllable switch, which are interconnected in a second connection point 21 and are connected in series to the positive and negative terminals, respectively, of the power supply 1.

As in a conventional class-D amplifier the switches of the first 7 and second 15 switching legs are switched complementary and in synchronization, such that in a first state the first connection point 13 is connected to the positive supply terminal 3 while the second connection point 21 is connected to the negative supply terminal 5. In a second state this is reversed, such that the first connection point 13 is connected to the negative supply terminal 5 while the second connection point 21 is connected to the positive supply terminal 3. Switching between the first and second state is carried out at a high switching frequency, typically a few hundred kHz.

A load 23 with an impedance Z_L can be connected to the class-D amplifier between a first 25 and a second 27-load terminal. The first load terminal 25 is connected to the first connection point 13 via a first low-pass filter 29, and the second load terminal 27 is connected to the second connection point 21 via a second low-pass filter 31. The low-pass filters 29, 31 are used to block the switching frequency from reaching the load 23 and are tuned accordingly.

In the illustrated embodiment the second load terminal 27 is connected to earth by means of an earth connection 32. Alternatively however, the first load terminal could be connected to earth. The amplifier is thus asymmetric. Thanks to the earth connection 32 and the floating power supply 1, the common mode voltage over the load is zero, which means that a simple but yet accurate feedback arrangement can be used as will be illustrated later.

As in many conventional non-asymmetric class-D amplifiers the first and second low-pass filters 29, 31 may comprise an inductor. In the first low-pass filter, the inductor L1 is connected between the first connection point 13 and the first load terminal 25. In the second low-pass filter, the inductor L2 is connected between the second connection point 21 and the second load terminal 27. The inductors serve to make the load voltage an averaged version of the voltage between the first and second connection points 13, 21 by only allowing the current through the inductors to rise and fall slowly.

In addition to the inductors, the low pass filters 29, 31 comprise capacitors connected between the respective load terminals and the positive and negative supply terminals 3, 5. Thus, in the first filter 29 one capacitor C1 is connected between the first load terminal 25 and the positive supply terminal 3 and another capacitor C2 is connected between the first load terminal 25 and the negative supply terminal 5. In the second filter 31 one capacitor C3 is connected between the second load terminal 27 and the positive supply terminal 3 and another capacitor C4 is connected between the second load terminal 27 and the negative supply terminal 5. The capacitors are used to improve the low-pass filter

function and also to automatically balance the power supply. The four capacitors may preferably have substantially the same capacitance.

It should be noted that the illustrated embodiment is preferred, since it is very well balanced vis-à-vis the positive and negative supply voltages. However it may be possible to provide fewer capacitors and still obtain good results. For all loads, a capacitor on each side of the load, connected to the positive or negative supply terminal, should be enough for many less demanding applications. If the load has a capacitive characteristic it may even be enough with one capacitor attached at one side of the load.

In general, the described class-D amplifier output stage in Fig. 1 inherently balances the power supply around the ground reference point by means of duty ratio control of the switches, and the averaging output filter being connected to the power supply terminals.

Below one example of used components and settings is listed:

V_s	80 V
Switches	FDP3652 (MOSFET)
L_1	3.0 μH
C_1	820 nF
C_2	820 nF
L_2	3.0 μH
C_3	820 nF
C_4	820 nF
Z_L	2 Ω
Switching frequency	375 kHz

Fig. 2 illustrates the amplifier of Fig. 1 with an arrangement for providing a floating power supply 1 as used in the amplifier stage in Fig. 1. An insulated switched arrangement is used where an input voltage V from a power supply 33, that need not be floating, is used. In series with this power supply, two switches 35, 37 are series connected, and a transformer winding 39 is connected to the connection point between the two switches 35, 37. The switches 35, 37 are switched complementary, such that a first side of the transformer primary winding 39 is alternating connected to the positive and negative potential of the power supply 33. The second side of the transformer primary winding 39 is

connected via two capacitors 41, 43 to the positive and negative power supply 33 potential, respectively, such that the primary transformer winding alternating forms an LC circuit with each of the capacitors driving the voltage at the second side of the primary transformer winding up and down corresponding to the switching of the switches 35, 37.

This creates an alternating current through the primary transformer winding 39, which generates a corresponding current in a secondary transformer winding 45 of the same transformer T1, which winding is insulated from the primary winding 39. The current may be rectified, as illustrated using a full bridge rectifier with four diodes 47, 49, 51, 53 which feeds the rectified current to a filter capacitor 55, thus generating a floating voltage at the power supply terminals 3, 5.

The described embodiment is only an example. A corresponding floating power supply can be achieved with other insulated converters, e.g. a fly back converter. Fig. 3 illustrates the amplifier of Fig. 1 with a control arrangement. An input signal V_{in} to be amplified is fed to a comparator 57 via an input impedance R_{in}. In the same way the output voltage from the (not grounded) load terminal 25 is fed to the comparator via a specific feedback network 59. Expensive high-precision voltage dividers are not needed thanks to the avoided common mode voltage. The comparator generates a pulse width modulated signal that is fed to a control block 61. The control block generates control signals O_1, O_2, O_3, O_4 for each of the switches 9, 11, 17, 19 in the amplifier stage based on the pulse width modulation signal. It should be noted that the feedback signal is collected from a point after the output filter in a similar way as illustrated in WO 03/090343 A1. This feedback approach is considered particularly suitable for the above application with the floating power supply.

At one place in the control path an isolation barrier should be inserted to obtain galvanic insulation between the switches and the amplifier output. Such a barrier IB1 can be introduced in each switch's driving circuitry 63, 65, 67, and 69. Alternatively, a barrier IB2 in the control block 61 can be used. Another alternative is to have a barrier IB3 in the comparator 57. One of the barriers IB1 or IB2 is preferred, since such a barrier operates in the digital domain and can be accomplished by means of an opto-coupler or a pulse transformer with good timing characteristics.

Fig. 4 illustrates two amplifiers of the kind shown in Fig. 1 arranged in a bridge-tied load (BTL) configuration. This arrangement can be used to obtain extra high power output. Two class-D amplifiers 71, 73 of the above-described type are used. The load 23' is connected between the not earthed load terminal 25, 25' of each amplifier, the other load terminals 27, 27' of each amplifier being earthed.

In summary, the invention relates to a full bridge class-D amplifier where one of the output terminals is grounded, and which is arranged to be supplied by a floating power supply. Each amplifier switching leg is connected to the corresponding load terminal via a low-pass filter, at least one of which comprises a capacitor, connected between the load terminal and the positive or negative output terminal of the floating power supply.

The invention is not restricted to the described embodiments. It can be altered in different ways within the scope of the appended claims.

CLAIMS:

1. A full-bridge class-D power amplifier comprising a first switching leg (7), having a first (9) and a second (11) controllable switch, which are interconnected in a first connection point (13) and connected in series to the positive (3) and negative (5) terminals of a power supply (1), a second switching leg (15), having a third (17) and a fourth (19) controllable switch, which are interconnected in a second connection point (21) and connected in series to the positive (3) and negative (5) terminals of the power supply (1), a first low pass filter (29) being connected between the first connection point (13) and a first load terminal (25), the second connection point (21) being connected to a second load terminal (27) and the first or the second load terminal being connected to earth by means of an earth connection (32), wherein

the second connection point (21) is connected to the second load terminal (27) via a second low pass filter (31), and

at least one of the first and second low pass filters (29, 31) comprises a capacitor (C_1) connected to the positive (3) or negative (5) terminal of the power supply.

2. A full-bridge class-D power amplifier according to claim 1, wherein each of the first and second low-pass filters (29, 31) has a capacitor (C1, C3) connected to the positive (3) or negative (5) terminal of the power supply.

3. A full-bridge class-D power amplifier according to claim 2, wherein the first low-pass filter (29) has a capacitor (C1) connected between the first load terminal (25) and the positive terminal (3) of the power supply (1) and a capacitor (C2) connected between the first load terminal (25) and the negative terminal (5) of the power supply (1), and wherein the second low-pass filter (31) has a capacitor (C3) connected between the second load terminal (27) and the positive terminal (3) of the power supply (1) and a capacitor (C4) connected between the second load terminal (27) and the negative terminal (5) of the power supply (1).

4. A full-bridge class-D power amplifier according to any of the preceding claims, wherein said first, second third and fourth switches (9, 11, 17, 19) are MOSFET switches.

5. A full-bridge class-D power amplifier (71) according to any of the preceding claims, wherein the amplifier is arranged to be connected in a bridge tied load arrangement with a similar auxiliary full-bridge class-D power amplifier (73).

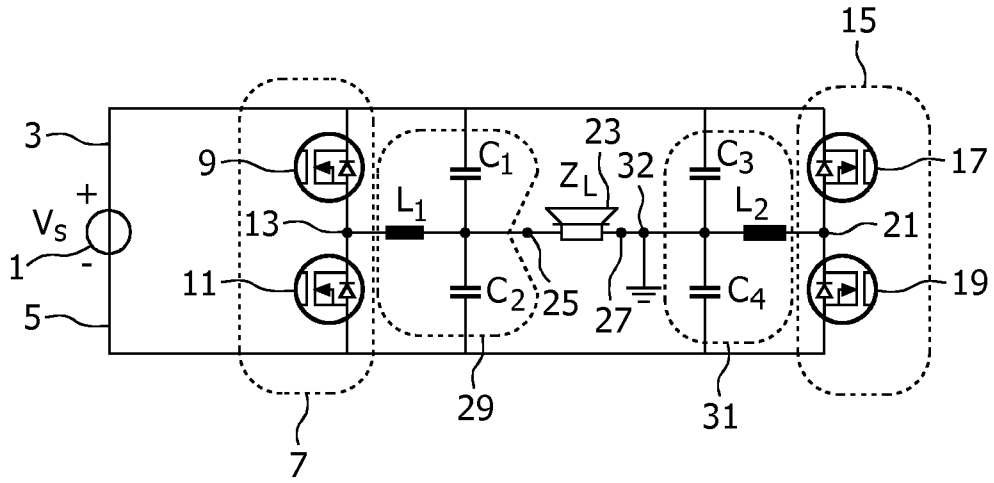

15
3
9
C1
23
ZL
32
C3
17
+
Vs
13
L1
L2
21
1
-
11
C2
25
27
C4
19
5
29
31
7

FIG. 1

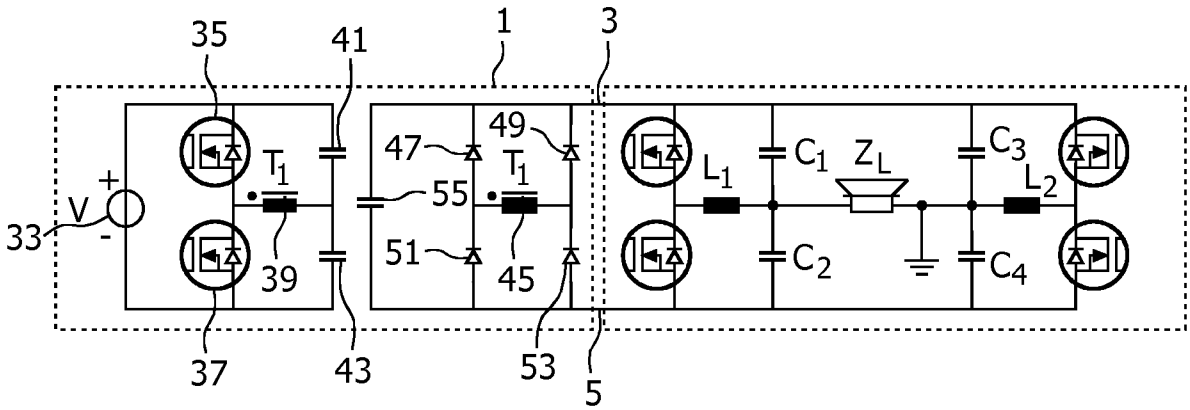
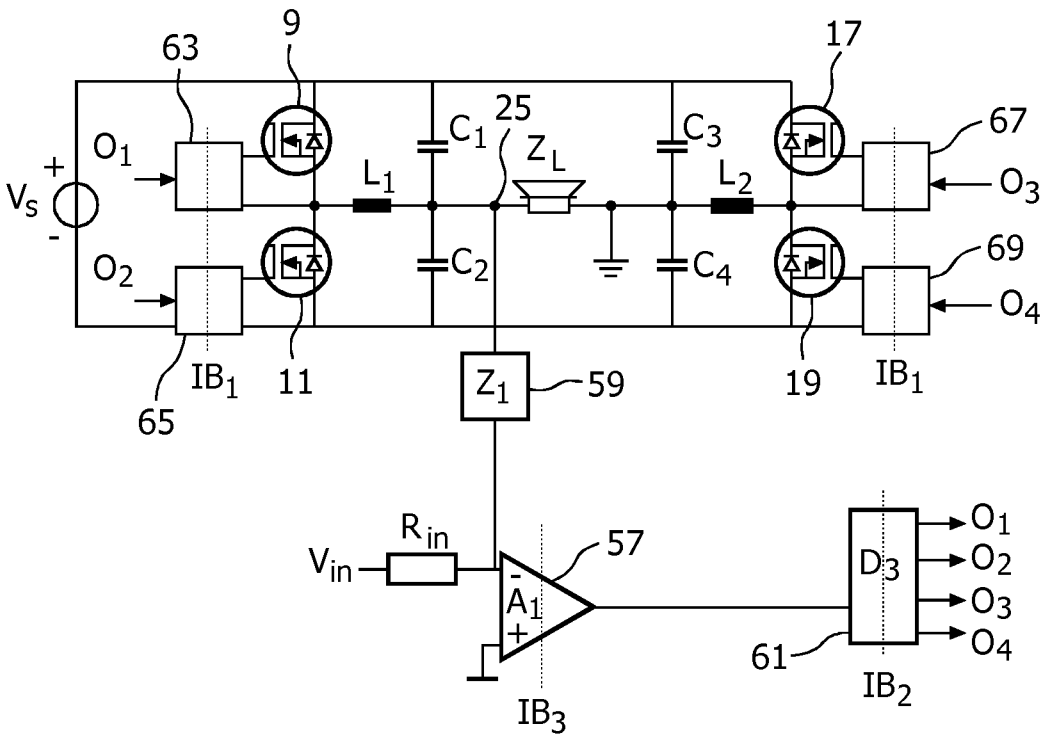

35
41
1
3
49
47
T1
L1
C1
ZL
C3
+
V
55
L2
33
-
51
45
C2
C4
39
37
43
53
5

FIG. 2


63
9
17
25
67
O1
C1
ZL
C3
O3
Vs
+
-
L1
L2
O2
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69
O4
IB1
11
Z1
59
19
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O2
O3
O4
Vin
A1
61
IB2
IB3

FIG. 3

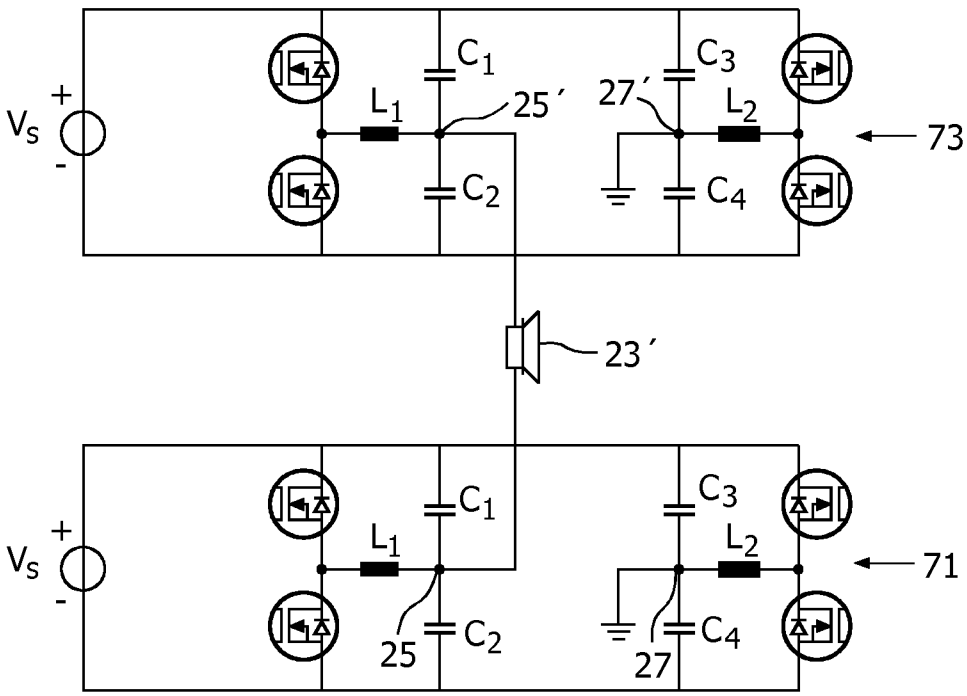
C1
C3
Vs
+
-
L1
25´
27´
L2
73
C2
C4
23´
C1
C3
Vs
+
-
L1
L2
71
25
C2
27
C4

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2006/054480

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F1/26 H03F1/30 H03F3/217

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/151459 A1 (LEEDHAM ROBERT [GB]) 14 August 2003 (2003-08-14) paragraphs [0031] - [0036]; figures 2,6	1-5
X	US 2005/264354 A1 (MENDENHALL ERIC [US]) 1 December 2005 (2005-12-01) paragraphs [0014] - [0078]; figures 2,4,7-12	1-5
A	US 2005/231276 A1 (GOTO MASAO [JP]) 20 October 2005 (2005-10-20) paragraphs [0024] - [0080]; figures 4-6	1-5
A	WO 01/91287 A (KONINKL PHILIPS ELECTRONICS NV [NL]) 29 November 2001 (2001-11-29) page 3, lines 1-28; figure 2	1-5

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
26 April 2007	07/05/2007

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2006/054480

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 2002011880 A1	31-01-2002