Prof. Dr. Thomas C. Baier, DG8SAQ

University of Applied Sciences, Prittwitzstrasse 10, 89075 Ulm, Germany; baier@hs-ulm.de

A Small, Simple, USB-Powered Vector Network Analyzer Covering 1 kHz to 1.3 GHz

You will want to build this new variation on a popular project!

Summary

Since I had published my ideas for a simple and low cost vector network analyzer (VNWA) in *QEX* in 2007, I have received lots of feedback, showing, that there is a great interest in this field.[1] The original design (VNWA1.0) had a few shortcomings. It only covered a fundamental frequency range up to 160 MHz. On the other hand, it could measure at some limited higher frequency bands up to 500 MHz, with reduced accuracy, by using higher DDS alias frequencies.[2] Another drawback was that it was a veroboard design. This made it very tough to duplicate. So, I have thought about how to make the VNWA design even simpler, better, and last but not least easier to build. In this article, I describe the very satisfactory result of this development process, which is a small single printed circuit board VNWA covering 1 kHz to 1.3 GHz in one continuous frequency band, which can be powered directly from a computer USB interface.

VNWA Design

Figure 1 shows the fundamental design of the new VNWA2.1. Like the original VNWA1.0, it consists of two digitally tunable Direct Digital Synthesizers (DDSs), now realized by two fast Analog Devices AD9859 chips.[3] Here, the clock generation could be realized in a very simple way, because the AD9859 contains an on-chip clock multiplier PLL circuit. Both DDSs are clocked from the same crystal oscillator, realized with a low cost standard 12.3 MHz crystal, which is oscillating on the third overtone at about 37 MHz. The exact crystal frequency is of no importance, since it can be accounted for in the software. As described in my letter to the Editor in *QEX* (see Note 2), it is crucial that the two DDS cores are clocked with *different* frequencies, if one wants to omit anti-aliasing filters and make use of higher order alias frequencies. This is simply achieved by setting the clock multipliers of the two DDS chips to two different values — for example, 20 and 19 — leading to clock frequencies of 703 MHz and 740 MHz respectively. Note, that in this frequency scheme, the DDSs operate well beyond their specification limits of 400 MHz maximum core clock. Quite remarkably, all tested DDS chips (about 30 pieces so far), work nicely without getting hot under these conditions. This is a very experimental approach, but pushing the DDS clock frequency means pushing the usable fundamental frequency range of the VNWA, which spans to 600 MHz under the selected operating conditions.

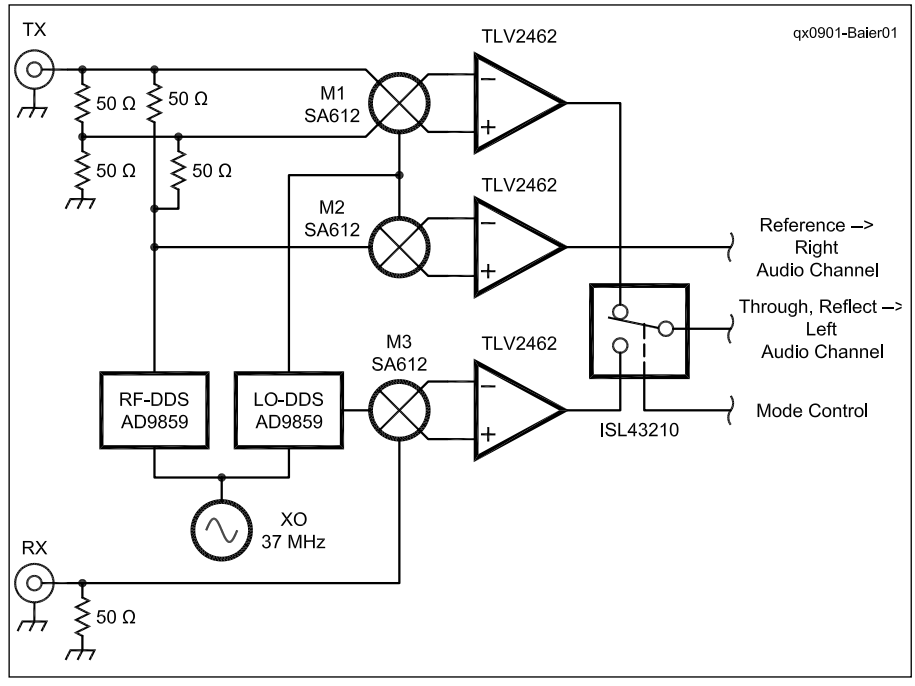

Figure 1 — A block diagram showing the fundamental design of the VNWA2.1.

Like in the VNWA1.0 design, the RF DDS output signal is fed into an SWR-bridge, now formed by 50 Ω resistors in order to simplify power level adaptations by an optional 50 Ω attenuator pad between the DDS and the bridge. The balanced bridge output signal is fed into the balanced inputs of the Gilbert cell mixer, M1, followed by an operational amplifier. The amplifier output signal is guided through a CMOS switch into

[1]Notes appear on page 36.

the left channel of the computer sound card line-in. The CMOS switch multiplexes this Reflect signal with the Through measurement signal originating from mixer M3 and its following amplifier. The multiplexing is necessary, as standard sound cards have only a stereo line-in channel, which can capture just two signals simultaneously. But a third signal, the Reference signal, is required to determine the signal phases. The Reference signal is obtained by mixing the LO and RF DDS signals with M2 and amplifying the output signal with the following operational amplifier. It is then fed into the right channel of the sound card line-in. Note that the VNWA works with an IF of about 1 kHz. The sound card is used as an IF amplifier, so the computer realizes a digital IF filter.

If a Device Under Test (DUT) with two ports is placed between the TX and RX terminals of the VNWA, its scattering parameters S_{11} and S_{21} can be derived from the three measurement signals (Through, Reflect, Reference). By manually turning the device, also S_{12} and S_{22} can be measured.

In the current design, both the CMOS switch and the DDSs are digitally controlled with the computer parallel printer port. Software integration of a USB interface is under development.[4]

Hardware

Figure 2 shows the VNWA2.1 board mounted into a small metal sheet box as seen from top. The left SMA connector is the TX port output. It is directly connected to the internal SWR bridge. The bridge is surrounded by the mixers M1, M2 (left) and the RF-DDS (right). The right SMA connector is the RX port input. Above, the mixer M3 and to the left the LO DDS are found.

The SubD9 connector on the upper side of Figure 2 is the digital control port, which is directly connected to the computer parallel printer port. Also, the power supply is provided through this connector.

The 3.5 mm audio connector on the upper right of Figure 2 is the stereo audio output to be connected to the computer sound card line-in.

The digital part of the board runs on 1.8 V dc and 3.3 V dc. These voltages can directly be obtained with low drop regulators by tapping 5 V dc from a computer USB port. The analog circuitry requires a low noise 6 V dc power supply. Fortunately, it only consumes 10 mA of current. In order to power the whole board from 5 V dc, a low power step up switching regulator was added on the upper left corner of the board. It translates 5 V input voltage to 8.5 V on output, which is then reduced to 6 V dc with a dissipative voltage regulator. This way, a very low noise 6 V power supply could be obtained and no interference from the switching regulator could be observed. The whole board consumes 350 mA from a 4.5 V supply when overclocked to the limit. A USB port can deliver up to 500 mA and thus is able to power the board.

The printed circuit board is a simple two layer design. Thanks to a lot of brainwork and the terrific layout work of Dan, MØDFI, almost all components and connections could be placed on the top side. Only one semi rigid coax line had to go to the bottom, connecting the TX section mixers with the LO DDS. The bottom side of the board is almost completely covered with a metal ground plane. The latter is crucial to obtain good isolation between the TX and RX section up into the GHz range. The board size is 100 × 60 mm² and the passive components are mostly 0603 size.

Test results

Figure 3 shows the frequency dependent available signal amplitudes under various operating conditions and the isolation level.

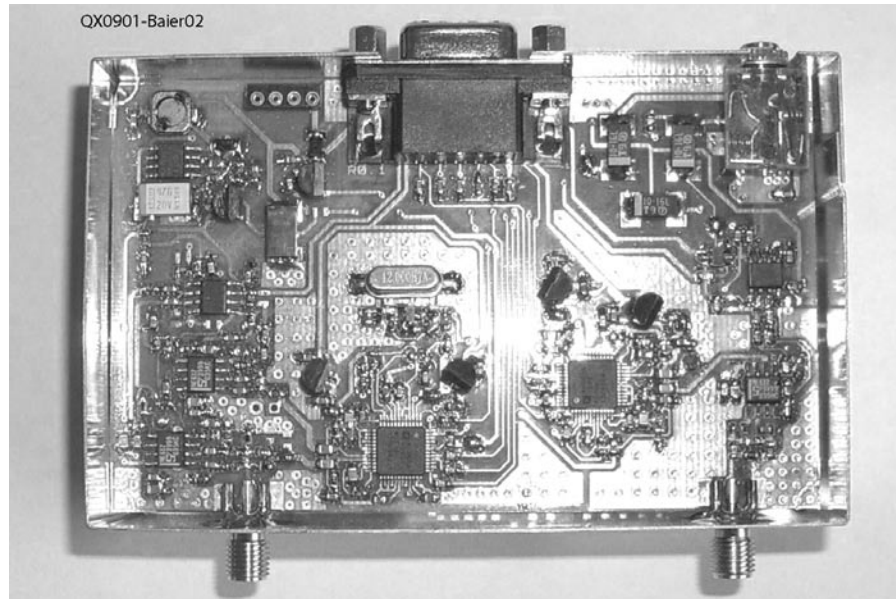

Figure 2 — Top view of the VNWA2.1 board. Board size is 100 × 60 mm².

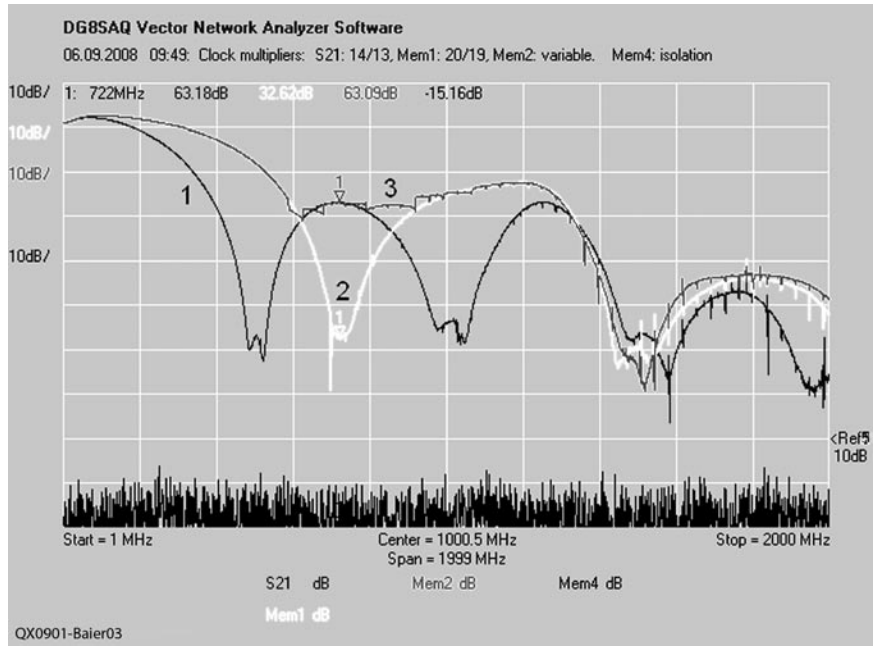

Figure 3 — Frequency dependent available signal amplitudes: Trace 1/S21: clock multipliers are 14/13; trace 2/Mem1: clock multipliers are 20/19; trace 3/Mem2: clock multipliers are dynamically switched during the frequency sweep. Also shown is the noise floor of the system with TX output and RX input isolated (bottom trace, Mem4). Note that traces 2 and 3 exactly match from the starting point up to their first crossing of trace 1.

The isolation trace on the bottom shows, that there is no crosstalk between TX output and RX input measurable within the available dynamic range.

It can be seen from traces 1 and 2, that there are strong alias signals up to 1.3 GHz, which become increasingly noisy with increasing frequency, though. Also, there are distinct notches visible, which result from the fact that the output levels of DDSs drop to zero near integer multiples of their core clock frequency, which is around 500 MHz for trace 1 and 700 MHz for trace 2. The notches are in fact double notches, as the two DDSs run on slightly different clocks and the product of both DDS output powers enters into the signal amplitude. Observe that trace 1 rather nicely fills the first notch of trace 2 and vice versa. This leads to the idea of dynamically switching the DDS clock multipliers during the frequency sweep — in other words, measuring at different frequencies with different clock multipliers. Trace 3 was obtained in this way. Here, the notches are gone altogether and sufficient signal amplitude is obtained for a continuous frequency sweep from audio frequencies up to 1.3 GHz. This idea is also nicely described by Sam Wetterlin.[5]

Figure 4 shows a wideband transmission response of a through calibration standard (traces 1 and 2) and an isolation measurement (trace 3) from 1 MHz to 1.3 GHz obtained with dynamic clock multiplier adaptation during the sweep as described above. Note, that by virtue of a through calibration prior to measurement, all amplitude discontinuities from Figure 3 have vanished. An amplitude accuracy of a few hundredths of a dB and a phase accuracy of a few tenths of a degree are achieved up to 1.3 GHz. Obviously the uncertainties increase and the dynamic range decreases from 500 MHz upwards because of a decreasing signal amplitude. Up to the 70 cm amateur radio band a dynamic range of about 90 dB is achieved. Above that, the dynamic range drops, but still remains around a remarkable 70 dB.

Figure 5 shows a reflection measurement on a 1 m long open ended coaxial cable over the same frequency range as in Figure 4. A SOL (short, open, load) calibration has been performed prior to the measurement. The amplitude plot nicely shows the cable attenuation, which increases with frequency. The amplitude ripple is not a hardware error, but it is caused by port mismatch. This describes the fact that the reflection coefficients of the calibration standards (open, short, load) are not exactly known to the correction algorithm. The Smith chart shows the expected spiral, which has corners due to the rather small number of frequency points (200) used here.

It is quite remarkable, that the instrument works up to 1.3 GHz, as the mixers I used are only specified up to 500 MHz. The latter originally was the targeted upper frequency limit. The degradation of the mixer performance leads to measurement errors beyond 500 MHz, though. Still, the instrument is sufficient for most ham purposes up into the 23 cm range, as hams usually don't require extremely high precision results.

It is to be noted that there are also measurement errors due to interference at some integer multiples of the DDS input clock frequencies. Remember that the design contains no signal shaping RF filters whatsoever. The interferences were mostly avoided so far by

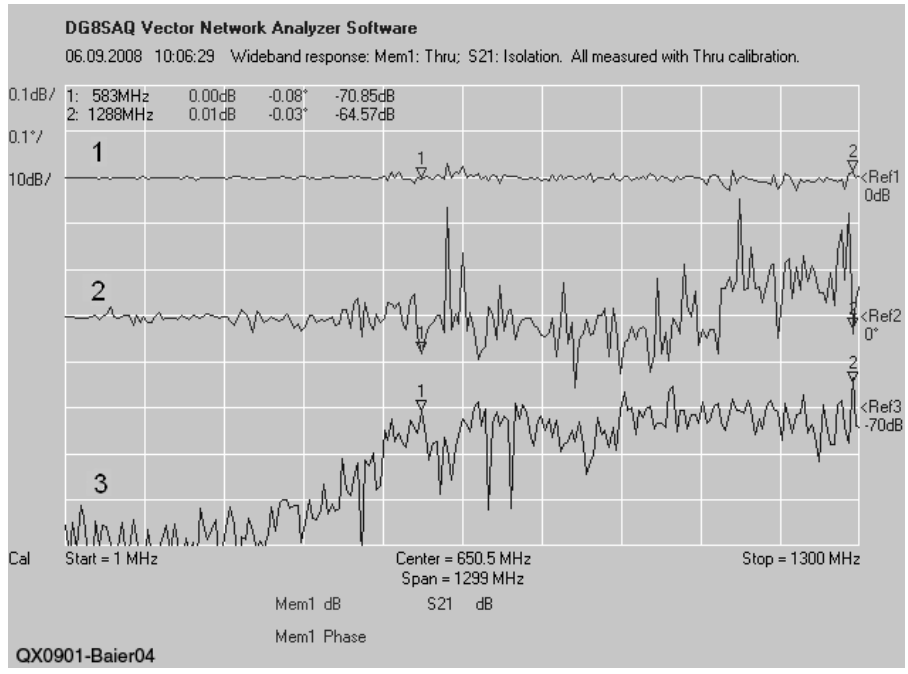

Figure 4 — Wideband transmission response of a through calibration standard from 1 MHz to 1.3 GHz obtained with dynamic clock multiplier adaptation during the sweep (trace 1 / Mem1-dB: amplitude response; trace 2 / Mem1-Phase: phase response) and wideband isolation (trace 3 / S21-dB). A through calibration has been performed prior to measurement.

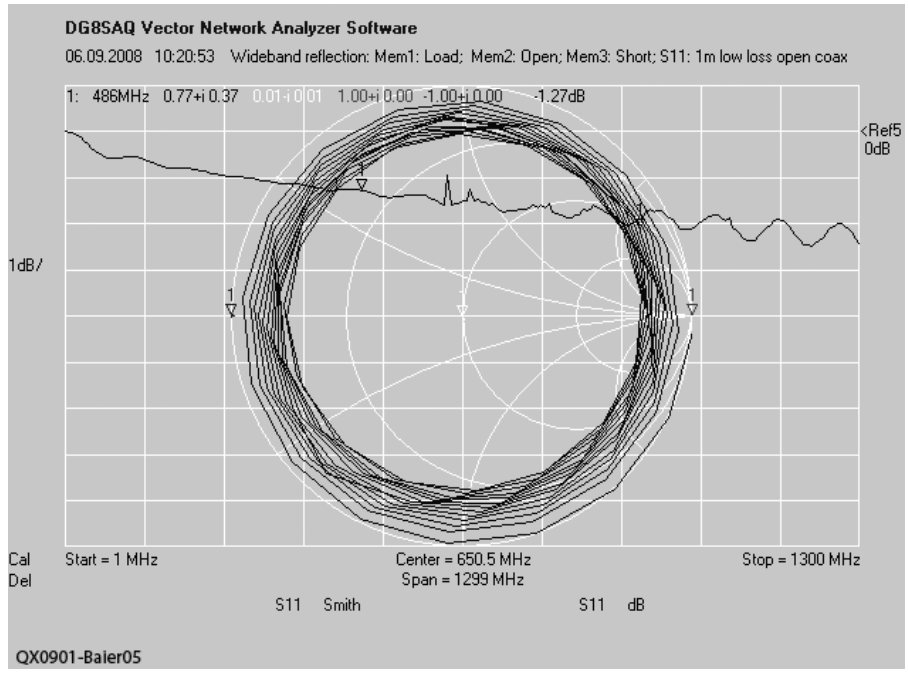

Figure 5 — Reflection measurement on a 1 m open ended coaxial cable from 1 MHz to 1.3 GHz. A SOL (short, open, load) calibration has been performed prior to measurement.

selection of the measurement frequency grid. One such interference can be seen in Figure 6, where it manifests itself as a peak with about 0.15 dB amplitude in trace 2 at about 360 MHz (= half of the DDS core clock frequency). It is caused by interference of two aliases, which happen to cross there, when the DDSs are swept.

Figure 6 shows a high precision comparison of reflection coefficients between VNWA2.1 and Rohde & Schwarz ZVM measurements on a 30 cm open ended low loss semi rigid coaxial cable in the fundamental VNWA frequency range up to 600 MHz. In the Smith chart, only the VNWA2.1 data is shown, since the data of both instruments are so similar, that they cannot be distinguished there. This is also seen from the amplitude traces 1 and 2. Note, that their scales are only 0.02 dB per division, demonstrating, that the VNWA2.1 works very accurately up to 500 MHz. Note, that it is most challenging to precisely measure reflection coefficients near magnitude 1.

Figure 7 shows the wideband measurement of a "real" device, namely a 1 GHz SAW filter. Also, this measurement has been obtained by dynamically switching the clock multipliers during the sweep. Obviously, the dynamic range of the instrument is still good enough to measure such a device at 1.3 GHz.

Due to the huge usable continuous frequency range from 1 kHz to 1.3 GHz, it makes sense to perform measurements on a logarithmic frequency grid with the VNWA2.1, in order to obtain Bode plots. A simple example is shown in Figure 8. It shows a Bode plot of the transmission through an SMA T, terminated with a 120 nH SMD inductor at the base of the T (S_{21}, trace 2) compared to the transmission of the through calibration standard (Mem4, trace 1) from 1 kHz to 1.3 GHz. In the lower frequency region, the ohmic resistance of the inductor limits the attenuation to about 40 dB. The mid frequency region shows the expected linear decrease of the attenuation on the doubly logarithmic scale, due to the increasing ac resistance of the inductor with increasing frequency. Traces 3 and 4 (Cus2 and Cus4) show two different simulations of the transmission through the T. Trace 3 uses the actually measured reflection coefficient of the inductor, which is stored in Mem1, to calculate the T transmission. Trace 4 uses a simple model of an ideal 120 nH inductor connected in series with a resistor of 0.26 Ω to simulate the T transmission. Trace 5 (Mem1) actually shows the measured series resistance of the inductor. Note, that all simulations have been performed within the VNWA measurement software, which includes a parser and compiler for complex mathematical expressions. So, measurement results can be manipulated in real-time during the sweep or simulation traces can be calculated and displayed in customized ways. Figure 9 shows the input mask of the mathematical expression parser containing the impedance formula of the lossy 120 nH inductor normalized to 50 Ω used in the simulation trace 4 in Figure 8.

Summary and outlook

I have described a very simple computer-based vector network analyzer, which operates on a continuous frequency band from

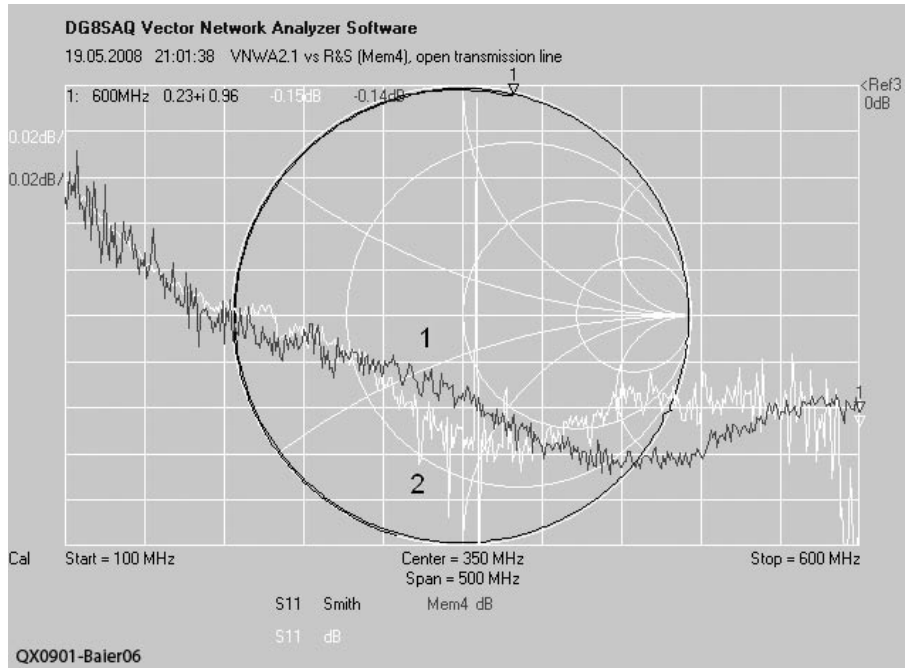

Figure 6 — High precision comparison of reflection coefficients between VNWA2.1 and Rohde & Schwarz ZVM measurements on a 30 cm open ended low loss semi rigid coaxial cable in the fundamental VNWA frequency range up to 600 MHz. Trace 1 / Mem4: ZVM; Trace 2 / S11: VNWA2.1.

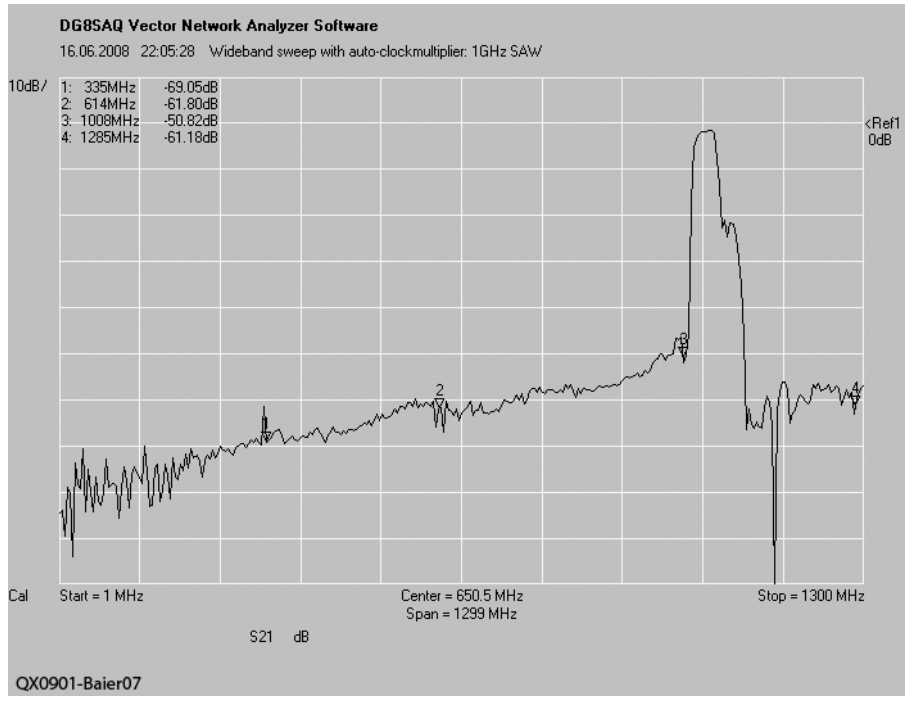

Figure 7 — Wideband measurement of a 1 GHz SAW filter. The filter isolation of 60 dB at 1.3 GHz can still be measured.

1 kHz to 1.3 GHz, thus still covering the 23 cm Amateur Radio band. The wide operating frequency range was obtained by deliberately using aliasing frequencies of the built-in direct digital synthesizers and by dynamically switching their clock frequencies during the measurement sweep. The design is implemented on a single two layer printed circuit board with all components placed on the top layer. The board is powered by a single non-stabilized 4.5 V to 5.5 V dc source consuming a current of 350 mA.

The design is very experimental, as the DDS chips and the mixers are operated well outside their specification limits. Therefore, I do not intend to provide preassembled boards. Nevertheless, I would like to give experimenters the possibility to work with such an instrument by providing unassembled printed circuit boards. Good experience, steady hands and an excellent eye sight are required for manual assembly. Look at my Web site for details and for my most recent VNWA software.[6, 7]

I want to thank Dan, M0DFI, for a great job laying out the circuit board. I also want to thank Hermann, DF2DR, Andreas, DL1TT, and Ferdinand, DB2SG for great support on board production and for beta-testing the project and Stefan Fuchs for his support with the ZVM reference measurements.

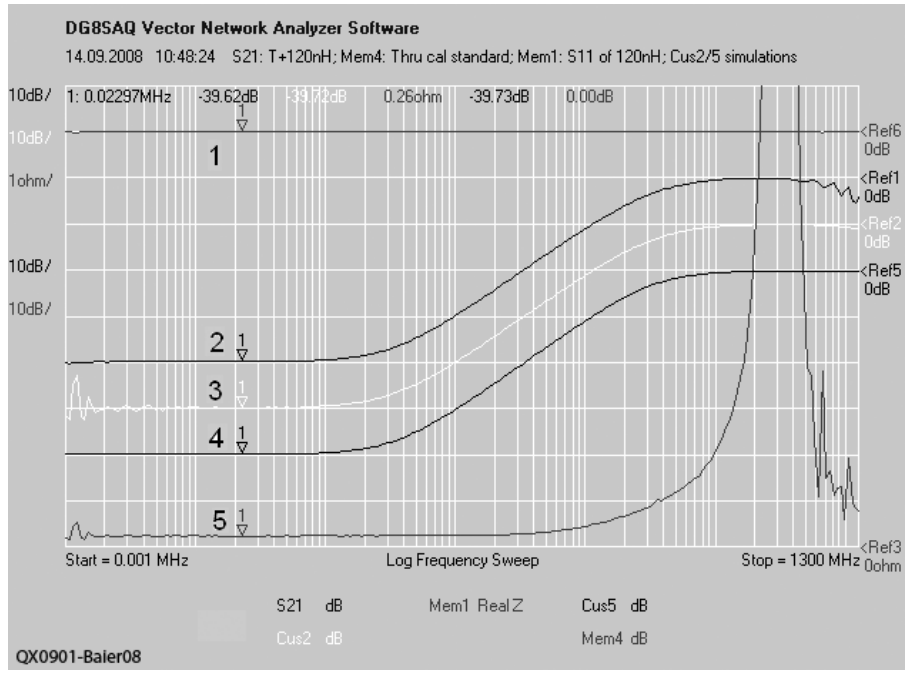

Figure 8 — Bode plot of the transmission through an SMA T connector, terminated with a 120 nH SMD inductor at the base of the T (S21, trace 2) from 1 kHz to 1.3 GHz. Also shown are two simulations of the transmission (Cus2, trace3, calculated from measured S11 of the inductor), (Cus5, trace 4, calculated with model inductor 120 nH in series with 0.26 Ω) and the transmission of the through calibration standard (Mem4, trace 1). Note that all mentioned traces have been shifted in reference level positions for better visibility. Mem1, trace 5 shows the measured real part of the inductor impedance.

Notes

[1]Professor Dr. Thomas C. Baier, DG8SAQ, "A Low Budget Vector Network Analyzer for AF to UHF," *QEX*, Mar/Apr 2007, ARRL. See also **www.mydarc.de/DG8SAQ/VNWA/**

[2]Professor Dr. Thomas C. Baier, DG8SAQ, "Letters to the Editor," *QEX*, Jul/Aug 2007, ARRL.

[3]**www.analog.com/en/rfif-components/direct-digital-synthesis-dds/ad9859/products/product.html**

[4]Professor Dr. Thomas C. Baier, DG8SAQ, "A Low-Cost, Flexible USB Interface," *QEX*, Jan/Feb 2008, ARRL, pp 11-15.

[5]Sam Wetterlin, "Using DDS Aliases to Extend the Frequency Range," **www.wetterlin.org/sam/AD9952/MultipleClockAliases.pdf**

[6]**www.mydarc.de/DG8SAQ/NWA.html**

[7]Please see **www.SDR-kits.net** or contact **sdrkits@gmail.com** for information about the availability of circuit boards and kits. Details are being worked out at press time.

Professor Dr. Thomas Baier, MA, teaches physics, mathematics and electronics at the University of Applied Sciences in Ulm, Germany. Before his teaching assignment, he spent 10 years of work on research and development of surface acoustic wave filters for mobile communication with Siemens and EPCOS. He holds 10 patents.

Tom, DG8SAQ, has been a licensed radio amateur since 1980. He prefers the soldering iron to the microphone, though. His interests span from microwave technology to microcontrollers. Lately, he has started Windows programming with Delphi. Tom spent one year in Oregon USA rock climbing and working on his master's degree.

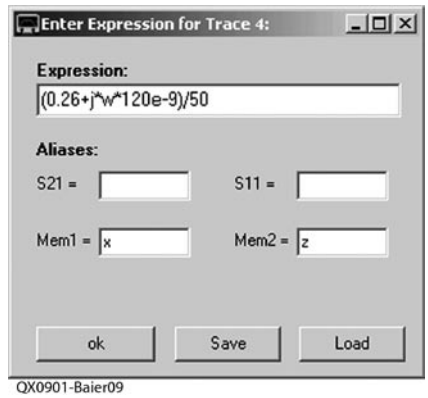

Figure 9 — VNWA software input mask showing the impedance formula of the lossy 120 nH inductor normalized to 50 Ω used in the simulation trace 4 of Figure 8.