

Eddy Current Losses in Transformer Windings and Circuit Wiring

Lloyd H. Dixon, Jr.

Introduction

As switching power supply operating frequencies increase, eddy current losses and parasitic inductances can greatly impair circuit performance. These high frequency effects are caused by the magnetic field resulting from current flow in transformer windings and circuit wiring.

This paper is intended to provide insight into these phenomena so that improved high frequency performance can be achieved. Among other things, it explains (1) why eddy current losses increase so dramatically with more winding layers, (2) why parallelling thin strips doesn't work, (3) how passive conductors (Faraday shields and C.T. windings) have high losses, and (4) why increasing conductor surface area will actually worsen losses and parasitic inductance if the configuration is not correct.

Basic Principles

The following principles are used in the development of this topic and are presented here as a review of basic magnetics.

1. **Ampere's Law:** The total magneto-motive force along *any* closed path is equal to the total current enclosed by that path:

$$F = \oint H d\ell = I_t = NI \quad \text{Amps} \quad (1)$$

where F is the total magneto-motive force (in Amperes) along a path of length ℓ (m), H is field intensity (A/m), and I_t is the total current through all turns enclosed by the path.

2. **Conservation of energy:** At any moment of time, the current within the conductors and the magnetic field are distributed so as to minimize the energy taken from the source.

3. **Energy content of the field:** The magnetic field *is* energy. The energy density at any point in the field is:

$$w = \int H dB \quad \text{Joules/m}^3$$

where B is the flux density (Tesla). In switching power supplies, almost all magnetic

energy is stored in air gaps, insulation between conductors, and within the conductors, where relative permeability μ_r is essentially 1.0 and constant. The energy density then becomes:

$$w = \frac{1}{2}BH = \frac{1}{2}\mu_0H^2 \quad \text{J/m}^3$$

where μ_0 is the absolute permeability of free space ($=4\pi \cdot 10^{-7}$ in S.I. units). Total energy W (Joules) is obtained by integrating the energy density over the entire volume, v , of the field:

$$W = \frac{1}{2}\mu_0 \int H^2 dv \quad \text{Joules}$$

Within typical transformers and inductors, the magnetic energy is almost always confined to regions where the field intensity H is relatively constant and quite predictable. This often occurs in circuit wiring, as well. In these cases:

$$W = \frac{1}{2}\mu_0 H^2 A \cdot \ell \quad \text{Joules} \quad (2)$$

and from (1), $H\ell = NI$. Substituting for H :

$$W = \frac{1}{2}\mu_0 N^2 I^2 A / \ell \quad \text{Joules} \quad (3)$$

where A is the cross-section area (m^2) of the region normal to the flux, and ℓ is the length of the region in meters (and the effective length of the field).

4. **Circuit inductance:** Inductance is a measure of an electrical circuit's ability to store magnetic energy. Equating the energy stored in the field from (3) with the same energy in circuit terms:

$$W = \frac{1}{2}LI^2 = \frac{1}{2}\mu_0 N^2 I^2 A / \ell$$
$$L = \mu_0 N^2 A / \ell \quad (4)$$

Skin Effect

Figure 1 shows the magnetic field (flux lines) in and around a conductor carrying dc or low frequency current I . The field is radially symmetrical, as shown, only if the return current with its associated field is at a great distance.

At low frequency, the energy in the magnetic field is trivial compared to the energy loss in the resistance of the wire. Hence the current

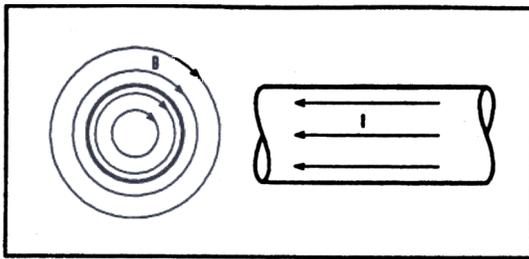


Fig. 1 - Isolated Conductor at Low Frequency distributes itself uniformly throughout the wire so as to minimize the resistance loss and the total energy expended.

Around any closed path outside the wire (and inside the return current), magneto-motive force F is constant and equal to total current I . But field intensity H varies inversely with the radial distance, because constant F is applied across an increasing ℓ ($=2\pi r$).

Within the conductor, F at any radius must equal the enclosed current at that radius, therefore F is proportional to r^2 .

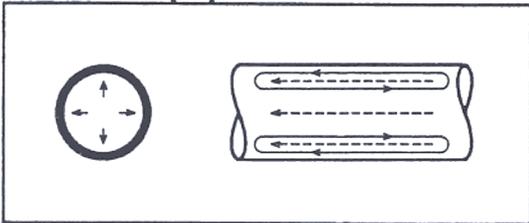


Fig. 2 - Eddy Current at High Frequency

At high frequency: Figure 2 is a superposition model that explains what happens when the frequency rises. The dash lines represent the uniform low frequency current distribution, as seen in Fig. 1. When this current changes rapidly, as it will at high frequency, the flux within the wire must also change rapidly. The changing flux induces a voltage loop, or eddy, as shown by the solid lines near the wire surface. Since this induced voltage is within a conductor, it causes an eddy current coincident with the voltage. Note how this eddy current reinforces the main current flow at the surface, but opposes it toward the center of the wire.

The result is that as frequency rises, current density increases at the conductor surface and decreases toward zero at the center. as shown in Fig. 3. The current tails off exponentially within the conductor. The portion of the conductor that is actually carrying current is

reduced, so the resistance at high frequency (and resulting losses) can be many times greater than at low frequency.

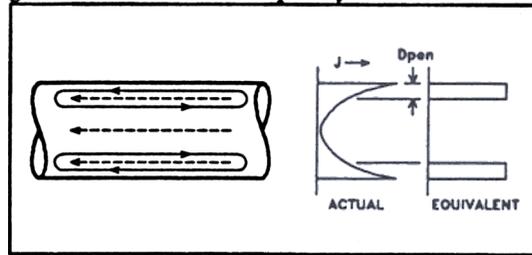


Fig. 3 - High Frequency Current Distribution

Penetration depth: Penetration or skin depth, D_{PEN} , is defined as the distance from the surface to where the current density is $1/e$ times the surface current density (e is the natural log base)[1]:

$$D_{PEN} = [\rho / (\pi \mu f)]^{1/2} \text{ m} \quad (5)$$

where ρ is resistivity. For copper at 100°C , $\rho = 2.3 \cdot 10^{-6} \Omega\text{-cm}$, $\mu = \mu_0 = 4\pi \cdot 10^{-7}$, and:

$$D_{PEN} = 7.5 / (f)^{1/2} \text{ cm} \quad (6)$$

From (6), $D_{PEN} = .024 \text{ cm}$ at 100 kHz , or $.0075 \text{ cm}$ at 1 MHz .

Eqs. (5) and (6) are accurate for a flat conductor surface, or when the radius of curvature is much greater than the penetration depth.

Although the current density tails off exponentially from the surface, the high frequency resistance (and loss) is the same as if the current density were constant from the surface to the penetration depth, then went abruptly to zero as shown on the right hand side of Fig. 3. This equivalent rectangular distribution is easier to apply.

Equivalent circuit model: Another way of looking at the high frequency effects in transformer windings and circuit wiring is through the use of an equivalent electrical circuit model. This approach is probably easier for a circuit designer to relate to.

Figure 4 is the equivalent circuit of the isolated conductor of Figs. 1 to 3. With current I flowing through the wire, L_x accounts for the energy $\frac{1}{2} L_x I^2$ stored in the external magnetic field. L_x is the inductance of the wire at high frequencies.

Point A represents the outer surface of the conductor, while B is at the center. R_i is the

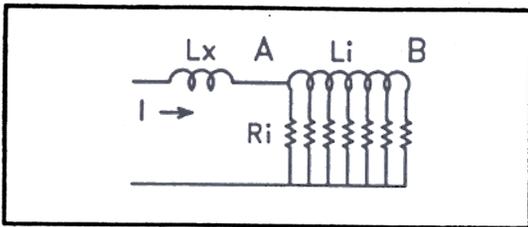


Fig. 4 - Conductor Equivalent Circuit

resistance, distributed through the wire from surface to center. Think of the wire as divided into many concentric cylinders of equal cross section area. The R_i elements shown in the drawing would correspond to the equal resistance of each of the cylinders. Likewise, the internal inductance L_i accounts for the magnetic energy distributed through the cylindrical sections. The energy stored in each section depends on the cumulative current flowing through the elements to the right of that section in the equivalent circuit.

Note that external inductance L_x of the wire (or the leakage inductance of a winding) limits the maximum di/dt through the wire, depending on the source compliance voltage, no matter how fast the switch turns on.

The time domain: If a rapidly rising current is applied to the wire, the voltage across the wire is quite large, mostly across L_x . Internal inductance L_i blocks the current from the wire interior, forcing it to flow at the surface through the left-most resistance element, even after the current has reached its final value and the voltage across L_x collapses. Although the energy demand of L_x is satisfied, the voltage across the wire is still quite large because current has not penetrated significantly into the wire and must flow through the high resistance of the limited cross-section area at the surface. Additional source energy is then mostly dissipated in the resistance of this surface layer.

The voltage across this R_i element at the surface is impressed across the adjacent L_i elements toward the center of the wire, causing the current in L_i near the surface to rise. Current cannot penetrate without a field being generated within the conductor, and this requires energy. As time goes on, conduction propagates from the surface toward the center (at B in the equivalent circuit), storing energy in L_i . More of the resistive elements conduct,

lowering the total resistance and reducing the energy going into losses. Finally, conduction is uniform throughout the wire, no further energy goes into the magnetic fields external or internal to the wire, and a small amount of energy continues to be dissipated in R_i over time.

Note that the concept of skin depth has no meaning in the time domain.

The frequency domain: Referring again to Fig. 4 with a sine wave current applied to the terminals, it is apparent that at low frequencies, the reactance of internal inductance L_i is negligible compared to R_i . Current flow is uniform throughout the wire and resistance is minimum. But at high frequency, current flow will be greatest at the surface (A), tailing off exponentially toward the center (B).

Penetration depth (skin depth) is clearly relevant in the frequency domain. At any frequency, the penetration depth from Eq. (5) or (6) reveals the percentage of the wire area that is effectively conducting, and thus the ratio of dc resistance to ac resistance at that frequency.

Although the current waveforms encountered in most switching power supplies are not sinusoidal, most papers dealing with the design of high frequency transformer windings use a sinusoidal approach based on work done by Dowell in 1966.[2] Some authors use Fourier analysis to extend the sinusoidal method to non-sinusoidal waveforms.

Proximity Effect

Up to this point a single isolated conductor has been considered. Its magnetic field extends radially in all directions, and conduction occurs across the entire surface.

When another conductor is brought into close proximity to the first, their fields add vectorially. Field intensity is no longer uniform around the conductor surfaces, so high frequency current flow will not be uniform.

For example, if the round wire of Fig. 1 is close to another wire carrying an equal current in the opposite direction (the return current path?), the fields will be additive between the two wires and oppose and cancel on the outside. As a result, high frequency current flow is concentrated on the wire surfaces facing each other, where the field intensity is greatest, with

little or no current on the outside surfaces where the field is low. This pattern arranges itself so as to minimize the energy utilized, hence inductance is minimized. As the wires are brought closer together, cancellation is more complete. The concentrated field volume decreases, so the inductance is reduced.

Circuit wiring: The field and current distribution with round wires is not easy to compute. A simpler and more practical example is given in Figure 5. The two flat parallel strips shown are actually the best way to implement high frequency wiring, minimizing the wiring inductance and eddy current losses. These strips could be two wide traces on opposite sides of a printed circuit board. (Don't use point-to-point wiring. It is much more important to collapse the loop and keep the outgoing and return conductors as intimate as possible, even if the wiring distances are greater.)

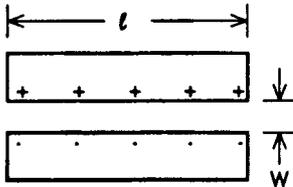


Fig. 5 - Circuit Wiring - Flat Parallel Strip

The + signs indicate current flow into the upper strip, the - indicates current out of the lower strip. Between the strips, the magnetic field is high and uniform, so the current is spread out uniformly on the inner surfaces. On the outside of the strips the field is very low, so the current is almost zero. This results in the minimum possible energy storage (and wiring inductance) for this configuration. If the breadth of the strip, l , is much greater than the separation, w , the energy is almost entirely contained between the two strips. Then l and w are the length and width of the field, and can be used to calculate the inductance. Converting Eq. (4) to cm and with $N = 1$ turn, the inductance per centimeter length of the 2-conductor strip is:

$$L = 12.5 w/l \quad \text{nH/cm} \quad (7)$$

If the strips have a breadth of 1 cm and are separated by 0.1 cm, the combined inductance of the pair is only 1.25 nH for each centimeter

length, divided equally between each of the two conductors. If one conductor is much wider than the other, such as a strip vs. a ground plane, most of the inductance calculated in (6) is in series with the narrower conductor. This is good for keeping down noise in the ground returns.

Note that current penetration is from one side only -- the side where the field is. This means that a strip thicker than the penetration depth is not fully utilized. The equivalent circuit model of Fig. 4 still applies, with A at the surface adjacent to the field. But B becomes the *opposite* side of the strip, not the center, since there is no penetration from the side with no field.

Bad practice: Figures 6 and 7 show what *not* to do for circuit wiring (unless you want high inductance and eddy current losses). Although these strips have large surface areas, proximity effects in these configurations result in very little surface actually utilized. Remember that the field is concentrated directly between the two conductors so as to minimize the stored energy.

In Fig. 6 this results in current flow only at the *edges* facing each other. Also, because the concentrated field region is short, the energy density is very high, and the inductance is several times greater than in Fig. 5.

The Fig. 7 configuration is not *quite* as bad as Fig. 6 because the current does spread out somewhat in one of the two conductors, but it is still many times worse than the proper configuration in Fig. 5. The message is: large



Fig. 6 - Bad Wiring Practice - Side by Side

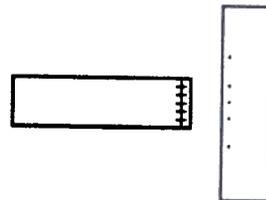


Fig. 7 - Bad Wiring Practice - Right Angled

surface area doesn't improve high frequency performance if the configuration is wrong.

Inductor Windings: Figure 8 is a simple inductor. The winding consists of 4 turns in a single layer. Assuming a current of 1 Ampere through the winding, the total magneto-motive force $F = NI$ along any path linking the 4 turns is 4 Ampere-turns. The field is quite linear across the length of the window because of the addition of the fields from the individual wires in this linear array. The winding could have been a flat strip carrying 4 Amps with the same result.

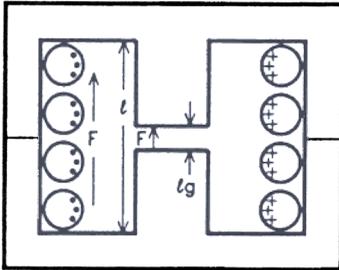


Fig. 8 - Inductor Winding

Without the ferrite core, the field outside of the winding would have been weak because of cancellation, but with the high permeability core, the external field is completely shorted out. This means the entire field, $F = NI$ is contained across the window inside the winding. Field intensity, H equals NI/l . In the center, the entire field is compressed across the small air gap. Field intensity ($H_g = NI/l_g$) is therefore much greater within the gap, so the energy stored in the gap (using Eq. 2 or 3) is much greater than the energy in the much larger window.

At high frequency, current flow is concentrated on the inner surface of the coil, adjacent to the magnetic field. The field outside the coil is negligible, so no current flows on the outer surface.

Transformer Windings: Figure 9 shows a transformer with a four turn single layer primary and a 1 turn single layer copper strip secondary. In any transformer, the sum of the Ampere-turns in all windings must equal zero (except for a small magnetizing current which

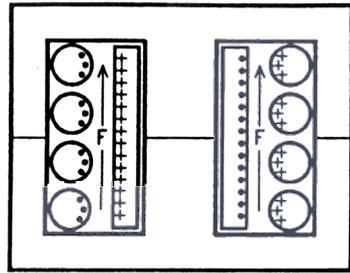


Fig. 9 - Transformer Windings

is neglected). So if the secondary load current is 4 A through 1 turn, the primary current through 4 turns must be 1 Amp. The fields tend to cancel not only outside both windings, but in the center of the two windings as well. Whatever field might remain is shorted out by the high permeability core which has no gap. Thus the field generated by the current in the windings, $F = 4 \text{ A}$, exists only *between* the windings. So at high frequency, current flow is on the outside of the inner winding and on the inside of the outer winding, adjacent to the field.

Multiple Layer Windings

Figure 10 shows a transformer with multi-layer windings and its associated *low frequency* mmf (F) and energy density diagrams. One half of the core and windings are depicted. At low frequency, current (not shown) is uniformly distributed through all conductors, because they are much thinner than the penetration depth.

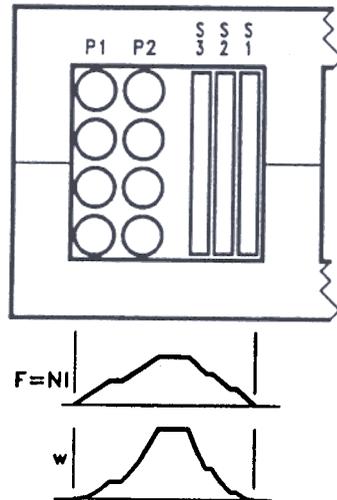


Fig. 10 - Multiple Layer Winding

The primary winding has 8 turns arranged in two 4-turn layers, while the secondary has 3 turns of copper strip in 3 layers. With 2 Amp load current, the secondary has $3T \cdot 2A = 6 \text{ A-T}$. The primary must also have 6 A-T, so primary current is 0.75 A.

As shown in the mmf diagram below the core in Fig. 10, there is no field outside of the primary or inside the secondary, but starting at the outside of the primary and moving toward the center, the field rises to its maximum value between the two windings. With uniform current distribution at low frequency, note how the field builds uniformly within each conductor according to Faraday's law, staying constant between the conductors. The energy density in the field goes up with the square of the field strength, as shown below the mmf diagram. The area under the energy density curve is the total leakage inductance energy stored in and between the windings.

So multiple layers cause the field to build. At high frequencies, it will be shown that the eddy current losses go up exponentially as the number of layers is increased. The number of layers should be kept to a minimum by using a core with a long narrow window to accommodate all the turns in fewer layers (this also causes a dramatic reduction in leakage inductance). The window shape illustrated in Fig. 10 is far from optimum.

Interleaved Windings: Another way to reduce the effective number of layers is to break up the winding into smaller sections through

interleaving, as shown in Figure 11.

With interleaving, each winding is essentially divided into two or more sections, as shown on each side of the dotted line in Fig. 11. The primary now has two sections a and b, each with 1 layer of 4 turns. The secondary is also divided down the middle into two sections of $1 \frac{1}{2}$ layers, 1 turn per layer. (This is why half layers are included in eddy current loss curves.) Note that the 2 amperes through the $1 \frac{1}{2}$ turns of secondary section (a) cancels the 0.75 A, 4 turns of primary section (a), and the field goes through zero in the middle of the center secondary turn at the dotted line. F builds up to only half the peak value compared to Fig. 10, and reverses direction between alternate winding sections. It will be shown that the reduced field causes a great reduction in eddy current losses.

Because of the reduced field, the total energy under the energy density curve in Fig. 11 is only 1/4 the total energy in Fig. 10. Thus, interleaving reduces the leakage inductance by a factor of 4!

Multiple layers at high frequency: Figure 12 is an enlarged section of Fig. 10 but at a high frequency where the penetration depth is 20% of the secondary winding strip thickness. The field strength and current density are the same as at low frequency in the spaces between the conductors. But *within* the conductors, current density, magnetic field and energy density all fall off rapidly moving in from the surface. (Dash lines show low frequency distributions.)

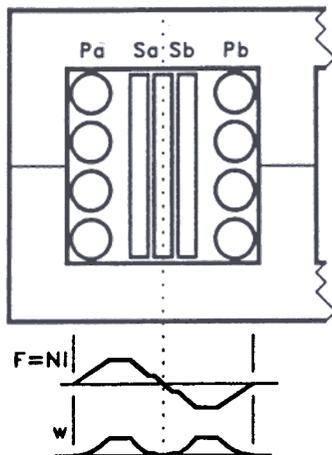


Fig. 11 - Interleaved Windings

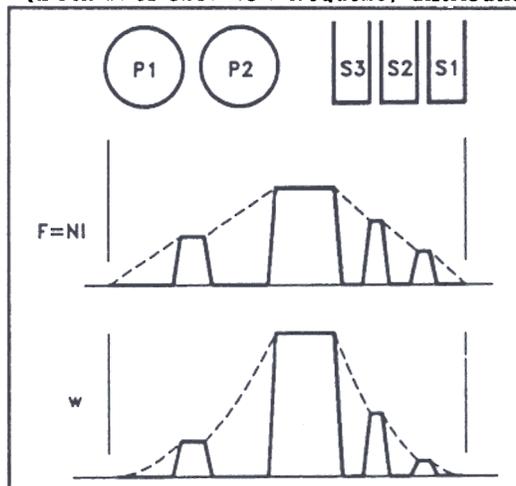


Fig. 12 - Multiple Layers at High Frequency

The heavier lines showing the high frequency distributions are approximations based on the current distribution ending abruptly at the penetration depth. Actually, the slopes are steeper at the surfaces, and tail off within the wire.)

Notice that the total energy under the energy density curve is about half the amount at low frequency. This means the leakage inductance has decreased at high frequency, but only because the energy within the conductors is practically eliminated. This is not a very practical way to reduce leakage inductance -- the penalty is a huge increase in eddy current losses.

With the penetration depth 20% of the strip thickness, the ac resistance might be expected to be 5 times the dc resistance. But with three layers building up the field, the ac resistance is actually 32 times greater!

Why multiple layers cause high losses:

Figure 13 is an even more enlarged view of the 3 secondary layers of Fig. 12, together with their high frequency mmf diagram. Assume a current of 1 Ampere through the 3 layer winding. There is only one turn (strip) per layer.

To the right of layer S1, the mmf is 0. At the left of S1, $F=1$ A-T. The 1 Amp current in S1 is crowded into the 20% penetration depth adjacent to the field. Field F also cannot penetrate more than 20% into S1. This 1 A-T

field exists only between S1 and S2. F cannot penetrate S2, either. It must terminate on the right side of S2, but it cannot just magically disappear.

According to Faraday's law, for the mmf to be zero in the center of S2, the enclosed current must be zero. This requires a current of 1 Amp on the right surface of S2 in the opposite direction to normal current flow to cancel the 1 Amp in S1. Then, to achieve the 2 A-T field to the left of S2 requires a surface current of 2 Amps! (The net current in S2 is still 1 Amp.)

The 2 A-T field must be terminated at the right side of S3 with 2 A reverse current flow. Then 3 Amps must flow on the S3 left surface to support the 3 A-T field and to conform to the net 1 Amp through the winding.

If the current in each layer were just the 1 Amp, limited in penetration to 20% of the conductor thickness, the ac to dc resistance ratio, F_R , would be 5:1. But the surface currents in successive layers become much larger, as discussed above. The tabulation above the conductors in Fig. 13 gives the current at each surface and the current squared, which indicates the relative power loss at each surface. The two surfaces of S2 together dissipate $1+4 = 5$ times as much as S1, while dissipation in S3 is $4+9=13$ times S1!

The average resistance of the 3 layers is $(9+4+4+1+1)/3 = 19/3 = 6.333$ times the resistance of layer S1. Since the ac resistance of S1 is already 5 times the dc resistance (because of the 20% penetration depth), the ratio of average ac resistance to the dc resistance, F_R , is 31.67 : 1. Hardly negligible.

Referring to S3 with 3A and -2A at its surfaces, if conductor thickness is decreased or if frequency is decreased to improve penetration, the penetration "tails" of these opposing currents will reach across and partially cancel. When D_{PEN} is much larger than the conductor thickness, cancellation is complete, conductor current is 1 Amp uniformly distributed, and $F_R = 1$.

Although each layer was a 1 turn strip carrying 1 Amp in this illustration, each layer could have been 10 turns carrying 0.1 Amps with the same results.

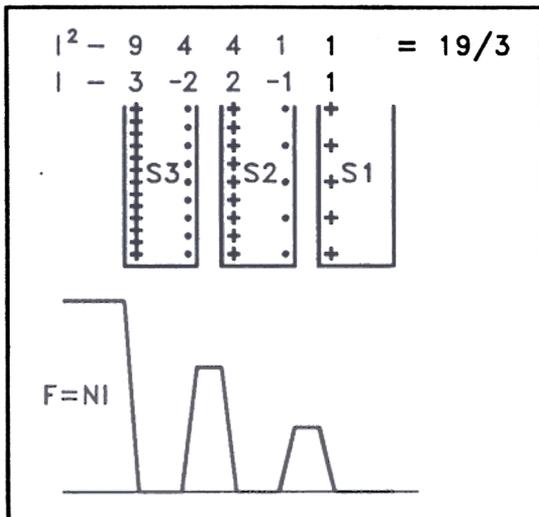


Fig. 13 - Surface Currents

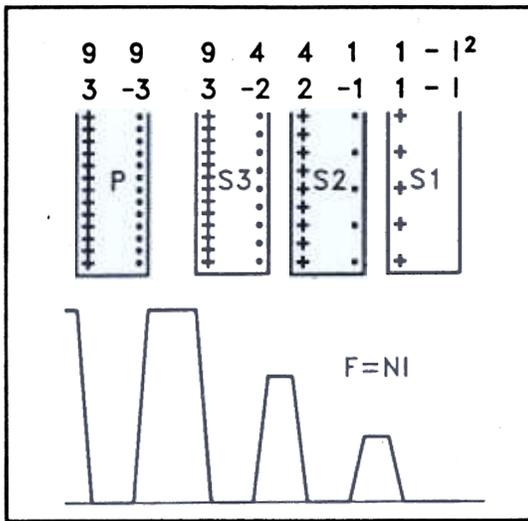


Fig. 14 - Passive Winding Losses

Passive layers: A passive layer is any conductor layer that is not actively "working" by carrying net useful current. Faraday shields and the non-conducting side of center-tapped windings are examples of passive layers.

Figure 14 shows what happens if a Faraday shield is inserted in the 3 A-T field between the secondary winding of Fig. 13 and the primary (off to the left). If the Faraday shield thickness is much greater than D_{PEN} , 3 Amps must flow on each surface because the field cannot penetrate. At each surface, I^2 is 9 Amps squared, and both surfaces together dissipate 18 times as much as S1, or almost as much as all three secondary turns combined.

Faraday shields are always located where the field is highest. Their thickness should be less than 1/3 of D_{PEN} keep the loss to an acceptable level.

For another example, consider a center-tapped secondary with sides A and B each side of the center-tap. If A is physically between B and the primary, A is a passive conductor in the high field region when B is conducting, but B is outside the field when A conducts. The *additional* passive dissipation in A will probably exceed the active dissipation in either A or B. This is one reason that single-ended transformers overtake or even surpass push-pull and half-bridge versions at frequencies above a few hundred kHz.

Paralleled windings: When ac resistance of a strip secondary winding is too high because the required strip thickness is too great, it is tempting to simply subdivide it into several thinner strips, insulated from each other. This doesn't work -- the parallel combination will have the same losses as an equivalent solid strip. This is because the individual thin strips occupy different positions in the field, causing eddy currents to circulate between the outer and innermost strips where they are connected in parallel at their ends, similar to what happens in a single solid strip.

Conductors can be successfully paralleled only when they experience the same field, averaged along their length:

1. Wires in the same layer can be paralleled, as long as they progress together from one layer to the next.
2. Litz wire -- fine wires woven or twisted in such a manner that they successively occupy the same positions in the field.
3. Portions of a winding at comparable field levels in different interleaved sections can be paralleled. For example the two four-turn primary sections in Fig. 11 could be paralleled. The field must remain apportioned equally between in the two sections or much more energy would be required. If the secondary in Fig. 11 were a single solid turn, it could be divided into two thinner paralleled turns.

Calculating ac resistance: It has been shown that it is not difficult to calculate F_R when the conductor thickness is much greater than the penetration depth. It is also easy when the conductor thickness is much less than D_{PEN} -- $F_R = 1$. But the condition of greatest interest to the transformer designer is when the conductor thickness is in the same range as D_{PEN} , and here the calculations are quite difficult.

Dowell solved the problem for sinusoidal waveforms in his 1966 paper.[2] The curves in Figure 15 are derived from Dowell's work. The vertical scale is F_R , the ratio of R_{ac}/R_{dc} . The horizontal scale, Q , is the ratio of the effective conductor height, or layer thickness, to the penetration depth, D_{PEN} . For strip or foil windings, the layer thickness is the strip thickness. For round wires touching each other in the layer, the effective layer thickness is 0.83 times

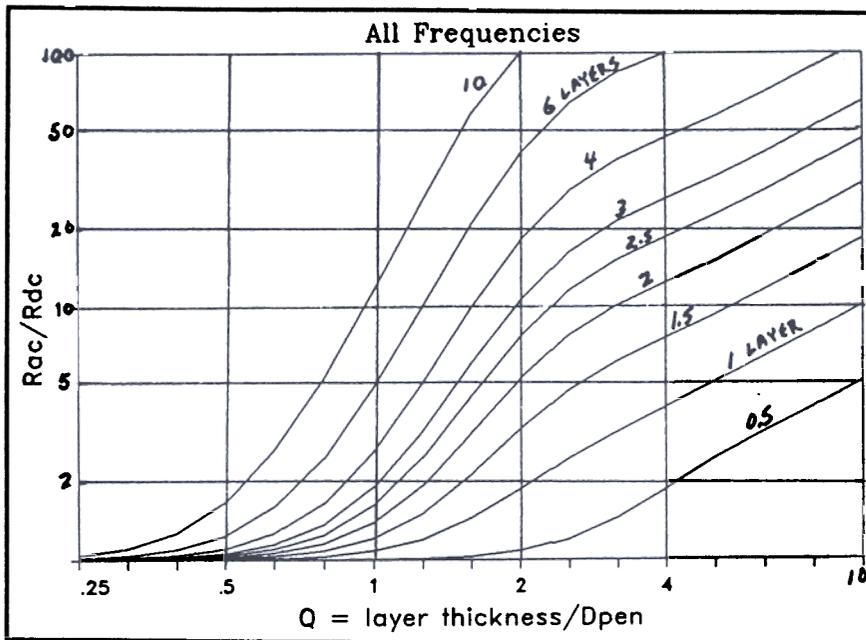


Fig. 15 - Eddy Current Losses - R_{ac}/R_{dc}

the wire diameter. For round wires spaced apart in a layer, the effective layer thickness is $.83 \cdot d \cdot (d/s)^{1/2}$, where d is wire diameter and s is the center-to-center spacing of the wires.

Referring to the calculation of $F_R = 31.67$ on page 7, enter Fig. 15 with $Q=5$ and 3 layers. The resulting F_R value agrees.

At the extreme right of Fig. 15 is the region where the conductor thickness is much greater than D_{PEN} and F_R is very large. The curves are parallel and have a +1 slope. On the extreme left, conductor thickness is much less than D_{PEN} and F_R approaches 1.0. In the center of the graph, the curves plunge downward as Q gets smaller. An F_R of 1.5 is a good goal to achieve. With a much higher value, losses hurt too much. To go much below 1.5 is past the point of diminishing returns, requires much finer conductor sizes. Achieving F_R of 1.5 requires a Q value ranging from 1.6 with 1 layer, to 0.4 with 10 layers.

Starting with a conductor thickness much greater than D_{PEN} and subdividing into smaller conductors usually makes F_R worse before it gets better. For example, assume a single layer winding of 10 close spaced turns, and a Q of 4. F_R from the Fig. 15 is 3.8 -- not good enough. If four parallel wires of half the diameter are

substituted for the original wire (taking care to handle this properly), there will be 40 wires, 20 per layer, 2 layers deep. Q is now 2. Entering Fig. 15 at $Q=2$ and 2 layers, F_R is 5.2 -- it went up! The reason for this is the wire size is still too large for effective penetration and cancellation of the eddy currents, and the number of layers has been doubled with the extra eddy current surfaces this generates.

Subdividing again into 16 parallel wires

of $1/4$ the original diameter there are 160 total wires, 40 per layer, 4 layers deep. Q is 1 and F_R is down to 2.8.

A third subdivision to 64 parallel wires with $1/8$ the original diameter results in 640 total wires, 80 per layer, 8 layers. Q is 0.5 and F_R finally reaches 1.5.

Non-sinusoidal waveforms: Venkatramen[3] and Carsten[4] have applied Dowell's sine wave solution to various non-sinusoidal waveforms more relevant to switching power supplies. This is done by taking the Fourier components of the current waveform, then using Dowell's approach to calculate the loss for each harmonic and adding the losses. They have also redefined the way the data is presented in an attempt to make it more useful.

Their curves show that as the pulse width narrows, the effective ac resistance goes up because the higher frequency harmonics are more important. But the worst losses are not at narrow pulse widths. In most switching supplies, the *peak* pulse current is constant (at full load). The high frequency harmonics and losses are much the same regardless of pulse width, but the total rms, the dc and low frequency components get much worse as the pulse width widens. Worst case for total copper

losses is probably near a duty ratio of 0.5.

In applications where current pulse widths in the vicinity of 0.5 duty ratio are the worst case conditions for copper losses, a shortcut method to achieve satisfactory results is to design the winding for an F_R of 1.5 at the fundamental of the current waveform, then allow an extra 30-50% for additional losses due to the high frequency components.

References

- [1] D. G. Fink et al, *Electronics Engineer's Handbook*, McGraw-Hill, 1975
- [2] P. L. Dowell, "Effects of Eddy Currents in Transformer Windings," *Proceedings IEE (UK)*, Vol. 113, No. 8, August, 1966, pp. 1387-1394.
- [3] P. S. Venkatramen, "Winding Eddy Current Losses in Switch Mode Power Transformers Due to Rectangular Wave Currents," *Proceedings of Powercon 11*, 1984, Sec. A1.
- [4] B. Carsten, "High Frequency Conductor Losses in Switchmode Magnetics," *High Frequency Power Converter Conference*, 1986, pp. 155-176

In switching power supply transformers, if the conductor thickness is similar to or greater than penetration (skin) depth at the operating frequency, ac current flows in only a portion of each conductor, resulting in high ac losses. This effect is magnified exponentially the more layers there are in the winding. To bring the ac losses back down to an acceptable level, the conductor thickness must be reduced.

Thin strip with a width equal to the winding width is often used, especially for low voltage, high current windings with few turns and large conductor area. Each turn is a layer and each turn must be insulated from the others. Strips cannot be subdivided into several paralleled thinner strips unless the individual strips are in different winding sections, otherwise unequal induced voltages will cause large eddy currents to circulate from one strip to another and losses will be high.

When strip or foil is not appropriate for a winding, the conductor can be divided into multiple strands of fine wire which are then connected in parallel at the terminations of the winding.

All wires in the group must be individually insulated and must encompass the identical flux to avoid eddy currents circulating from one wire to another through their terminating interconnections. If only a few wires in parallel are to be used, they can be laid together side-by-side (as though they were tied together as a flat strip). Each wire must have *exactly* the same number of turns as the other wires within *each layer*, to avoid cross-circulating eddy currents. This is not practical when large numbers of fine wires must be used.

Another solution is to interweave or twist the wires together in such a manner that each wire moves within the group to successively occupy each level within the field. But when this is done properly, voids are introduced, resulting in poor utilization of the available winding area compared with closely packed (untwisted) conductors.

Low power, high frequency Litz wire is usually woven from very fine wires, but the woven structure results in a large percentage of

voids and poor copper utilization. Litz wire for power applications is usually made with a few wires twisted together in a strand and a few of these strands twisted into bigger strands, etc. The amount of twist required is moderate -- not enough to significantly increase the strand diameter or the length of the individual wires.

Consider a bundle of seven wires twisted into a strand, with one wire in the center. The packing structure is hexagonal -- as efficient as possible, with an outer surface which is almost circular. The amount of copper in this strand is .778 of a single solid wire with the same max. diameter as the strand. The outer six wires rotationally occupy each of the outside positions, but the center wire is fixed in its location. ac losses are actually improved by eliminating the seventh, inner wire. (In practice, it should be replaced by a non-conductive filler to maintain the shape of the strand.) This reduces the winding area utilization factor to .667 of the equivalent solid wire.

Even solid wire does not achieve 100% utilization of the winding area. The bottoms of the wires in each layer ride diagonally across the tops of the wires in the layer below, so they cannot pack down into the valleys between the wires below, except in a limited and unpredictable way. This means that round wire occupies the area of a square with sides equal to wire diameter, hence the utilization is $\pi/4$, or .785. If a six-wire strand described above is substituted for the solid wire, overall utilization is further reduced to $.785 \cdot .667 = .524$.

Table I shows the utilization factor of 3 to 6-wire strands. Although the utilization factors are quite similar, it will be shown that they do not perform equally well in achieving a multi-strand cable with a large number of wires.

TABLE I
Utilization Factor of Single Strands

Number of Wires:	3	4	5	6
Utilization Factor:	.65	.686	.685	.667

It is not unusual to require *hundreds* of fine wires in parallel to achieve the required dc and ac resistances at 100 kHz or higher. This requires that strands be twisted into larger strands, and these twisted with each other, progressing to a cable containing the total number of fine wires needed to carry the desired high frequency current. The effective diameter of each strand is the circle of rotation of the outer extremities of the wires. Each level of twisting further reduces the utilization factor. As shown in Table II, much better utilization is achieved when more wires/strands are twisted together at one time, because fewer levels of twisting are required to achieve a similar number of wires.

For example, with 4 strands/twist, 4 wires twisted comprise a Level 1 strand, four Level 1 strands are twisted to obtain a Level 2 strand having 16 wires. Four Level 2 strands are then twisted resulting in a Level 3 strand with 64 wires, etc. Add levels until the desired number of wires is reached.

The utilization factors of Table II are further reduced by $\pi/4$ (.785) because round cable made according to Table II occupies a square portion of the winding space.

Instead of making up one cable containing all of the wires needed, it is often advantageous not to twist the final level. This may provide greater flexibility in fitting the winding to the

available breadth and height, and improves the utilization factor by eliminating one level of twisting.

For example, assume 256 wires of a given diameter are required. This could be achieved in one Level 4 cable using 4 strands/twist and 4 twist levels. The utilization is .22 compared with solid wire the same diameter as the cable, and $.22 \cdot .785 = .17$ of the winding space is copper. However if 4 Level 3 cables are used in parallel, the utilization is .32 compared to solid wire, and $.32 \cdot .785 = .25$ of the occupied winding area. Remember that *each of the paralleled cables must have the same number of turns in each layer.*

Insulation on the wires further reduces the utilization, especially with fine wires whose insulation is an increasing percentage of the wire area. With more and more turns of finer wire, the total area of the winding must increase if the desired copper area is maintained. When the maximum available window area is reached, improvement may still be obtained by going to more turns of finer wire, even though the dc resistance will increase, if the reduction in ac resistance is sufficient. Otherwise, the only solutions are: (a) Let the transformer run hotter, or (b) use a larger size core which will provide a bigger window (and fewer turns are usually required).

TABLE II

Utilization Factor vs. Twist Levels

	<u>3</u>		<u>4</u>		<u>5</u>		<u>6</u>	
	<u>Wires</u>	<u>Util.</u>	<u>Wires</u>	<u>Util.</u>	<u>Wires</u>	<u>Util.</u>	<u>Wires</u>	<u>Util.</u>
Level 1	3	.65	4	.69	5	.69	6	.67
Level 2	9	.42	16	.47	25	.47	36	.44
Level 3	27	.28	64	.32	125	.32	216	.30
Level 4	81	.18	256	.22	625	.22	1296	.20
Level 5	243	.12	1024	.15				

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265