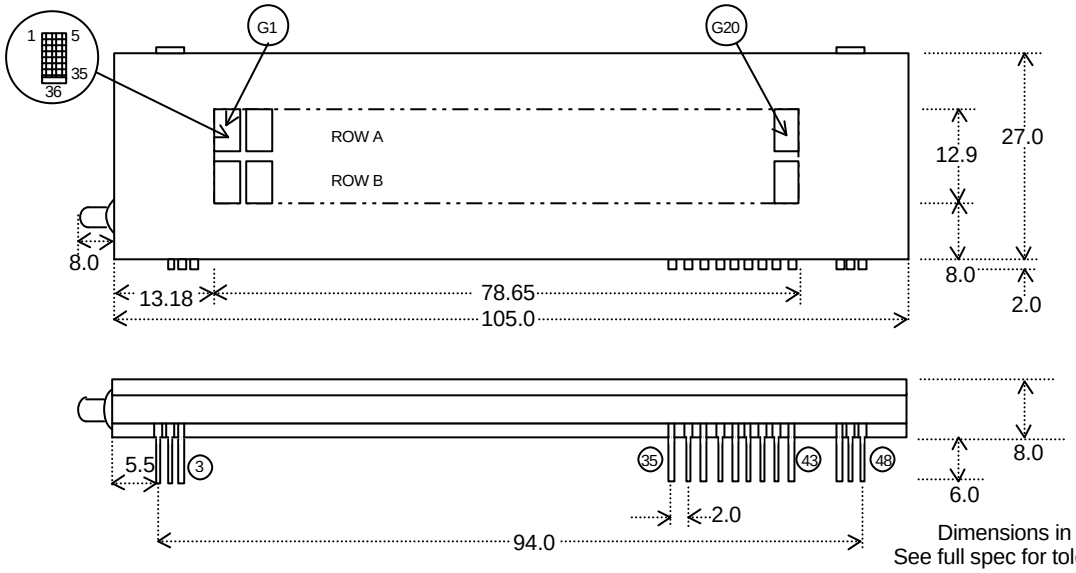
5 x 7 Dot Character Chip In Glass VFD — DN2025E

- **2 Lines of 20 Characters**
- **5mm High 5 x 7 Dot Matrix Font**
- **Chip In Glass Driver IC**
- **High Brightness Blue Green Display**
- **Low Pinout Count**
- **Wide Operating Temperature**

This VF glass includes a 96 bit serial shift register, latched driver which connects to the anode and grid electrodes. An external host is required to provide a multiplexing data stream to refresh the display. The signal inputs can be connected to the ports of a CMOS microprocessor. The a.c. filament supply (F1, F2) can be derived from a source of 10KHz to 200KHz. Consult our application notes for further information.



Dimensions in mm
See full spec for tolerances

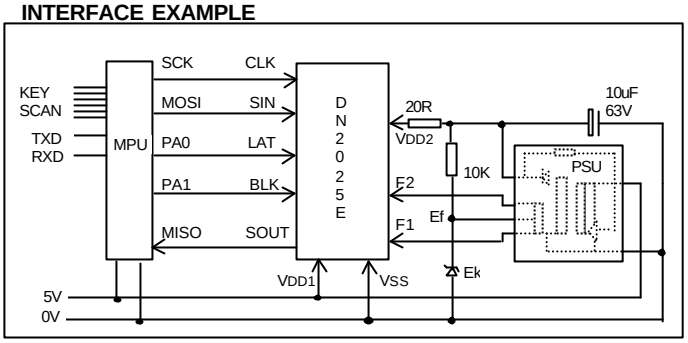
PIN OUT

Pin	Sig
1	F1
2	F1
3	F1
35	SIN
36	$V_{DD\ 1}$
37	SOUT
38	LAT
39	BLK
40	CLK
41	V_{SS}
42	V_{SS}
43	V_{DD2}
46	F2
47	F2
48	F2

ELECTRICAL SPECIFICATION

Parameter	Sym	Min	Typ	Max	Unit	Condition
Logic Voltage	V_{DD1}	4.5	5.0	5.5	V	V_{SS}=0V
Logic Current	I_{DD1}	-	3.0	5.0	mA	V_{DD1}=5V
Filament Voltage	E f	3.5	3.9	4.3	Vac	V_{DD2}=0V
Filament Current	I f	135.0	150.0	165.0	mAac	V_{DD2}=0V
Display Voltage	V_{DD2}	30.0	40.0	43.0	V	V_{SS}=0V
Display Current	I_{DD2}	-	10.0	20.0	mA	V_{DD2}=40V
Filament Bias	E_K	4.0	5.0	6.0	V	V_{SS}=0V
Logic High Input	V_{IH}	+2.4	-	V_{DD1}	V	V_{SS}=0V
Logic Low Input	V_{IL}	0	-	+0.7	V	V_{SS}=0V
Logic High Input	I_{IH}	-	-	0.1	µA	V_{DD1}=5V
Logic Low Input	I_{IL}	-250	-70	-35	µA	V_{DD1}=5V

INTERFACE EXAMPLE

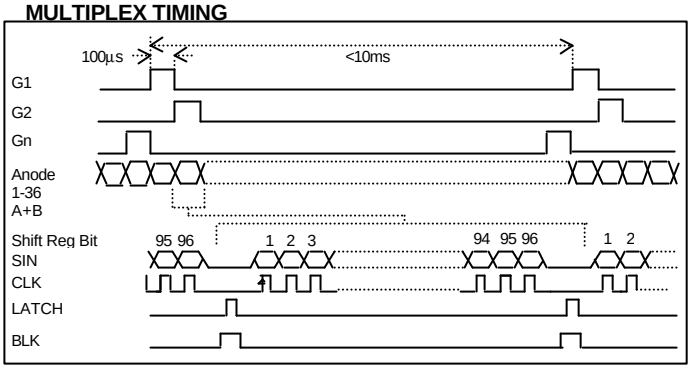


ENVIRONMENTAL and OPTICAL SPECIFICATION

Parameter	Value
Character Size/Pitch (XxY mm)	2.65 x 4.7/4.0 X 7.2
Dot Size/Pitch (XxY mm)	0.45 x 0.5/0.55 x 0.7
Luminance	700 cd/m^2 Typ
Colour of Illumination	Blue-Green (505nm)
Operating Temperature	-40°C to +85°C
Storage Temperature	-50°C to +85°C
Operating Humidity (non condensing)	5 to 95% @ 25°C

1. Optical filters can provide additional colours.
2. The power on rise time should be less than 50ms.
3. The 20R resistor at the V_{DD2} input is required to prevent current surge during switching.
4. If scanning of the display stops with V_{DD2} applied, the BLK input must be set high to prevent damage to the display

MULTIPLEX TIMING



SHIFT REGISTER ASSIGNMENT

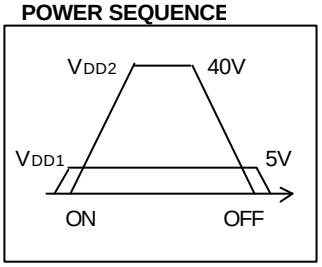
Electrode	Bit Numbers
Grid G1-G20	1-20
Dot A36, A35-A1	59, 62-96
Dot B36, B35-B1	21, 24-58
Not Connected	22,23, 60,61

The interlaced dot anode and grid data is clocked into the shift register in the above 96 bit sequence for each character scanned.

INTERFACE TIMING

Parameter	Time
CLK Cycle	500ns min
CLK High	200ns min
CLK Low	200ns min
SIN Setup	40ns min
SIN Hold	30ns min
LAT High	300ns min
CLK then LAT	250ns min
BLK Hold	10µs min

POWER SEQUENCE



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