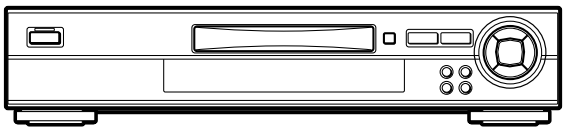
aiwa SERVICE

XD-DV370 HR(N) EZ(N, B) K(N) U(B)

<HR(N)>



<Except for HR(N)>

SERVICE MANUAL

DVD PLAYER

BASIC DVD/CD MECHANISM : DP2[6721R-0308A](HR/K/U)
DP3[6721R-0309A](EZ)

If requiring information about the ELECTRICAL ADJUSTMENT & MECHANSIM ADJUSTMENT & MECHANISM PARTS LOCATION <EZ> & MECHANISM DISASSEMBLY <EZ> & FL GRID ASSINGMENT/ANODE CONNECTION/PIN CONNECTION.
see Supplement Service manual of XD-DV370(HR/U/K/EZ) (S/M Code No. 09-00C-349-9S1)

aiwa

S/M Code No. 09-009-349-9N1

DATA

TABLE OF CONTENTS

SPECIFICATIONS

<HR, EZ, K MODELS>

Power supply	110 - 240 V AC, 50/60 Hz <HR, EZ> 230 V AC, 50 Hz <K>
Power consumption	16 W
Weight	3.2 kg
External dimensions	430 × 88 × 245 mm (w × h × d)
Laser	Semicounductor laser, wave length 650/750 nm
Signal format	PAL/NTSC
Supported discs	DVD video discs 12 cm (single-sided single-layer, single-sided double-layer, double-sided-double layer) 8 cm (single-sided single-layer, single-sided double-layer, double-sided-double layer) Compact discs (CD-DA, video CD) 12 cm and 8 cm discs
S video output	Y output: 1 Vp-p (75 ohms, sync negative) C output: 0.286 Vp-p 1 Mini DIN 4 pin
Video output	Video composite output 1 Vp-p (75 ohms, sync negative) 1 RCA jack 1 Scart connector Video component output <HR> Y output: 1 Vp-p (75 ohms, sync negative) 1 RCA jack P_B,P_R output: 0.7 Vp-p (75 ohms) 1 RCA jacks (P_B,P_R)
Audio output	Digital output 0.5 Vp-p (75 ohms) 1 Fiber optical connector 1 RCA jack Analogue output 2.0 Vrms (1kHz, 0dB, 330 ohms) 1 RCA jacks (L/R)
Audio output characteristics	Signal to noise ratio More than 105 dB (EIAJ) Dynamic range More than 95 dB (EIAJ) Harmonic distortion 0.003% Frequency range: CD / VCD: 2 Hz to 20 kHz DVD: 2Hz to 22kHz (48kHz sampling) 2Hz to 44kHz (96kHz sampling) Wow and flutter: unmeasurable
Operating conditions	5˚C to 35˚C

<U MODEL>

Power supply	120 V AC, 60 Hz
Power consumption	16 W
Weight	3.2 kg (7.1 lbs)
External dimensions	430 × 88 × 245 mm (w × h × d) (17× 3.5 × 9.9 inches)
Signal format	NTSC
Supported discs	DVD video discs 12 cm (single-sided single-layer, single-sided double-layer, double-sided-double layer) 8 cm (single-sided single-layer, single-sided double-layer, double-sided-double layer) Compact discs (CD-DA, video CD) 12 cm and 8 cm discs
S video output	Y output: 1 Vp-p (75 ohms, sync negative) C output: 0.286 Vp-p 1 Mini Din 4 pin
Video output	Video composite output 1 Vp-p (75 ohms, sync negative) 1 RCA jack Video component output Y output: 1 Vp-p (75 ohms, sync negative) 1 RCA jack P_B,P_R output: 0.7 Vp-p (75 ohms) 1 RCA jacks (P_B,P_R)
Audio output	Digital output 0.5 Vp-p (75 ohms) 1 Fiber optical connector Analog output 2.0 Vrms (1kHz, 0dB, 330 ohms) 2 RCA jacks (L/R)
Audio output characteristics	Signal to noise ratio More than 105 dB (EIAJ) Dynamic range More than 95 dB (EIAJ) Harmonic distortion 0.003% Frequency range: CD / VCD: 2 Hz to 20 kHz DVD: 2Hz to 22kHz (48kHz sampling) 2Hz to 44kHz (96kHz sampling) Wow and flutter: unmeasurable
Operating conditions	5 ˚C to 35 ˚C (41 ˚F to 95 ˚F)

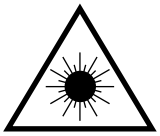
- Design and specifications are subject to change without notice.

- Manufactured under license from Dolby Laboratories. Dolby , Pro Logic and the double-D symbol are trademarks of Dolby Laboratories. Confidential unpublished works. c1992-1997 Dolby Laboratories. All rights reserved.
- Manufactured under license from Digital Theater Systems, Ino. US Pat. No. 5,451,942 and other worldwide patents issued and pending. DTS and DTS Digital Surround are trademarks of Digital Theater Systems, Inc. c1996 Digital Theater systems, Ino. All rights reserved.
- Spatializer¤ 3-D Stereo, Spatializer N-2-2 (TM) and the circle-in-square device are trademarks owned by Desper Products, Inc,.

PROTECTION OF EYES FROM LASER BEAM DURING SERVICING

This set employs laser. Therefore, be sure to follow carefully the instructions below when servicing.

WARNING!
WHEN SERVICING, DO NOT APPROACH THE LASER EXIT WITH THE EYE TOO CLOSELY. IN CASE IT IS NECESSARY TO CONFIRM LASER BEAM EMISSION. BE SURE TO OBSERVE FROM A DISTANCE OF MORE THAN 30cm FROM THE SURFACE OF THE OBJECTIVE LENS ON THE OPTICAL PICK-UP BLOCK.



- Caution: Invisible laser radiation when open and interlocks defeated avoid exposure to beam.
- Advarsel: Usynlig laserstråling ved åbning, når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling.

VAROITUS!
Laiteen Käyttäminen muulla kuin tässä käyttöohjeessa mainitulla tavalla saataa altistaa käyt-täjän turvallisuusluokan 1 ylittävälle näkymättömälle lasersäteilylle.

VARNING!
Om apparaten används på annat sätt än vad som specificeras i denna bruksanvising, kan användaren utsättas för osynling laserstrålning, som överskrider gränsen för laserklass 1.

Precaution to replace Optical block

Body or clothes electrostatic potential could ruin laser diode in the optical block. Be sure ground body and workbench, and use care the clothes do not touch the diode.

1) After the connection, remove solder shown in the figures below.

CAUTION
Use of controls or adjustments or performance of procedures other than those specified herin may result in hazardous radiation exposure.

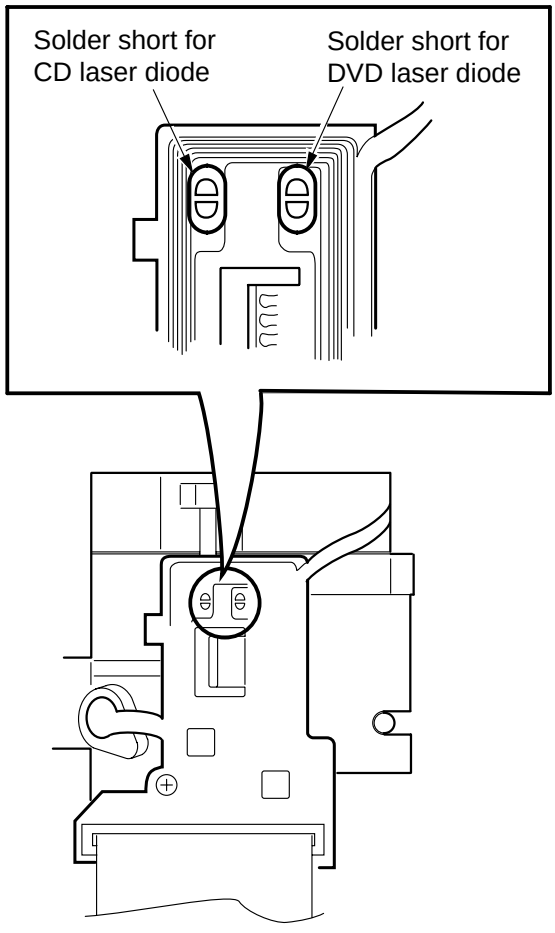
ATTENTION
L'utillisation de commandes, réglages ou procédures autres que ceux spécifiés peut entraîner une dangereuse exposition aux radiations.

ADVARSEL!
Usynlig laserstråling ved åbning, når sikkerhedsafbrydereer ude af funktion. Undgå udsættelse for stråling.

This Compact Disc player is classified as a CLASS 1 LASER product.
The CLASS 1 LASER PRODUCT label is located on the rear exterior.

CLASS 1	LASER PRODUCT
KLASSE 1	LASER PRODUKT
LUOKAN 1	LASER LAITE
KLASS 1	LASER APPARAT

(SPU3140)



ACCESSORIES LIST

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
1	S8-35R-S00-12X		INSTRUCTION ASSY<HRN>
1	S8-35R-S00-12W		INSTRUCTION ASSY<UB>
1	S8-35R-S00-12V		INSTRUCTION ASSY<KN>
1	S8-35R-S00-12Z		INSTRUCTION ASSY<EZB,EZN>
2	S7-11R-2N0-13F		REMOTE CONTROLLER ASSY<HRN>
2	S7-11R-2N0-13D		REMOTE CONTROLLER ASSY<UB,EZB>
2	S7-11R-2N0-13E		REMOTE CONTROLLER ASSY<KN,EZN>
3	S5-640-17B-000		PLUG ASSY PHONE CORD 1WAY
3	S5-640-18B-000		PLUG ASSY PHONO CORD

CABINET DISASSEMBLY

1. Top Case

1. Release 7 screws (A). (See Fig. 2-1)
2. Lift the top case with holding the back of it, and remove it in the direction of the arrow

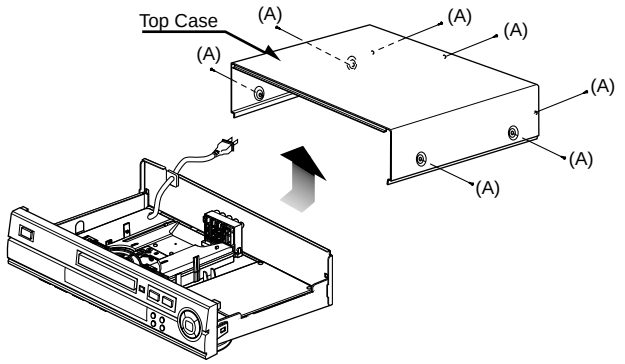


Fig. 2-1

2. Tray Door

1. Eject the disc tray.
2. Lift up the tray door in the direction of the arrow.

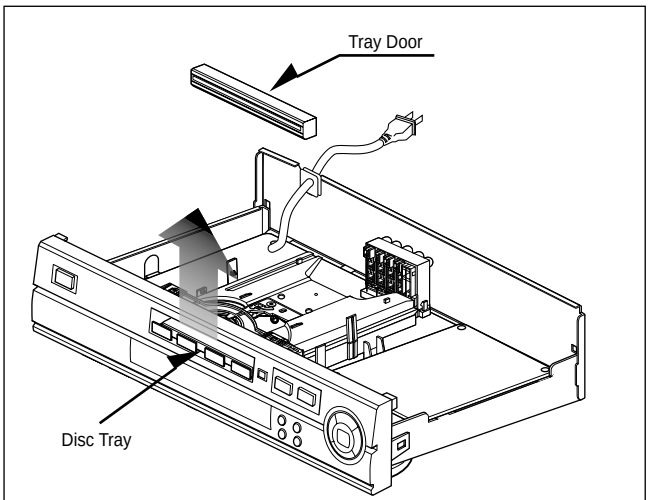


Fig. 2-2

3. Front Panel

1. Eject the disc tray. (See Fig. 2-2)
2. Remove the tray door. (See Fig. 2-2)
3. Release 2 screws (B).
4. Pull the front panel toward you while pressing 7 stoppers to disengage, and remove the front panel. (See Fig. 2-3)

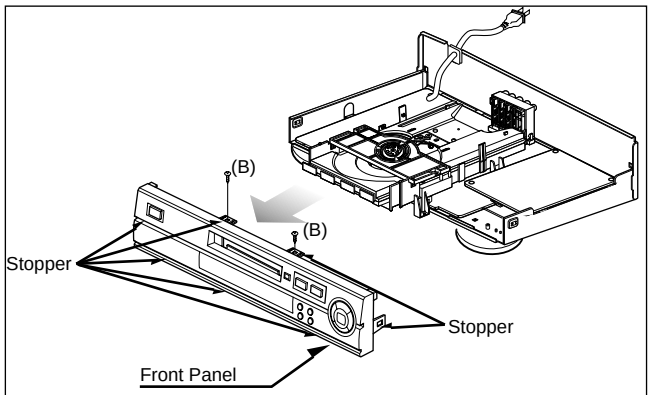


Fig. 2-3

CIRCUIT BOARD DISASSEMBLY

1. Disassembling of Main Circuit Board and Interface Board

1. Remove the top case.(See Fig. 2-1)
2. Remove 12 screw (C).
3. Remove FF-cable (PMD02, PMD04), and remove the DVD MECHANISM.
4. Remove 2 connector (P3901, P5901) and remove Main Circuit Board from Interface Board.
5. Remove 2 screw (D).
6. Remove Interface Board from the chassis.

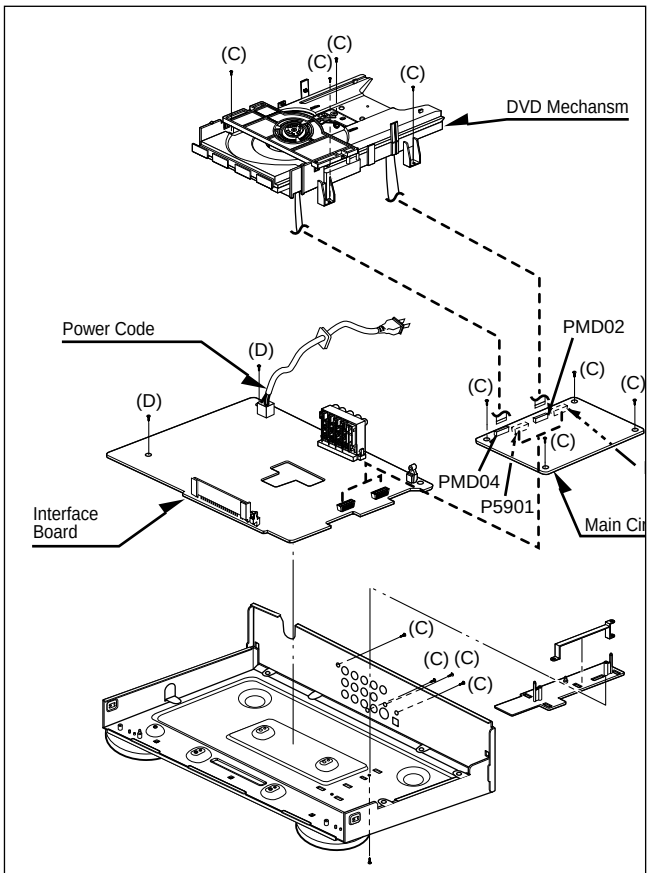


Fig. 2-4

2. Key1 and Key2 Circuit Board

1. Remove the front panel.(See Fig. 2-3)
2. Release 4 screws (E), and remove the Key1, 2 circuit board.

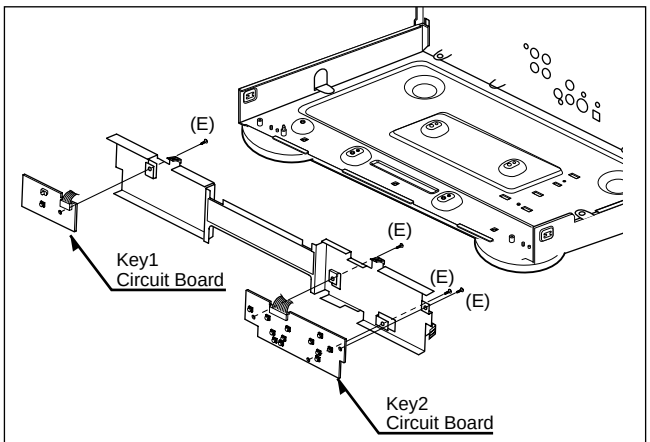


Fig. 2-5

ELECTRICAL MAIN PARTS LIST - 1/3

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
IC			
⚠	SI-SK6-153-00A		IC,STR-G6153T 5P<EXCEPT U>
	S2-309-024-040		SENSORLTV-817B PHOTO COU
	SI-SS4-310-00A		IC,KA431AZ
	SI-SS7-808-00H		IC,KA78R08 4P
	SI-SH3-130-00B		IC,PQ3RD13
	SI-HY2-580-10B		IC,GDC25D801C
	SI-JR3-414-00C		IC,NJM3414AM-TE1,3K/REEL
	87-017-856-080		IC,TC4W53FU
	SI-GL4-411-64A		IC,GLT441L16-40
	SI-TI3-337-21A		IC,SSI33P3721
	SI-FA3-032-00A		IC,KA3032
	SI-CU3-000-00A		IC,ZIVA3-PE0<HR>
	SI-CU4-100-00A		IC,ZIVA4.1<EXCEPT HR>
	SI-GS7-216-16C		ICGM72V161621ET-7
	SI-BB1-700-00A		IC,PLL1700E 20P
	SI-PH7-128-00A		IC,SAA7128<HR>
	87-A21-254-040		IC,BA7660FS<HR>
	SI-SH2-050-00A		IC,PQ20WZ5U 20WZ51
	SI-SA7-135-00A		IC,LA7135A<EXCEPT HR>
	SI-BB1-716-00A		IC,PCM1716E 28P
	SI-JR4-580-00B		IC,NJM4580M
	SI-TO7-040-00F		IC,TC7W04FU
	SI-CB5-331-00A		IC,CS5331A-KS<HR>
	SI-HI6-417-03B		IC,HD6417034AFI20
	SI-AL4-981-92B		IC,AT49F8192A-90TC
	SI-MQ5-316-25A		IC,V53C16256HK50
	SI-SS2-402-10A		IC,KS24C021CS
	SI-TI7-437-40K		IC,SN74AHC374PWLE
	SI-XL9-536-15B		IC,XC9536-15VQ44C-PROG
	SI-RH3-308-00A		IC,BA3308<HR>
	SI-KE4-558-00A		IC,KIA4558P<HR>
	SI-SA8-661-12C		IC,LC866112B-5N21
	87-001-196-010		IC,KIA7042P
TRANSISTOR			
⚠	ST-R44-190-0AA		TR,KTC4419<U>
	ST-R31-980-9AC		TR,KTC3198-TP-BL
	ST-R11-510-0AA		TR,KSB1151-Y
	ST-R10-370-9BB		C-TR,2SA1037K-Q
	87-A30-273-040		TR,DTC124EK
	89-324-122-080		TR,2SC2412KR
	ST-R15-040-9BF		TR,KTA1504S-Y<EXCEPT HR>
	ST-R15-050-9AD		TR,KTA1505S-Y
	ST-R10-000-9BM		TR,UMZ1N 3K
	87-026-609-080		TR,KTA1266-GR
	ST-R10-300-9AE		TR,KRC103M<K,EZ>
	ST-R10-500-9AB		TR,KRC105M
	ST-R10-500-9AD		TR,KRA105M
DIODE			
	87-A40-284-080		DIODE,ERA22-10<EXCEPT U>
	SD-D22-060-9AA		DIODE,ERA22-06<U>
	SD-D01-000-9AC		DIODE,EU01W
	87-020-465-080		DIODE,1SS133
	SD-R10-400-9AB		DIODE,RL104
	87-017-352-010		DIODE,RU3YXLF-C1 100V2
	SD-R18-020-9AA		DIODE,ERA18-02KFRB
	SD-R10-451-0AA		DIODE,B10A45V1
	SD-R15-402-0BA		DIODE,1N5402
	SD-R10-400-0AA		DIODE,RZ1040<U>
	87-020-331-080		DIODE,DAN202K
MAIN C.B			
C232	SC-H71-06C-611		C-CAP,10UF-6.3V
C271	SC-H71-06C-611		C-CAP,10UF-6.3V
C272	SC-H84-76C-611		C-CAP,47UF-6.3V
C274	SC-H84-76C-611		C-CAP,47UF-6.3V
C275	SC-H71-06C-611		C-CAP,10UF-6.3V
C276	SC-H71-06C-611		C-CAP,10UF-6.3V
C278	SC-H71-06C-611		C-CAP,10UF-6.3V
C279	SC-H71-06C-611		C-CAP,10UF-6.3V
C280	SC-H71-06C-611		C-CAP,10UF-6.3V
C281	SC-H71-06C-611		C-CAP,10UF-6.3V
C284	SC-H84-76C-611		C-CAP,47UF-6.3V
C2D1	SC-H84-76C-611		C-CAP,47UF-6.3V
C2D2	SC-H84-76C-611		C-CAP,47UF-6.3V
C2D3	SC-H84-76C-611		C-CAP,47UF-6.3V
C2D4	SC-H84-76C-611		C-CAP,47UF-6.3V
C2D5	SC-H71-06C-611		C-CAP,10UF-6.3V
C2M1	SC-H81-07F-611		C-CAP,100UF-16V
C340	SC-H71-06C-611		C-CAP,10UF-6.3V
C361	SC-H81-07F-611		C-CAP,100UF-16V<HR>
C362	87-A12-114-080		C-CAP,TN 22UF-6.3V<HR>
C363	SC-H81-07F-611		C-CAP,100UF-16V<HR>
C364	87-A12-114-080		C-CAP,TN 22UF-6.3V<HR>
C367	SC-H81-07F-611		C-CAP,100UF-16V<HR>
C368	87-A12-114-080		C-CAP,TN 22UF-6.3V<HR>
C369	SC-H81-07F-611		C-CAP,100UF-16V<HR>
C370	87-A12-114-080		C-CAP,TN 22UF-6.3V<HR>
C371	SC-H81-07F-611		C-CAP,100UF-16V<HR>
C372	87-A12-114-080		C-CAP,TN 22UF-6.3V<HR>
C375	SC-H81-07F-611		C-CAP,100UF-16V<EXCEPT HR>
C382	SC-H84-76C-611		C-CAP,47UF-6.3V<EXCEPT HR>
C383	SC-H84-76C-611		C-CAP,47UF-6.3V<EXCEPT HR>
C384	SC-H84-76C-611		C-CAP,47UF-6.3V<EXCEPT HR>
C406	SC-H81-07F-611		C-CAP,100UF-16V
C407	SC-H84-76C-611		C-CAP,47UF-6.3V
C409	SC-H84-76C-611		C-CAP,47UF-6.3V
C410	SC-H84-76C-611		C-CAP,47UF-6.3V
C419	SC-H84-76C-611		C-CAP,47UF-6.3V
C421	SC-H84-76C-611		C-CAP,47UF-6.3V
C429	SC-H81-07F-611		C-CAP,100UF-16V
C430	SC-H81-07F-611		C-CAP,100UF-16V
C536	SC-H71-06F-621		C-CAP,10UF-16V
L201	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L202	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L203	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L204	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L207	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L208	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L211	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L2A1	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L2A2	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L301	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L302	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L303	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L304	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L305	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L306	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L307	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L308	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L309	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT<HR>
L371	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT<EXCEPT HR>
L401	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L402	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L4M1	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT<HR>
L501	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L502	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L503	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L505	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L506	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
L507	S2-00H-JC1-02A		CER,FILTER HB-1M2012-102JT
P3901	S6-30R-BE0-340		CONN,BOAR2254-30S-T
P5502	S6-30H-XC1-15A		CONN,04-6232-115-008-800
P5901	S6-30R-BE0-340		CONN,BOAR2254-30S-T

ELECTRICAL MAIN PARTS LIST - 2/3

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
PMD02	S6-30R-FB0-2W0		CONN,04-6232-123-008-80
PMD03	S6-30R-FB0-2H0		CONN,04-6232-108-008-800
PMD04	S6-30R-3S0-06F		CONN,5P
X301	S2-02R-BL0-1A0		X'TAL,HC-49/SM5H
X501	S2-12S-AML-CB0		RESONATOR CSTCV20.00MXJ040-TC
INTERFACE C.B			
BC101	S6-360-04C-000		COIL,BFS3550R2FD8<EXCEPT U>
BD101	87-070-173-010		DIODE,S1WBA60
C100	87-010-408-040		CAP,E 47UF-50V<EXCEPT U>
⚠C101	S6-240-88F-000		CAP,PCX2 275V 0.1UF,M
⚠C102	S6-240-88F-000		CAP,PCX2 275V 0.1UF,M<EXCEPT U>
⚠C103	SC-E10-7CT-610		CAP,100UF-350V<U>
⚠C103	SC-E68-6CU-611		CAP,E 68UF-400V<EXCEPT U>
⚠C105	87-016-375-010		CAP,0.01UF-630V
⚠C106	S6-240-87B-000		CAP,100P-1KV
C111	87-010-403-040		CAP,E 3.3-50V<U>
⚠C114	87-012-379-010		CAP,3300PF-400V<EXCEPT U>
⚠C114	S6-240-86B-000		CAP,103-400V<U>
C116	87-010-387-010		CAP,E 470UF-25V KME
C118	87-010-112-080		CAP,E 100-16V
C119	87-010-408-040		CAP,E 47UF-50V
⚠C120	S6-240-86B-000		CAP,103-400V<U>
C121	SC-E22-76F-638		CAP,E 220UF-16V
⚠C122	SC-G33-10U-510		CAP,CER 330PF-400V<EXCEPT U>
C123	87-010-237-910		CAP,E 1000UF-16V
C124	87-010-237-910		CAP,E 1000UF-16V
C125	87-010-375-080		CAP,E 330-10V
C126	87-010-387-010		CAP,E 470UF-25V KME
C127	87-010-408-080		CAP,E 47-50V
C129	SC-E47-7CD-638		CAP,E 470UF-10V
C130	87-010-112-080		CAP,E 100-16V
C131	87-010-112-080		CAP,E 100-16V
C134	87-010-112-080		CAP,E 100-16V
C137	SC-E47-7CD-638		CAP,E 470UF-10V
C140	SC-E47-7CD-638		CAP,E 470UF-10V
C601	87-010-378-080		CAP,E 10-16V<EXCEPT HR>
C602	SC-E47-7CD-638		CAP,E 470UF-10V<EXCEPT HR>
C603	SC-E47-7CD-638		CAP,E 470UF-10V<EXCEPT HR>
C604	87-010-380-080		CAP,E 47-16V<K,EZ>
C663	SC-E47-7CD-638		CAP,E 470UF-10V<K,EZ>
C6Z1	SC-E47-7CD-638		CAP,E 470UF-10V<U>
C6Z2	SC-E47-7CD-638		CAP,E 470UF-10V<U>
C6Z3	SC-E47-7CD-638		CAP,E 470UF-10V<U>
C6Z4	SC-E47-7CD-638		CAP,E 470UF-10V<K,EZ>
C6Z5	SC-E47-7CD-638		CAP,E 470UF-10V<K,EZ>
C6Z6	SC-E47-7CD-638		CAP,E 470UF-10V<K,EZ>
C801	87-010-378-080		CAP,E 10-16V<HR>
C802	87-010-112-080		CAP,E 100-16V<HR>
C803	87-010-378-080		CAP,E 10-16V<HR>
C804	87-010-378-080		CAP,E 10-16V<HR>
C806	87-010-112-080		CAP,E 100-16V<HR>
C807	87-010-378-080		CAP,E 10-16V<HR>
C810	87-010-378-080		CAP,E 10-16V<HR>
C812	87-010-378-080		CAP,E 10-16V<HR>
C813	87-010-380-080		CAP,E 47-16V<HR>
C814	87-010-378-080		CAP,E 10-16V<HR>
C818	87-010-380-080		CAP,E 47-16V<HR>
C824	87-010-378-080		CAP,E 10-16V<HR>
C902	87-010-378-080		CAP,E 10-16V
C906	87-010-408-080		CAP,E 47-50V
C907	87-010-378-080		CAP,E 10-16V
C912	87-010-380-080		CAP,E 47-16V
C913	87-010-380-080		CAP,E 47-16V
C914	87-010-380-080		CAP,E 47-16V
DIG901	S3-02R-V10-3A0		DIGITRON 7-BT-273GN
⚠F101	S5-850-11T-000		FUSE,1600MA 250V<EXCEPT U>
⚠F101	S5-850-27B-000		FUSE,1600MA 250V<U>
⚠F102	87-001-196-010		ICP-N10 T104<EXCEPT U>

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
F602	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<EXCEPT HR>
F603	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF
F604	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF
F605	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<EXCEPT HR>
F606	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<EXCEPT HR>
F607	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<EXCEPT HR>
F608	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<U>
F609	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<U>
F610	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<U>
F611	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<K,EZ>
F612	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<EXCEPT HR>
F613	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<EXCEPT HR>
F614	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<K,EZ>
F615	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<K,EZ>
F616	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<K,EZ>
F617	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<K,EZ>
F618	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<K,EZ>
F619	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<K,EZ>
F620	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<K,EZ>
F621	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<K,EZ>
F622	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<K,EZ>
F801	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<HR>
F802	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<HR>
F803	S2-00H-JC9-01A		SAM,FILTER CFI06B1H101MF<HR>
⚠FH101	S5-860-08B-000		HOLDER,FUSE CLIP
⚠FH102	S5-860-08B-000		HOLDER,FUSE CLIP
JK601	S6-12R-L00-1A0		TOTX178 HORIZONTA JK
JK602	S6-12R-C00-6G0		JACK,RCA<HR,U>
JK602	S6-12R-C00-6H0		JACK,RCA<K,EZ>
JK603	S6-20R-M00-02B		SOCKET 1F-21P<K,EZ>
⚠L101	S6-161-45E-000		FILTER KSE-145E<U>
L101	S6-161-45H-000		FILTER SHT LFS2020V4-04350<EXCEPT U>
L102	S6-330-88G-000		COIL,CHOCK TP 5MM
L103	S6-330-88D-000		COIL,20UH
L602	87-005-208-080		COIL,100<K,EZ>
L902	87-005-208-080		COIL,100
LED901	SD-L32-531-9AA		LED SPR325MVWT31(GRN)
MJ801	S6-12R-B00-3A0		JACK,HEADPHONE<HR>
MJ802	S6-12R-B00-3A0		JACK,HEADPHONE<HR>
P6401	S6-30R-BE0-240		CONN,BOAR2254-30P-T
P9501	S6-30R-BE0-240		CONN,BOAR2254-30P-T
P9902	S5-617-11D-000		CONN,GIL-S-04P-S2T2-EF
P9904	S5-617-11L-000		CONN,12P
⚠PW101	S5-612-92B-000		GP390 LGC 3P STRAIG P
⚠R101	S6-140-07A-000		RES,CEM 2.7/2W
⚠R102	SR-S10-03K-619		RES,100K-2W<EXCEPT U>
⚠R104	SR-S33-02K-619		RES,M/F 33K-2W<U>
⚠R104	SR-S56-02K-619		RES,56K-2W<EXCEPT U>
R110	SR-S12-00J-619		RES,M/F 120-1W<U>
⚠R111	SR-S01-01K-619		RES,1-2W<U>
⚠R111	SR-S05-10K-619		RES,0.51-2W<EXCEPT U>
R122	SR-S12-00J-619		RES,M/F 120-1W
R144	SR-S12-00J-619		RES,M/F 120-1W<U>
RC901	S7-12R-193-8GA		REMOTE CONTROLLER RECEI
SW601	S6-00R-SH0-3A0		SW,SLIDE SKQ-23D15-G3-NA<EXCEPT U>
⚠T101	S6-420-21G-000		KSE-021G KWANG SUNG NARRO<U>
⚠T101	S6-420-23T-000		PT,SHT-023T/KSE-023T<EXCEPT U>
⚠V101	S6-560-04C-000		V SVC681D-10A
VR801	S1-10R-RK0-3A0		VOLUME,ROTARY 20KB<HR>
VR802	S1-10R-RK0-3A0		VOLUME,ROTARY 20KB<HR>
VR803	S1-10R-RK0-3A0		VOLUME,ROTARY 20KB<HR>
X901	S6-160-20P-000		CSA6.00MGU MURATA 6MHZ
ZD101	SD-Z56-260-9AA		ZENER,GDZJ5.6B 26MM TP
ZD102	SD-Z62-000-9BC		ZENER,MTZJ6.2B<U>
ZD605	SD-Z56-260-9AA		ZENER,GDZJ5.6B 26MM TP<EXCEPT HR>
ZD606	SD-Z56-260-9AA		ZENER,GDZJ5.6B 26MM TP<EXCEPT HR>
ZD635	SD-Z56-260-9AA		ZENER,GDZJ5.6B 26MM TP
ZD636	SD-Z56-260-9AA		ZENER,GDZJ5.6B 26MM TP
ZD637	SD-Z56-260-9AA		ZENER,GDZJ5.6B 26MM TP
ZD638	SD-Z56-260-9AA		ZENER,GDZJ5.6B 26MM TP

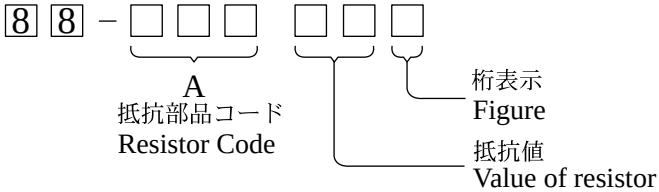
ELECTRICAL MAIN PARTS LIST - 3/3

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
ZD639	SD-Z56-260-9AA		ZENER,GDZJ5.6B 26MM TP<K,EZ>
ZD640	SD-Z56-260-9AA		ZENER,GDZJ5.6B 26MM TP<K,EZ>
KEY1 C.B			
P9901	S5-636-02R-000		CONN,4P
SW901	S5-562-19B-000		SW,SKHV10910B
KEY2 C.B			
P9903	S5-636-02S-000		CONN,12P
SW902	S5-562-19B-000		SW,SKHV10910B
SW903	S5-562-19B-000		SW,SKHV10910B
SW904	S5-562-19B-000		SW,SKHV10910B
SW905	S5-562-19B-000		SW,SKHV10910B
SW906	S5-562-19B-000		SW,SKHV10910B
SW907	S5-562-19B-000		SW,SKHV10910B
SW908	S5-562-19B-000		SW,SKHV10910B
SW910	S5-562-19B-000		SW,SKHV10910B
SW911	S5-562-19B-000		SW,SKHV10910B
SW912	S5-562-19B-000		SW,SKHV10910B
SW913	S5-562-19B-000		SW,SKHV10910B
SW914	S5-562-19B-000		SW,SKHV10910B

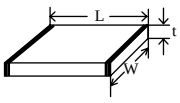
- Regarding connectors, they are not stocked as they are not the initial order items.
  The connectors are available after they are supplied from connector manufacturers upon the order is received.

○チップ抵抗部品コード／CHIP RESISTOR PART CODE

チップ抵抗部品コードの成り立ち
Chip Resistor Part Coding



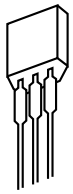
チップ抵抗
Chip resistor

容量 Wattage	種類 Type	許容誤差 Tolerance	記号 Symbol	寸法／Dimensions (mm) 外形／Form	L	W	t	抵抗コード : A Resistor Code : A
1/16W	1005	± 5%	CJ		1.0	0.5	0.35	104
1/16W	1608	± 5%	CJ		1.6	0.8	0.45	108
1/10W	2125	± 5%	CJ		2	1.25	0.45	118
1/8W	3216	± 5%	CJ		3.2	1.6	0.55	128

TRANSISTOR ILLUSTRATION

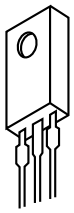
E C B

KTA1266
KTC3198



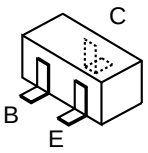
E C B

KTA1015
KTC103
KTC1015

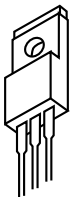


E C B

KSB1151

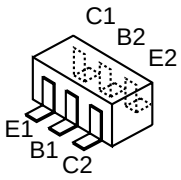


2SA1037
2SC2412
DTC124EK
KTA1504
KTA1505

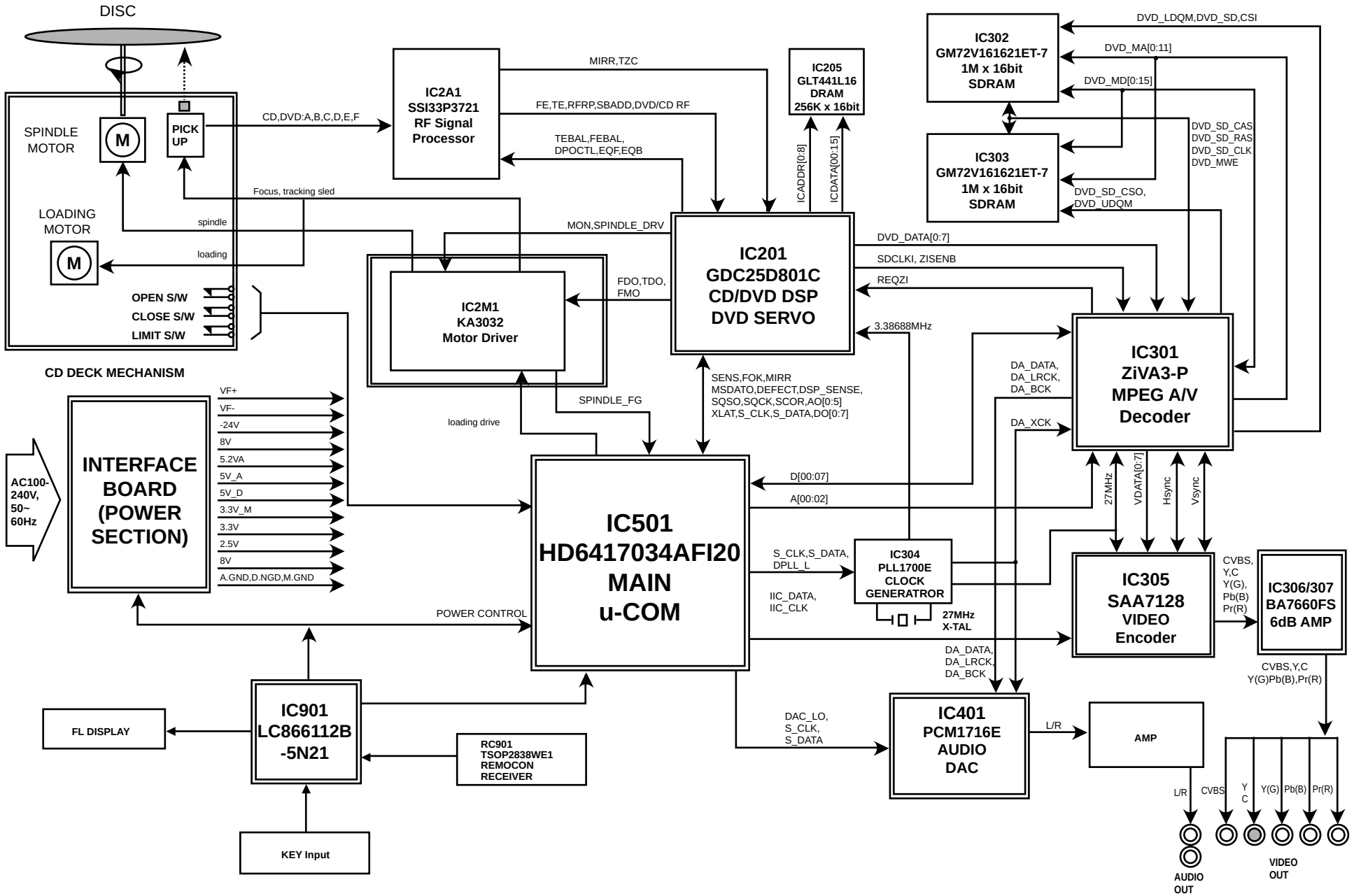


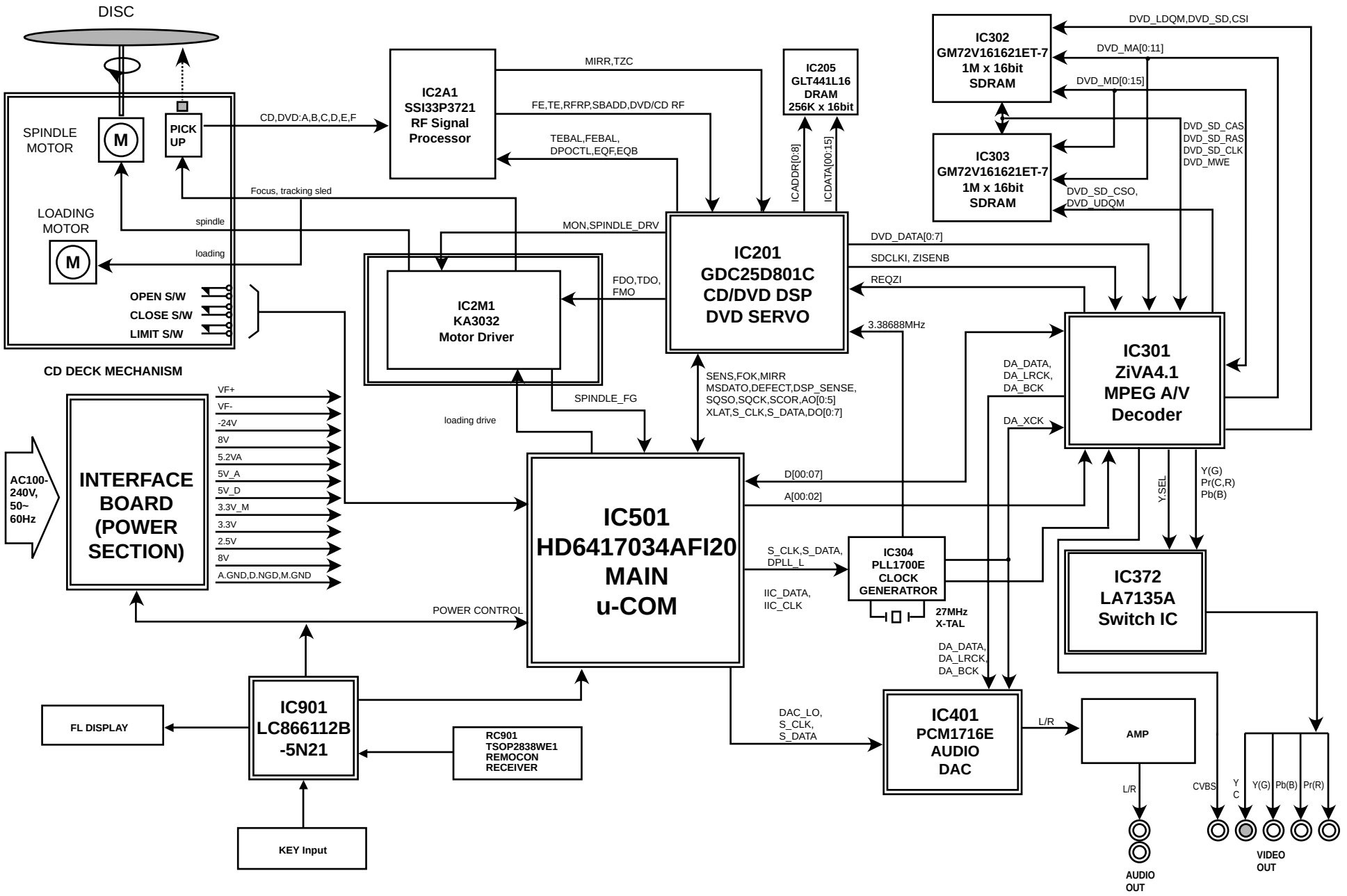
B C E

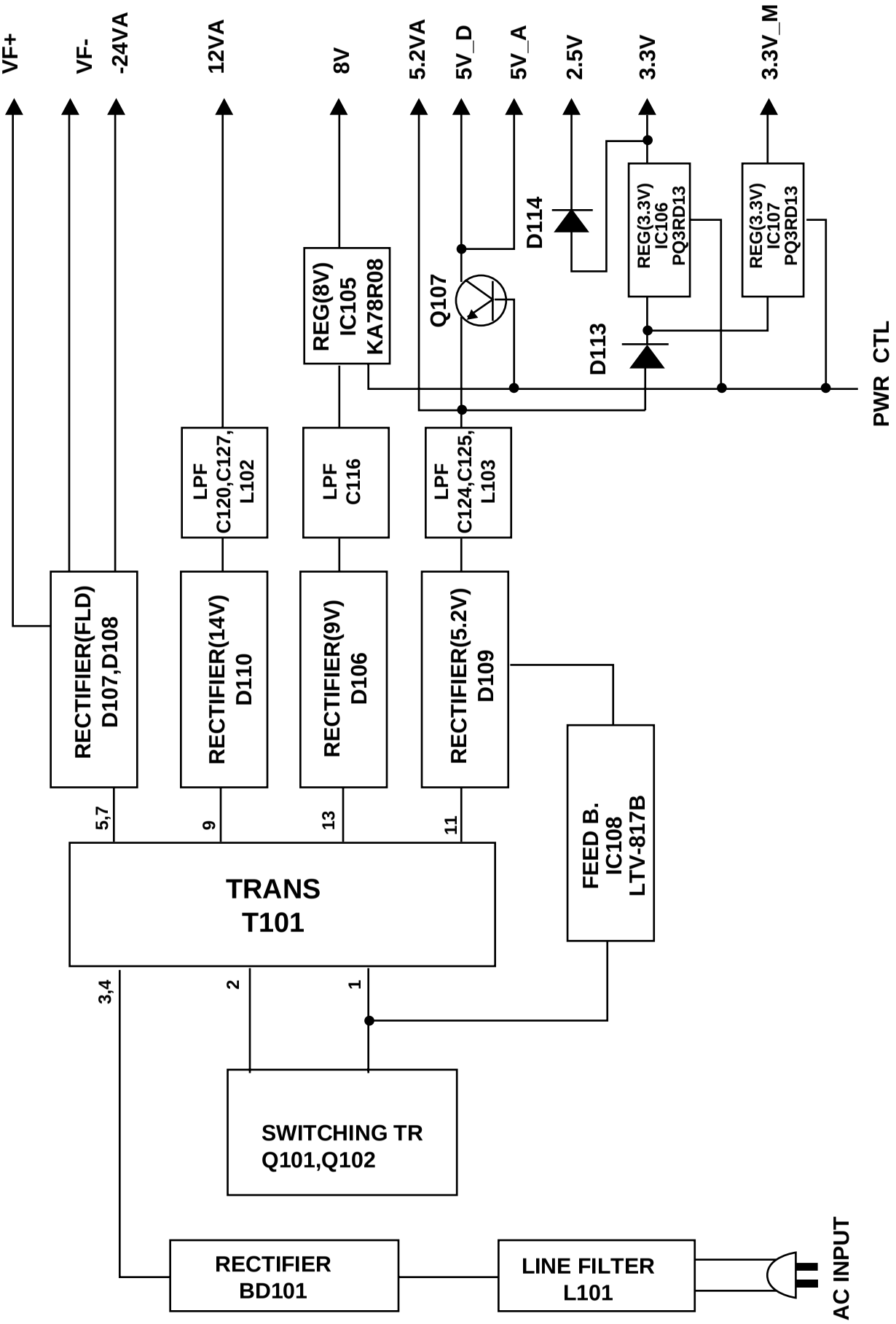
KTC4419



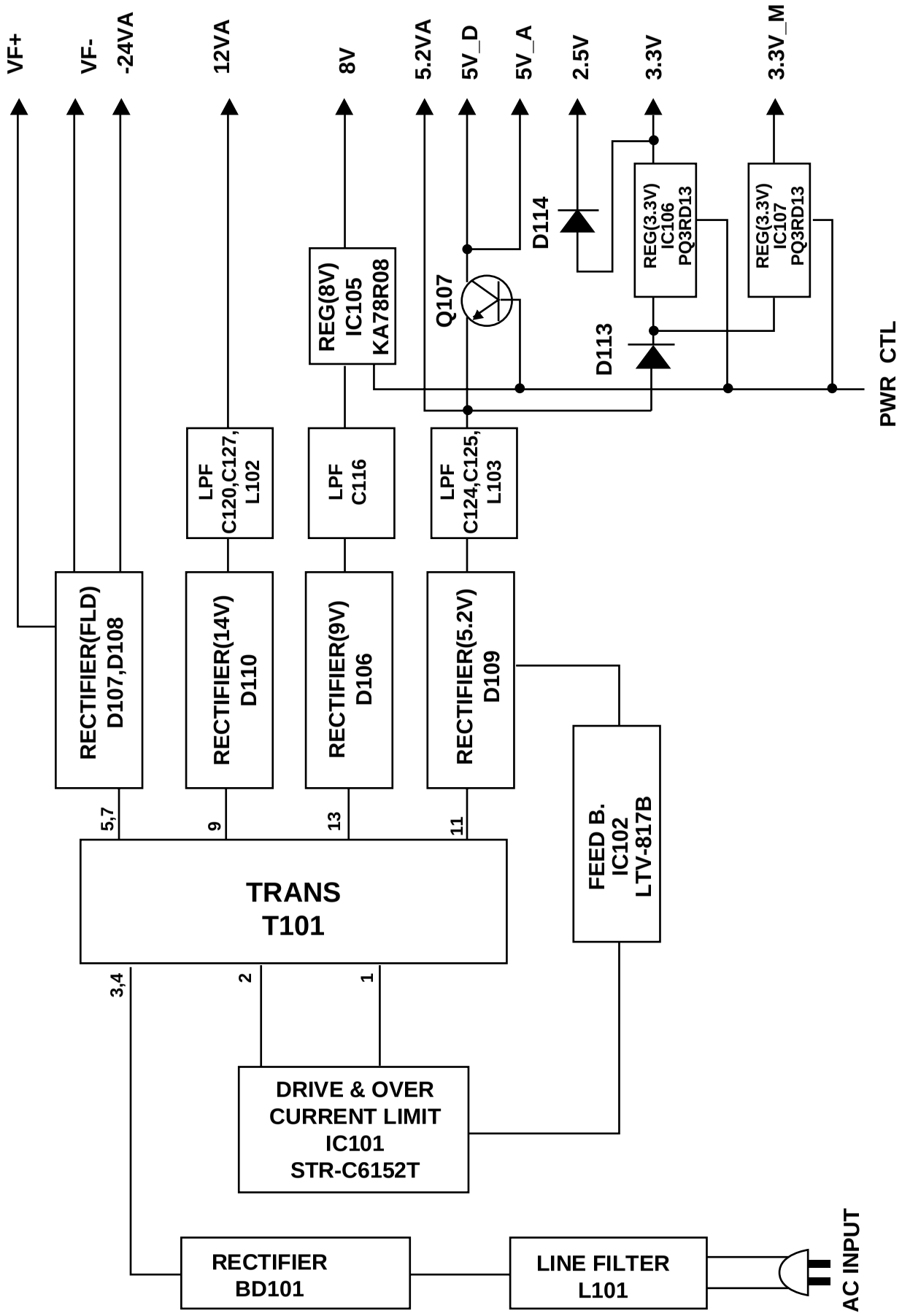
UMZ1N 3K


DISC
SPINDLE MOTOR
M
PICK UP
LOADING MOTOR
M
OPEN S/W
CLOSE S/W
LIMIT S/W
CD DECK MECHANISM
CD,DVD:A,B,C,D,E,F
Focus, tracking sled
spindle
loading
IC2A1
SSI33P3721
RF Signal
Processor
MIRR,TZC
FE,TE,RFRP,SBADD,DVD/CD RF
TEBAL,FEBAL,
DPOCTL,EQF,EQB
IC205
GLT441L16
DRAM
256K x 16bit
ICADDR[0:8]
ICDATA[00:15]
IC302
GM72V161621ET-7
1M x 16bit
SDRAM
IC303
GM72V161621ET-7
1M x 16bit
SDRAM
DVD_LDQM,DVD_SD,CSI
DVD_MA[0:11]
DVD_MD[0:15]
DVD_SD_CAS
DVD_SD_RAS
DVD_SD_CLK
DVD_MWE
DVD_SD_CSO,
DVD_UDQM
MON,SPINDLE_DRV
IC2M1
KA3032
Motor Driver
FDO,TDO,
FMO
IC201
GDC25D801C
CD/DVD DSP
DVD SERVO
DVD_DATA[0:7]
SDCLKI, ZISENB
REQZI
3.38688MHz
SENS,FOK,MIRR
MSDATO,DEFECT,DSP_SENSE,
SQSO,SQCK,SCOR,AO[0:5]
XLAT,S_CLK,S_DATA,DO[0:7]
SPINDLE_FG
loading drive
DA_DATA,
DA_LRCK,
DA_BCK
DA_XCK
IC301
ZiVA3-P
MPEG A/V
Decoder
AC100-240V, 50~60Hz
INTERFACE BOARD (POWER SECTION)
VF+
VF-
-24V
8V
5.2VA
5V_A
5V_D
3.3V_M
3.3V
2.5V
8V
A.GND,D.NGD,M.GND
IC501
HD6417034AFI20
MAIN
u-COM
D[00:07]
A[00:02]
27MHz
VDATA[0:7]
Hsync
Vsync
S_CLK,S_DATA,
DPLL_L
IIC_DATA,
IIC_CLK
IC304
PLL1700E
CLOCK
GENERATROR
27MHz
X-TAL
IC305
SAA7128
VIDEO
Encoder
CVBS,
Y,C
Y(G),
Pb(B)
Pr(R)
IC306/307
BA7660FS
6dB AMP
CVBS,Y,C
Y(G)Pb(B),Pr(R)
POWER CONTROL
DA_DATA,
DA_LRCK,
DA_BCK
IC901
LC866112B
-5N21
FL DISPLAY
RC901
TSOP2838WE1
REMOCON
RECEIVER
KEY Input
DAC_LO,
S_CLK,
S_DATA
IC401
PCM1716E
AUDIO
DAC
L/R
AMP
L/R
CVBS
Y
C
Y(G)
Pb(B)
Pr(R)
AUDIO OUT
VIDEO OUT

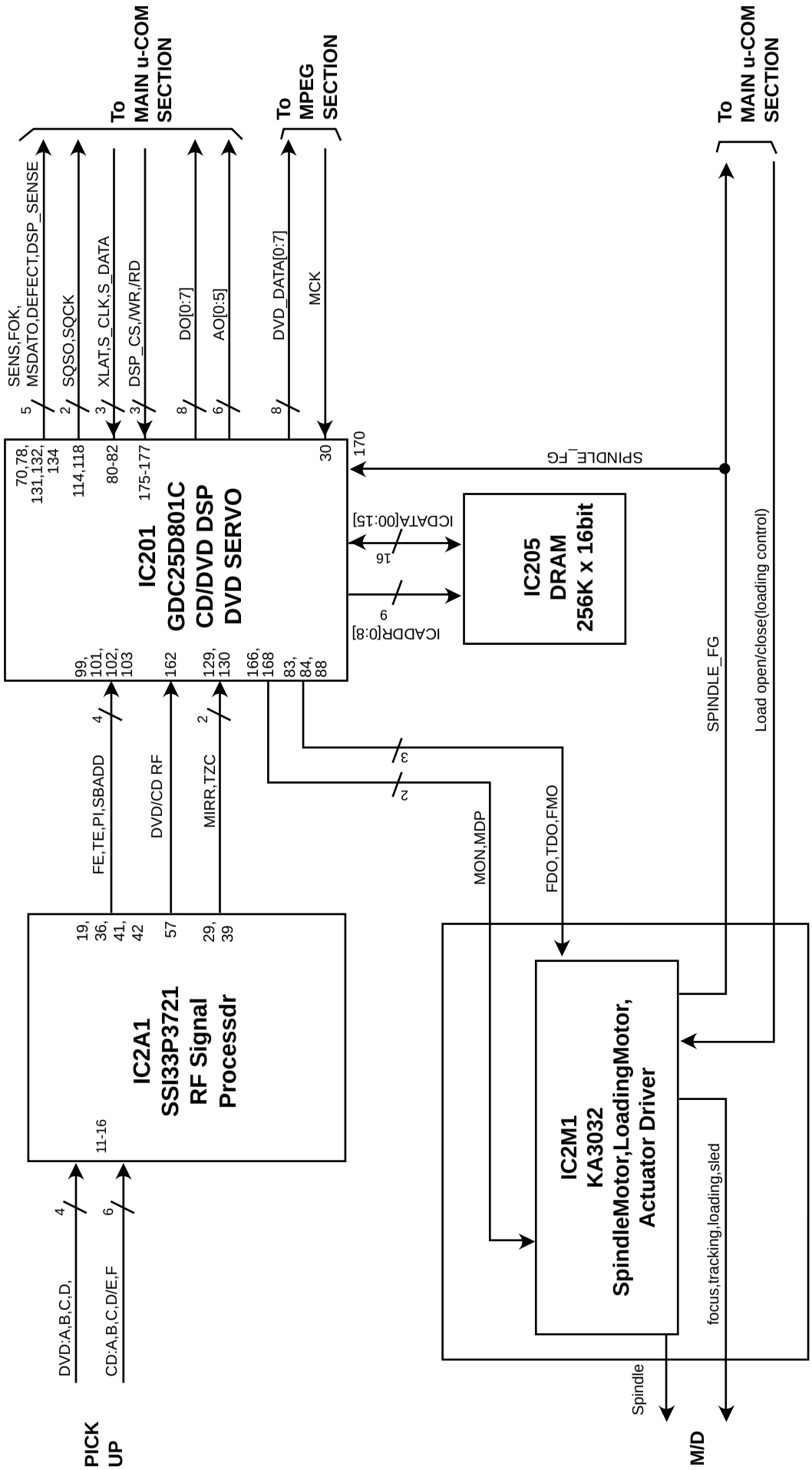

DISC
SPINDLE MOTOR
M
PICK UP
LOADING MOTOR
M
OPEN S/W
CLOSE S/W
LIMIT S/W
CD DECK MECHANISM
CD,DVD:A,B,C,D,E,F
IC2A1
SSI33P3721
RF Signal Processor
MIRR,TZC
FE,TE,RFRP,SBADD,DVD/CD RF
TEBAL,FEBAL,
DPOCTL,EQF,EQB
IC205
GLT441L16
DRAM
256K x 16bit
ICADDR[0:8]
ICDATA[00:15]
IC302
GM72V161621ET-7
1M x 16bit
SDRAM
IC303
GM72V161621ET-7
1M x 16bit
SDRAM
DVD_LDQM,DVD_SD,CSI
DVD_MA[0:11]
DVD_MD[0:15]
DVD_SD_CAS
DVD_SD_RAS
DVD_SD_CLK
DVD_MWE
DVD_SD_CSO,
DVD_UDQM
Focus, tracking sled
spindle
loading
MON,SPINDLE_DRV
IC201
GDC25D801C
CD/DVD DSP
DVD SERVO
DVD_DATA[0:7]
SDCLKI, ZISENB
REQZI
3.38688MHz
IC2M1
KA3032
Motor Driver
FDO,TDO,
FMO
SENS,FOK,MIRR
MSDATO,DEFECT,DSP_SENSE,
SQSO,SQCK,SCOR,AO[0:5]
XLAT,S_CLK,S_DATA,DO[0:7]
SPINDLE_FG
loading drive
IC301
ZiVA4.1
MPEG A/V
Decoder
DA_DATA,
DA_LRCK,
DA_BCK
DA_XCK
AC100-240V, 50~60Hz
INTERFACE BOARD (POWER SECTION)
VF+
VF-
-24V
8V
5.2VA
5V_A
5V_D
3.3V_M
3.3V
2.5V
8V
A.GND,D.NGD,M.GND
IC501
HD6417034AFI20
MAIN
u-COM
D[00:07]
A[00:02]
Y.SEL
Y(G)
Pr(C,R)
Pb(B)
S_CLK,S_DATA,
DPLL_L
IIC_DATA,
IIC_CLK
IC304
PLL1700E
CLOCK
GENERATROR
27MHz
X-TAL
IC372
LA7135A
Switch IC
POWER CONTROL
DA_DATA,
DA_LRCK,
DA_BCK
IC901
LC866112B
-5N21
FL DISPLAY
RC901
TSOP2838WE1
REMOCON
RECEIVER
KEY Input
DAC_LO,
S_CLK,
S_DATA
IC401
PCM1716E
AUDIO
DAC
L/R
AMP
L/R
AUDIO OUT
CVBS
Y
C
Y(G)
Pb(B)
Pr(R)
VIDEO OUT

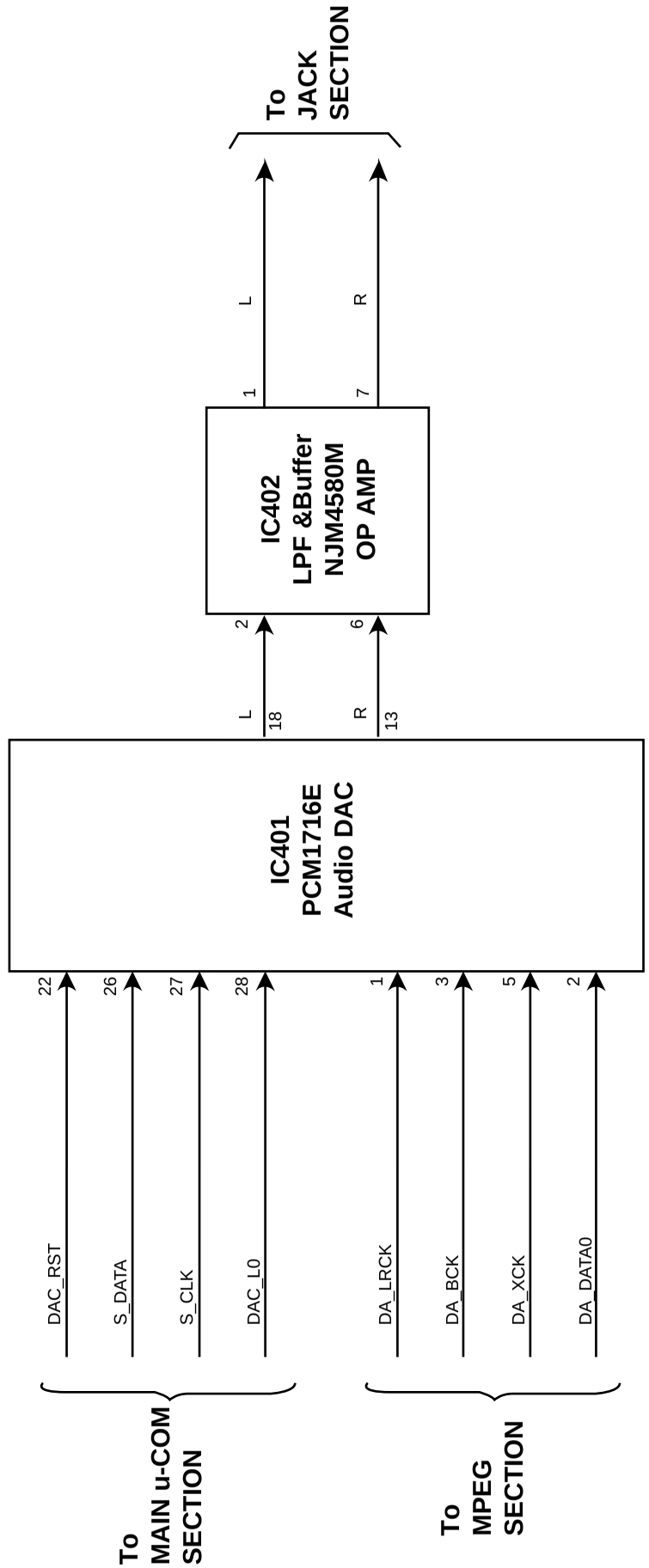

VF+
VF-
-24VA
12VA
8V
5.2VA
5V_D
5V_A
2.5V
3.3V
3.3V_M
D114
REG(3.3V)
IC106
PQ3RD13
REG(3.3V)
IC107
PQ3RD13
REG(8V)
IC105
KA78R08
Q107
D113
PWR CTL
LPF
C120,C127,
L102
LPF
C116
LPF
C124,C125,
L103
RECTIFIER(FLD)
D107,D108
RECTIFIER(14V)
D110
RECTIFIER(9V)
D106
RECTIFIER(5.2V)
D109
FEED B.
IC108
LTV-817B
5,7
9
13
11
TRANS
T101
3,4
2
1
SWITCHING TR
Q101,Q102
RECTIFIER
BD101
LINE FILTER
L101
AC INPUT

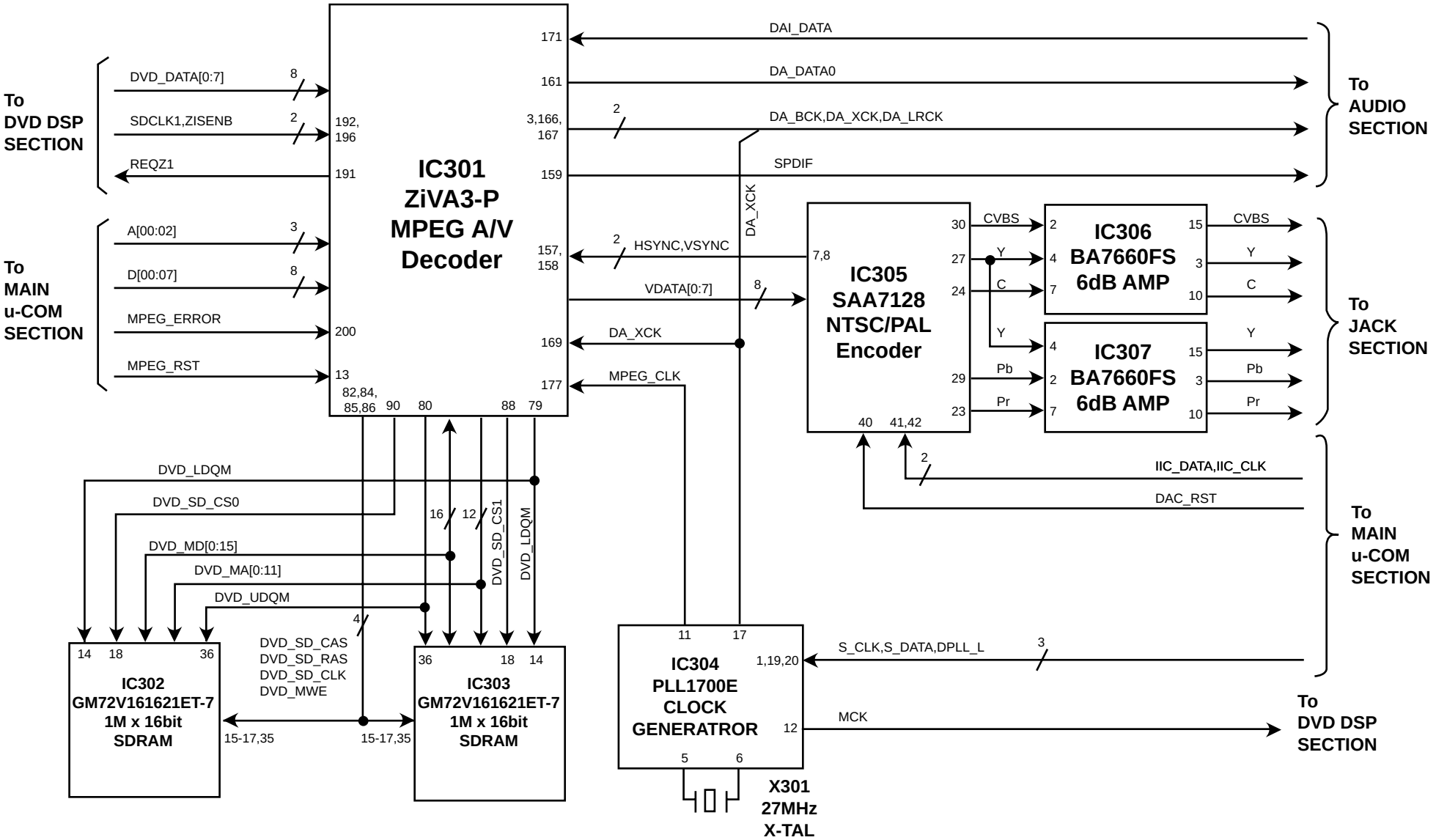
BLOCK DIAGRAM - 4 (POWER) <Except U>

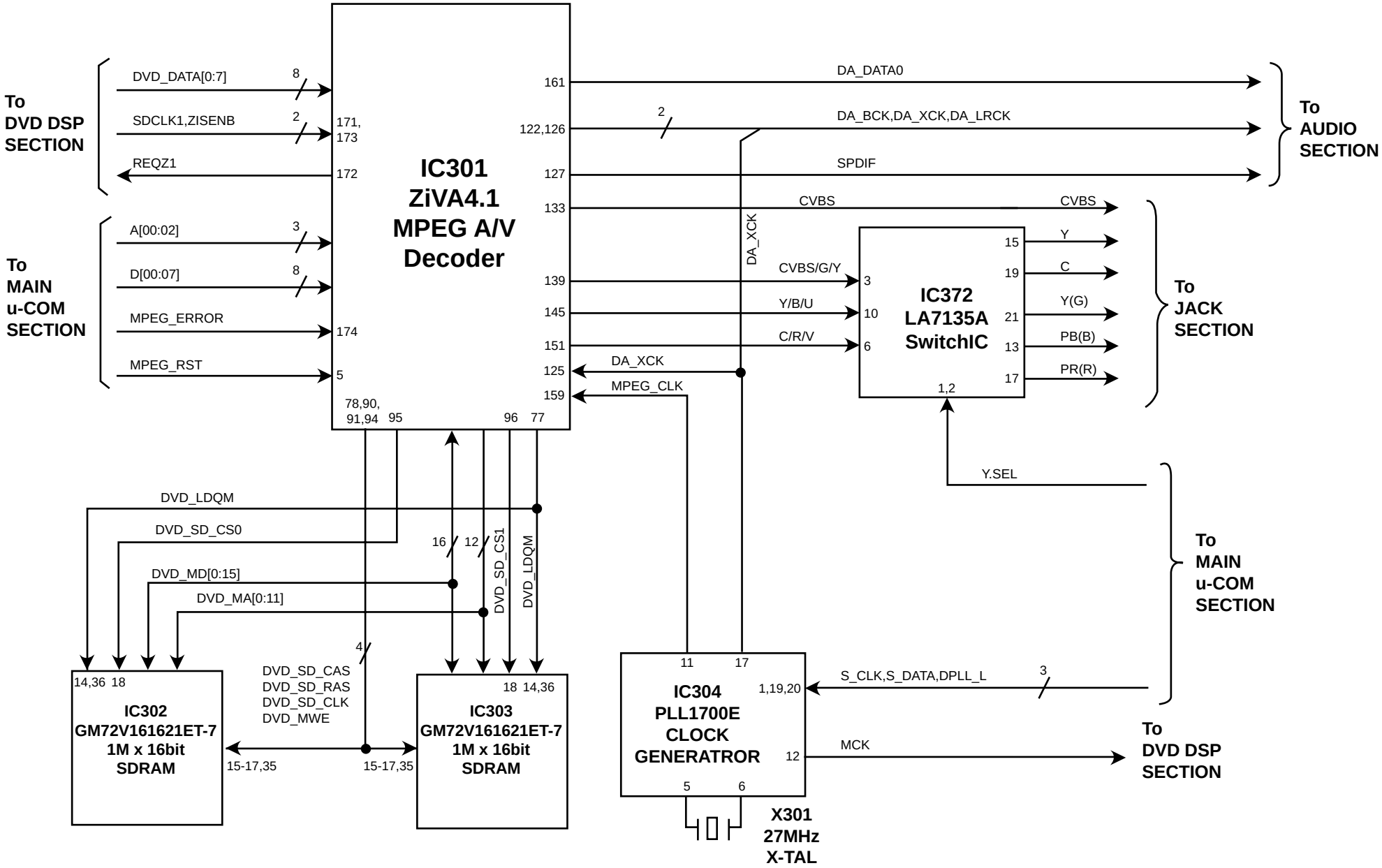


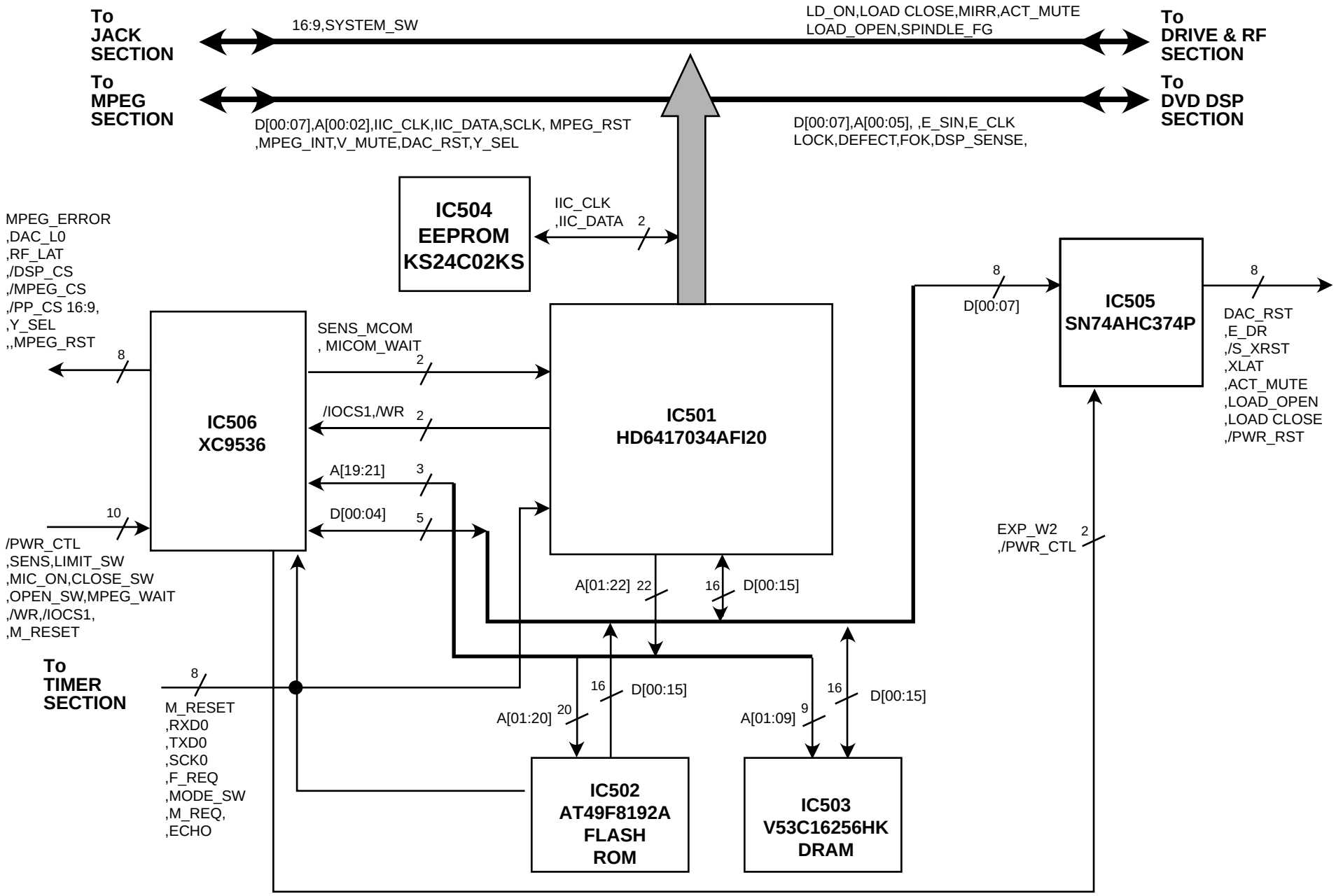
BLOCK DIAGRAM - 5 (RF/CD DSP/DVD SERVO)

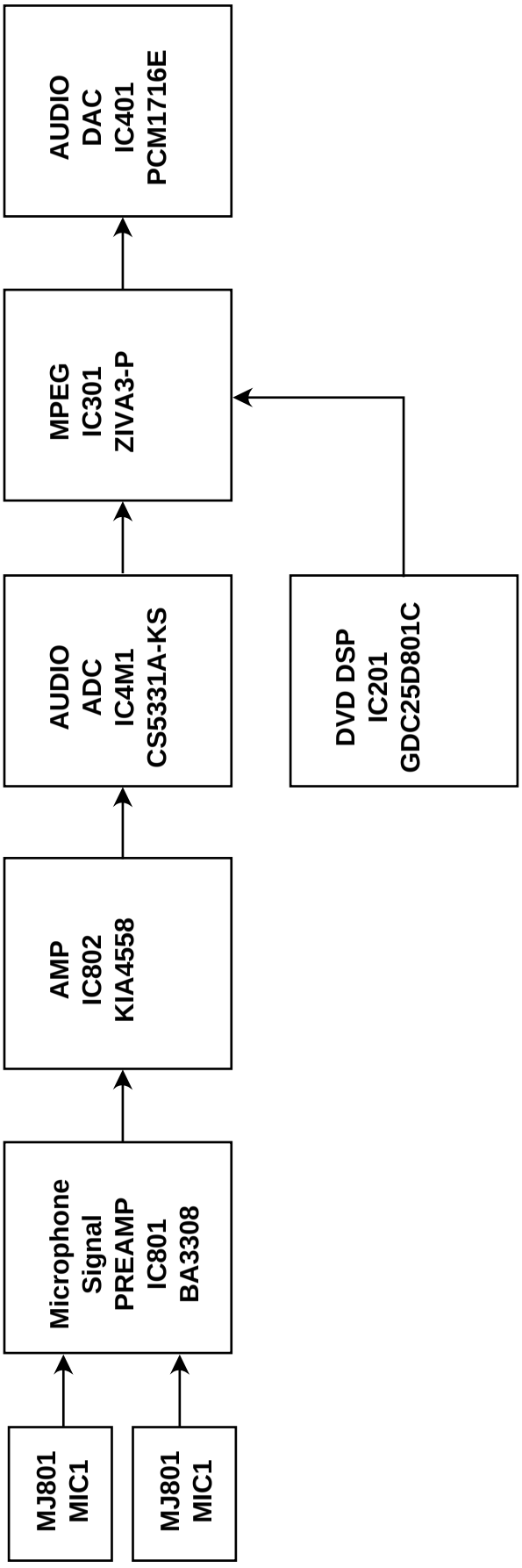



To
JACK
SECTION
IC402
LPF &Buffer
NJM4580M
OP AMP
IC401
PCM1716E
Audio DAC
To
MAIN u-COM
SECTION
To
MPEG
SECTION
DAC_RST
S_DATA
S_CLK
DAC_L0
DA_LRCK
DA_BCK
DA_XCK
DA_DATA0
L
R

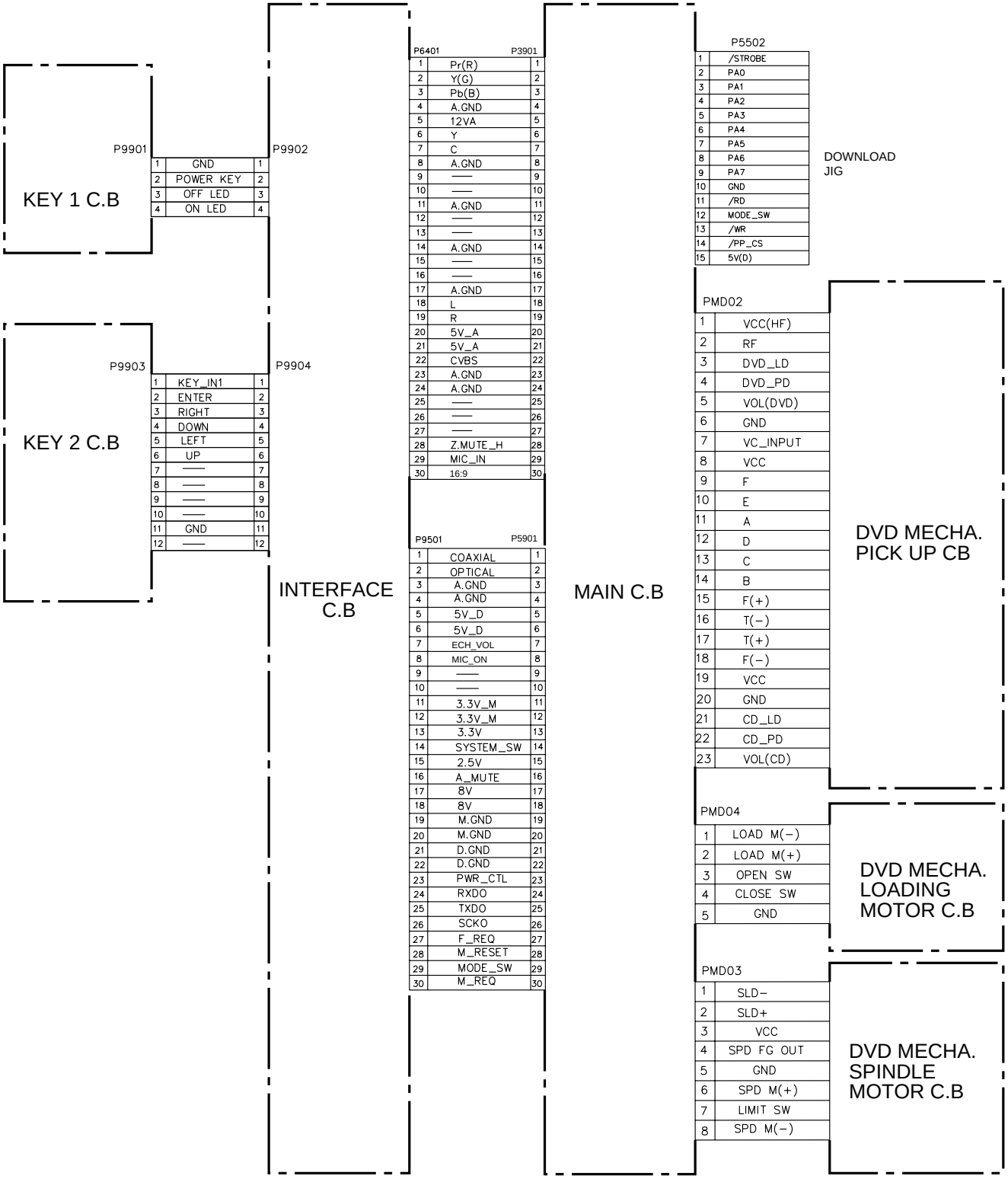

To DVD DSP SECTION
DVD_DATA[0:7]
SDCLK1,ZISENB
REQZ1
To MAIN u-COM SECTION
A[00:02]
D[00:07]
MPEG_ERROR
MPEG_RST
IC301 ZiVA3-P MPEG A/V Decoder
DAI_DATA
DA_DATA0
DA_BCK,DA_XCK,DA_LRCK
SPDIF
HSYNC,VSYNC
VDATA[0:7]
DA_XCK
MPEG_CLK
IC305 SAA7128 NTSC/PAL Encoder
CVBS
Y
C
Pb
Pr
IC306 BA7660FS 6dB AMP
IC307 BA7660FS 6dB AMP
To AUDIO SECTION
To JACK SECTION
IIC_DATA,IIC_CLK
DAC_RST
To MAIN u-COM SECTION
DVD_LDQM
DVD_SD_CS0
DVD_MD[0:15]
DVD_MA[0:11]
DVD_UDQM
DVD_SD_CS1
DVD_SD_CAS
DVD_SD_RAS
DVD_SD_CLK
DVD_MWE
IC302 GM72V161621ET-7 1M x 16bit SDRAM
IC303 GM72V161621ET-7 1M x 16bit SDRAM
15-17,35
IC304 PLL1700E CLOCK GENERATROR
S_CLK,S_DATA,DPLL_L
MCK
To DVD DSP SECTION
X301 27MHz X-TAL


To
DVD DSP
SECTION
DVD_DATA[0:7]
8
SDCLK1,ZISENB
2
REQZ1
To
MAIN
u-COM
SECTION
A[00:02]
3
D[00:07]
8
MPEG_ERROR
MPEG_RST
IC301
ZiVA4.1
MPEG A/V
Decoder
171,
173
172
174
5
78,90,
91,94
95
96
77
161
122,126
127
133
139
145
151
125
159
DA_DATA0
DA_BCK,DA_XCK,DA_LRCK
SPDIF
CVBS
CVBS/G/Y
Y/B/U
C/R/V
DA_XCK
MPEG_CLK
DA_XCK
To
AUDIO
SECTION
IC372
LA7135A
SwitchIC
3
10
6
1,2
15
19
21
13
17
CVBS
Y
C
Y(G)
PB(B)
PR(R)
To
JACK
SECTION
Y.SEL
DVD_LDQM
DVD_SD_CS0
DVD_MD[0:15]
DVD_MA[0:11]
16
12
DVD_SD_CS1
DVD_LDQM
4
DVD_SD_CAS
DVD_SD_RAS
DVD_SD_CLK
DVD_MWE
14,36 18
IC302
GM72V161621ET-7
1M x 16bit
SDRAM
15-17,35
15-17,35
18 14,36
IC303
GM72V161621ET-7
1M x 16bit
SDRAM
11
17
IC304
PLL1700E
CLOCK
GENERATROR
1,19,20
12
5
6
X301
27MHz
X-TAL
S_CLK,S_DATA,DPLL_L
3
To
MAIN
u-COM
SECTION
MCK
To
DVD DSP
SECTION

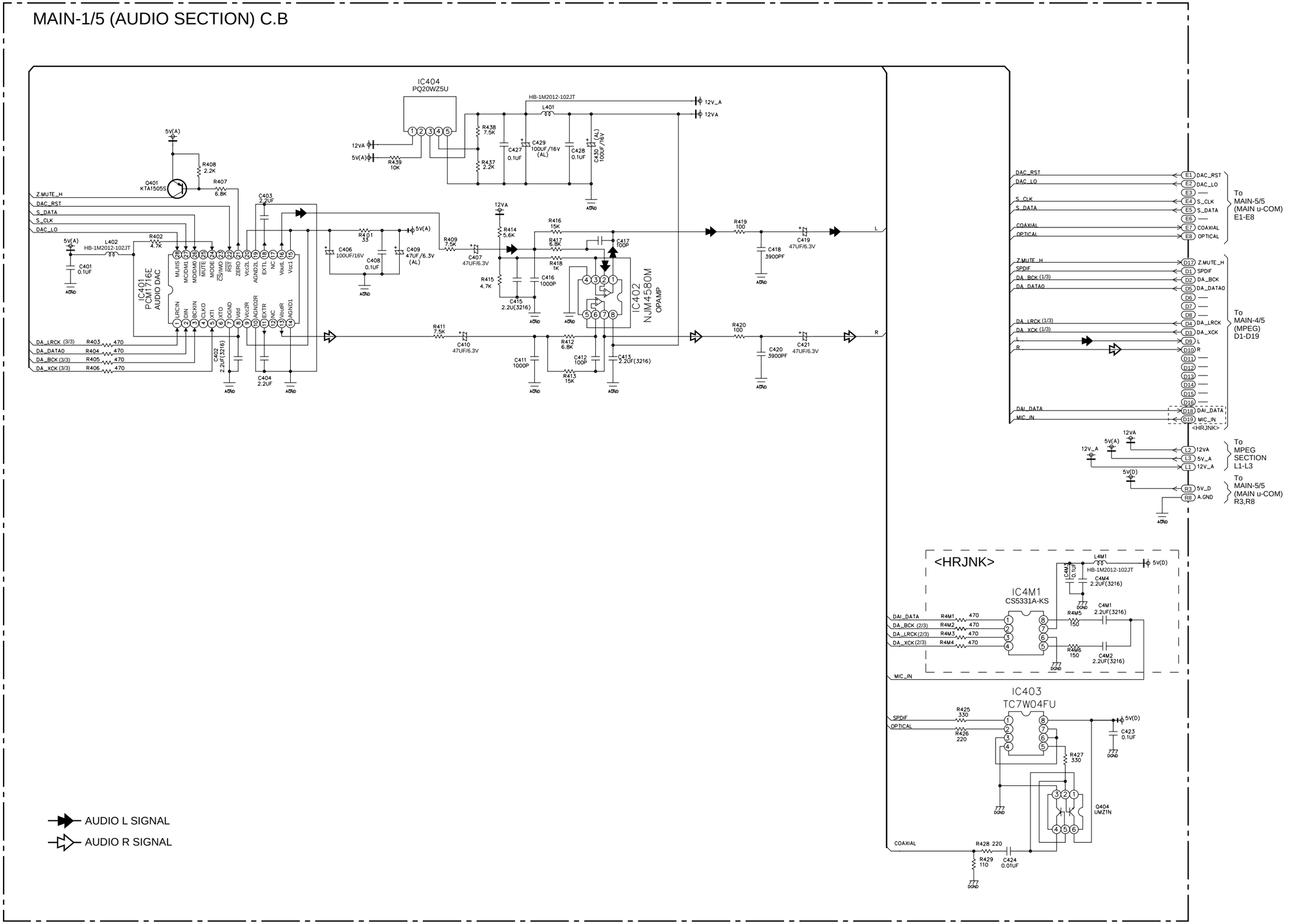

To JACK SECTION
16:9,SYSTEM_SW
LD_ON,LOAD CLOSE,MIRR,ACT_MUTE
LOAD_OPEN,SPINDLE_FG
To DRIVE & RF SECTION
To MPEG SECTION
D[00:07],A[00:02],IIC_CLK,IIC_DATA,SCLK, MPEG_RST
,MPEG_INT,V_MUTE,DAC_RST,Y_SEL
D[00:07],A[00:05], ,E_SIN,E_CLK
LOCK,DEFECT,FOK,DSP_SENSE,
To DVD DSP SECTION
IC504
EEPROM
KS24C02KS
IIC_CLK
,IIC_DATA 2
MPEG_ERROR
,DAC_L0
,RF_LAT
,/DSP_CS
,/MPEG_CS
,/PP_CS 16:9,
,Y_SEL
,,MPEG_RST
8
IC506
XC9536
SENS_MCOM
, MICOM_WAIT
2
/IOCS1,/WR 2
A[19:21] 3
D[00:04] 5
IC501
HD6417034AFI20
8
D[00:07]
IC505
SN74AHC374P
8
DAC_RST
,E_DR
,/S_XRST
,XLAT
,ACT_MUTE
,LOAD_OPEN
,LOAD CLOSE
,/PWR_RST
10
/PWR_CTL
,SENS,LIMIT_SW
,MIC_ON,CLOSE_SW
,OPEN_SW,MPEG_WAIT
,/WR,/IOCS1,
,M_RESET
A[01:22] 22
16 D[00:15]
EXP_W2 2
,/PWR_CTL
To TIMER SECTION
8
M_RESET
,RXD0
,TXD0
,SCK0
,F_REQ
,MODE_SW
,M_REQ,
,ECHO
A[01:20] 20
16 D[00:15]
A[01:09] 9
16 D[00:15]
IC502
AT49F8192A
FLASH
ROM
IC503
V53C16256HK
DRAM


AUDIO
DAC
IC401
PCM1716E
MPEG
IC301
ZIVA3-P
AUDIO
ADC
IC4M1
CS5331A-KS
DVD DSP
IC201
GDC25D801C
AMP
IC802
KIA4558
Microphone
Signal
PREAMP
IC801
BA3308
MJ801
MIC1
MJ801
MIC1

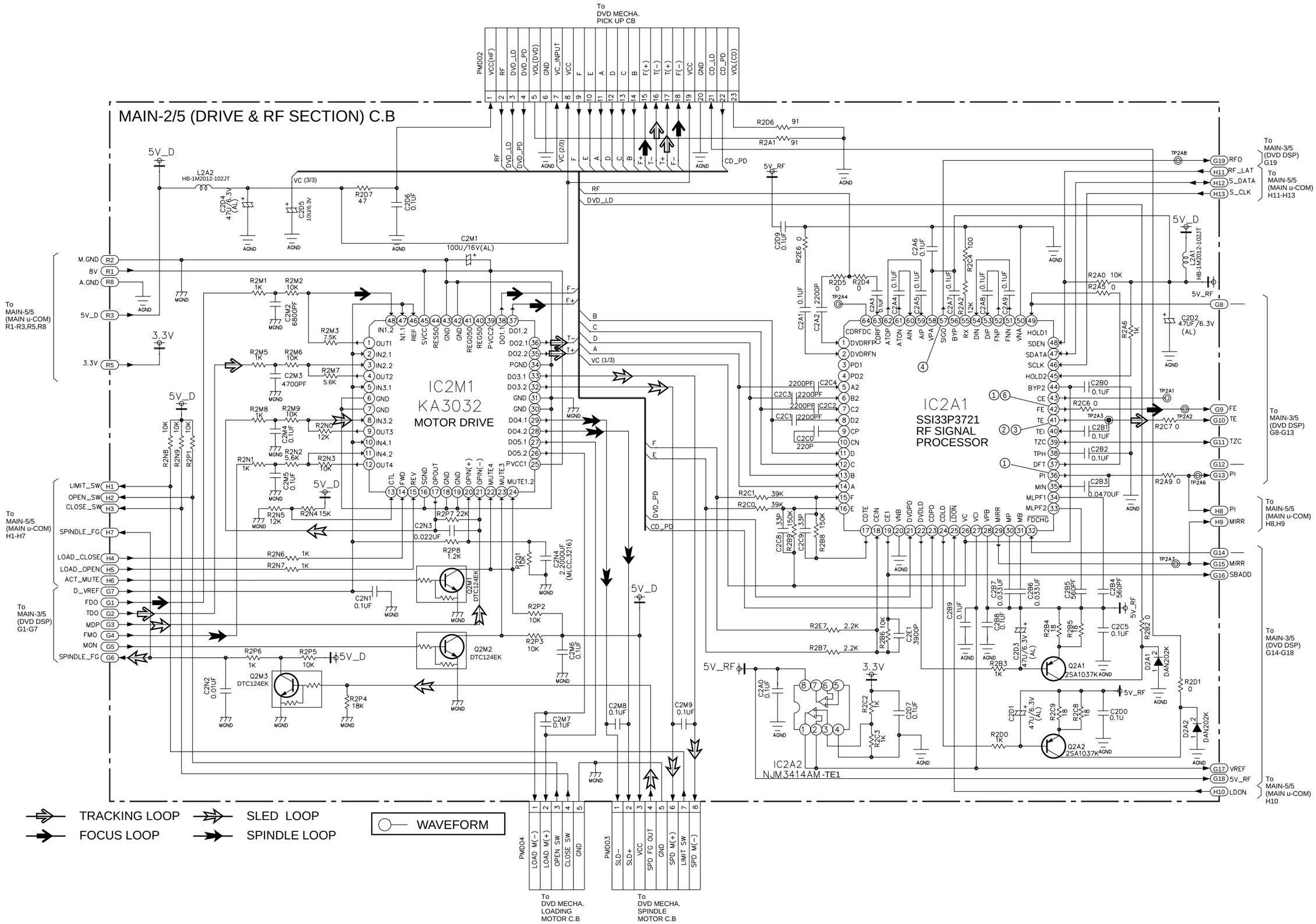
WIRE HARNESS DIAGRAM



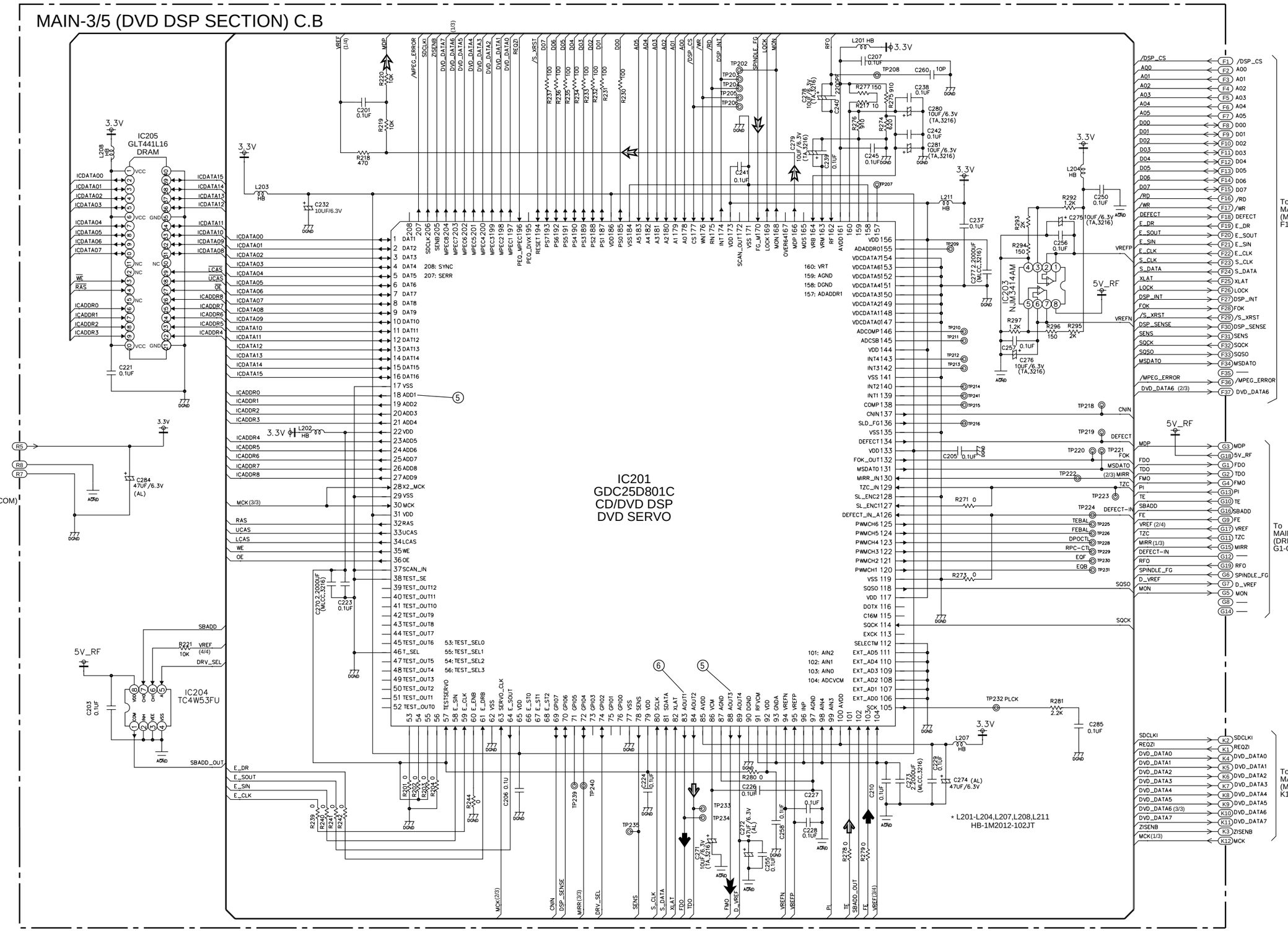
MAIN-1/5 (AUDIO SECTION) C.B



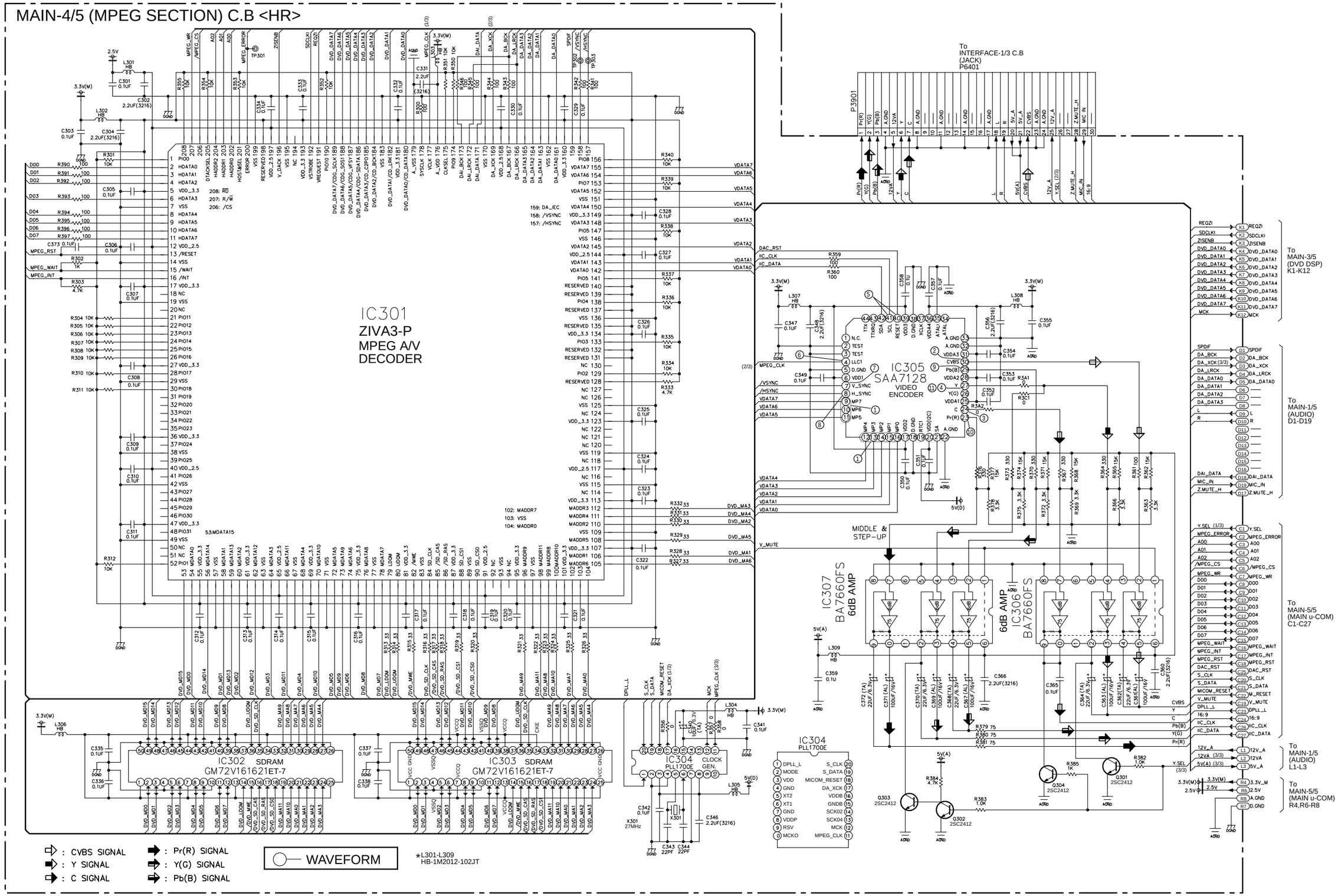
SCHEMATIC DIAGRAM - 2 (MAIN -2/5, DRIVE & RF SECTION)



SCHEMATIC DIAGRAM - 3 (MAIN -3/5, DVD DSP SECTION)



MAIN-4/5 (MPEG SECTION) C.B <HR>



MAIN-4/5 (MPEG SECTION) C.B <U, K, EZ>

IC301
ZIVA4.1
MPEG A/V
DECODER

IC302 SDRAM GM72V161621ET-7

IC303 SDRAM GM72V161621ET-7

IC304 PLL1700E CLOCK GEN.

IC371
PQ20WZ5U

IC372
LA7135A
SWITCH

IC304
PLL1700E

To
INTERFACE-1/3 C.B
(JACK)
P6401

To
MAIN-3/5
(DVD DSP)
K1-K12

To
MAIN-1/5
(AUDIO)
D1-D17

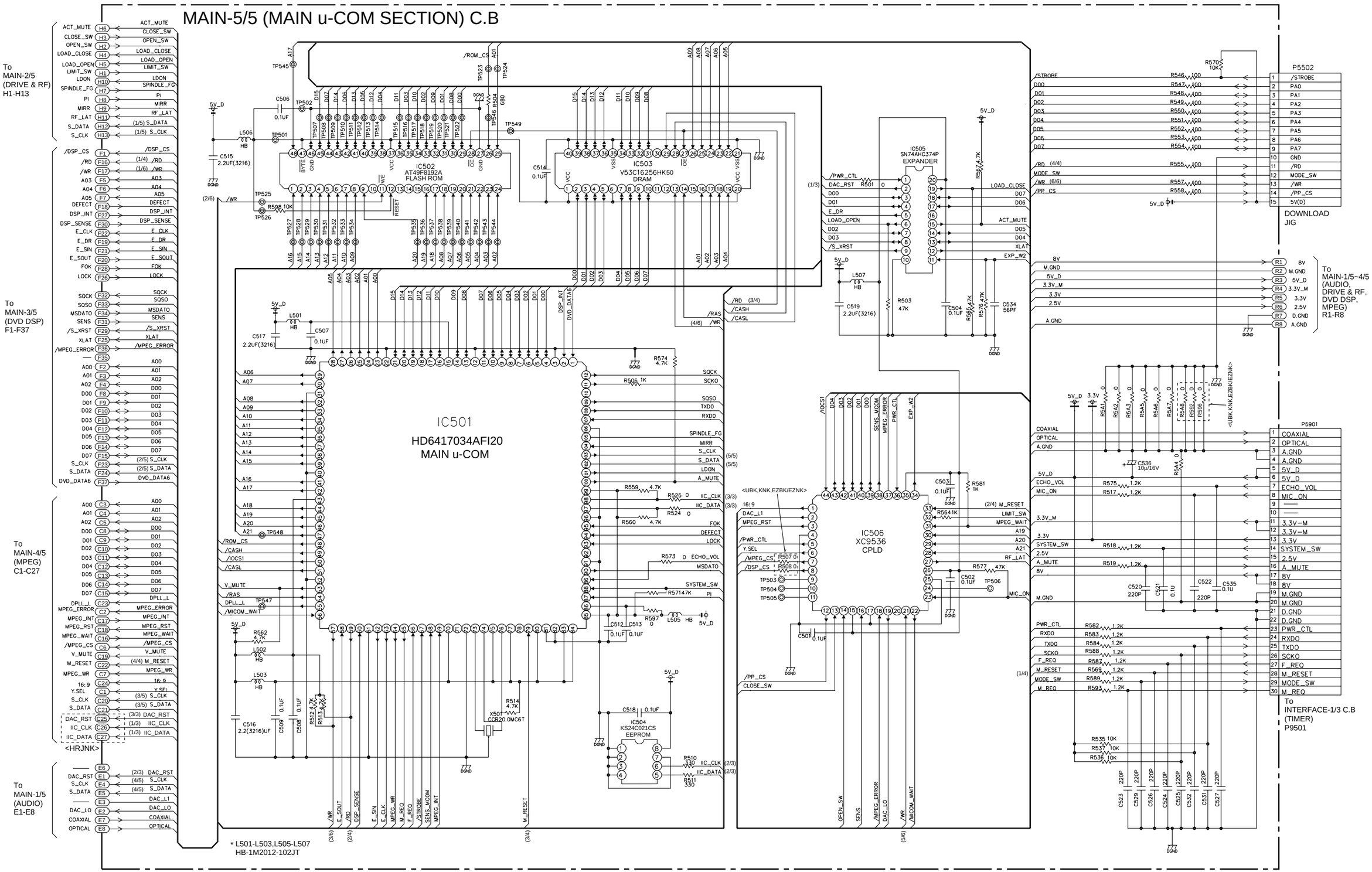
To
MAIN-5/5
(MAIN u-COM)
C1-C24

To
MAIN-1/5
(AUDIO)
L1-L3

To
MAIN-5/5
(MAIN u-COM)
R4,R6-R8

*L301-L308,L371
HB-1M2012-102JT

: CVBS SIGNAL
: Y SIGNAL
: C SIGNAL
: Pr(R) SIGNAL
: Y(G) SIGNAL
: Pb(B) SIGNAL

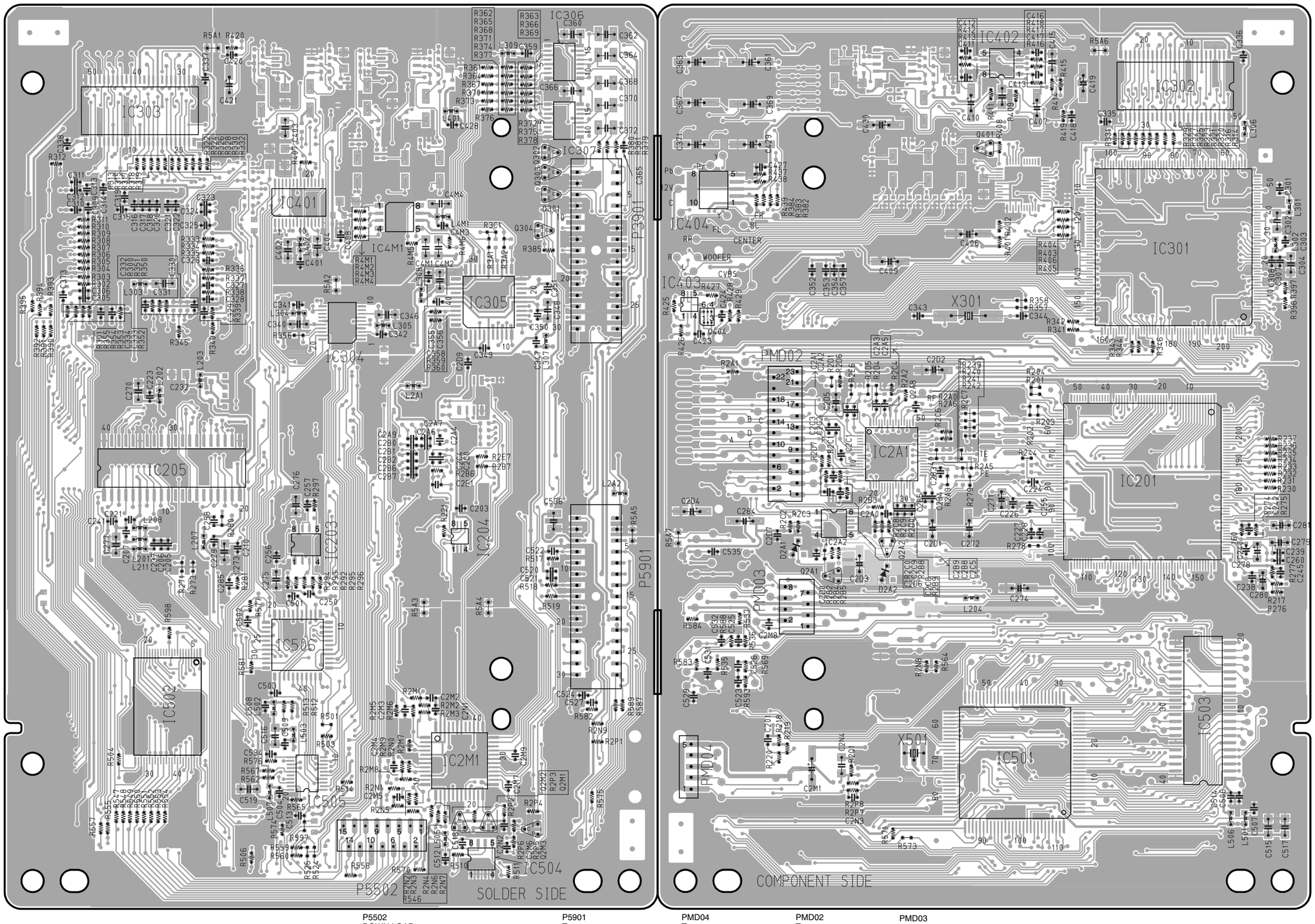

MAIN-5/5 (MAIN u-COM SECTION) C.B
IC501
HD6417034AFI20
MAIN u-COM
IC502
AT49F8192A
FLASH ROM
IC503
V53C16256HK50
DRAM
IC504
KS24C021CS
EEPROM
IC505
SN74AHC374P
EXPANDER
IC506
XC9536
CPLD
DOWNLOAD
JIG
P5502
P5901
To
MAIN-2/5
(DRIVE & RF)
H1-H13
To
MAIN-3/5
(DVD DSP)
F1-F37
To
MAIN-4/5
(MPEG)
C1-C27
To
MAIN-1/5
(AUDIO)
E1-E8
To
MAIN-1/5~4/5
(AUDIO,
DRIVE & RF,
DVD DSP,
MPEG)
R1-R8
To
INTERFACE-1/3 C.B
(TIMER)
P9501
<HRJNK>
<UBK,KNK,EZBK/EZNK>
* L501-L503,L505-L507
HB-1M2012-102JT

32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

A B C D E F G H I J K L M N O P Q R S T U

MAIN C.B <HR>

P3901
To
INTERFACE C.B
P6401



P5502
DOWN LOAD
JIG

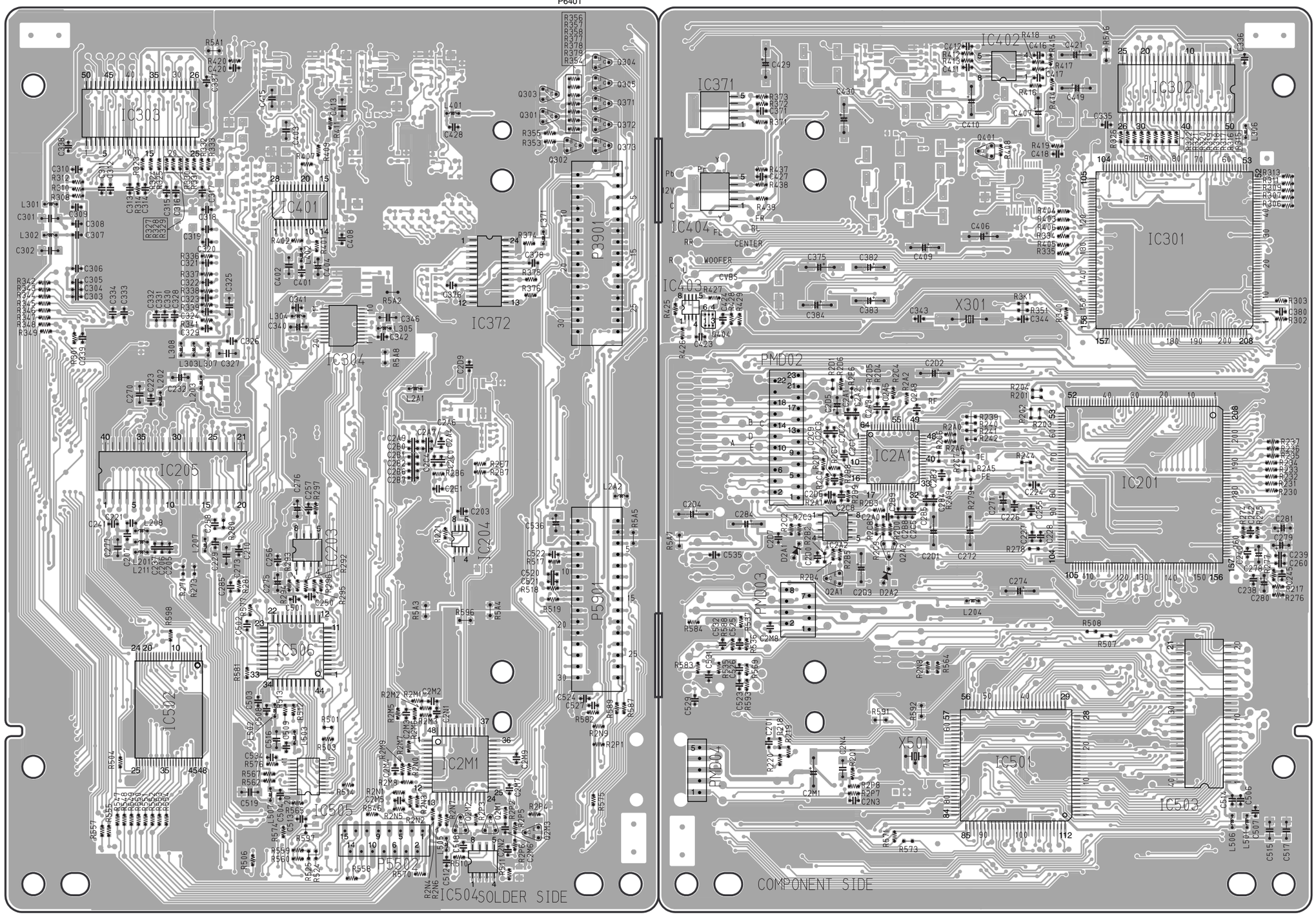
P5901
To
INTERFACE C.B
P9501

PMD04
To
DVD MECHA.
LOADING
MOTOR C.B

PMD02
To
DVD MECHA.
PICK UP C.B

PMD03
To
DVD MECHA.
SPINDLE
MOTOR C.B

MAIN C.B <U, K, EZ>



P5502
DOWN LOAD
JIG

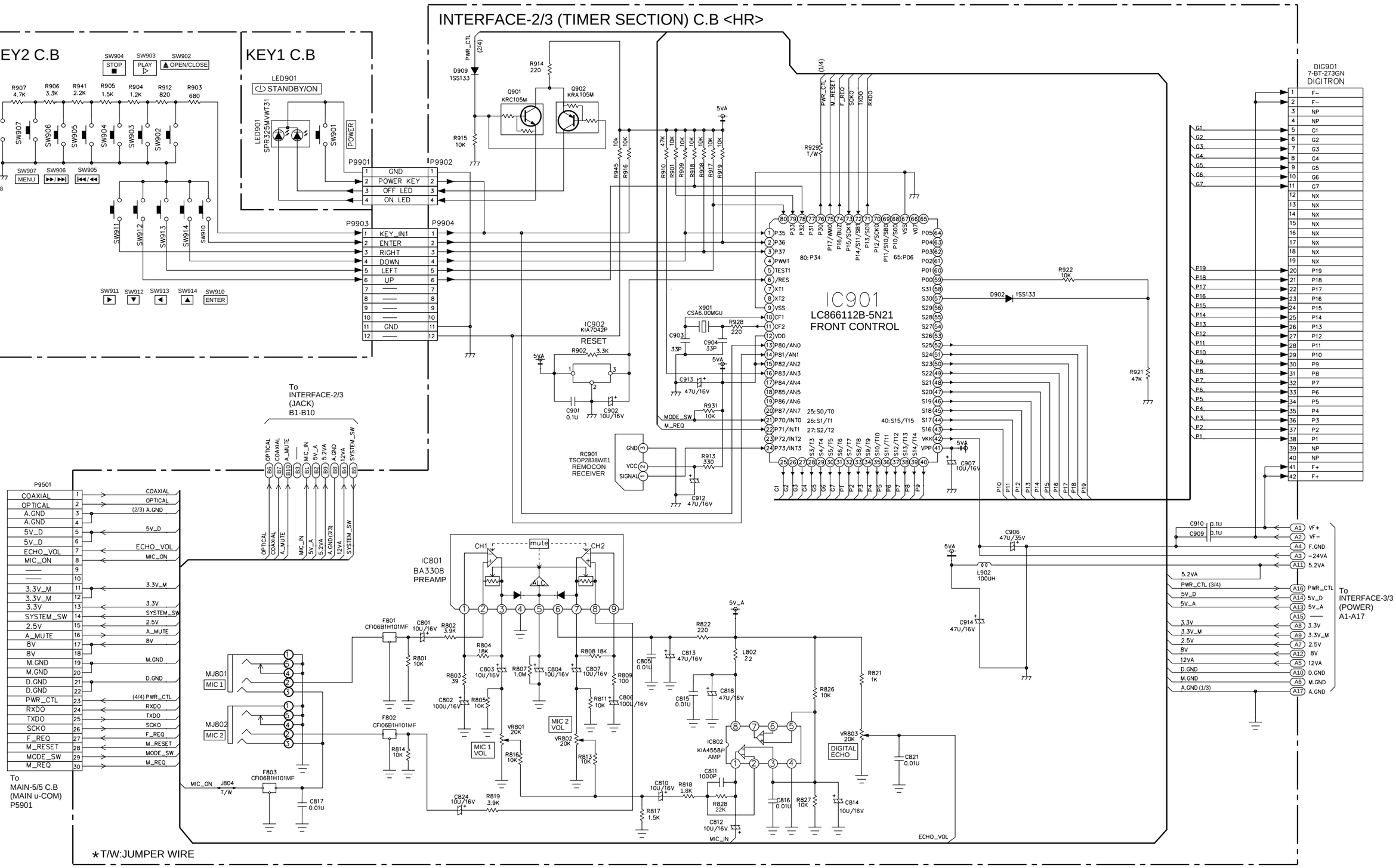
P5901
To
INTERFACE C.B
P9501

PMD04
To
DVD MECHA.
LOADING
MOTOR C.B

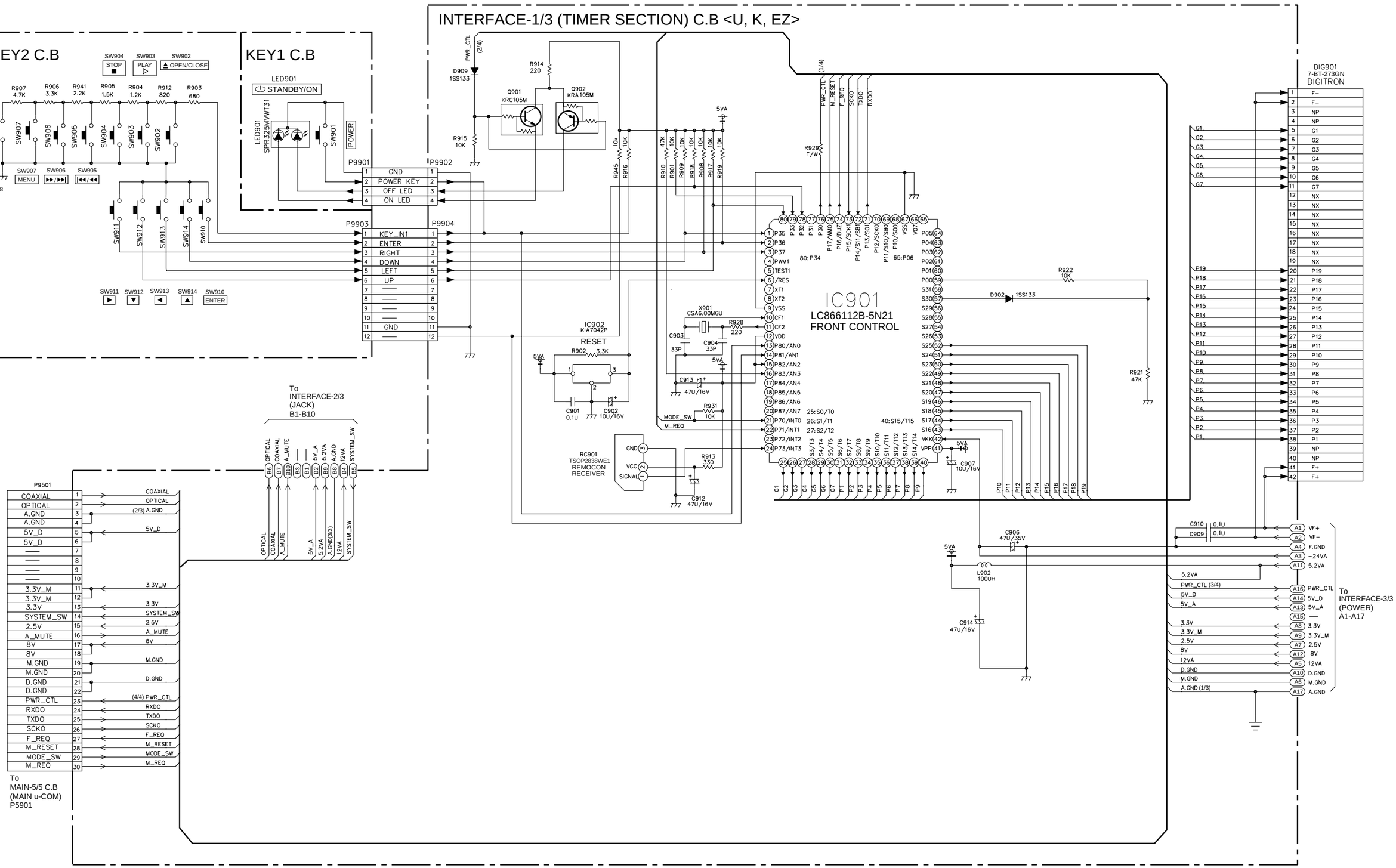
PMD02
To
DVD MECHA.
PICK UP C.B

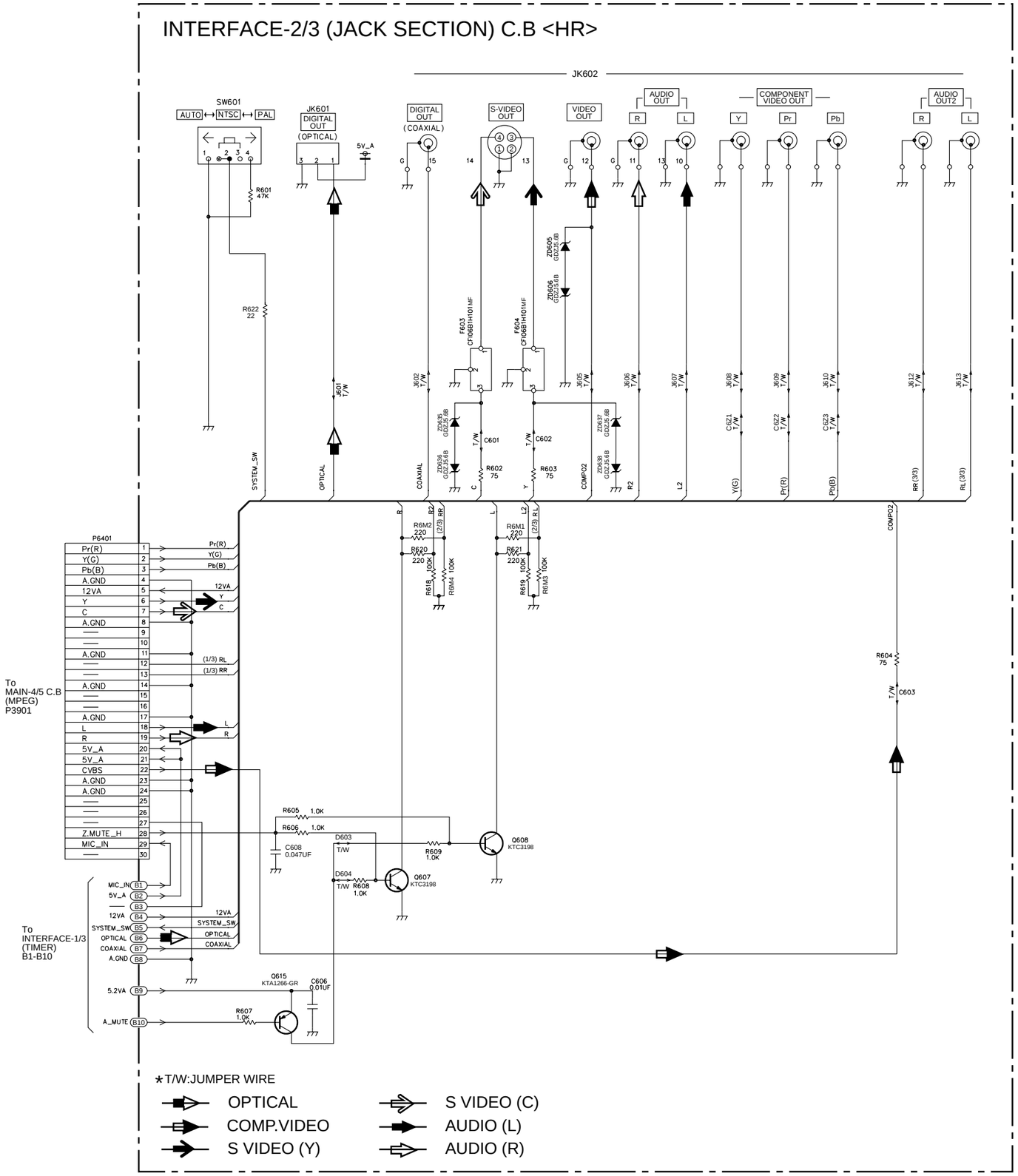
PMD03
To
DVD MECHA.
SPINDLE
MOTOR C.B

SCHEMATIC DIAGRAM - 7 (INTERFACE - 1/3, TIMER SECTION) (KEY1, KEY2 SECTION) <HR>

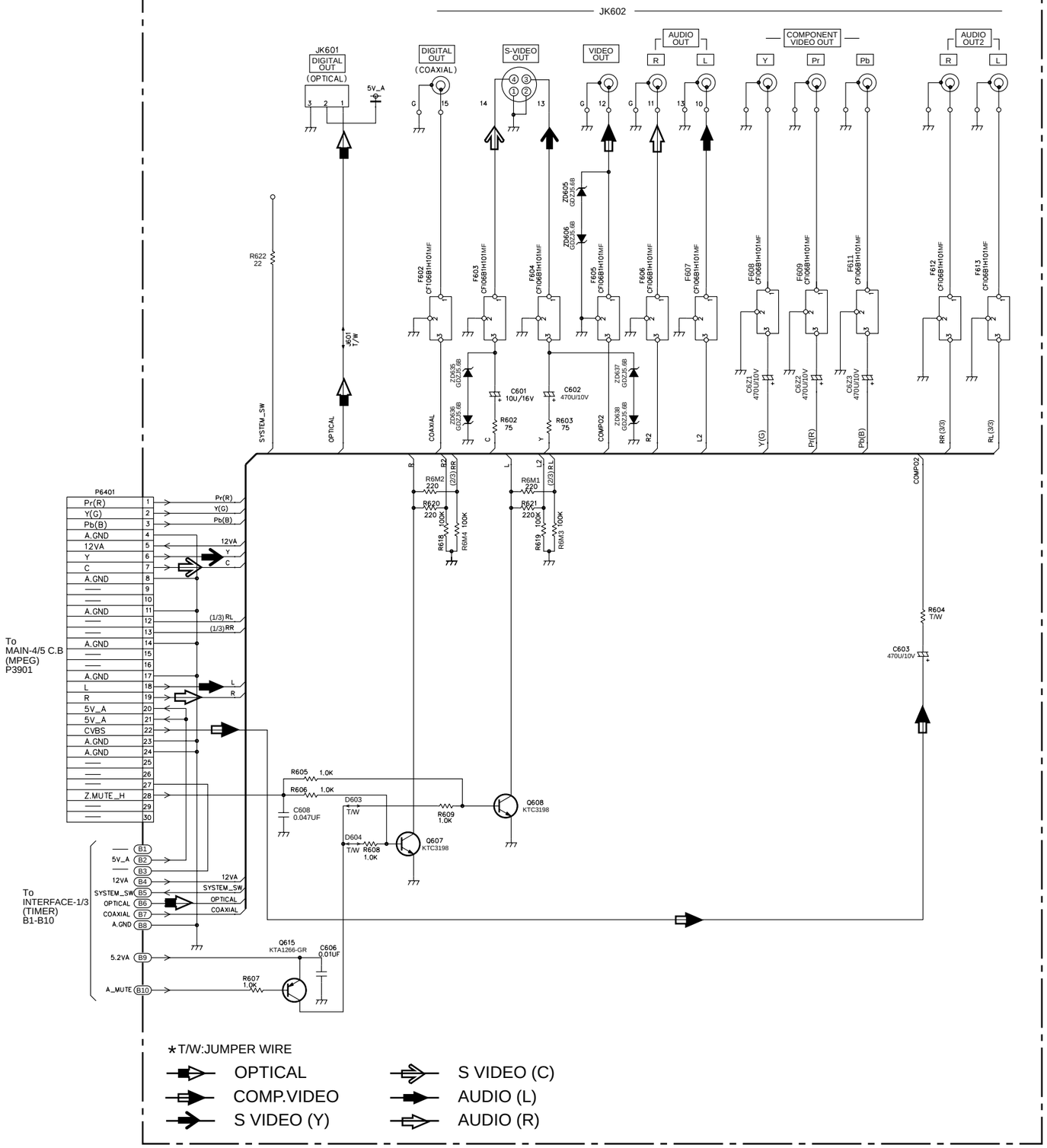


SCHEMATIC DIAGRAM - 8 (INTERFACE - 1/3, TIMER SECTION) (KEY1, KEY2 SECTION) <Except HR>




INTERFACE-2/3 (JACK SECTION) C.B <HR>
JK602
SW601
AUTO
NTSC
PAL
R601 4.7K
R622 22
JK601
DIGITAL OUT (OPTICAL)
5V_A
DIGITAL OUT (COAXIAL)
S-VIDEO OUT
VIDEO OUT
AUDIO OUT
COMPONENT VIDEO OUT
AUDIO OUT2
F603 CF06BHH01MF
F604 CF06BHH01MF
ZD605 GDZJ5.6B
ZD606 GDZJ5.6B
ZD636 GDZJ5.6B
ZD637 GDZJ5.6B
ZD638 GDZJ5.6B
J601 T/W
J602 T/W
J605 T/W
J606 T/W
J607 T/W
J608 T/W
J609 T/W
J610 T/W
J612 T/W
J613 T/W
C601
C602
R602 75
R603 75
C621 T/W
C622 T/W
C623 T/W
SYSTEM_SW
OPTICAL
COAXIAL
COMPO2
R2
L2
Y(G)
Pr(R)
Pb(B)
RR (3/3)
RL (3/3)
R6M2 220
R6M1 220
R620 220
R621 220
R618 100K
R619 100K
R6M4 100K
R6M3 100K
R604 75
C603 T/W
P6401
Pr(R) 1
Y(G) 2
Pb(B) 3
A.GND 4
12VA 5
Y 6
C 7
A.GND 8
9
10
A.GND 11
12
13
A.GND 14
15
16
A.GND 17
L 18
R 19
5V_A 20
5V_A 21
CVBS 22
A.GND 23
A.GND 24
25
26
27
Z.MUTE_H 28
MIC_IN 29
30
(1/3) RL
(1/3) RR
L
R
12VA
Y
C
To MAIN-4/5 C.B (MPEG) P3901
R605 1.0K
R606 1.0K
C608 0.047UF
D603 T/W
D604 T/W
R608 1.0K
R609 1.0K
Q607 KTC3198
Q608 KTC3198
MIC_IN B1
5V_A B2
B3
12VA B4
SYSTEM_SW B5
OPTICAL B6
COAXIAL B7
A.GND B8
5.2VA B9
A_MUTE B10
To INTERFACE-1/3 (TIMER) B1-B10
Q615 KTA1266-GR
C606 0.01UF
R607 1.0K
*T/W:JUMPER WIRE
OPTICAL
COMP.VIDEO
S VIDEO (Y)
S VIDEO (C)
AUDIO (L)
AUDIO (R)

INTERFACE-2/3 (JACK SECTION) C.B <U>



*T/W:JUMPER WIRE

OPTICAL
COMP.VIDEO
S VIDEO (Y)
S VIDEO (C)
AUDIO (L)
AUDIO (R)

INTERFACE-2/3 (JACK SECTION) C.B <K, EZ>

JK602

SW601 AUTO ↔ NTSC ↔ PAL

JK601 DIGITAL OUT (OPTICAL)

DIGITAL OUT (COAXIAL)

S-VIDEO OUT

VIDEO OUT

AUDIO OUT R L

To 21PIN SCART CONNECTOR

JK603

P6401

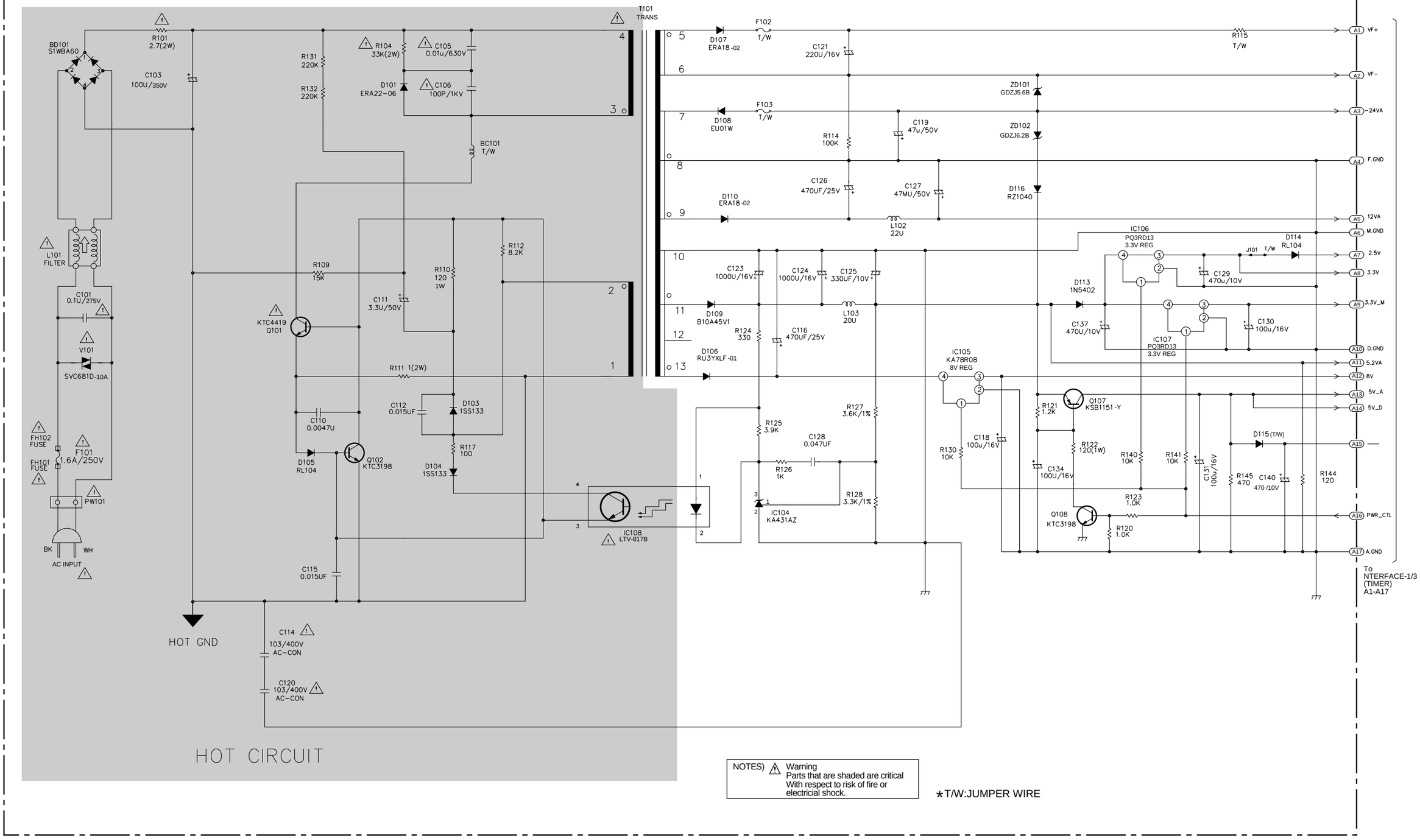
To MAIN-4/5 C.B (MPEG) P3901

To INTERFACE-1/3 (TIMER) B1-B10

*T/W:JUMPER WIRE

OPTICAL
COMP.VIDEO
S VIDEO (Y)
S VIDEO (C)
AUDIO (L)
AUDIO (R)

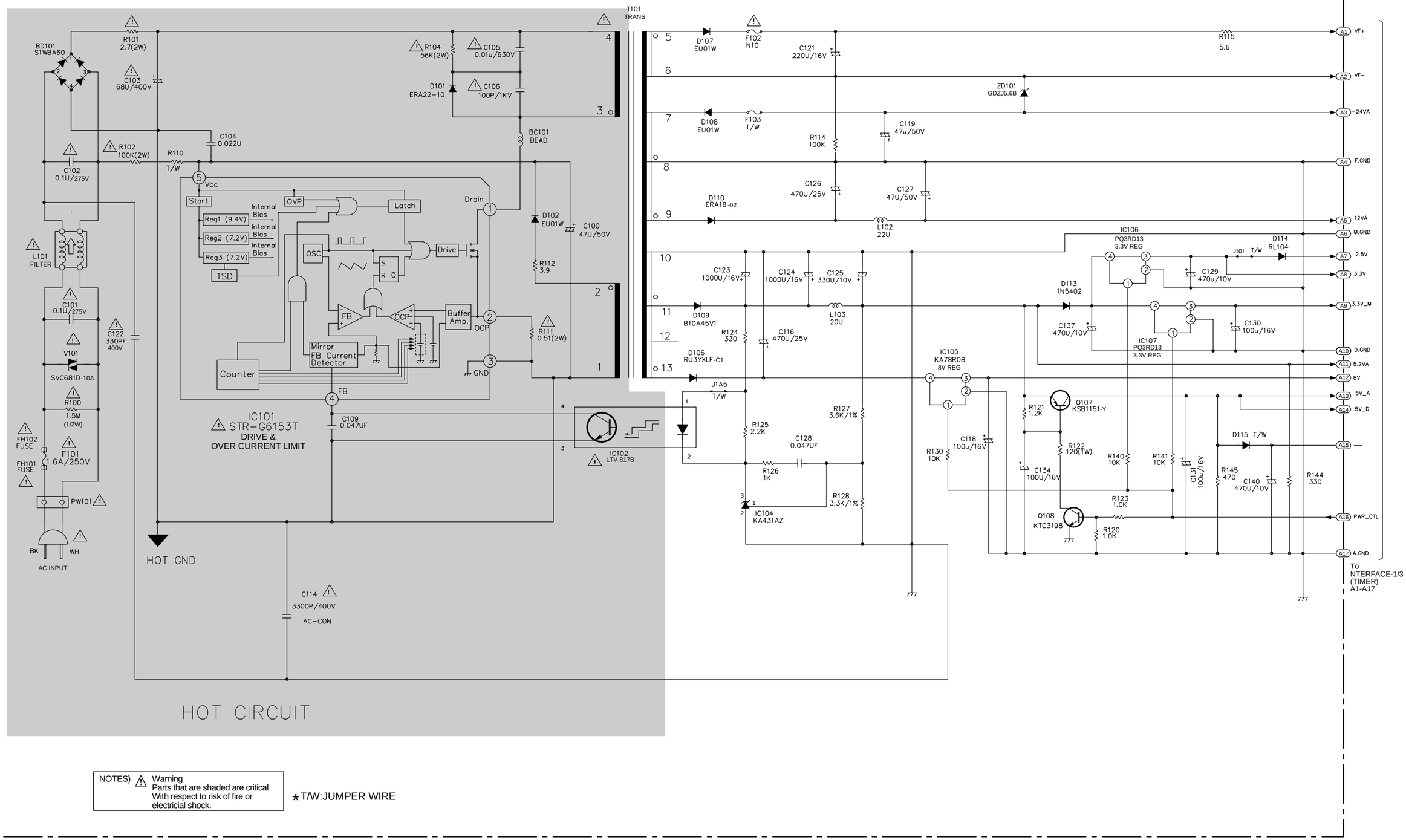
INTERFACE-3/3 (POWER SECTION) C.B <U>



NOTES) ⚠ Warning
Parts that are shaded are critical With respect to risk of fire or electricial shock.

*T/W:JUMPER WIRE

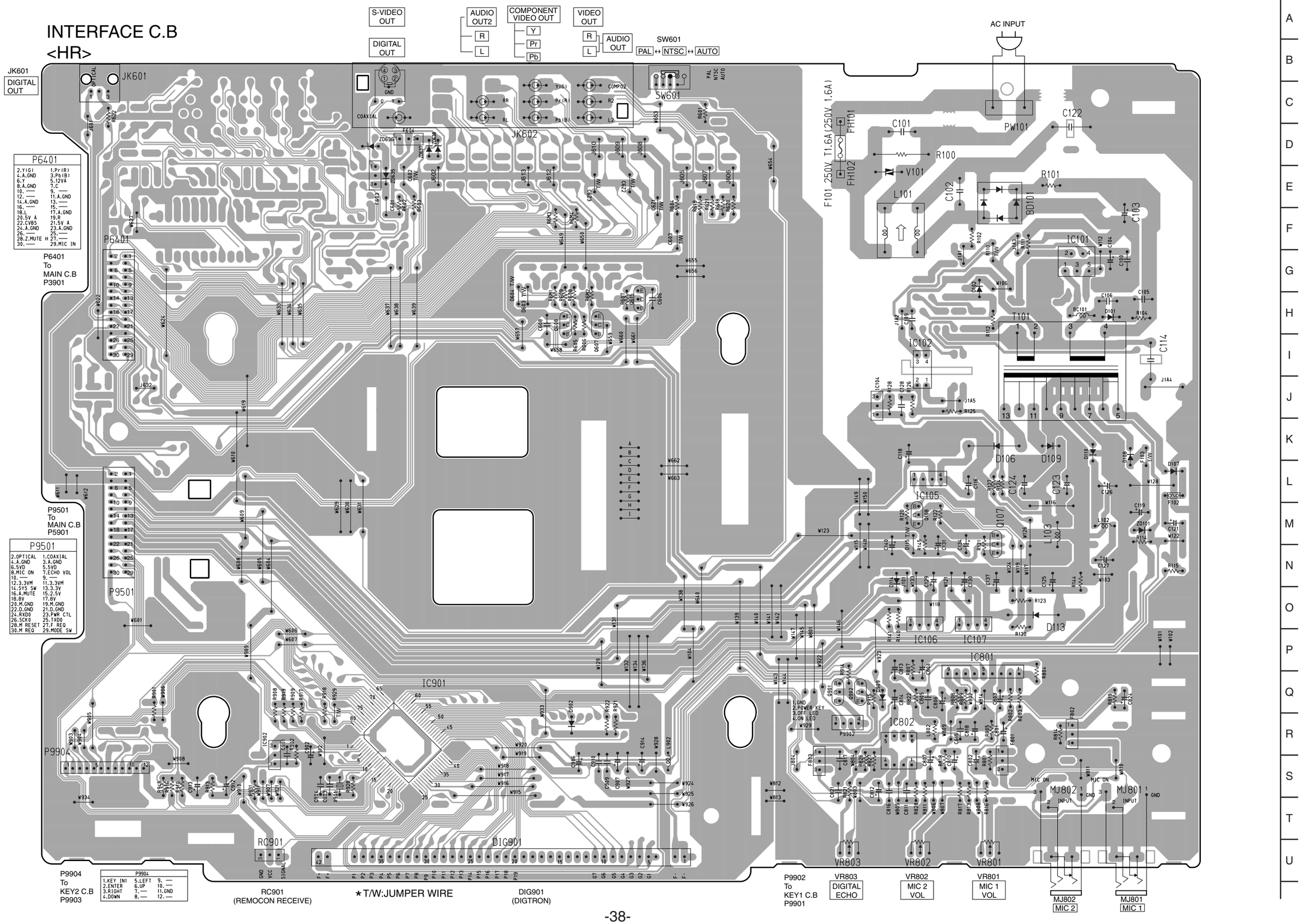
INTERFACE-3/3 (POWER SECTION) C.B <HR, K, EZ>



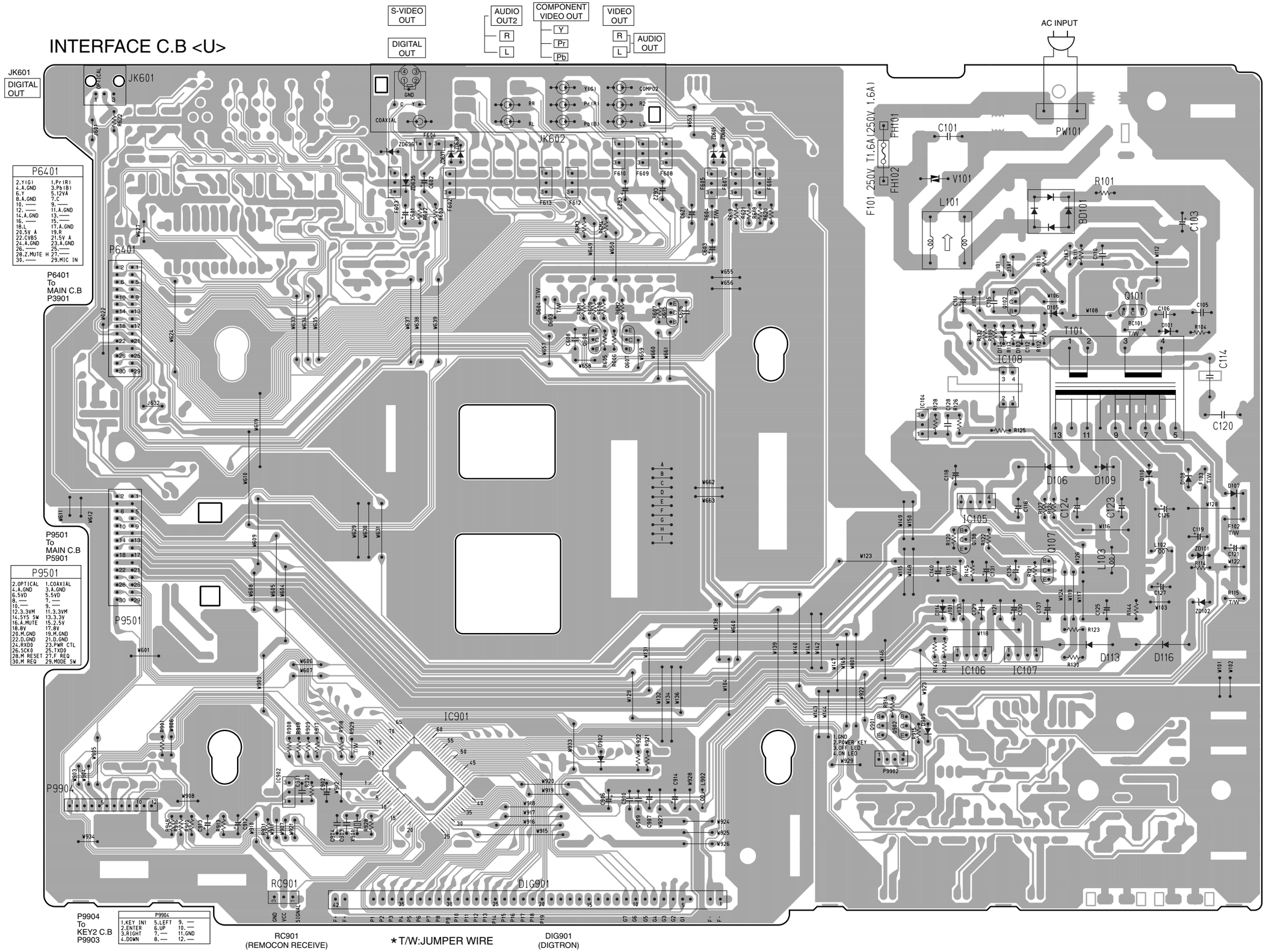
NOTES) ⚠ Warning
Parts that are shaded are critical With respect to risk of fire or electricial shock.

*T/W:JUMPER WIRE

INTERFACE C.B <HR>



INTERFACE C.B <U>

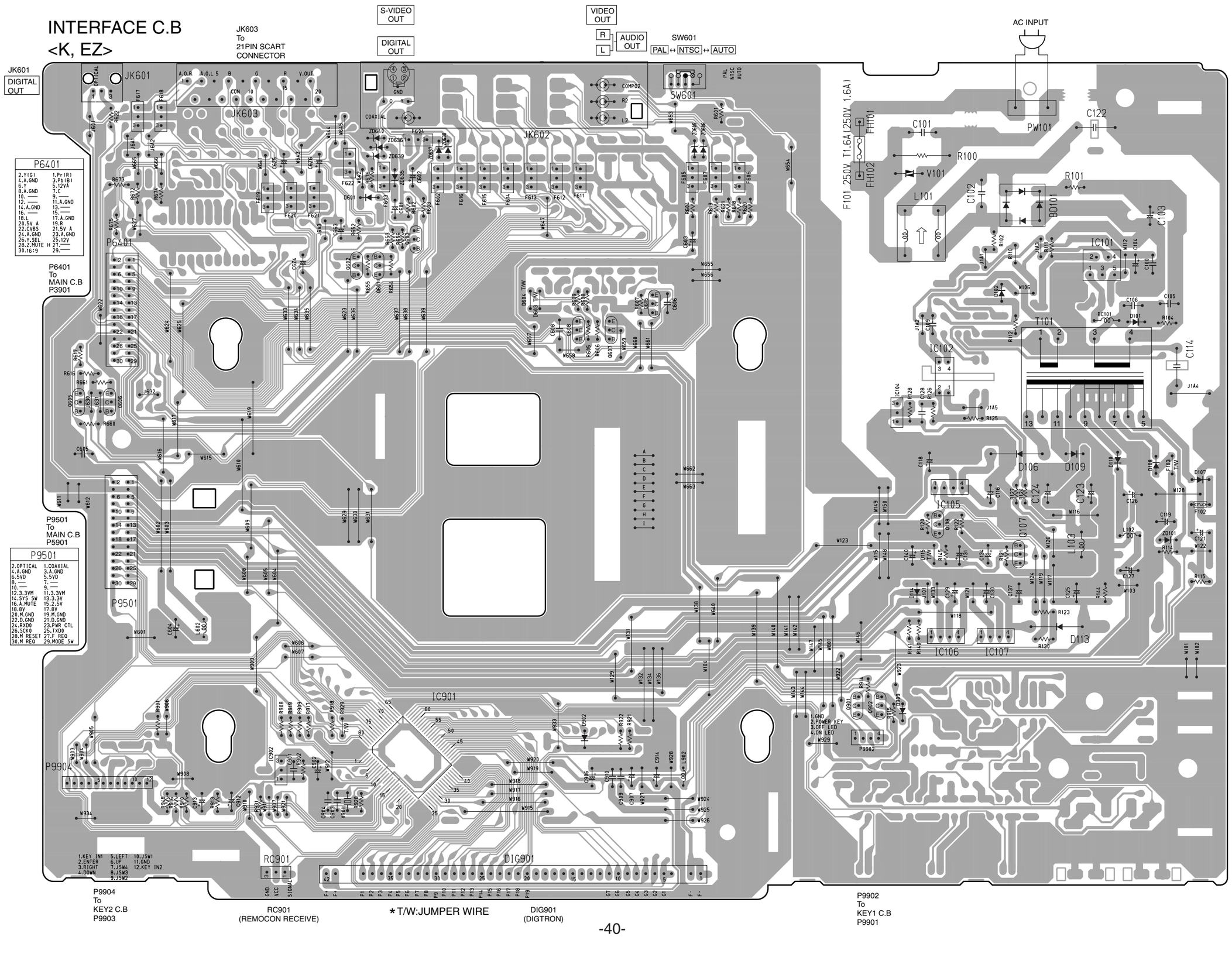


P6401	
2.YIGI	1.Pr(R)
4.A.GND	3.Pb(B)
6.Y	5.12VA
8.A.GND	7.C
10.—	9.—
12.—	11.A.GND
14.A.GND	13.—
16.—	15.—
18.L	17.A.GND
20.5V A	19.R
22.CVBS	21.5V A
24.A.GND	23.A.GND
26.—	25.—
28.Z.MUTE H	27.—
30.—	29.MIC IN

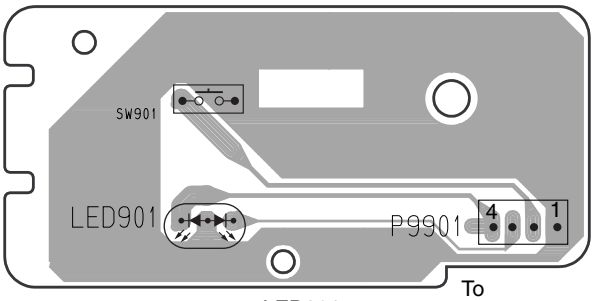
P9501	
2.OPTICAL	1.COAXIAL
4.A.GND	3.A.GND
6.5VD	5.5VD
8.—	7.—
10.—	9.—
12.3.3VM	11.3.3VM
14.SYS SW	13.3.3V
16.A.MUTE	15.2.5V
18.8V	17.8V
20.M.GND	19.M.GND
22.D.GND	21.D.GND
24.RXD0	23.PWR CTL
26.SCK0	25.TXD0
28.M RESET	27.F REQ
30.M REQ	29.MODE SW

P9904		
1.KEY IN1	5.LEFT	9.—
2.ENTER	6.UP	10.—
3.RIGHT	7.—	11.GND
4.DOWN	8.—	12.—

INTERFACE C.B
<K, EZ>



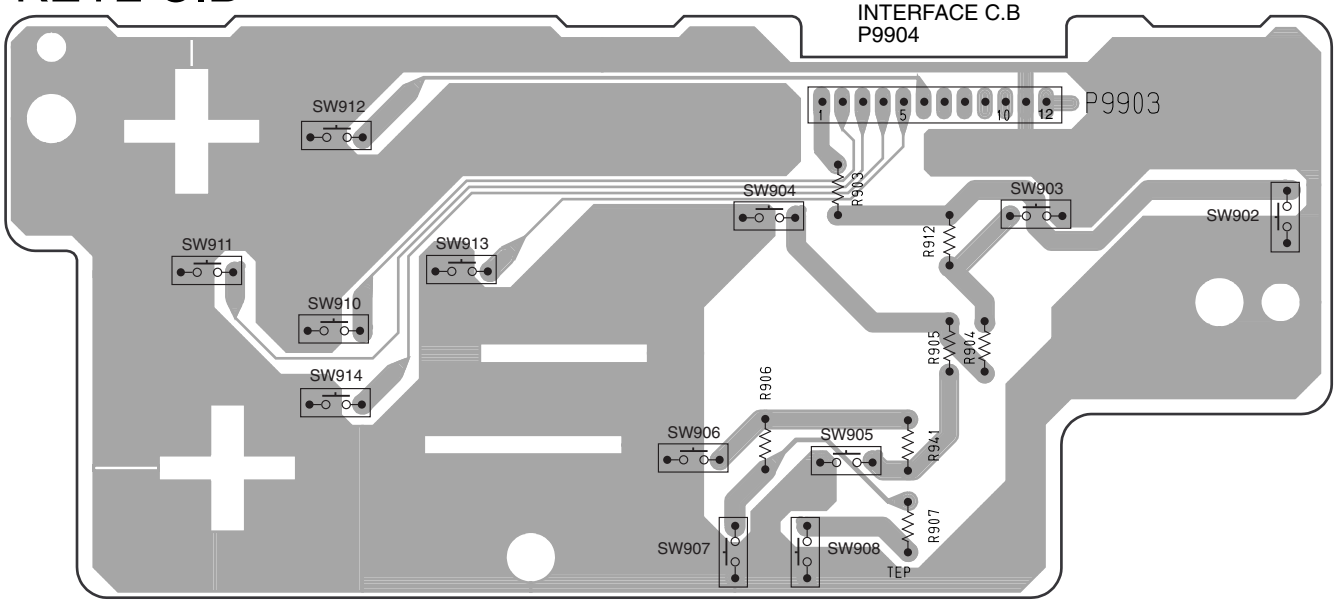
KEY1 C.B

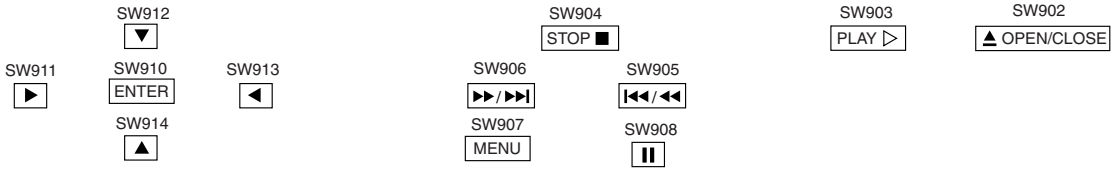


SW901
POWER

LED901
STANDBY/ON

KEY2 C.B

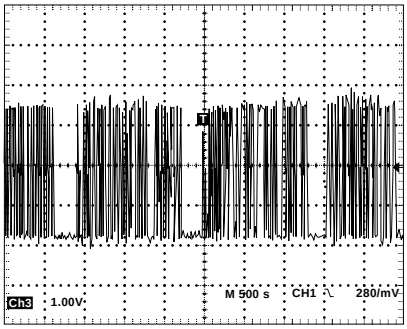




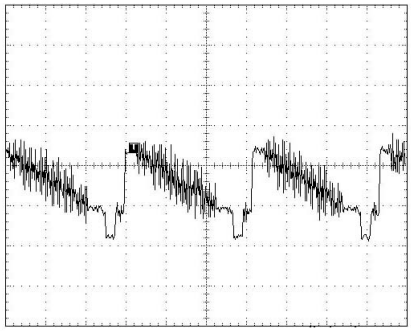
WAVEFORMS - 1/2

IC305 (VIDEO ENCODER)

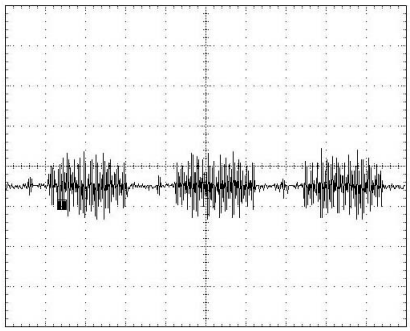
① IC305 Pins 9 ~ 16 MPEG Data
1.0V/500µs



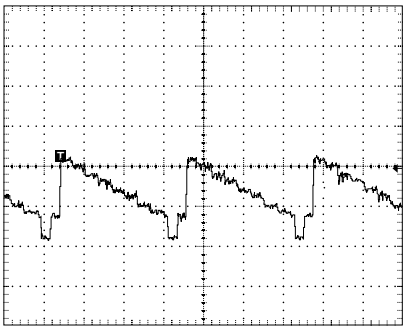
② IC305 Pin30 Composite
500mV/20µs



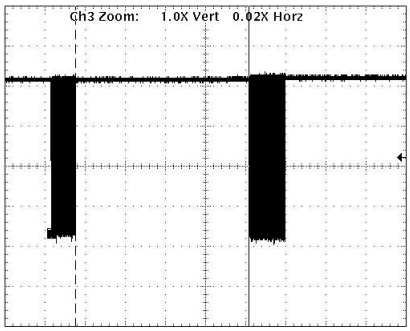
③ IC305 Pin24 Chrominance
500mV/20µs



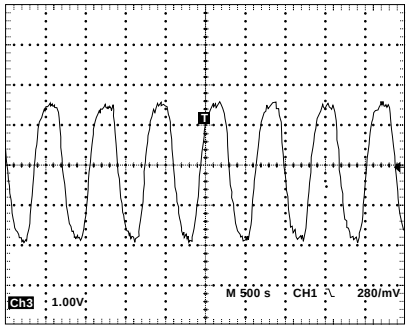
④ IC305 Pin27 Luminance
500mV/20µs



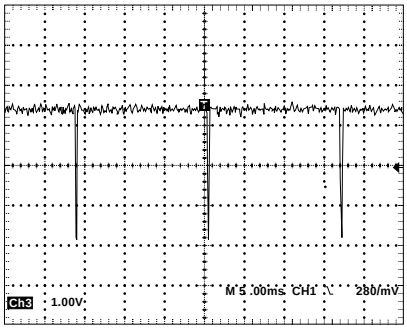
⑤ IC305 Pins 40,41 SDA/SCL
1.0V/25ms



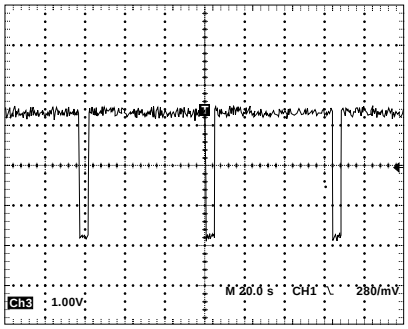
⑥ IC305 Pin4 MPEG Clock (27MHz)
1.0V/500µs



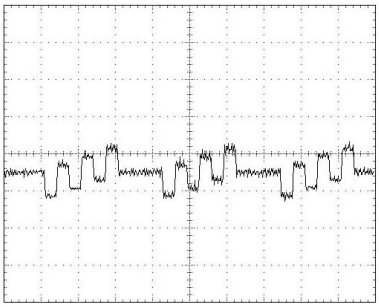
⑦ IC305 Pin7 Vertical SYNC
1.0V/5ms



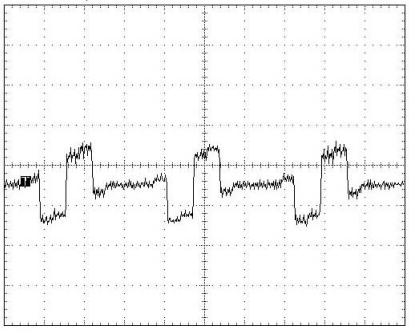
⑧ IC305 Pin8 Horizontal SYNC
1.0V/20µs



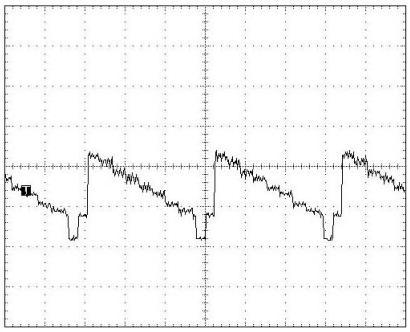
⑨ IC305 Pin29 Component Pb
500mV/20µs



⑩ IC305 Pin23 Component Pr
500mV/20µs



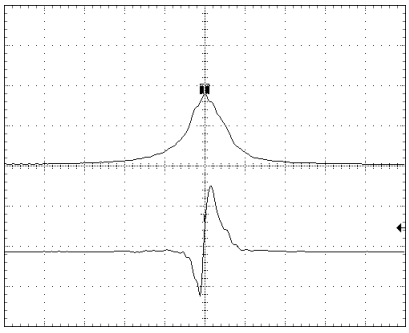
⑪ IC305 Pin27 Component Y
500mV/20µs



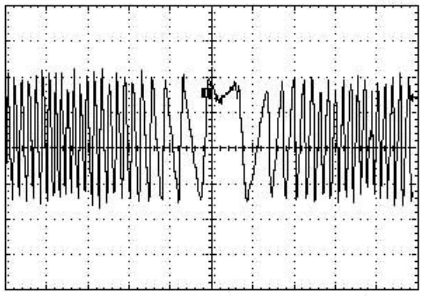
WAVEFORMS - 2/2

IC2A1, IC201 (RF/SERVO)

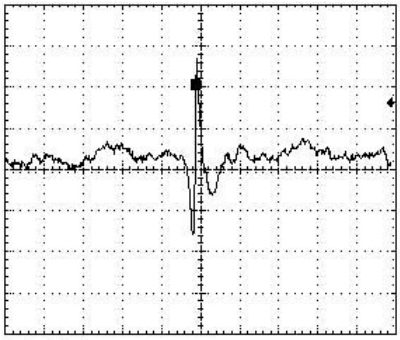
① IC2A1 Pin24 Focus Error
IC2A1 Pin36 Pi
500mV/5ms



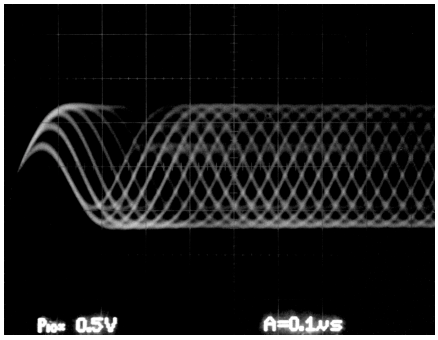
② IC2A1 Pin41 Tracing Error
500mV/2ms



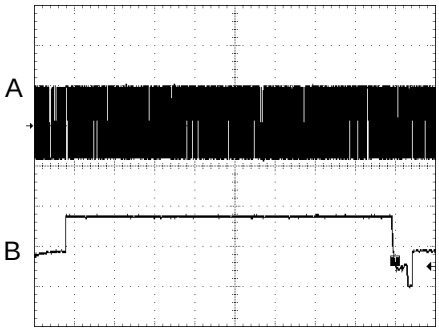
③ IC2A1 Pin41 VBR Tracking Error
500mV/300µs



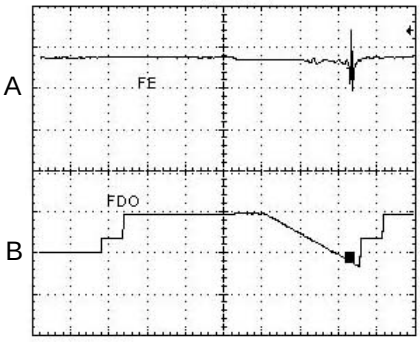
④ IC2A1 Pin57 RF
0.5V/0.1µs



⑤ IC201 Pin88 SLED Driver (FMO)
IC201 Pin18 SLED FG
A: 2.0V/500ms, B: 500mV/500ms

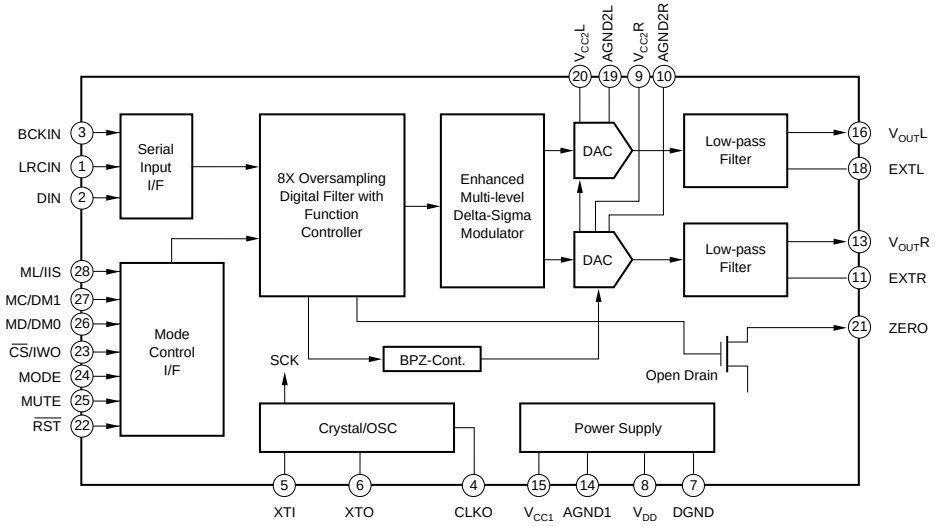


⑥ IC2A1 Pin42 Focus Error(in Focus Search)
IC201 Pin83 Focus Drive (FDO)
A: 200mV/100ms, B: 500mV/100ms

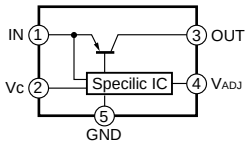


IC BLOCK DIAGRAM - 1/2

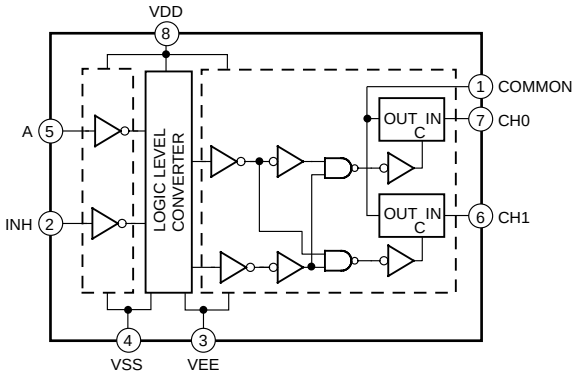
IC, PCM1716E



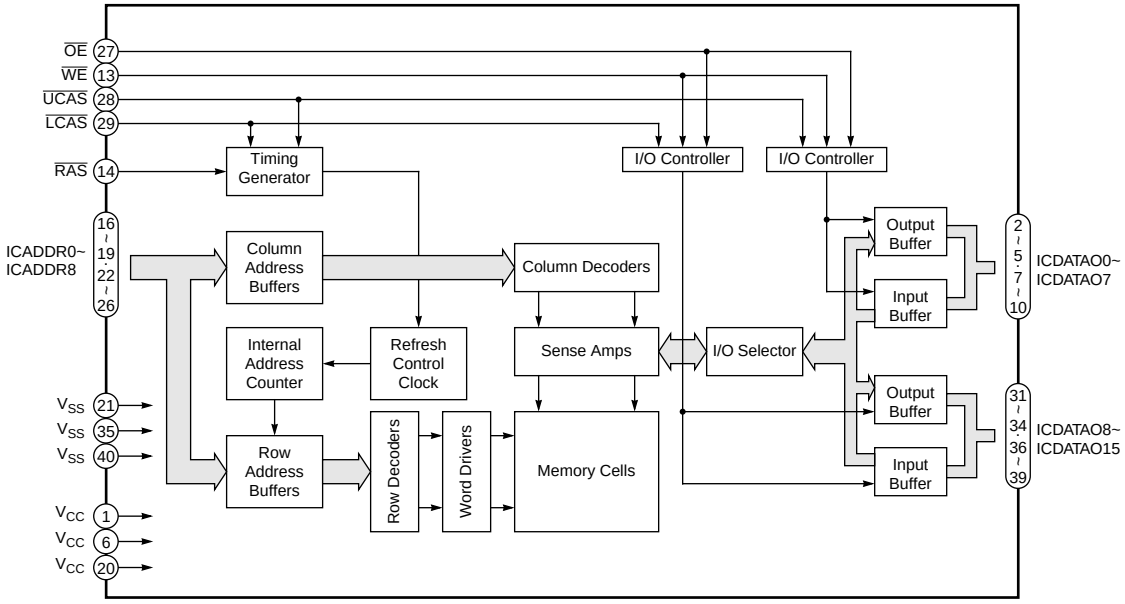
IC, PQ20WZ5U



IC, TC4W53FU

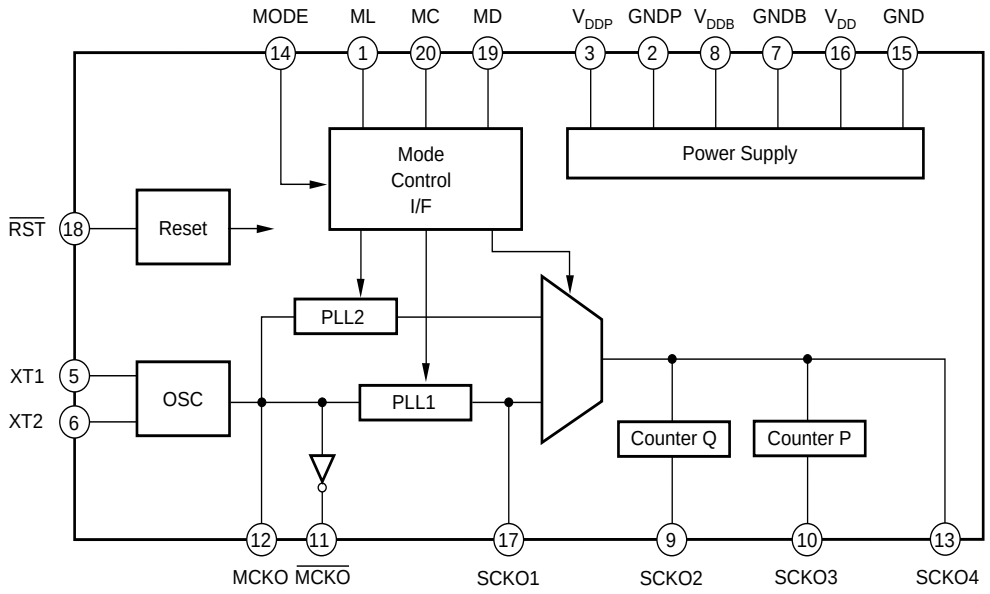


IC, GLT441L16-40

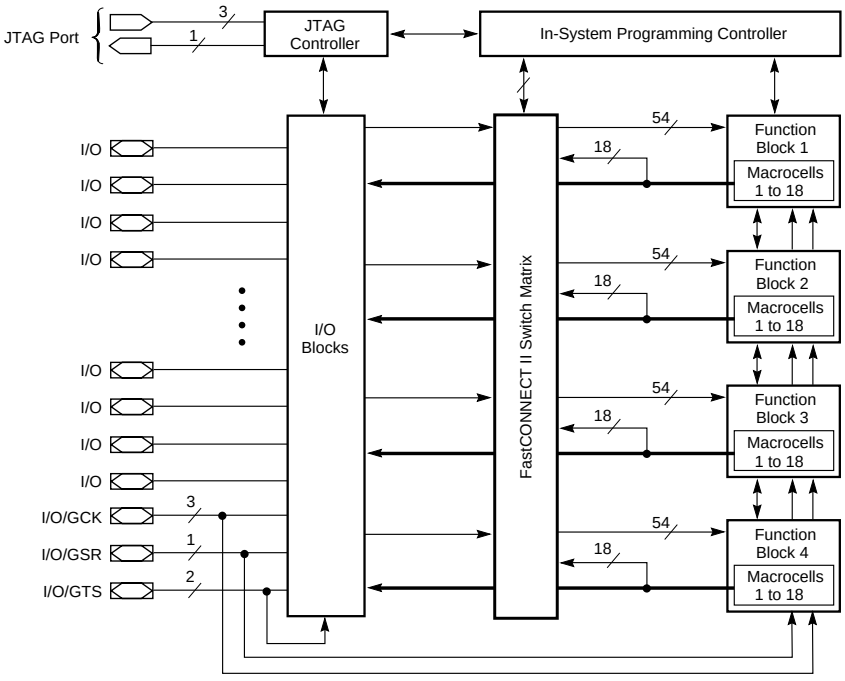


IC BLOCK DIAGRAM - 2/2

IC, PLL1700E



IC, XC9536_15VQ44C-PROG



Pin No.	Pin Name	I/O	Description
1	DVDRFP	I	RF SIGNAL INPUTS: Differential RF signal attenuator input pins.
2	DVDRFN	I	
3	PD1	I	CD PHOTO DETECTOR INTERFACE INPUTS: Inputs from the CD photo detector outputs.
4	PD2	I	
5	A2	I	PHOTO DETECTOR NTERFACE INPUTS: AC coupled inputs for the DPD from the main beam Photo detector matrix outputs.
6	B2	I	
7	C2	I	
8	D2	I	
9	CP	–	DIFFERENTIAL PHASE TRACKING LPF PIN: The external capacitance is connected between CN.
10	CN	–	DIFFERENTIAL PHASE TRACKING LPF PIN: The external capacitance is connected between CP.
11	D	I	PHOTO DETECTOR INTERFACE INPUTS: Inputs from the main beam Photo detector matrix outputs.
12	C	I	
13	B	I	
14	A	I	
15	F	I	CD TRACKING ERROR INPUTS: Inverted(F) and non-inverted(E) inputs of the OP-Amp for the CD tracking error.
16	E	I	
17	CDTE	–	CD TRACKING: E-F Opamp output for feed back.
18	CEIN	I	CD CENTER ERROR INPUT: Inverted input of the OP-Amp for the CD center error.
19	CE1	I	CENTER ERROR OPAMP OUTPUT: CEIN Opamp output for feedback.
20	VNB	–	Ground pin for the servo block.
21	DVDRD	I	APC INPUT: DVD APC input pin from the monitor photo diode.
22	DVDLD	O	APC OUTPUT: DVD APC output pin to control the laser power.
23	CDPD	I	APC INPUT: CD APC input pin from the monitor photo diode.
24	CDLD	O	APC OUTPUT: CD APC output pin to control the laser power.
25	$\overline{\text{LDON}}$	I	APC OUTPUT ON/OFF: APC output control pin. A low level activates LD output.(open high)
26	VC	–	REFERENCE VOLTAGE OUTPUT: This pin provides the internal DC bias reference voltage (+2.5 V fix). Output impedance is less than 50 ohm.
27	VCI	–	REFERENCE VOLTAGE INPUT : DC bias voltage input for servo output reference.
28	VPB	–	Power supply pin for the servo block
29	MIRR	O	MIRROR DETECT OUTPUT: Mirror detect comparator output. Pseudo CMOS output.
30	MP	–	MIRR SIGNAL PEAK HOLD PIN: The external capacitance is connected to VPB.
31	MB	–	MIRR SIGNAL BOTTOM HOLD PIN: The external capacitance is connected to VPB.
32	$\overline{\text{FDCHG}}$	I	LOW IMPEDANCE ENABLE: TTL compatible input pin that activates the FDCHG switches. A low level activates the switches and the falling edge of the internal FDCHG triggers the fast decay for the MIRR bottom hold circuit.(open high)
33	MLPF2	–	MIRR SIGNAL LPF PIN: The external capacitance is connected to VPB.
34	MLPF1	–	MIRR SIGNAL LPF PIN: The external capacitance is connected to VPB.
35	MIN	I	RF SIGNAL INPUT FOR MIRROR: AC coupled inputs for the mirror dection circuit from pull-in signal output (PI).

Pin No.	Pin Name	I/O	Description
36	PI	O	PULL-IN SIGNAL OUTPUT: The summing signal output of A,B,C,D inputs for mirror detection. Reference to VCI.
37	DFT	O	DEFECT OUTPUT: Pseudo CMOS output. When defect is detected, the DFT output goes high. Also the servo AGC output can be monitored at this DFT pin, when CAR bit7-4 is '0011'.
38	TPH	–	PI TOP HOLD PIN: An external capacitance is connected to VPB.
39	TZC	O	TRACKING ZERO CROSSING SIGNAL OUTPUT: Tracking zero crossing output. Pseudo CMOS output.
40	TEI	I	TRACKING ERROR AC COUPLED INPUT: AC couple input for the tracking zero crossing signal output.
41	TE	O	TRACKING ERROR SIGNAL OUTPUT: Tracking error output reference to VCI.
42	FE	O	FOCUSING ERROR SIGNAL OUTPUT: Focus error output reference to VCI.
43	CE	O	CENTER ERROR SIGNAL OUTPUT: Center error output reference to VCI.
44	BYP2	–	The Servo AGC integration capacitor CBYP2, is connected between BYP2 and VNB.
45	HOLD2	I	HOLD CONTROL: TTL compatible control pin which, when pulled high,disables the Servo AGC charge pump and holds the Servo AGC amplifier gain as its present value. (open high)
46	SCLK	I	SERIAL CLOCK: Serial clock CMOS input. The clock applied to this pin is synchronized with the data applied to SDATA. (not to be left open)
47	SDATA	I/O	SERIAL DATA: Serial data bidirectional CMOS pin. NRZ programming data for the internal registers is applied to this input. (not to be left open)
48	SDEN	I	SERIAL DATA ENABLE: Serial enable CMOS input. A high level input enables the serial port. (not to be left open)
49	HOLD1	I	HOLD CONTROL: TTL compatible control pin which, when pulled high, disables the RF AGC charge pump and holds the RF AGC amplifier gain as its present value. (open high)
50	VNA	–	Ground pin for the RF block and serial port.
51	FNN	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal outputs.
52	FNP	O	
53	DIP	I	ANALOG INPUTS FOR RF SINGLE BUFFER: Differential analog inputs to the RF single-end output buffer and full wave rectifier.
54	DIN	I	
55	RX	–	REFERENCE RESISTOR INPUT: An external 12.1 or 8.2 k ohm, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.
56	BYP	–	The RF AGC integration capacitor CBYP, is connected between BYP and VPA.
57	SIGO	O	SINGLE-ENDED NORMAL OUTPUT: Single-ended RF output.
58	VPA	–	Power supply pin for the RF block and serial port.
59	AIP	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
60	AIN	I	
61	ATON	O	DIFFERENTIAL ATTENUATOR OUTPUTS: Attenuator outputs.
62	ATOP	O	
63	CDRF	I	RF SIGNAL INPUT : Single-ended RF signal attenuator input pin.
64	CDRFDC	O	CD RF SIGNAL OUTPUT: Single-ended CD RF summing output.

IC DESCRIPTION - 2/11 (KA3032)-1/1

Pin No.	Pin Name	I/O	Description
1	OUT1	O	CH 1 op-amp output
2	IN2.1	I	CH 1 op-amp input (+)
3	IN2.2	I	CH 2 op-amp input (-)
4	OUT2	O	CH 2 op-amp output
5	IN3.1	I	CH 3 op-amp input (+)
6, 7	GND	–	Ground
8	IN3.2	I	CH 3 op-amp input (-)
9	OUT3	O	CH 3 op-amp output
10	IN4.1	I	CH 4 op-amp input (+)
11	IN4.2	I	CH 4 op-amp input (-)
12	OUT4	O	CH 4 op-amp output
13	CTL	I	CH 5 motor speed control
14	FWD	I	CH 5 forward input
15	REV	I	CH 5 reverse input
16	SGND	–	Signal ground
17	OPOUT	O	Opamp output
18, 19	GND	–	Ground
20	OPIN (+)	I	Opamp input (+)
21	OPIN (-)	I	Opamp inpt (-)
22	MUTE4	I	CH 4 mute
23	MUTE3	I	CH 3 mute
24	MUTE1, 2	I	CH 1, CH 2 mute
25	PVCC1	–	Power supply voltage (For CH 5)
26, 27	DO5.2, DO5.1	O	CH 5 drive output
28, 29	DO4.2, DO4.1	O	CH 4 drive output
30, 31	GND	–	Ground
32, 33	DO3.2, DO3.1	O	CH 3 drive output
34	PGND	–	Power ground
35, 36	DO2.2, DO2.1	O	CH 2 drive output
37, 38	DO1.2, DO1.1	O	CH 1 drive output
39	PVCC2	–	Power supply voltage (For CH 1, CH 2, CH 3, CH 4)
40	REG50	O	Regulator output
41	REG050	O	Regulator 5V output
42, 43	GND	–	Ground
44	RES50	I	Regulator reset
45	SVCC	–	Signal supply voltage
46	REF	I	Bias voltage input
47	IN1.1	I	CH 1 opamp input (+)
48	IN1.2	I	CH 1 opamp input (-)

Pin No.	Pin Name	I/O	Description
1	VCC	–	Power Supply (+3.3 V)
2 ~ 5	DQ0 ~ DQ3	I/O	Data-In / Data-Out
6	VCC	–	Power Supply (+3.3 V)
7 ~ 10	DQ4 ~ DQ7	I/O	Data-In / Data-Out
11, 12	NC	–	Not used
13	$\overline{WE}$	I	Write Enable
14	$\overline{RAS}$	I	Row Address Strobe
15	NC	–	Not used
16 ~ 19	A0 ~ A3	I	Address Input
20	VCC	–	Power Supply (+3.3 V)
21	GND	–	Ground (0 V)
22 ~ 26	A4 ~ A8	I	Address Input
27	$\overline{OE}$	I	Output Enable
28	$\overline{UCAS}$	I	Column Address Strobe
29	$\overline{LCAS}$	I	Column Address Strobe
30	NC	–	Not used
31 ~ 34	DQ8 ~ DQ11	I/O	Data-In / Data-Out
35	GND	–	Ground (0 V)
36 ~ 39	DQ12 ~ DQ15	I/O	Data-In / Data-Out
40	GND	–	Ground (0 V)

Pin No.	Pin Name	I/O	Description
1	VCC	–	3.3 V is applied. (VCC is for the internal circuit.)
2	DQ0	I/O	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
3	DQ1		
4	VSSQ	–	Ground is connected. (VSSQ is for the output buffer.)
5	DQ2	I/O	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
6	DQ3		
7	VCCQ	–	3.3 V is applied. (VCCQ is for the output buffer.)
8	DQ4	I/O	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
9	DQ5		
10	VSSQ	–	Ground is connected. (VSSQ is for the output buffer.)
11	DQ6	I/O	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
12	DQ7		
13	VCCQ	–	3.3 V is applied. (VCCQ is for the output buffer.)
14	LDQM	I	DQM controls input/output buffers. - Read operation: If DQM is High, The output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z. - Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written.
15	$\overline{\text{MWE}}$	I	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
16	$\overline{\text{CAS}}$		
17	$\overline{\text{RAS}}$		
18	$\overline{\text{CS1}}$	I	When $\overline{\text{CS}}$ is Low, the command input cycle becomes valid. When $\overline{\text{CS}}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
19	MA11	I	A11 is a bank select signal (BS). The memory array of the GM72V161621ET/ELT Series is divided into bank 0 and bank 1. GM72V161621ET/ELT Series contain 2048 row x 256 column x 16bits. If A11 is Low, bank 0 is selected, and if A11 is High , bank 1 is selected.
20	MA10	I	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CLK rising edge. Column address is determined by A0 to A7 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A11 (BS) is precharged.
21	MA0		
22	MA1		
23	MA2		
24	MA3		
25	VCC	–	3.3 V is applied. (VCC is for the internal circuit.)
26	GND	–	Ground is connected. (VSS is for the internal circuit.)
27	MA4	I	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CLK rising edge. Column address is determined by A0 to A7 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A11 (BS) is precharged.
28	MA5		
29	MA6		
30	MA7		
31	MA8		
32	MA9		
33	NC	–	Not used.

Pin No.	Pin Name	I/O	Description
34	CKE	I	This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.
35	CLK	I	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
36	UDQM	I	DQM controls input/output buffers. - Read operation: If DQM is High, The output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z. - Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written.
37	NC	–	Not used
38	VCCQ	–	3.3 V is applied. (VCCQ is for the output buffer.)
39	MD8	I/O	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
40	MD9		
41	VSSQ	–	Ground is connected. (VSSQ is for the output buffer.)
42	MD10	I/O	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
43	MD11		
44	VCCQ	–	3.3 V is applied. (VCCQ is for the output buffer.)
45	MD12	I/O	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
46	MD13		
47	VSSQ	–	Ground is connected. (VSSQ is for the output buffer.)
48	MD14	I/O	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
49	MD15		
50	GND	–	Ground is connected. (VSS is for the internal circuit.)

Pin No.	Pin Name	I/O	Description
1	D PLL L	I	Latch Enable for Software Mode/Sampling Rate Selection for Hardware Mode. When MODE pin is LOW, ML is selected.(1)
2	MODE	I	Mode Control Select. When this pin is HIGH, device is operated in hardware mode using SR0 (pin 1), FS0 (pin 19), and FS1 (pin 20). When this pin is LOW, device is operated in software mode by three-wire interface using ML (pin 1), MD (pin 19) and MC (pin 20).(1)
3	VDD	–	Digital Power Supply, +5V.
4	GND	–	Digital Ground.
5	XT2	–	27MHz Crystal. When an external 27MHz clock is applied to XT1 (pin 6), this pin must be connected to GND.
6	XT1	I	27MHz Oscillator Input/External 27MHz Input.
7	GNDP	–	Ground for PLL.
8	VDDP	–	Power Supply for PLL, +5V.
9	RSV	–	Reserved. Must be left open.
10	MCKO	O	27MHz Output.
11	MPEG CLK	O	Inverted 27MHz Output.
12	SCKO1 MCK	O	Fixed 33.8688MHz Clock Output.
13	SCKO4	O	768fs Clock Output.
14	SCKO2	O	256fs Clock Output.
15	GNDB	–	Digital Ground for VDDB.
16	VDDB	–	Digital Power Supply for Clock Output Buffers, +3.3V.
17	DA XCK	O	384fs Output. This output has been optimized for the lowest jitter and should be connected to the audio DAC(s).
18	RESET	I	Reset. When this pin is LOW, device is held in reset.(1)
19	S DATA	I	Serial Data Input for Software Mode/Sampling Frequency Selection for Hardware Mode. When MODE pin is LOW, MD is selected.(1)
20	S CLK	I	Shift Clock Input for Software Mode/Sampling Frequency Selection for Hardware Mode. When MODE pin is LOW, MC is selected.(1)

IC DESCRIPTION - 6/11 (PCM1716E)-1/1

Pin No.	Pin Name	I/O	Description
1	LRCIN	I	Left and Right Clock Input. This clock is equal to the sampling rate - fs.(1)
2	DIN	I	Serial Audio Data Input. (1)
3	BCKIN	I	Bit Clock Input for Serial Audio Data.(1)
4	CLKO	O	Buffered Output of Oscillator. Equivalent to System Clock.
5	XTI	I	Oscillator Input (External Clock Input)
6	XTO	O	Oscillator Output
7	DGND	–	Digital Ground
8	VDD	–	Digital Power +5V
9	VCC2R	–	Analog Power +5V
10	AGND2R	–	Analog Ground
11	EXTR	O	Rch, Common Pin of Analog Output Amp
12	NC	–	Not used
13	VOUTR	O	Rch, Analog Voltage Output of Audio Signal
14	AGND1	–	Analog Ground
15	VCC1	–	Analog Power +5V
16	VOUTL	O	Lch, Analog Voltage Output of Audio Signal
17	NC	–	Not used
18	EXTL	O	Lch, Common Pin of Analog Output Amp
19	AGND2L	–	Analog Ground
20	VCC2L	–	Analog Power +5V
21	ZERO	O	Zero Data Flag
22	$\overline{\text{RST}}$	I	Reset. When this pin is low, the DF and modulators are held in reset. (2)
23	$\overline{\text{CS}}$/IWO	I	Chip Select/Input Format Selection. When this pin is low, the Mode Control is effective. (3)
24	MODE	I	Mode Control Select. (H: Software, L: Hardware). (2)
25	$\overline{\text{MUTE}}$	I	Mute Control
26	MD/DM0	I	Mode Control, DATA/De-emphasis Selection 1. (2)
27	MC/DM1	I	Mode Control, BCK/De-emphasis Selection 2. (2)
28	ML/IIS	I	Mode Control, WDCK/Input Format Selection. (2)

NOTES: (1) Pins 1, 2, 3; Schmitt Trigger input.
(2) Pins 22, 24, 25, 26, 27, 28; Schmitt Trigger input with pull-up resister.
(3) Pin 23; Schmitt Trigger input with pull-down resister.

Pin No.	Pin Name	I/O	Description
1 ~ 8	A16 ~ A9	I	Addresses
9	A20	I	Addresses
10	NC	–	Not used
11	$\overline{WE}$	I	Write Enable
12	$\overline{RESET}$	I	Reset
13 ~ 15	NC	–	Not used
16, 17	A18, A17	I	Addresses
18 ~ 25	A7 ~ A0	I	Addresses
26	$\overline{CE}$	I	Chip Enable
27	GND	–	Ground
28	$\overline{OE}$	O	Output Enable
29	I/O0	I/O	Data Inputs/Outputs
30	I/O8	I/O	
31	I/O1	I/O	
32	I/O9	I/O	
33	I/O2	I/O	
34	I/O10	I/O	
35	I/O3	I/O	
36	I/O11	I/O	
37	VCC	–	
38	I/O4	I/O	Data Inputs/Outputs
39	I/O12	I/O	
40	I/O5	I/O	
41	I/O13	I/O	
42	I/O6	I/O	
43	I/O14	I/O	
44	I/O7	I/O	
45	I/O15/A-1	I/O	I/O15 (Data Input/Output, Word Mode) A-1 (LSB Address Input, Byte Mode)
46	GND	–	Ground
47	$\overline{BYTE}$	I	Selects Byte or Word Mode
48	A17	I	Addresses

IC DESCRIPTION - 8/11 (V53C16256HK50)-1/1

Pin No.	Pin Name	I/O	Description
1	VCC	–	+5V Supply
2 ~ 5	D00 ~ D03	I/O	Data Input, Output
6	VCC	–	+5V Supply
7 ~ 10	D04 ~ D07	I/O	Data Input, Output
11, 12	NC	–	Not used
13	$\overline{WE}$	I	Write Enable
14	$\overline{RAS}$	I	Row Address Strobe
15	NC	–	Not used
16 ~ 19	A01 ~ A04	I	Address Inputs
20	VCC	–	+5V Supply
21	VSS	–	0V Supply (GND)
22 ~ 26	A05 ~ A09	I	Address Inputs
27	$\overline{OE}$	O	Output Enable
28	$\overline{CASH}$	I	Column Address Strobe Upper Byte Control
29	$\overline{CASL}$	I	Column Address Strobe Lower Byte Control
30	NC	–	Not used
31 ~ 34	D08 ~ D11	I/O	Data Input, Output
35	VSS	–	0V Supply
36 ~ 39	D12 ~ D15	I/O	Data Input, Output
40	VSS	–	0V Supply

Pin No.	Pin Name	I/O	Description
1	P35	I	Select $\overline{\text{DOWN}}$ SW input from SW914
2	P36	I	Enter SW input from SW910
3	P37	I	Select right SW input SW911
4	PWM1	O	Not used.
5	TEST1	–	Not used. (TEST port)
6	$\overline{\text{RES}}$	I	Reset signal input from IC902 3pin
7	XT1	I	Not used. (Input for 32.768 kHz crystal oscillation)
8	XT2	O	Not used. (Output for 32.768 kHz crystal oscillation)
9	VSS	–	Ground
10	CF1	I	Ceramic resonator X501 (6 MHz) oscillation input
11	CF2	O	Ceramic resonator X501 (6 MHz) oscillation output
12	VDD	–	Vcc (5 V)
13	P80	I	Key in input from SW901 ~ SW908
14	P81	I	Reserved
15	P82	I	
16	P83	I	Shuttle 3 line A/D input
17	P84	I	Reserved
18	P85	I	
19	P86	I	
20	P87	I	
21	MODE SW	I/O	“LOW” at program download mode
22	M REQ	I	Request signal (active “LOW”) from IC501 (Main µ-COM, HD64173034AFI20)
23	P72	I	Not used.
24	P73	I	Remocon receiver signal input
25	G1	O	VFD display control signal output. DIG901 G1 to G7
26	G2	O	
27	G3	O	
28	G4	O	
29	G5	O	
30	G6	O	
31	G7	O	
32	P1	O	VFD display control signal output. DIG901 P1 to P9
33	P2	O	
34	P3	O	
35	P4	O	
36	P5	O	
37	P6	O	
38	P7	O	
39	P8	O	
40	P9	O	
41	VPP	I	Vcc (5 VAU)
42	VKK	I	-24 V input

Pin No.	Pin Name	I/O	Description
43	P10	O	VFD display control signal output. DIG 901 P10 to P19
44	P11	O	
45	P12	O	
46	P13	O	
47	P14	O	
48	P15	O	
49	P16	O	
50	P17	O	
51	P18	O	
52	P19	O	
53	S26	–	Not used.
54	S27	–	
55	S28	–	
56	S29	–	
57	S30	–	D902 option (Present at AIWA remocon model)
58	S31	–	Not used.
59	P00	–	Diode option input
60	P01	–	Not used.
61	P02	–	
62	P03	–	
63	P04	–	
64	P05	–	Reserved
65	ZOOM RST	I/O	Not used
66	V07	–	Not used
67	VSS	–	Ground
68	P10	–	Reserved
69	P11	–	
70	P12	–	
71	RXDO	O	Serial data to IC501 (Main µ-COM)
72	TXDO	I	Serial data input from IC501 (Main µ-COM)
73	SCKO	I	Serial clock input from IC501 (Main µ-COM)
74	F REQ	O	Request signal (active “LOW”) to IC501 (main µ-COM)
75	M RESET	O	Reset signal (active “LOW”) to IC501 (main µ-COM)
76	PWR CTL	O	Power control (active “HIGH”) to main board
77	P31	I/O	Not used.
78	P32	I	UP signal input from SW912
79	P33	I	Jog signal “JSW1” input, Not used
80	P34	I	Left signal input from SW915

Pin No.	Pin Name	I/O	Description
1	DAT1	I/O	Bi-directional data to DRAM
2	DAT2	I/O	Bi-directional data to DRAM
3	DAT3	I/O	Bi-directional data to DRAM
4	DAT4	I/O	Bi-directional data to DRAM
5	DAT5	I/O	Bi-directional data to DRAM
6	DAT6	I/O	Bi-directional data to DRAM
7	DAT7	I/O	Bi-directional data to DRAM
8	DAT8	I/O	Bi-directional data to DRAM
9	DAT9	I/O	Bi-directional data to DRAM
10	DAT10	I/O	Bi-directional data to DRAM
11	DAT11	I/O	Bi-directional data to DRAM
12	DAT12	I/O	Bi-directional data to DRAM
13	DAT13	I/O	Bi-directional data to DRAM
14	DAT14	I/O	Bi-directional data to DRAM
15	DAT15	I/O	Bi-directional data to DRAM
16	DAT16	I/O	Bi-directional data to DRAM
17	VSS	–	Digital ground
18	ADD1	O	Address output to DRAM
19	ADD2	O	Address output to DRAM
20	ADD3	O	Address output to DRAM
21	ADD4	O	Address output to DRAM
22	VDD	–	Digital power supply
23	ADD5	O	Address output to DRAM
24	ADD6	O	Address output to DRAM
25	ADD7	O	Address output to DRAM
26	ADD8	O	Address output to DRAM
27	ADD9	O	Address output to DRAM
28	X2_MCK	I	Master clock from oscillator for 2x decoding
29	VSS	–	Digital GND
30	MCK	I	Master clock from oscillator
31	VDD	–	Digital power supply
32	RAS	O	Row address strobe to DRAM
33	UCAS	O	Column address upper byte control strobe to DRAM
34	LCAS	O	Column address lower byte control strobe to DRAM
35	WE	O	Write enable signal to DRAM
36	OE	O	Output enable signal to DRAM
37	SCAN_IN	I	Scan data input
38	TEST_SE	I	Test mode selection (low for normal)
39	TEST_OUT12	O	Test output (Not used)
40	TEST_OUT11	O	Test output (Not used)
41	TEST_OUT10	O	Test output (Not used)
42	TEST_OUT9	O	Test output (Not used)

Pin No.	Pin Name	I/O	Description
43	TEST_OUT8	O	Test output (Not used)
44	TEST_OUT7	O	Test output (Not used)
45	TEST_OUT6	O	Test output (Not used)
46	T_SEL	I	Test mode selection
47	TEST_OUT5	O	Test output (Not used)
48	TEST_OUT4	O	Test output (Not used)
49	TEST_OUT3	O	Test output (Not used)
50	TEST_OUT2	O	Test output (Not used)
51	TEST_OUT1	O	Test output (Not used)
52	TEST_OUT0	O	Test output (Not used)
53	TEST_SEL0	I	Test mode output selection
54	TEST_SEL1	I	Test mode output selection
55	TEST_SEL2	I	Test mode output selection
56	TEST_SEL3	I	Test mode output selection
57	TESTSERVO	I	TEST PIN (NORMAL STATE = H)
58	E_SIN	I	SERVO DSP PGM. DOWNLOADING DATA INPUT
59	E_CLK	I	SERVO DSP PGM. DOWNLOADING CLK
60	E_ENB	I	SERVO DSP DOWNLOADING ENABLE
61	E_DRB	I	SERVO DSP PGM. DOWNLOADING DIRECTION
62	VSS	–	Digital GND
63	SERVO_CLK	I	SERVO DSP CLOCK INPUT
64	E_SOUT	O	SERVO DSP PGM. DOWNLOADING DATA OUTPUT
65	VDD	–	Digital power supply
66	E_ST0	O	SERVO DSP DOWNLOADING STATUS 0 (Not used)
67	E_ST1	O	SERVO DSP DOWNLOADING STATUS 1 (Not used)
68	E_ST2	O	SERVO DSP DOWNLOADING STATUS 2 (Not used)
69	GPIO7	I/O	SERVO DSP GENERAL I/O: FSON(FOCUS OK INVERTING)
70	GPIO6	I/O	SERVO DSP GENERAL I/O: PSEL
71	GPIO5	I/O	SERVO DSP GENERAL I/O: ADADDR3
72	GPIO4	I/O	SERVO DSP GENERAL I/O: FKRST
73	GPIO3	I/O	SERVO DSP GENERAL I/O: FKSET (Not used)
74	GPIO2	I/O	SERVO DSP GENERAL I/O: FEL
75	GPIO1	I/O	SERVO DSP GENERAL I/O (Not used)
76	GPIO0	I/O	SERVO DSP GENERAL I/O: DSP_SENSE (Not used)
77	VSS	–	Digital GND
78	SENS	O	SERVO DSP INTERNAL STATUS MONITOR
79	VDD	–	Digital power supply
80	SCLK	I	Serial Command CLOCK
81	SDATA	I	Serial Command DATA
82	XLAT	I	Serial Command LATCH
83	AOUT1	O	FDO
84	AOUT2	O	TDO

Pin No.	Pin Name	I/O	Description
85	AVDD	–	Analog power supply for ADC
86	VCM	O	TDF
87	AGND	–	Analog GND for ADC
88	AOUT3	O	FMQ
89	AOUT4	O	D_VREF
90	DGND	–	Digital GND for ADC
91	RFVCM	I	TDF
92	VDD	–	Analog GND for ADC
93	AGND	–	TDF
94	VREFN	I	TDF
95	VREFP	I	TDF
96	INP	I	TDF
97	AGND	–	Analog GND for ADC
98	AIN4	I	TDF
99	AIN3	I	TDF
100	AVDD	–	Analog power for ADC
101	AIN2	I	TDF
102	AIN1	I	TDF
103	AIN0	I	TDF
104	ADCVCM	I	TDF
105	SCK	O	PLL clock output
106	EXT_AD0	I	ADC data input
107	EXT_AD1	I	ADC data input
108	EXT_AD2	I	ADC data input
109	EXT_AD3	I	ADC data input
110	EXT_AD4	I	ADC data input
111	EXT_AD5	I	ADC data input
112	SELEFM	I	EFMDATA INPUT SELECTION
113	EXCK	I	SUB DATA REQUEST INPUT (Not used)
114	SQCK	I	SUB Q DATA REQUEST
115	C16M	O	5.6448 MHz(DIGITAL OUT CLOCK) (Not used)
116	DOTX	O	CD DIGITAL DATA OUTPUT (Not used)
117	VDD	–	Digital power supply
118	SQSO	O	SUB Q DATA OUTPUT
119	VSS	–	Digital GND
120	PWMCH1	O	PWM CHANNEL1(x3 CARRIER)
121	PWMCH2	O	PWM CHANNEL1(x3 CARRIER)
122	PWMCH3	O	PWM CHANNEL1(x3 CARRIER):SLED DRIVE OUTPUT
123	PWMCH4	O	PWM CHANNEL1(x1 CARRIER):PDO_CTR PWM OUTPUT
124	PWMCH5	O	PWM CHANNEL1(x1 CARRIER):RF_GAIN_CTL PWM OUTPUT
125	PWMCH6	O	PWM CHANNEL1(x1 CARRIER):TE_BAL_CTL PWM OUTPUT
126	DEFECT_IN_A	I	EXTERNAL DEFECT INPUT PIN

Pin No.	Pin Name	I/O	Description
127	SI_ENC1	I	SLED ENCODER1 INPUT
128	SI_ENC2	I	SLED ENCODER2 INPUT
129	TZC	I	TRACK CROSS PULSE 2 INPUT
130	MIRR	I	TRACK CROSS PULSE 1 INPUT
131	MSDATAO	O	SERVO DSP INTENAL STATUS SERIAL OUTPUT
132	FOK	O	INTERNAL GENERATED FOK(Focus OK) H=OK
133	VDD	–	Digital power supply
134	DEFECT	O	INTERNAL GENERATED DEFECT : H=DEFECT
135	VSS	–	Digital GND
136	SLD_FG	O	SLD_FG=(SL_ENC1) XOR (SL_ENC2)
137	C_SIG	O	TRACK CROSS PULSE
138	COMP	O	TRACK CROSS MONITOR
139	INT1	O	SERVO DSP INTERRUPT 1 MONITOR(MICOM COMMAND INT)
140	INT2	O	SERVO DSP INTERRUPT 2 MONITOR(FOCUS SERVO INT)
141	VSS	–	Digital GND
142	INT3	O	SERVO DSP INTERRUPT 1 MONITOR(TRACK SERVO INT)
143	INT4	O	SERVO DSP INTERRUPT 1 MONITOR
144	VDD	–	Digital power supply
145	ADCSB	O	PLESSY D/A CHIP SELECTION
146	ADCOMP_	I	A/D 7824 A/D CONVERTER A/D CONVERSION END STATUS
147	VDCDATA0	I	A/D 7824 A/D CONVERTER DATA BUS0
148	VDCDATA1	I	A/D 7824 A/D CONVERTER DATA BUS1
149	VDCDATA2	I	A/D 7824 A/D CONVERTER DATA BUS2
150	VDCDATA3	I	A/D 7824 A/D CONVERTER DATA BUS3
151	VDCDATA4	I	A/D 7824 A/D CONVERTER DATA BUS4
152	VDCDATA5	I	A/D 7824 A/D CONVERTER DATA BUS5
153	VDCDATA6	I	A/D 7824 A/D CONVERTER DATA BUS6
154	VDCDATA7	I	A/D 7824 A/D CONVERTER DATA BUS7
155	ADADDR0	O	A/D 7824 A/D CONVERTER ADDRESS
156	DVDD	–	Digital power supply for ADC
157	ADADDR1	O	A/D 7824 A/D CONVERTER ADDRESS
158	DGND	–	Digital GND for ADC
159	AGND	–	Analog GND for ADC
160	VRT	I	TDF
161	AVDD	–	Analog power supply for ADC
162	RF	I	TDF
163	VRM	I	TDF
164	VRB	I	TDF
165	MDS	O	Spindle motor control signal (Not used)
166	MDP	O	Spindle motor control signal
167	OVER64	O	Spindle motor reversal sensing signal output (Not used)

Pin No.	Pin Name	I/O	Description
168	MON	O	Spindle motor ON/OFF control signal
169	LOCK	O	CLV servo lock signal
170	FG_M	I	TDF
171	VSS	–	Digital GND
172	SCAN_OUT	O	SCAN DATA OUTPUT (Not used)
173	VDD	–	Digital power supply
174	INT	O	Interrupt request to Host
175	RN	I	Read strobe from HOST
176	WN	I	Write strobe from HOST
177	CS	I	Chip select from HOST
178	A0	I	Internal register address from HOST
179	A1	I	Internal register address from HOST
180	A2	I	Internal register address from HOST
181	A3	I	Internal register address from HOST
182	A4	I	Internal register address from HOST
183	A5	I	Internal register address from HOST
184	VSS	I	Digital GND
185	PS0	I/O	Bi-directional data to Host
186	VDD	–	Digital power supply
187	PS1	I/O	Bi-directional data to Host
188	PS2	I/O	Bi-directional data to Host
189	PS3	I/O	Bi-directional data to Host
190	PS4	I/O	Bi-directional data to Host
191	PS5	I/O	Bi-directional data to Host
192	PS6	I/O	Bi-directional data to Host
193	PS7	I/O	Bi-directional data to Host
194	RESET	I	HARDWARE RESET
195	REQ_DIVX	I	Data request from DIVX module (Not used)
196	REQ_MPEG	I	Data request from MPEG
197	MPEG1	O	MPEG data
198	MPEG2	O	MPEG data
199	MPEG3	O	MPEG data
200	MPEG4	O	MPEG data
201	MPEG5	O	MPEG data
202	MPEG6	O	MPEG data
203	MPEG7	O	MPEG data
204	MPEG8	O	MPEG data
205	SENB	O	MPEG data valid signal (low for valid)
206	SDCLK	O	MPEG data transfer clock
207	SERR	O	MPEG data error detection signal (low indicates error occurred)
208	SYNC	O	SERVO DSP INTERRUPT 1 MONITOR(MICOM COMMAND INT) (Not used)

Pin No.	Pin Name	I/O	Description
1	$\overline{RD}$	I	Read strobe in I mode. Must be held HIGH in M Mode.
2	R/$\overline{W}$	I	Read/write strobe in M mode. Write strobe in I mode. Host asserts R/$\overline{W}$ LOW to select Write and LOW to select Read for M Mode only.
3	VDD_3.3	–	3.3-V supply voltage for I/O signals.
4	$\overline{WAIT}$	O	Transfer not complete / data acknowledge. Active LOW to indicate host initiated transfer is not complete. $\overline{WAIT}$ is asserted after the falling edge of $\overline{CS}$ and reasserted when decoder is ready to complete transfer cycle. Open drain signal, must be pulled-up via 1k ohm to 3.3 volts. Driven high for 10 ns before tristate.
5	$\overline{RESET}$	I	Active Low Reset. Assert for at least 5-milliseconds in the presence of clock to reset the entire chip.
6	VSS	–	Ground for core logic and I/O signals.
7	VDD_3.3_5	–	3.3/5-V supply voltage for I/O signals.
8	$\overline{INT}$	O	Host interrupt. Open drain signal, must be pulled-up via 4.7k ohm to 3.3 volts. Driven high for 10 ns before tristate.
9 ~ 12	NC	O	Not used
13	VDD_2.5	–	2.5-V supply voltage for core logic.
14	VSS	–	Ground for core logic and I/O signals.
15 ~ 18	NC	O	Not used
19	VSS	–	Ground for core logic and I/O signals.
20	VDD_3.3_5	–	3.3/5-V supply voltage for I/O signals.
21 ~ 28	VDATA0 ~ VDATA7	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA.
29	$\overline{VSYNC}$	I/O	Vertical sync. Bi-directional, the decoder outputs the top border of a new field on the first $\overline{HSYNC}$ after the falling edge of $\overline{VSYNC}$. $\overline{VSYNC}$ can accept vertical synchronization or top/ bottom field notification from an external source. ($\overline{VSYNC}$ HIGH = bottom field. $\overline{VSYNC}$ LOW = Top field)
30	$\overline{HSYNC}$	I/O	Horizontal sync. The decoder begins outputting pixel data for a new horizontal line after the falling (active) edge of $\overline{HSYNC}$.
31	VSS	–	Ground for core logic and I/O signals.
32	VDD_3.3_5	–	3.3/5-V supply voltage for I/O signals.
33 ~ 35	NC	O	Not used
36	VDD_2.5	–	2.5-V supply voltage for core logic.
37	VSS	–	Ground for core logic and I/O signals.
38 ~ 42	NC	O	Not used
43	PIO0	I/O	Programmable I/O pins.
44	VSS	–	Ground for core logic and I/O signals.
45	VDD_3.3_5	–	3.3/5-V supply voltage for I/O signals.
46 ~ 52	PIO1 ~ PIO7	I/O	Programmable I/O pins.
53, 54	MDATA0, MDATA1	I/O	SDRAM Data
55	VDD_3.3	–	3.3-V supply voltage for I/O signals.
56	VSS	–	Ground for core logic and I/O signals.

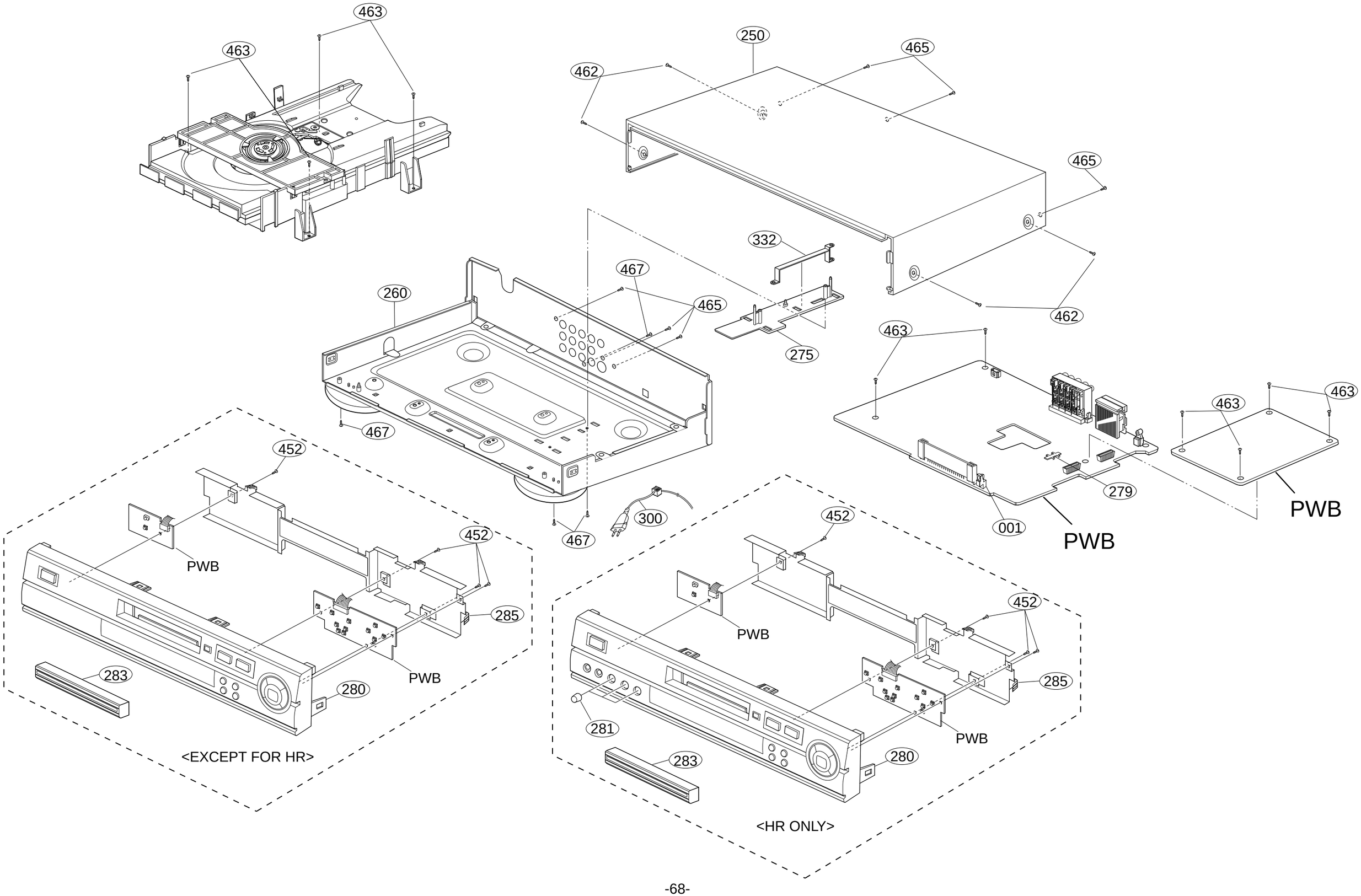
Pin No.	Pin Name	I/O	Description
57 ~ 62	MDATA2 ~ MDATA7	I/O	SDRAM Data
63	MDATA15	I/O	SDRAM Data
64	VDD_3.3	–	3.3-V supply voltage for I/O signals.
65	VSS	–	Ground for core logic and I/O signals.
66	MDATA14	I/O	SDRAM Data
67	VDD_2.5	–	2.5-V supply voltage for core logic.
68	VSS	–	Ground for core logic and I/O signals.
69 ~ 73	MDATA13 ~ MDATA9	I/O	SDRAM Data
74	VDD_3.3	–	3.3-V supply voltage for I/O signals.
75	VSS	–	Ground for core logic and I/O signals.
76	MDATA8	I/O	SDRAM Data
77	LDQM	O	SDRAM Lower or Upper Mask
78	SD-CLK	O	SDRAM Clock
79	CLKSEL	I	Selects SYSCLK or VCLK as clock source. Normal operation is to tie HIGH.
80, 81	MADDR9, MADDR8	O	SDRAM Address
82	VDD_3.3	–	3.3-V supply voltage for I/O signals.
83	VSS	–	Ground for core logic and I/O signals.
84 ~ 86	MADDR7 ~ MADDR5	O	SDRAM Address
87	VDD_2.5	–	2.5-V supply voltage for core logic.
88	VSS	–	Ground for core logic and I/O signals.
89	MADDR4	O	SDRAM Address
90	$\overline{\text{MWE}}$	O	SDRAM Write Enable
91	$\overline{\text{SD-CAS}}$	O	Active LOW SDRAM Column Address
92	VDD_3.3	–	3.3-V supply voltage for I/O signals.
93	VSS	–	Ground for core logic and I/O signals.
94	$\overline{\text{SD-RAS}}$	O	Active LOW SDRAM Row Address
95	$\overline{\text{SD-CS0}}$	O	Active LOW SDRAM Chip Select 0
96	$\overline{\text{SD-CS1}}$/MADDR11	O	Active LOW SDRAM Chip Select 1 or use as MADDR11 for larger SDRAM (64 Mbits).
97	$\overline{\text{SD-BS}}$	O	SDRAM Bank Select
98	MADDR10	O	SDRAM Address
99	MADDR0	O	SDRAM Address
100	VDD_3.3	–	3.3-V supply voltage for I/O signals.
101	VSS	–	Ground for core logic and I/O signals.
102 ~ 104	MADDR1 ~ MADDR3	O	SDRAM Address
105	VSS ADC	I	Not used
106 ~ 111	NC	–	Not used
112	DAI XCK	I	Tie to VSS or VDD_3.3
113	DAI-LRCK	I	PCM left/right clock.
114	DAI-BCK	I	PCM input bit clock.
115	VDD_3.3	–	3.3-V supply voltage for I/O signals.
116	VSS	–	Ground for core logic and I/O signals.

Pin No.	Pin Name	I/O	Description
117	DAI-DATA	I	PCM data input.
118 ~ 121	DA-DATA3~ DA-DATAO	O	PCM Data Out. Eight channels. Serial audio samples relative to DA_BCK and DA_LRCK.
122	DA-LRCK	O	PCM Left Clock. Identifies the channel for each sample. The polarity is programmable.
123	VDD_3.3	–	3.3-V supply voltage for I/O signals.
124	VSS	–	Ground for core logic and I/O signals.
125	DA-XCK	I/O	Audio External Frequency Clock input or output. DA_BCK and DA_LRCK are derived from this clock. DA_XCK can be 384 or 256 times the sampling frequency.
126	DA-BCK	O	PCM Bit Clock. Divided by 8 from DA_XCK. DA_BCK can be either 48 or 32 times the sampling frequency.
127	DA-IEC	O	PCM data out in IEC-958 format or compressed data out in IEC-1937 format.
128	VDD_2.5	–	2.5-V supply voltage for core logic.
129	VSS	–	Ground for core logic and I/O signals.
130	NC	–	Not used
131	VSS_DAC	–	Analog Video DAC Ground.
132	VSS_VIDEO	–	Analog Video Ground.
133	CVBS +sync	O	DAC video output format
134	VDD_DAC	–	3.3-V Analog Video Power.
135	VDD_VIDEO	–	3.3-V Analog Video Power.
136	NC	–	Not used
137	VSS_DAC	–	Analog Video DAC Ground.
138	VSS_VIDEO	–	Analog Video Ground.
139	CVBS/G/Y	O	DAC video output format.
140	VDD_DAC	–	3.3-V Analog Video Power.
141	VDD VIDEO	–	3.3-V Analog Video Power.
142	NC	–	Not used
143	VSS_DAC	–	Analog Video DAC Ground.
144	VSS_VIDEO	–	Analog Video Ground.
145	Y/B/U	O	DAC video output format
146	VDD DAC	–	3.3-V Analog Video Power.
147	VDD_VIDEO	–	3.3-V Analog Video Power.
148	NC	–	Not used
149	VSS_DAC	–	Analog Video DAC Ground.
150	VSS_VIDEO	–	Analog Video Ground.
151	C/R/V	O	DAC video output format
152	VDD DAC	–	3.3-V Analog Video Power.
153	VDD_VIDEO	–	3.3-V Analog Video Power.
154	VSS_RREF	–	Analog Video Ground.
155	RREF	I	Reference Resistor. Connecting to pin 139 through a 4.7k ± 1% resistor is recommended
156	VDD_RREF	–	3.3-V Analog Video Power.
157	A_VSS	–	Analog PLL Ground.
158	SYSCLK	I	Optional System Clock. Tie to A_VDD through a 1k Ohm resistor

Pin No.	Pin Name	I/O	Description
159	VCLK	I	Video clock. Clocks out data on input. VDATA[7:0]. Clock is typically 27 MHz. System clock that drives internal PLLs and internal DENC. ZiVA-4 requires an external 27-MHz TTL oscillator.
160	A_VDD	–	3.3-V Analog PLL Power
161	DVD-DATA0/CD-DATA	I	Serial CD data. This pin is shared with DVD compressed data DVD-DATA0.
162	DVD-DATA1/ CD-LRCK	I	Programmable polarity 16-bit word synchronization to the decoder (right channel HIGH). This pin is shared with DVD compressed data DVD-DATA1.
163	DVD-DATA2/ CD-BCK	I	CD bit clock. Decoder accept multiple BCK rates. This pin is shared with DVD compressed data DVD-DATA2.
164	DVD-DATA3/ CD-C2P0	I	Asserted HIGH indicates a corrupted byte. Decoder keeps the previous valid picture on-screen until the next valid picture is decoded. This pin is shared with DVD compressed data DVD-DATA3.
165	DVD-DATA4/ CDG-SDATA	I	DVD parallel compressed data from DVD DSP. Or CD+G (Subcode) data indicating serial subcode data input.
166	VSS	–	Ground for core logic and I/O signals.
167	VDD_3.3	–	3.3-V supply voltage for I/O signals.
168	DVD-DATA5/ CDG-VFSY	I	DVD parallel compressed data from DVD DSP. Or CD+G (Subcode) Frame Sync indicating frame-start or composite synchronization input.
169	DVD-DATA6/ CDG-SOS1	I	DVD parallel compressed data from DVD DSP. Or CD+G (Subcode) Block Sync indicating block-start synchronization input.
170	DVD-DATA7/ CDG-SCLK	I	DVD parallel compressed data from DVD DSP. Or CD+G (Subcode) Clock indicating subcode data clock input or output.
171	VDACK	I	In synchronous mode, bitstream data acknowledge. Asserted when DVD data is valid. Polarity is programmable.
172	VREQUEST	O	Bitstream request. Decoder asserts VREQUEST to indicate that the bitstream input buffer has available space. Polarity is programmable.
173	VSTROBE	I	Bitstream strobe. Programmable dual mode pulse. Asynchronous and synchronous. In Asynchronous mode, an external source pulses VSTROBE to indicate data is ready for transfer. In synchronous mode, VSTROBE clocks data.
174	ERROR	I	Error in input data. If ERROR signal is not available from the DSP it must be grounded.
175	VDD_3.3	–	3.3-V supply voltage for I/O signals.
176	RESERVED	I	Tie to VSS or VDD_3.3
177	VDD_3.3	–	3.3-V supply voltage for I/O signals.
178	VSS	–	Ground for core logic and I/O signals.
179	NC	–	Not used
180	RESERVED	I	Tie to VSS or VDD_3.3
181	NC	–	Not used
182 ~ 184	HADDR0 ~ HADDR2	I	Host address bus. 3-bit address bus selects one of eight host interface registers.
185 ~ 187	RESERVED	I	Tie to VSS or VDD_3.3
188	VSS	–	Ground for core logic and I/O signals.

Pin No.	Pin Name	I/O	Description
189	VDD_2.5	–	2.5-V supply voltage for core logic.
190	RESERVED	I	Tie to VSS or VDD_3.3.
191	VSS	–	Ground for core logic and I/O signals.
192	VDD_3.3	–	3.3-V supply voltage for I/O signals.
193 ~ 196	RESERVED	I	Tie to VSS or VDD_3.3.
197	HDATA7	I/O	HDATA[7] is the 8-bit bi-directional host data bus through which the host writes data to the decoder Code FIFO. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM/ROM via HDATA[7].
198	VSS	–	Ground for core logic and I/O signals.
199	HDATA6	I/O	HDATA[6 ~ 2] is the 8-bit bi-directional host data bus through which the host writes data to the decoder Code FIFO. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM/ROM via HDATA[6 ~ 2].
200	HDATA5	I/O	
201	HDATA4	I/O	
202	HDATA3	I/O	
203	HDATA2	I/O	
204	VDD_3.3	–	3.3-V supply voltage for I/O signals.
205	VSS	–	Ground for core logic and I/O signals.
206	HDATA1	I/O	HDATA[1, 0] is the 8-bit bi-directional host data bus through which the host writes data to the decoder Code FIFO. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM/ROM via HDATA[1, 0].
207	HDATA0	I/O	
208	$\overline{CS}$	I	Host chip select. Host asserts $\overline{CS}$ to select the decoder for a read or write operation. The falling edge of this signal triggers the read or write operation.

MECHANICAL EXPLODED VIEW 1/1



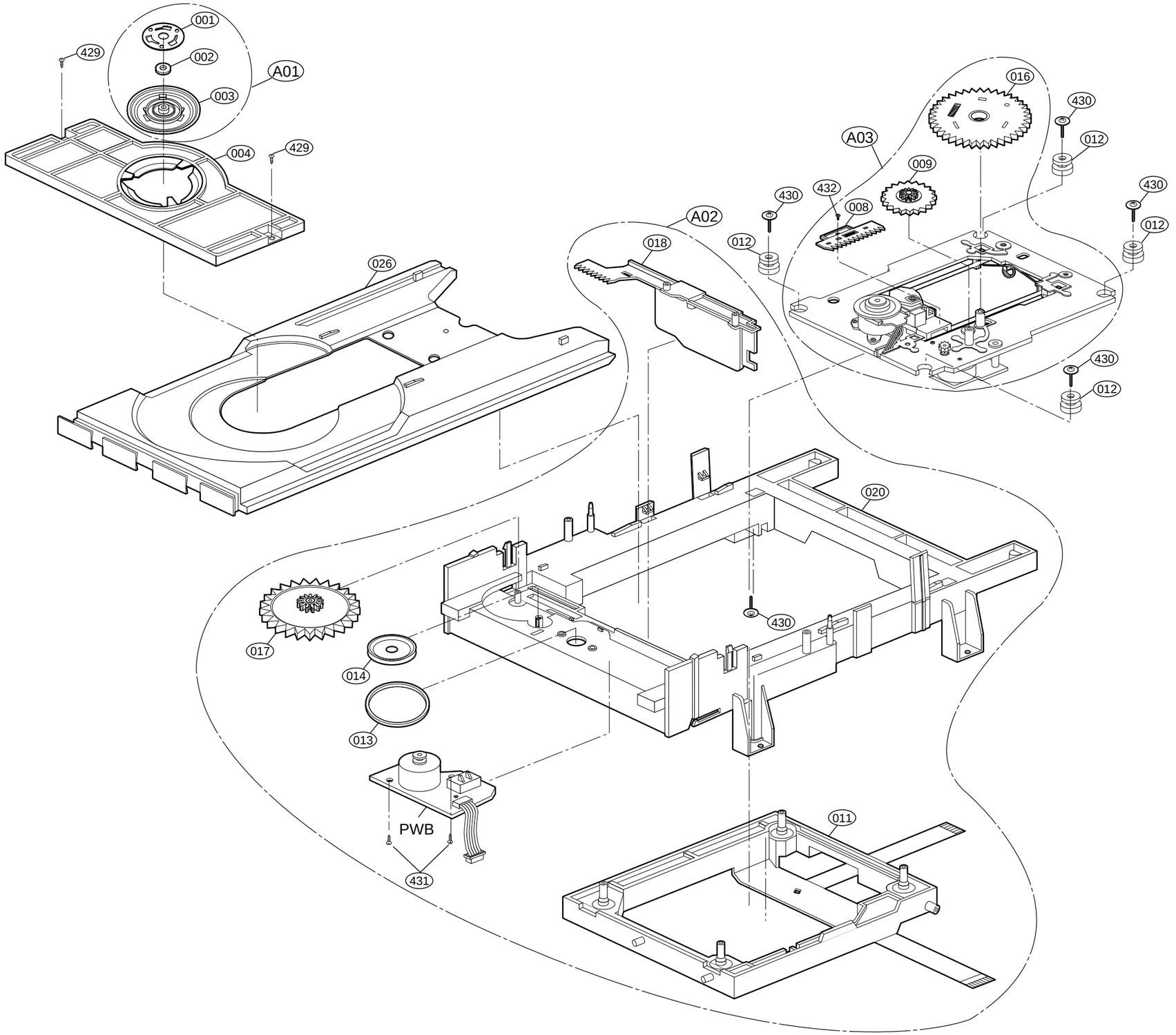
MECHANICAL MAIN PARTS LIST 1/1

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
001	S9-30R-018-5A0		HOLDER DIGITRON
250	S1-10R-018-4G0		CASE TOP<HRN,KN,EZN>
250	S1-10R-018-4A0		CASE TOP<UB,EZB>
260	———		CHASSIS ASSY MAIN
275	S9-30R-018-3A0		HOLDER MAIN PCB
279	S9-30R-019-9A0		HOLDER CONNECTOR
280	S7-21R-F15-7B0		PANEL ASSY FRONT<HRN>
280	S7-21R-F15-7A0		PANEL ASSY FRONT<UB>
280	S7-21R-F15-7C0		PANEL ASSY FRONT<KN,EZN>
280	S7-21R-F15-7D0		PANEL ASSY FRONT<EZB>
281	S9-40R-V01-0A0		KNOB,VOLUME<HRN>
283	S5-81R-T00-6B0		DOOR ASSY TRAY<HRN,KN,EZN>
283	S5-81R-T00-6A0		DOOR ASSY TRAY<UB,EZB>
285	———		PLATE ASSY
⚠ 300	S4-10R-CHR-02C		POWER CORD<HRN,EZB,EZN>
⚠ 300	S4-10R-AHC-02B		POWER CORD<UB>
⚠ 300	S4-10R-LHR-02E		POWER CORD<KN>
332	———		PLATE MAIN
452	S3-530-51A-000		SCREW,SPECIAL
462	S3-530-85A-000		SCREW,DECORATION
463	S3-530-51B-000		SPECIAL SCREW
465	S3-530-46K-000		SPECIAL SCREW 3-10 B.K
467	S3-530-46N-000		SPECIAL SCREW 3-8 BK

COLOR NAME TABLE

Basic color symbol	Color	Basic color symbol	Color	Basic color symbol	Color
B	Black	C	Cream	D	Orange
G	Green	H	Gray	L	Blue
LT	Transparent Blue	N	Gold	P	Pink
R	Red	S	Silver	ST	Titan Silver
T	Brown	V	Violet	W	White
WT	Transparent White	Y	Yellow	YT	Transparent Yellow
LM	Metallic Blue	LL	Light Blue	GT	Transparent Green
LD	Dark Blue	DT	Transparent Orange	GM	Metallic Green
YM	Metallic Yellow	DM	Metallic Orange	PT	Transparent Pink
LA	Aqua Blue	GL	Light Green		

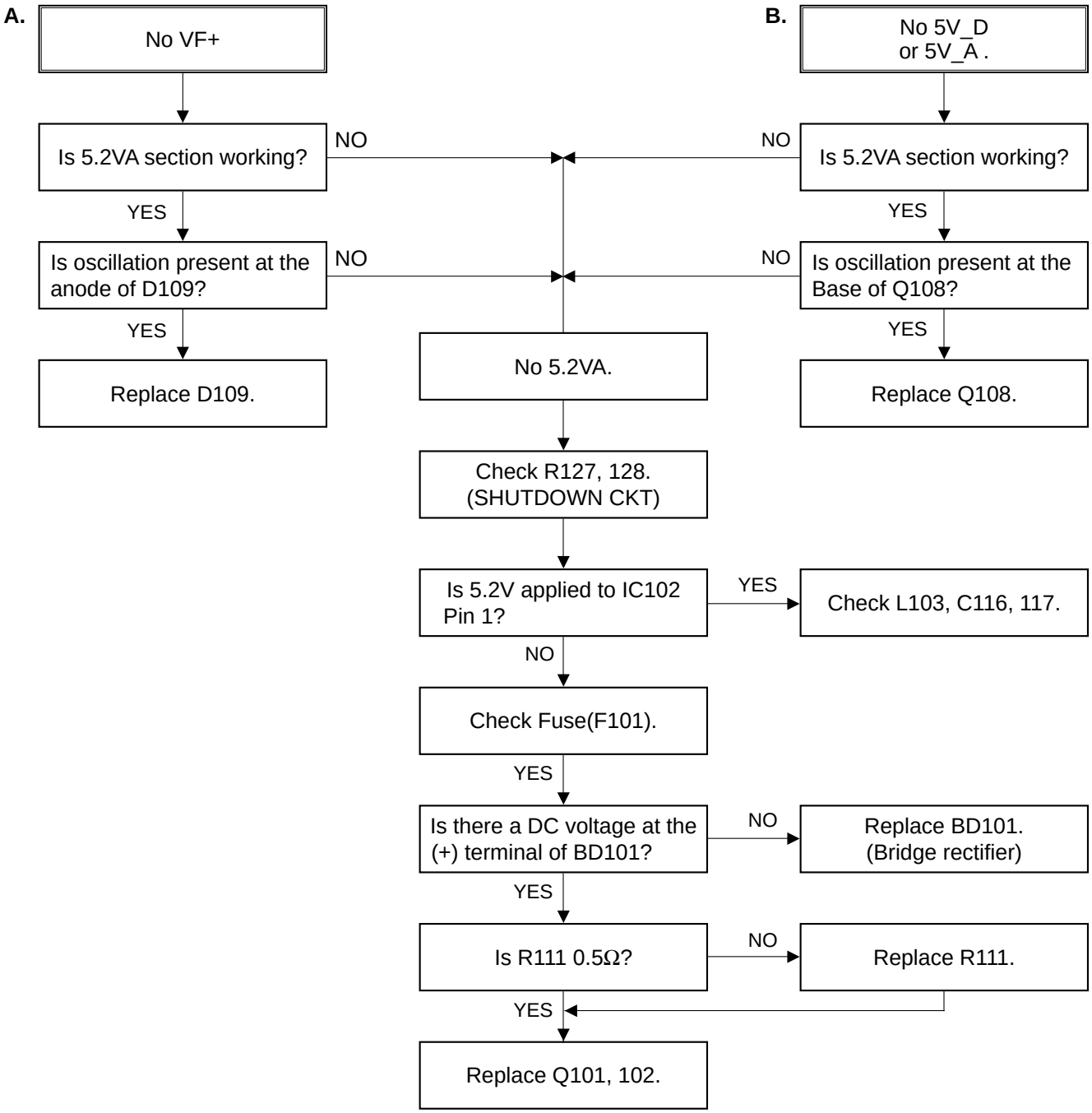
DVD MECHANISM EXPLODED VIEW 1/1



DVD MECHANISM MAIN PARTS LIST 1/1

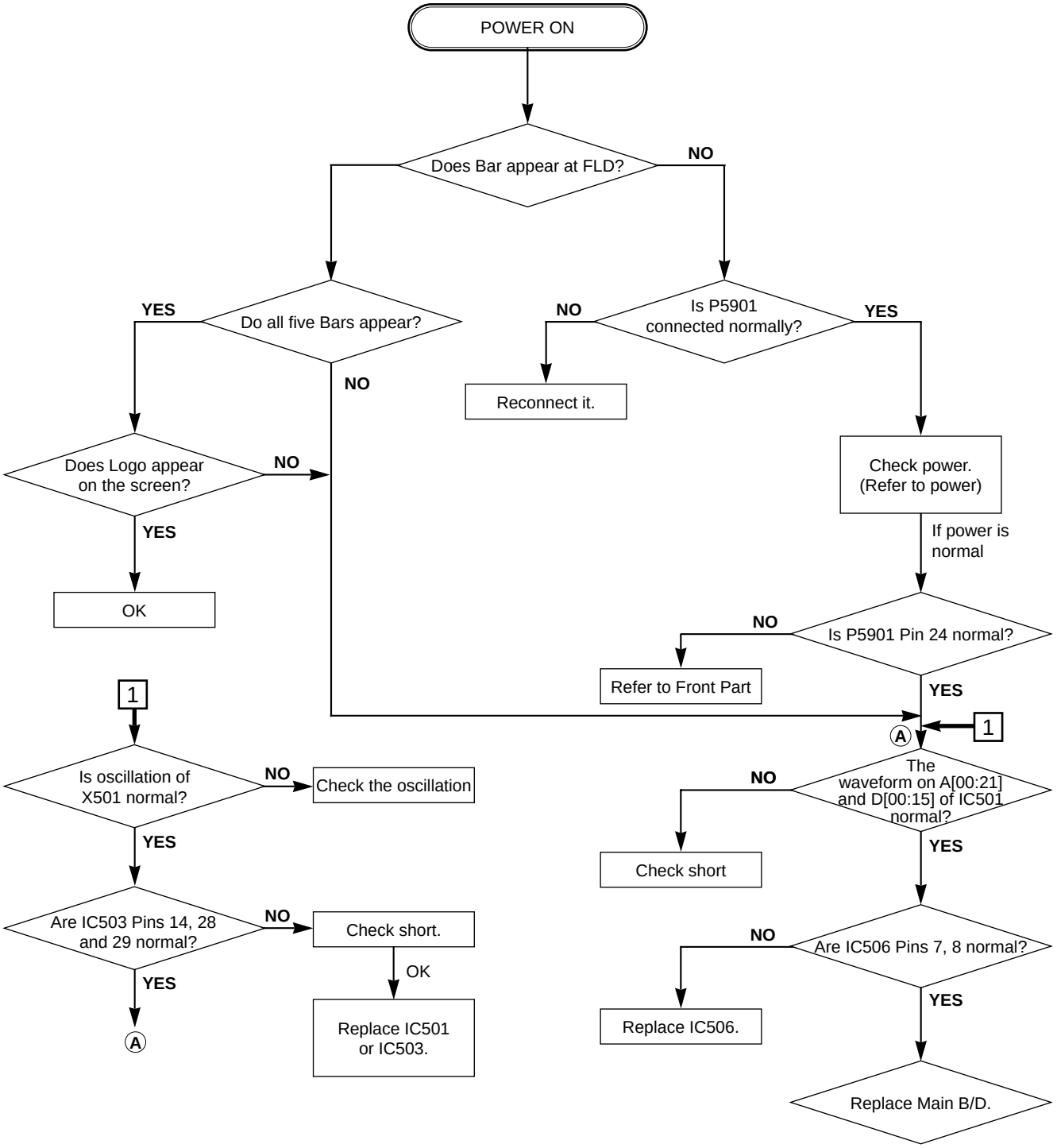
REF. NO	PART NO.	KANRI NO.	DESCRIPTION
001	S3-00R-054-7A0		PLATE CLAMP
002	———		CLAMP MAGNET 8,10-5,1-1.5
003	———		CLAMP UPPER
004	S9-30R-017-1A0		HOLDER CLAMP
008	S4-70R-004-7A0		GEAR ASSY RACK<HRN,UB,KN>
008	S4-70R-008-0A0		GEAR ASSY, RACK<EZB,EZN>
009	S4-70R-005-3A0		GEAR MIDDLE<HRN,UB,KN>
009	S4-70R-007-9A0		GEAR MIDDLE<EZB,EZN>
011	S2-11R-002-1B0		FRAME ASSY<HRN,UB,KN>
011	S2-11R-002-8A0		FRAME ASSY UP/DOWN<EZB,EZN>
012	———		RUBBER REAR
013	S4-00R-000-6A0		BELT LOADING
014	S4-70R-005-5A0		GEAR PULLEY
016	S4-70R-005-0A0		GEAR ASSY FEED<HRN,UB,KN>
016	S4-70R-008-1A0		GEAR ASSY, PINION<EZB,EZN>
017	S4-70R-005-6A0		GEAR LOADING
018	S9-74R-002-3A0		GUIDE UP/DOWN
020	———		BASE MAIN
026	S3-90R-000-5A0		TRAY DISC<HRN,UB,KN>
026	S3-90R-001-0A0		TRAY DISC<EZB,EZN>
429	SS-ZZR-001-2A0		SCREW,B-TITE
430	SS-ZZH-100-3A0		SCREW,+D2.0-6MM
431	87-741-035-410		SCREW,2.0-6
432	———		SCREW,MACHINE
A01	S8-61R-000-6A0		CLAMP ASSY DISC
A02	S0-41R-001-0C0		BASE ASSY MAIN<HRN,UB,KN>
A02	S0-41R-002-0A0		BASE ASSY MAIN<EZB,EZN>
A03	S0-41R-001-7A0		BASE ASSY SLED<HRN,UB,KN>
A03	S0-41R-001-8A0		BASE ASSY SLED<EZB,EZN>

1. Power(SMPS) Circuit

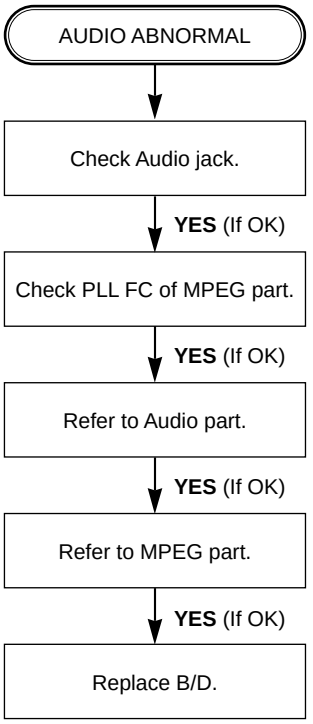


2. µ-COM Circuit

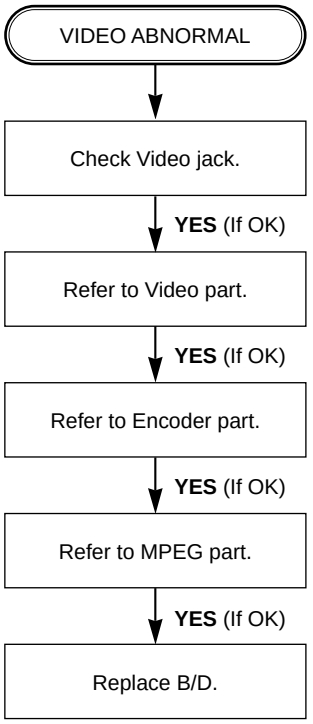
A. No Power



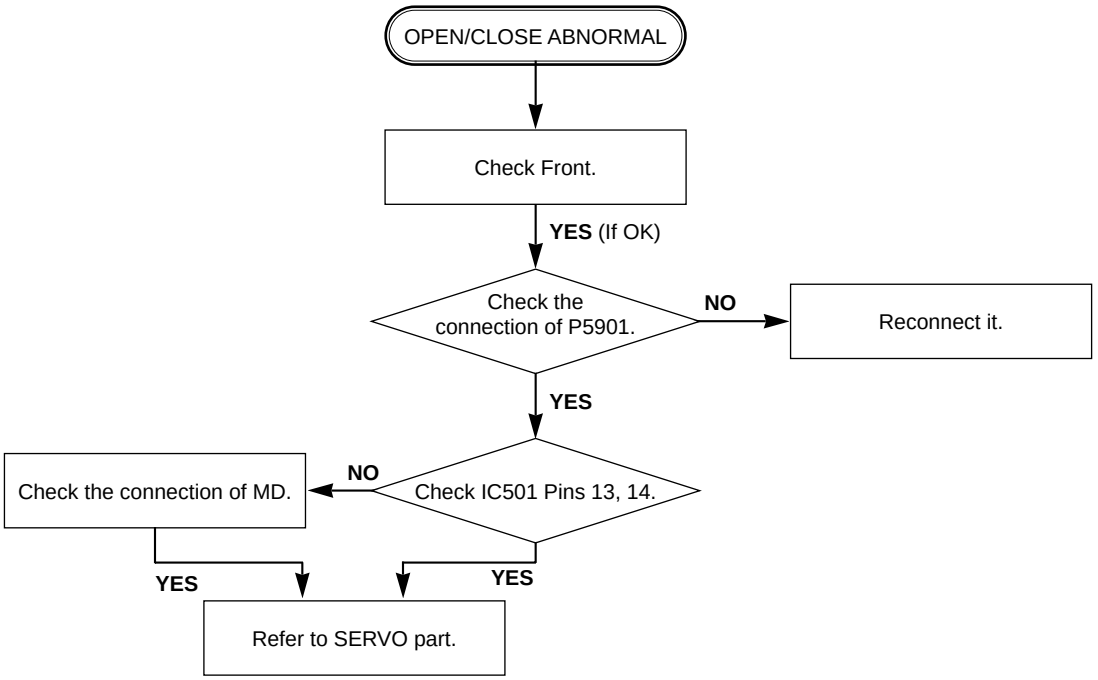
B. Audio abnormal



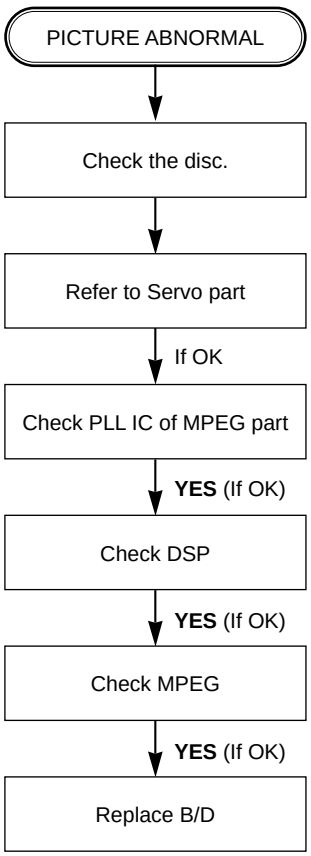
C. Video abnormal



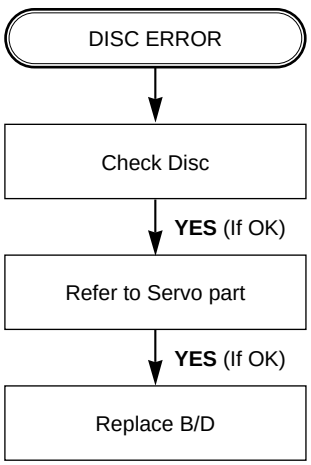
D. Open/Close abnormal



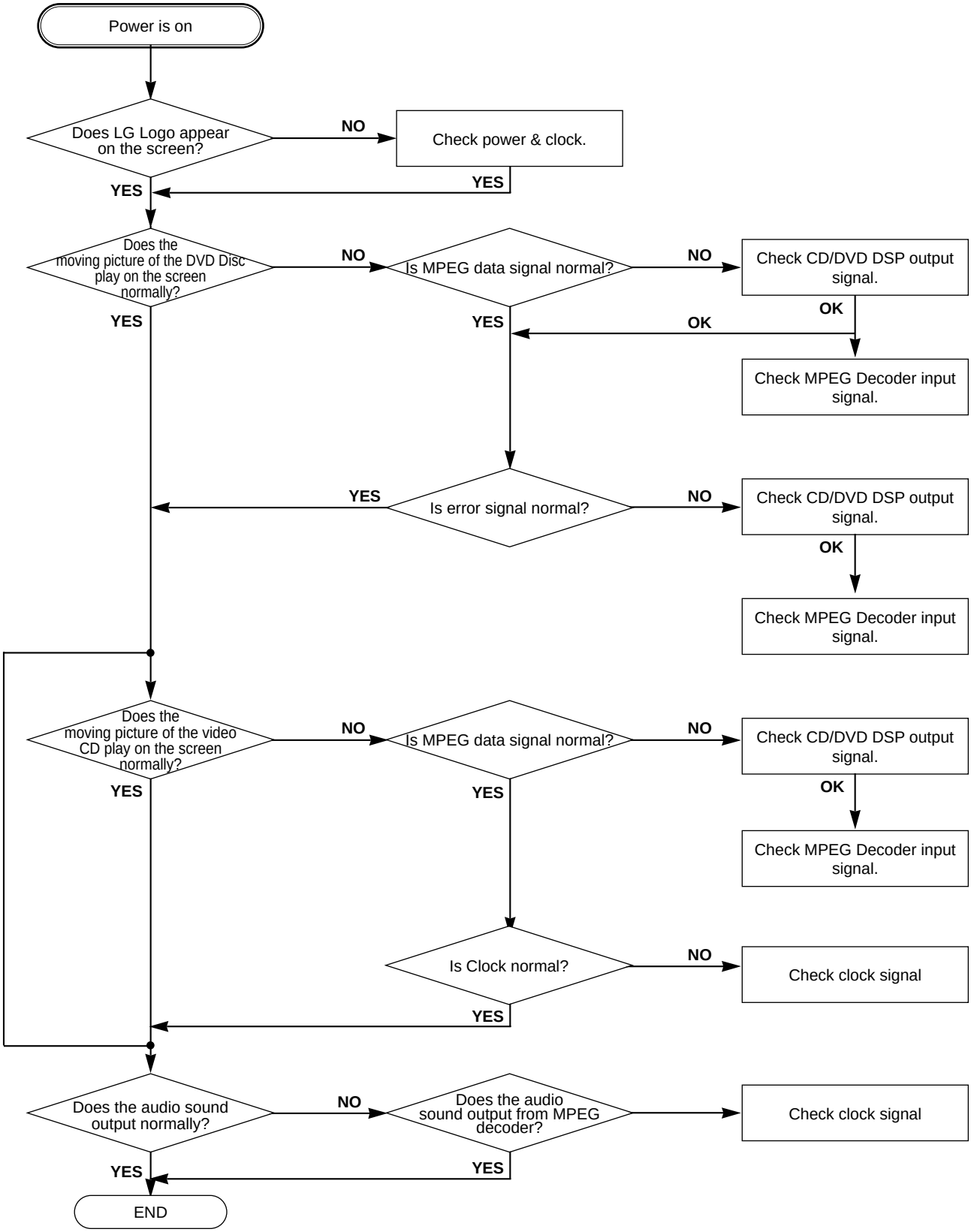
E. Picture abnormal



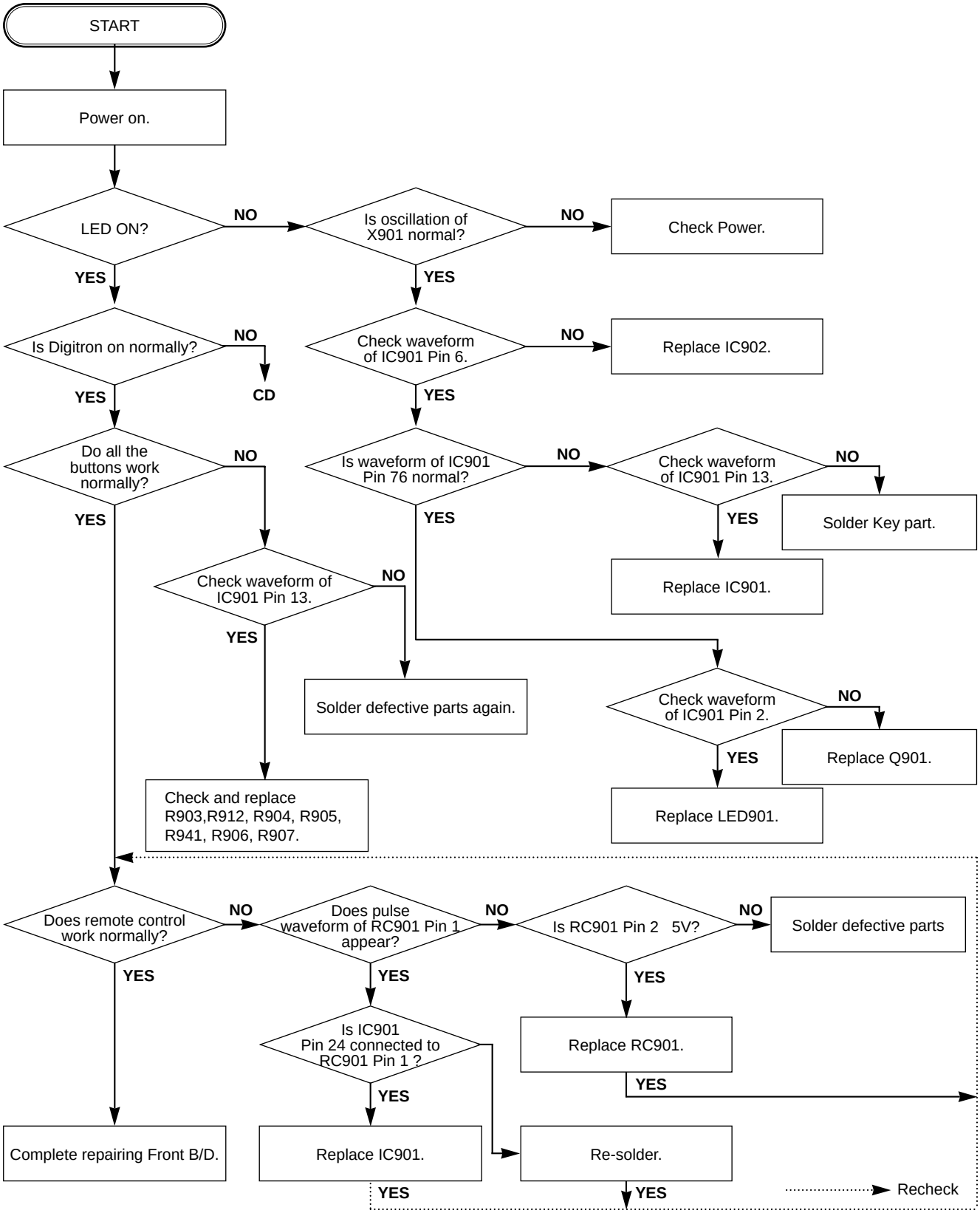
F. Disc Error



3. MPEG Circuit

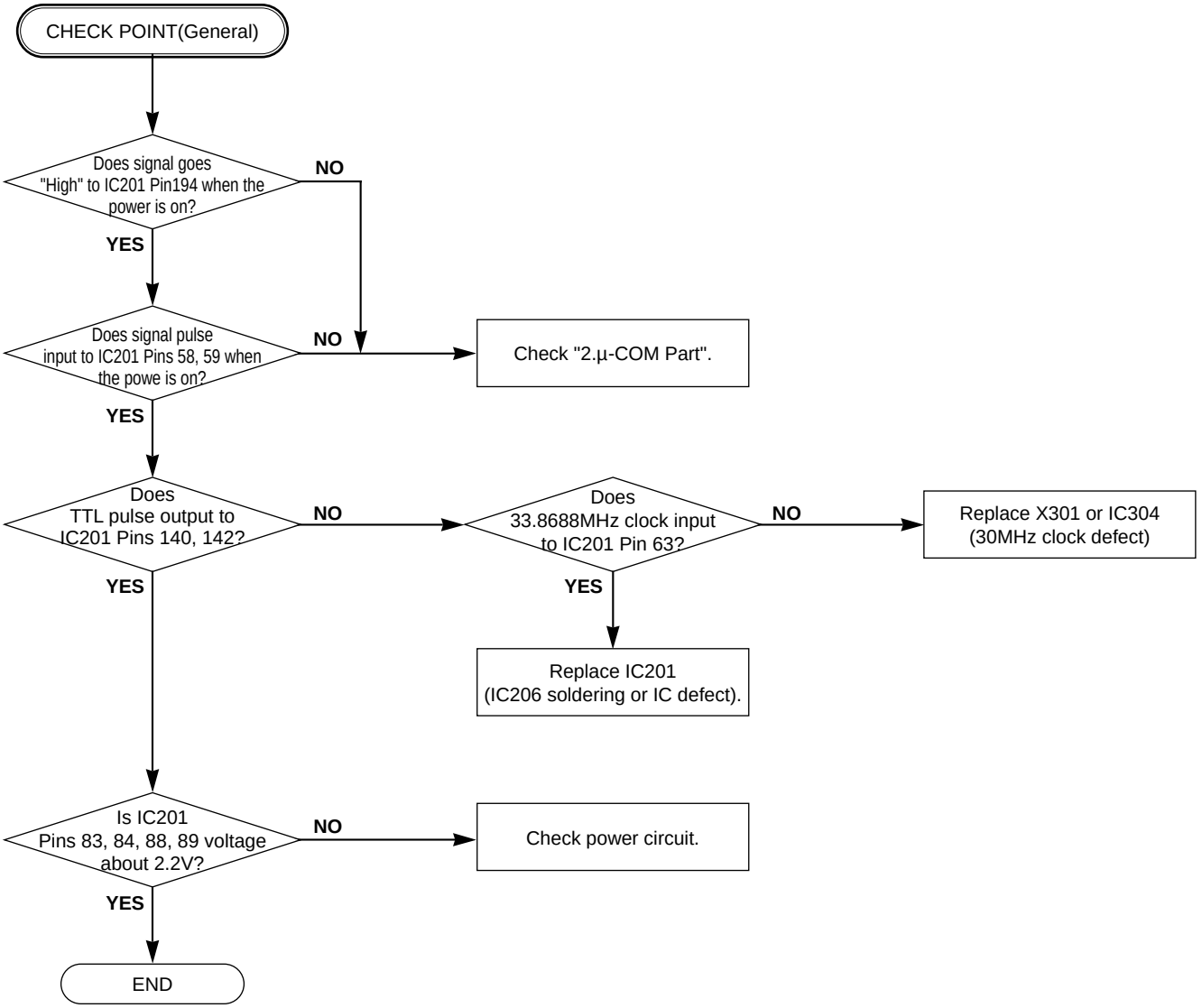


4. Front Circuit (Digitron & key)

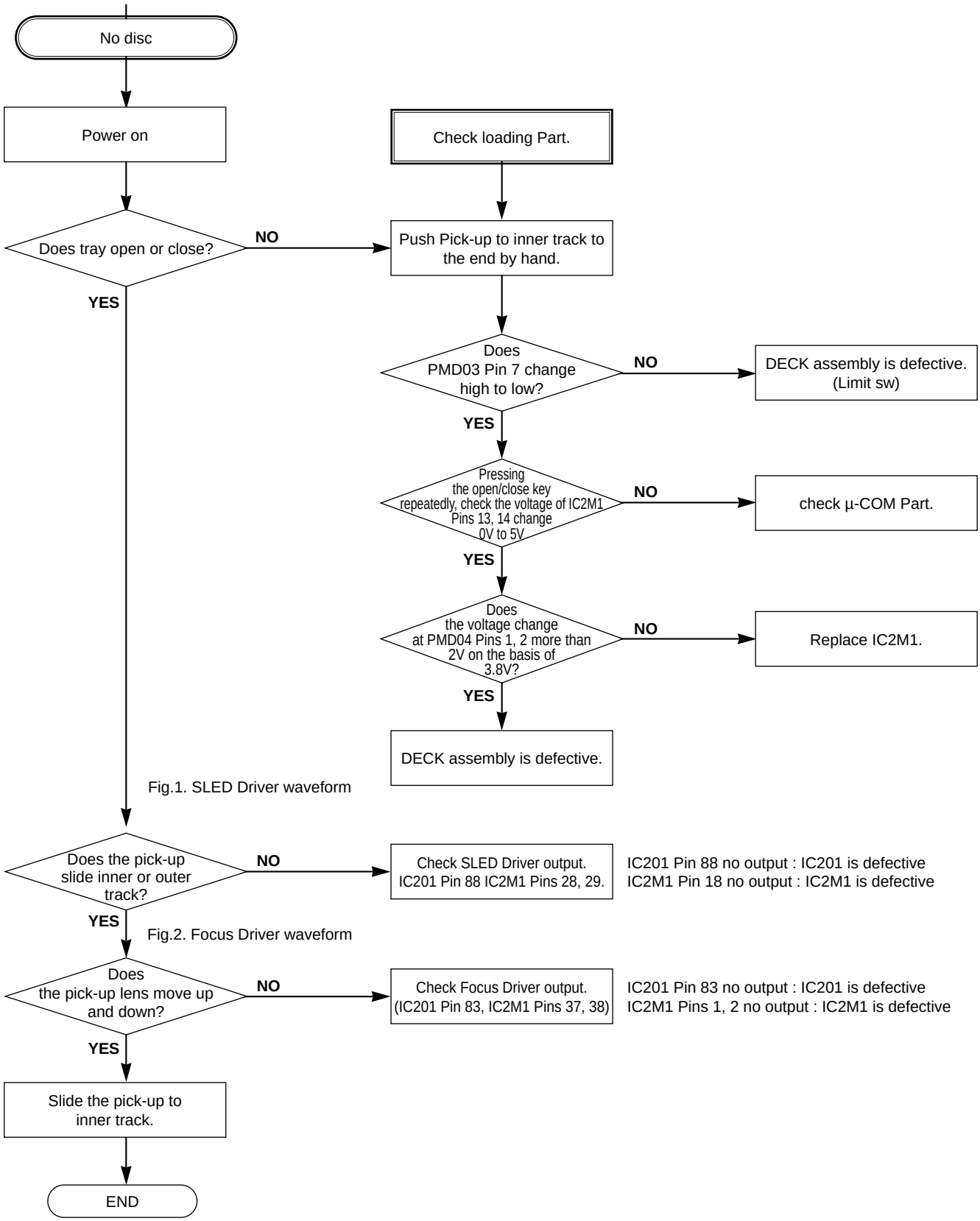


5. RF/Servo Circuit

A.



B.


No disc
Power on
Does tray open or close?
NO
YES
Check loading Part.
Push Pick-up to inner track to the end by hand.
Does PMD03 Pin 7 change high to low?
NO
DECK assembly is defective. (Limit sw)
YES
Pressing the open/close key repeatedly, check the voltage of IC2M1 Pins 13, 14 change 0V to 5V
NO
check µ-COM Part.
YES
Does the voltage change at PMD04 Pins 1, 2 more than 2V on the basis of 3.8V?
NO
Replace IC2M1.
YES
DECK assembly is defective.
Fig.1. SLED Driver waveform
Does the pick-up slide inner or outer track?
NO
Check SLED Driver output. IC201 Pin 88 IC2M1 Pins 28, 29.
IC201 Pin 88 no output : IC201 is defective
IC2M1 Pin 18 no output : IC2M1 is defective
YES
Fig.2. Focus Driver waveform
Does the pick-up lens move up and down?
NO
Check Focus Driver output. (IC201 Pin 83, IC2M1 Pins 37, 38)
IC201 Pin 83 no output : IC201 is defective
IC2M1 Pins 1, 2 no output : IC2M1 is defective
YES
Slide the pick-up to inner track.
END

C.

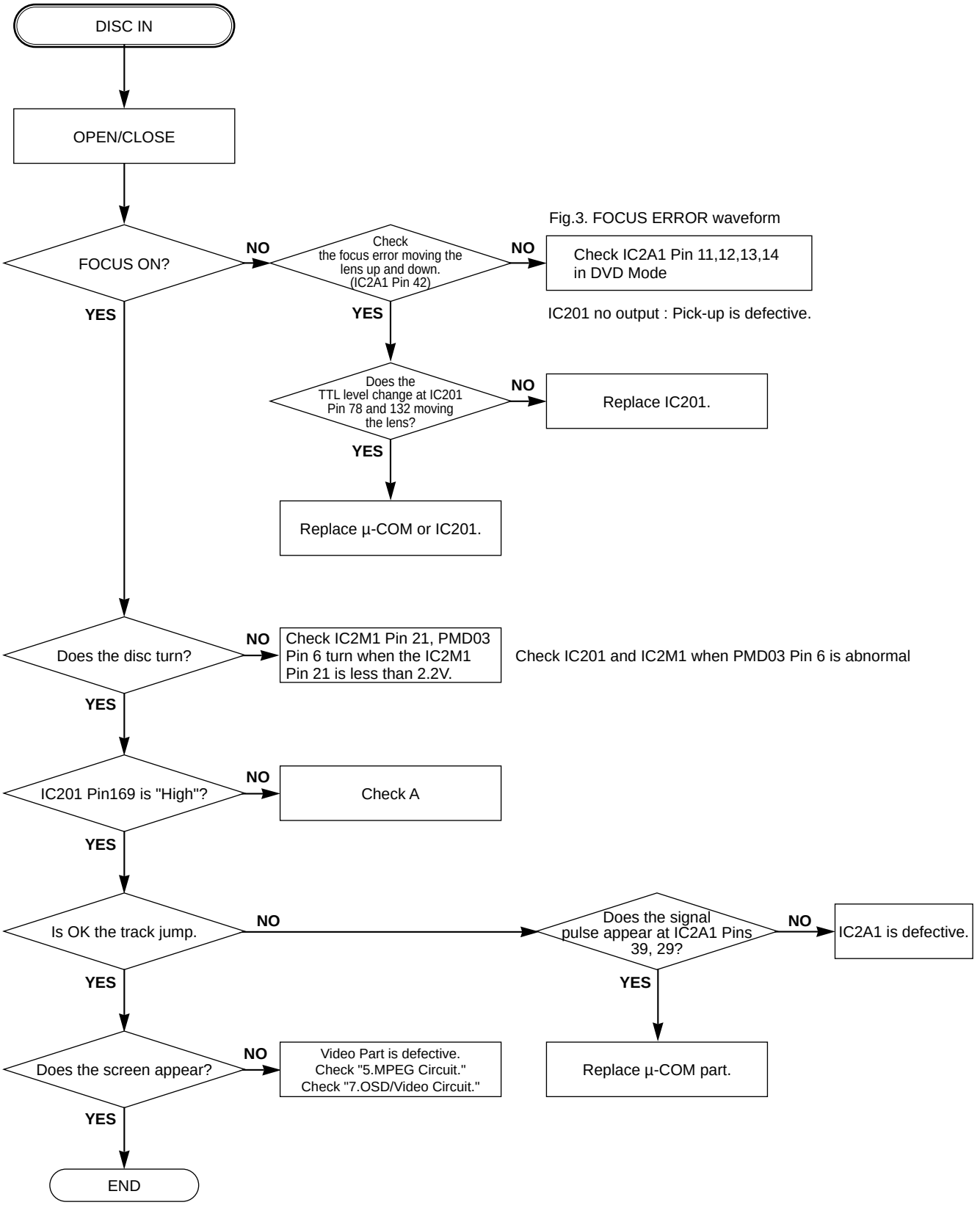
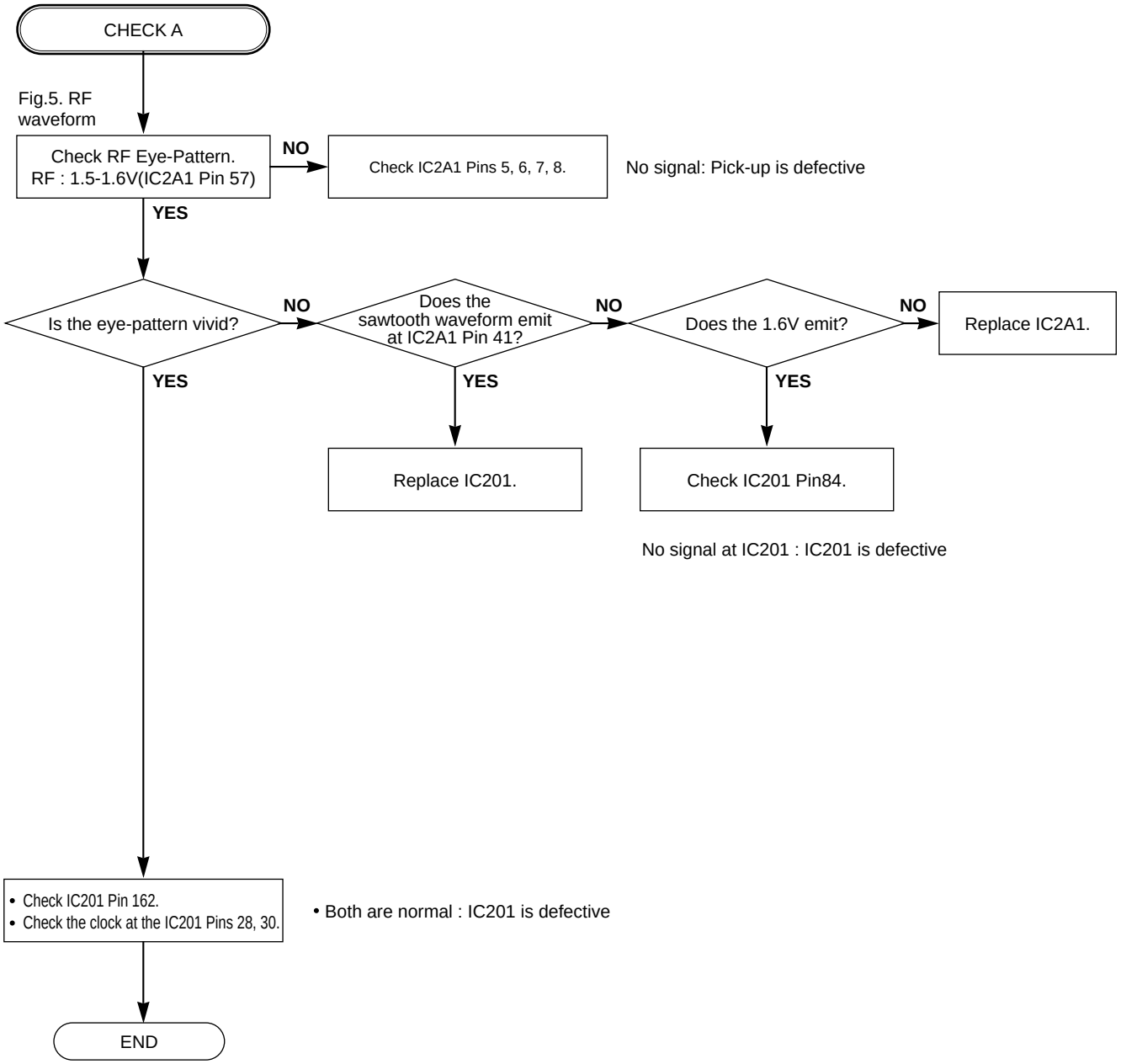


Fig.3. FOCUS ERROR waveform

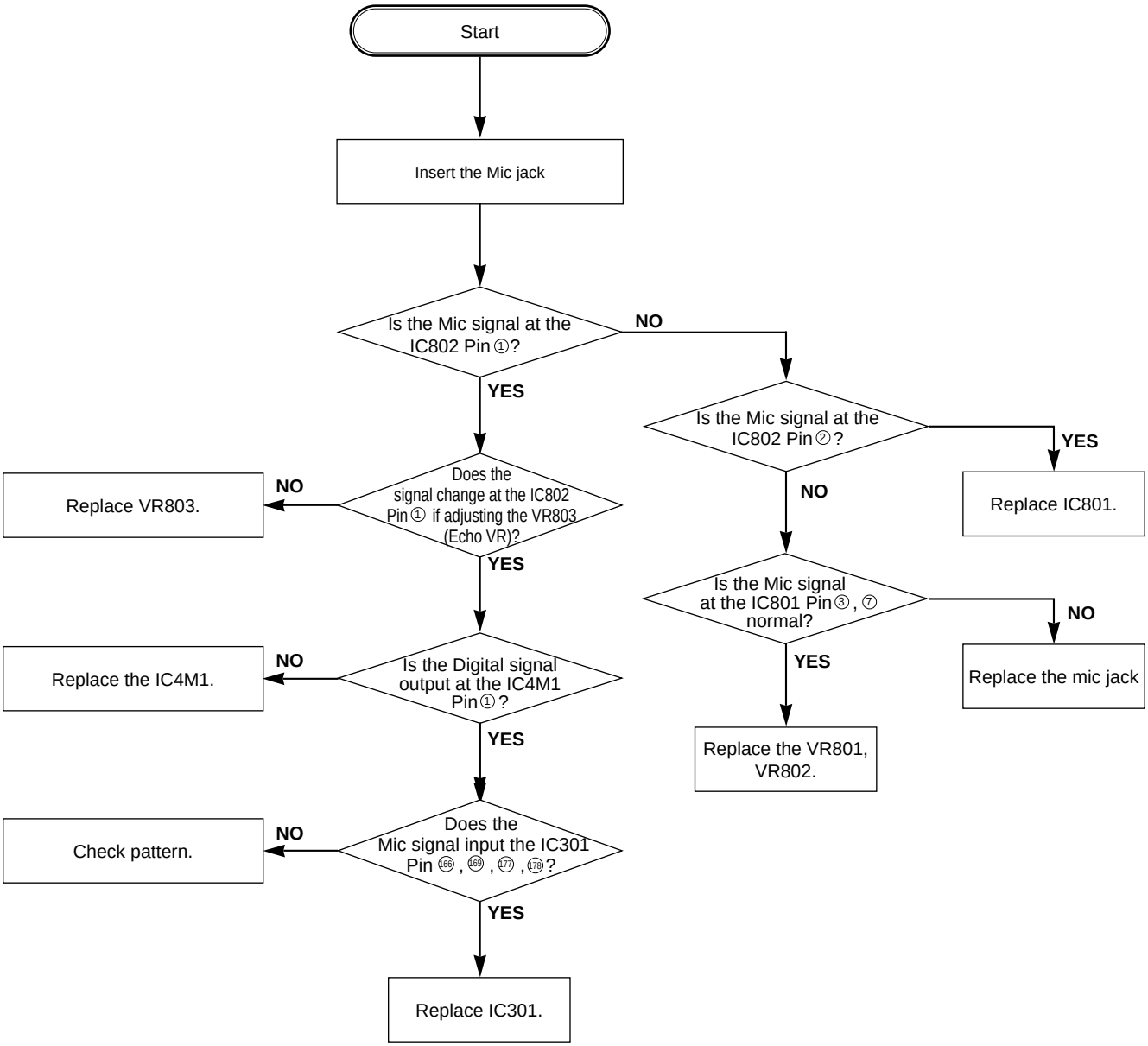
IC201 no output : Pick-up is defective.

Check IC201 and IC2M1 when PMD03 Pin 6 is abnormal

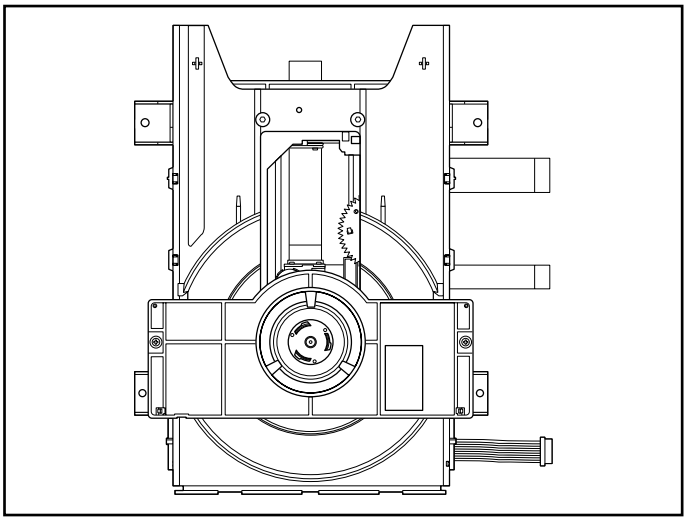
D.


CHECK A
Fig.5. RF waveform
Check RF Eye-Pattern.
RF : 1.5-1.6V(IC2A1 Pin 57)
NO
Check IC2A1 Pins 5, 6, 7, 8.
No signal: Pick-up is defective
YES
Is the eye-pattern vivid?
NO
Does the sawtooth waveform emit at IC2A1 Pin 41?
NO
Does the 1.6V emit?
NO
Replace IC2A1.
YES
YES
YES
Replace IC201.
Check IC201 Pin84.
No signal at IC201 : IC201 is defective
• Check IC201 Pin 162.
• Check the clock at the IC201 Pins 28, 30.
• Both are normal : IC201 is defective
END

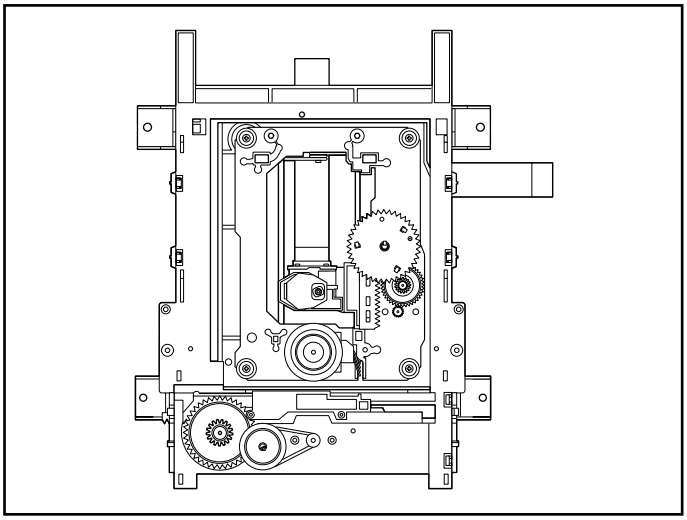
6. KARAOKE Circuit <EZ>



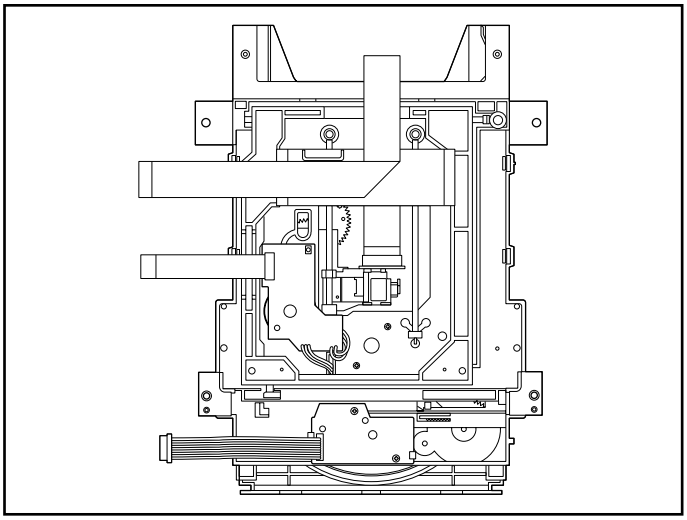
• Top View (With Tray)



• Top View (Without Tray)



• Bottom View



Procedure Starting No.		Parts	Fixing Type	Disassembly	Figure
	1	Holder Clamp	2 Screws, 2 Locking Tabs		4-1
1	2	Clamp Assembly Disc			4-1
1, 2	3	Plate Clamp			4-1
1, 2, 3	4	Magnet Clamp			4-1
1, 2, 3, 4	5	Clamp Upper			4-1
1	6	Tray Disc			4-2
1, 6	7	Base Assembly Sled			4-3
1, 2, 6	8	Gear Assembly Feed	4 Screws, 1 Connector 1 Locking Tabs		4-3
1, 2, 6, 8	9	Gear Middle			4-3
1, 2, 6, 8, 9	10	Gear Assembly Rack	1 Screw		4-3
1, 2, 7	11	Rubber Rear			4-3
1, 2, 7	12	Frame Assembly Up/Down	1 Screw	Bottom	4-4
1, 2	13	Belt Loading	1 Locking Tab		4-4
1, 2 ,13	14	Gear Pulley			4-4
1, 2, 13, 14	15	Gear Loading	1 Locking Tab		4-4
1, 2, 7, 12, 13, 14	16	Guide Up/Down			4-4
1, 2, 13	17	PWB Assembly Loading	1 Locking Tab 1 Hook 2Screw	Bottom	4-4
1, 2, 7, 12, 13, 14, 15, 16, 17	18	Base Main	2 Locking Tabs		4-4

Note

When reassembling, perform the procedure in reverse order.

The “Bottom” on Disassembly column of above Table indicates the part should be disassembled at the Bottom side.

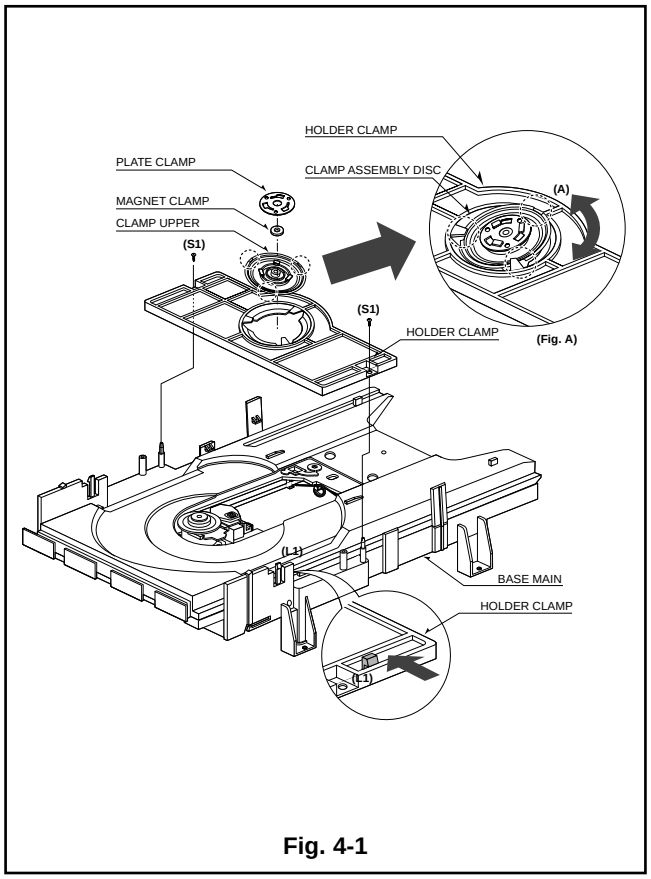


Fig. 4-1

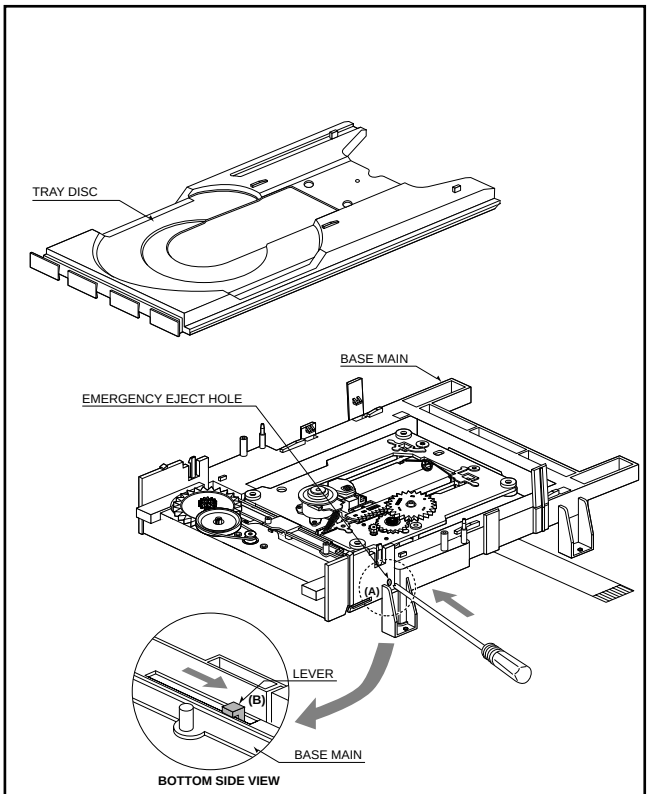


Fig. 4-2

1. Holder Clamp (Fig. 4-1)

1) Release 2 Screws(S1).
2) Unhook 2 Locking Tabs(L1).
3) Lift up the Holder Clamp and then separate it from the Base Main.

1-1. Clamp Assembly Disc

1) Place the Clamp Assembly Disc as Fig. (A)
2) Lift up the Clamp Assembly Disc in direction of arrow(A).
3) Separate the Clamp Assembly Disc from the Holder Clamp.

1-1-1. Plate Clamp

1) Turn the Plate Clamp to counterclockwise direction and then lift up the Plate Clamp.

1-1-2. Magnet Clamp

1-1-3. Clamp Upper

2. Tray Disc (Fig. 4-2)

1) Insert and push a Driver in the emergency eject hole(A) at the right side, or put the Driver on the Lever(B) of the Gear Emergency and pull the Lever(B) in direction of arrow so that the Tray Disc is ejected about 15~20mm.
2) Pull the Tray Disc until it is separated from the Base Main completely.

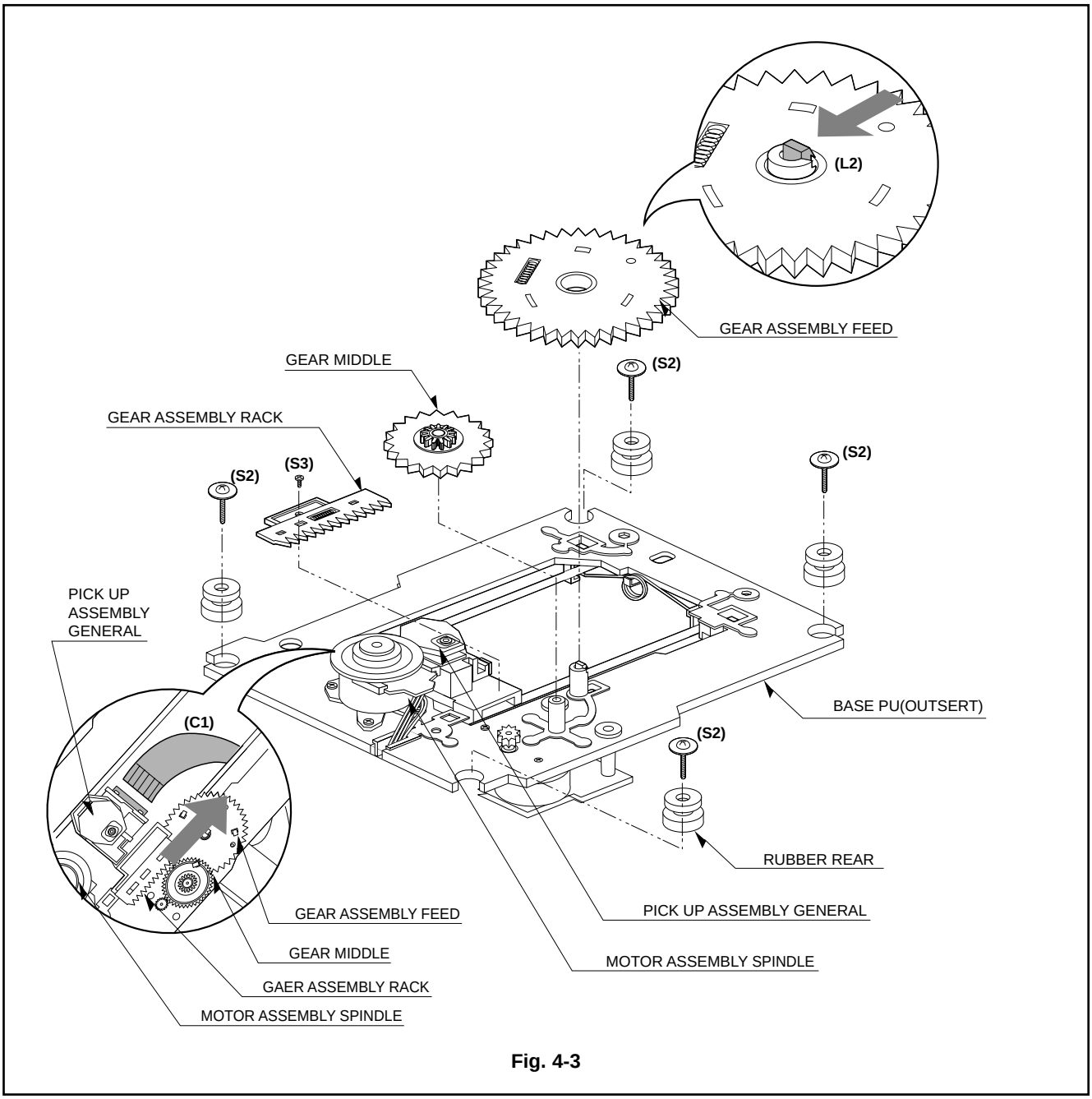


Fig. 4-3

3. Base Assembly Sled (Fig. 4-3)

1) Release 4 Screw(S2).
2) Disconnect the FFC Connector(C1)

3-1. Gear Assembly Feed

1) Unhook the Locking Tab(L2) in direction of arrow.

3-2. Gear Middle

3-3. Gear Assembly Rack

1) Release the Scerw(S3)

4. Rubber Rear (Fig. 4-3)

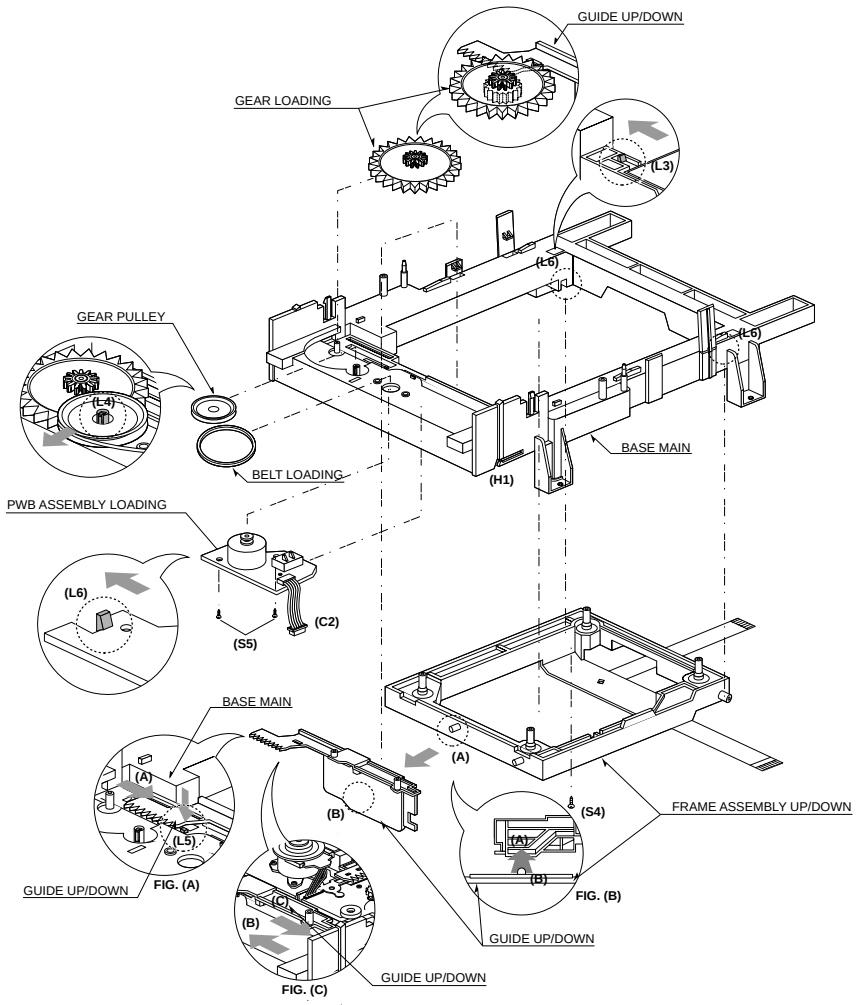


Fig. 4-4

5. Frame Assembly Up/Down

Note

Put the Base Main face down(Bottom Side)

1) Release the Screw(S4)
2) Unlock the Locking Tab(L3) in direction of arrow and then lift up the Frame Assembly Up/Down to separate it from the Base Main.

Note

- When reassembling move the Guide Up/Down in direction of arrow(C) until it is positioned as Fig.(C).
- When reassembling insert (A) portion of the Frame Assembly Up/Down in the (B) portion of the Guide Up/Down as Fig.(B)

6. Belt Loading(Fig. 4-4)

Note

Put the Base Assembly Main on original position(Top Side)

7. Gear pulley (Fig. 4-4)

1) Unlock the Locking Tab(L4) in direction of arrow(B) and then separate the Gear Pulley from the Base Main.

8. Gear Loading (Fig. 4-4)

9. Guide Up/Down (Fig. 4-4)

1) Move the Guide Up/Down in direction of arrow(A) as Fig.(A)
2) Push the Locking Tab(L5) down and then lift up the Guide Up/Down to separate it from the Base Main.

Note

When reassembling place the Guide Up/Down as Fig.(C) and move it in direction arrow(B) until it is locked by the Locking Tab(L5). And confirm the Guide Up/Down as Fig.(A)

10. PWB Assembly Loading

Note

Put the Base Main face down(Bottom Side)

1) Release 2 Screws(S5)
2) Unkool the Loading Motor Connector (C2) from the Hook (H1) on the Base Main.
3) Unlock 2 Locking Tabs(L6) and separate the PWB Assembly Loading from the Base Main.

11. Base Main(Fig. 4-4)

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