Design Review: 100W, 400kHz, DC/DC Converter With Current Doubler Synchronous Rectification Achieves 92% Efficiency

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ABSTRACT

A high efficiency, 100W, DC-to-DC converter design is presented and reviewed. This design employs a phase shifted full bridge primary power stage and the current doubler output with synchronous rectification on the secondary. This topology is particularly suited to supply low voltage, high current loads in distributed power systems. Low profile, off-the-shelf magnetic components are featured. Over 92% efficiency is achieved in an isolated, 5V output modular approach where converters can be paralleled for load-sharing. Design considerations for optimized zero voltage transition operation and critical timing issues of all semiconductor switches are also discussed. Operating waveforms and measurement results complement the paper.

TOPOLOGY OVERVIEW

Full Bridge Converter

At high power levels or extreme efficiency requirements where the use of four controlled switches are justifiable, the full bridge converter is probably the best choice. A conventional full bridge converter and its most important waveforms are shown in Figure 1. The converter is operated with a three-state PWM signal. During the first state the

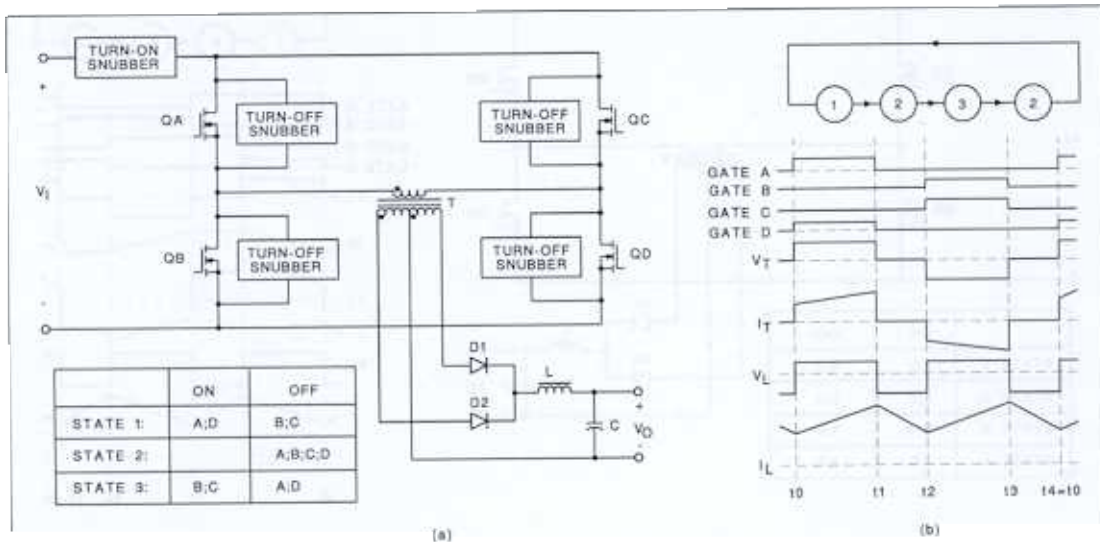


Figure Conventional Full Bridge Schematic

diagonal switches, QA and QD conduct, followed by State 2 when all four switches are turned off. The third state is the conduction period of QB and QC transistors which is again followed by State 2.

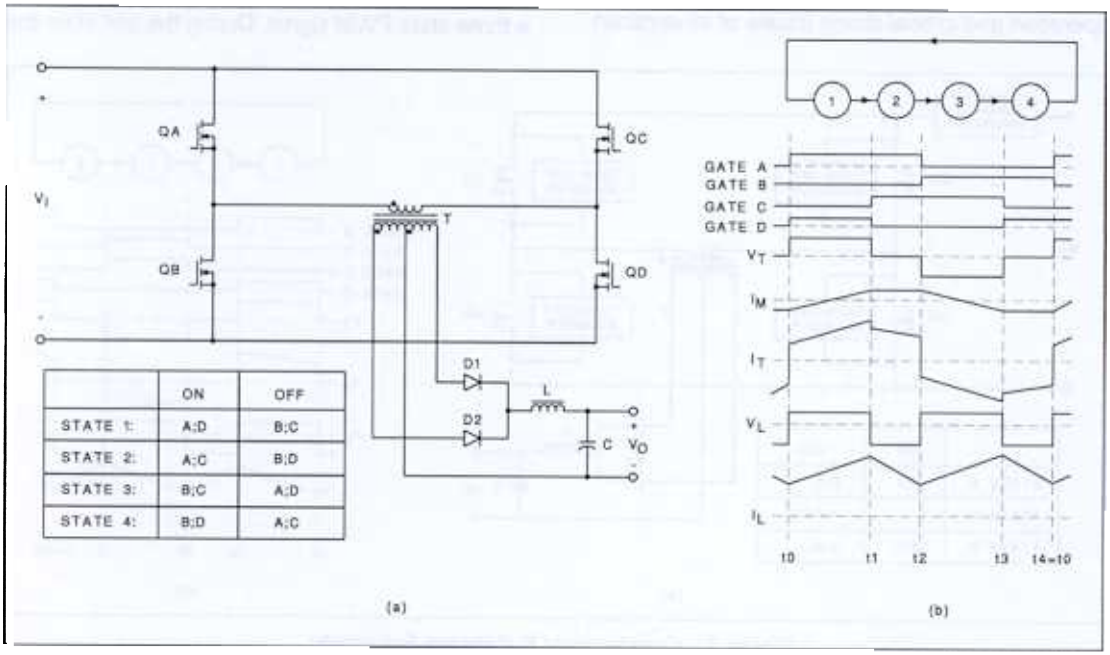
While the utilization of the magnetic components in this circuit are really excellent, the dynamic losses of the switching semiconductors at higher operating frequencies and/or elevated input voltages are excessive. The switching losses can be reduced by using snubbers (as shown in Figure 1), quasi- or fully resonant techniques, or soft-switching (ZVT) circuits. Soft-switching, also called Zero Voltage Transitions, is preferred because of its simpler power circuit, high efficiency, low EMI levels and simpler analysis than its resonant competitors.

Full-Bridge Converter with Phase Shifted Control

Outstanding performance of the phase shifted, ZVT full bridge converter in DC/DC applications are well documented in the literature ([6]-[10]). This circuit is capable of delivering high efficiency at high operating frequencies because it combines the advantages of zero voltage resonant transitions to reduce switching losses and square wave power conversion to maintain optimal utilization of the semiconductors. Additional benefits are constant frequency operation, reduced EMI and the integration of the parasitic circuit components, junction capacitances, leakage inductance and MOSFET body diodes in the power circuit. A few possible shortcomings of the circuit include the relatively complex phase-shift PWM algorithm and the potential loss of soft-switching at light load.

The circuit on the primary side resembles the conventional full bridge converter without the usual snubber circuits. Due to the phase-shift PWM control method applied to the circuit, the dominant turn-on losses of the MOSFET transistors are eliminated while soft-switching is maintained. However, turn-off losses are still present in the circuit. They can be significantly reduced by using a low impedance gate drive circuit for quick turn-off of the switching devices. The greatly reduced switching losses explain the absence of the snubber circuits commonly present in the conventional full bridge converters.

As shown in Figure 2, this circuit is controlled by a four-state PWM signal. According to the four



	ON	OFF
STATE 1:	A;D	B;C
STATE 2:	A;C	B;D
STATE 3:	B;C	A;D
STATE 4:	B;D	A;C

Figure 2. Phase Shifted Full Bridge Schematic

states of the PWM controller, the operation of the circuit is divided into four major intervals. Operation at high load in continuous conduction mode are shown in Figure 2(b) and discussed next.

State 1 (t0→t1):

During this state, QA and QD are on and the voltage is positive at the dotted end of the transformer windings. The magnetizing current starts ramping up from $-I_M$ towards $+I_M$. The reflected load current also flows through QA, the primary and QD. On the secondary side, D2 is on while D1 is reverse biased. The voltage across L is positive, which produces a positive slope in I_L.

State 2 (t1→t2):

In State 2, QA and QC are on, shorting the primary at the positive supply rail. The voltage V_T, on the secondary side equals 0V too. D1 and D2 are on, L freewheels. The output voltage across L makes I_L decrease. Note that despite both diodes are forward biased and connected in parallel, most of I_L keeps flowing through that half of the secondary which was conducting during State 1, because of the combined effect of the shorted primary winding and the parasitic inductances.

State 3 (t2→t3):

In this interval, QB and QC are on. V_T is negative and I_M goes from $+I_M$ to $-I_M$. The reflected load current also flows through the primary components. At the same time, D1 conducts and D2 is off on the output side. The voltage across L is positive again and I_L starts rising.

State 4 (t3→t4):

The full operating cycle is completed by another freewheeling period when QB and QD are on, shorting the transformer primary at the negative supply rail. Consequently, V_T on the secondary is zero. Diodes D1 and D2 are on simultaneously. The voltage across L is $-V_O$ to establish the freewheeling mode for L.

Soft-switching operation of all four primary semiconductors is achieved by inserting a delay time between the consecutive operating states. During this delay time, a resonant action takes place between the various capacitances and inductances connected to the center point of the bridge leg. This resonant transition is driven by the inductive energy stored in the magnetic components of the circuit. They are the magnetizing and leakage inductances of the transformer, any external commutating inductor might be used in series with the primary and the output filter inductor. The stored inductive energy has to overcome the capacitively stored energies in the C_{OSS} capacitances of the MOSFETs, in the parasitic capacitance of the isolation transformer and in any external capacitors might be needed to limit dv/dt during the resonant transitions. Since the stored inductive energy declines exponentially at decreasing current levels, achieving soft-switching under light load conditions can be troublesome.

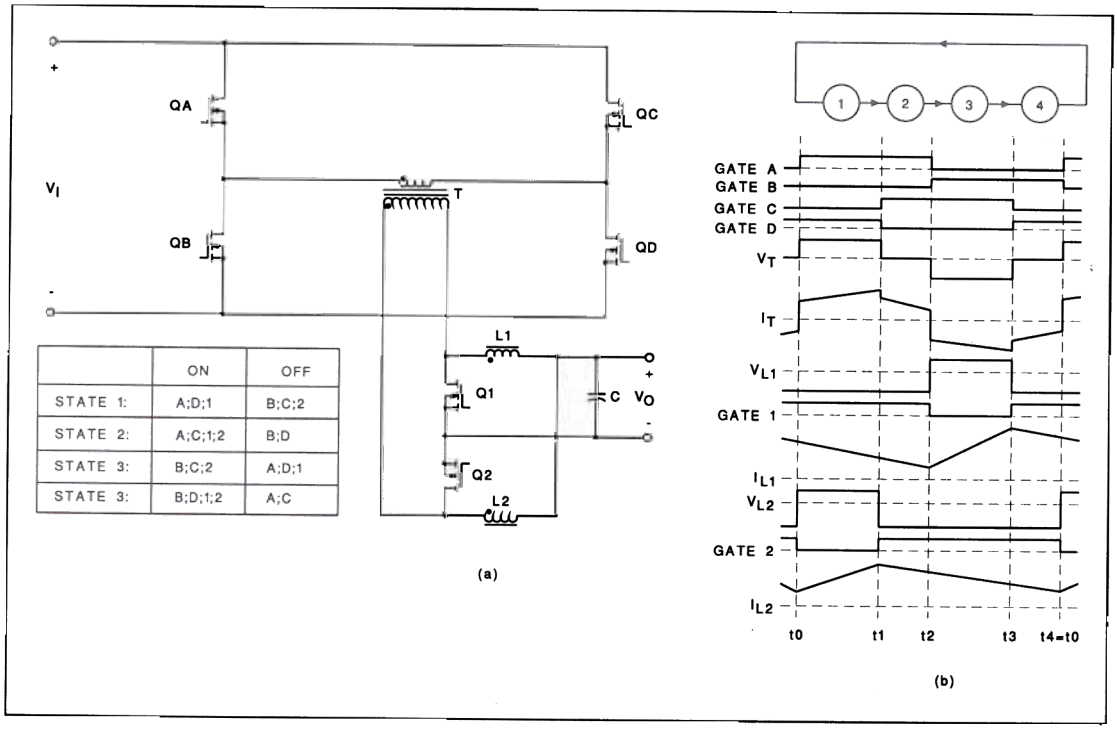
Phase Shifted Full Bridge Converter with Current Doubler Synchronous Rectifiers

The introduction of several integrated circuits [11] has provided effortless implementation of the complex phase-shift PWM control. On the other hand, designs with potential failure of soft-switching at light load can not really take advantage of the lower EMI generated at nominal load. Significant efforts have been made to retain soft-switching at light load ([9],[10]). In this paper, the current doubler technique with synchronous rectifiers [1] will be used to extend the soft-switching capability of the phase shifted full bridge converter under all load conditions.

Figure 3 introduces the power stage and its basic waveforms. The operation of the primary side was already discussed and this part focuses on the unique properties of the current doubler rectifiers.

The current doubler rectifier can be derived from the full-wave rectifier circuit using a simple conversion of the different current and voltage sources of the circuit. Figure 4 shows the steps of the transformation leading from the full wave to the current doubler configuration with synchronous rectifiers.

The current doubler offers an alternative rectification method for forward, push-pull and bridge type converters where bipolar voltages are



	ON	OFF
STATE 1:	A;D;1	B;C;2
STATE 2:	A;C;1;2	B;D
STATE 3:	B;C;2	A;D;1
STATE 3:	B;D;1;2	A;C

Figure 3. Phase Shifted Full Bridge Converter with Current Doubler Synchronous Rectifiers

utilized at the secondary side of the isolation transformer. Circuit operation greatly depends on the primary power stage since it has a profound effect on the current distribution during the passive or freewheeling period. In those cases, reported in [2], [3] and in the full bridge converter with phase shifted control, used in this design, currents can freely flow in the primary and in the secondary transformer windings during the freewheeling period. Thus, the current of the output inductors, I_{L1} and I_{L2} can change direction as is required by the load to extend the range of continuous conduction mode operation to lower output current values.

The circuits in Figure 4(d) and 4(e) are composed of the secondary winding of the isolation transformer which is not center-tapped now, two rectifier diodes, two identical filter inductors and an output capacitor. It offers a simpler structure, better window and copper utilization for the isolation transformer and a reduced turns ratio compared to full wave rectifiers. This technique requires two identical output inductors, L1 and L2,

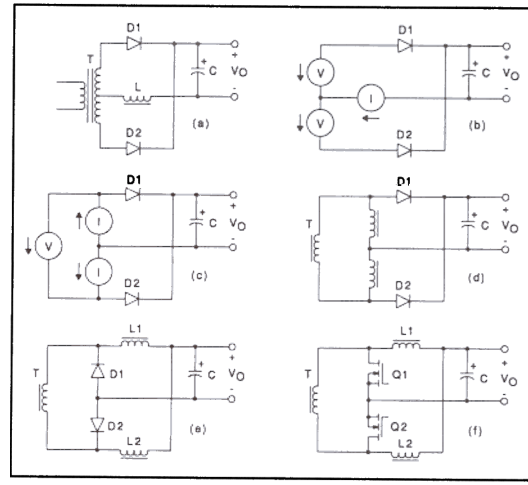


Figure 4. Derivation of the Current Doubler Rectifier

both working at half the operating frequency and at half the rated current of their full wave counterpart, L. One unique set of benefits of the circuit is that the diode and output capacitor stresses are identical to the full-wave technique.

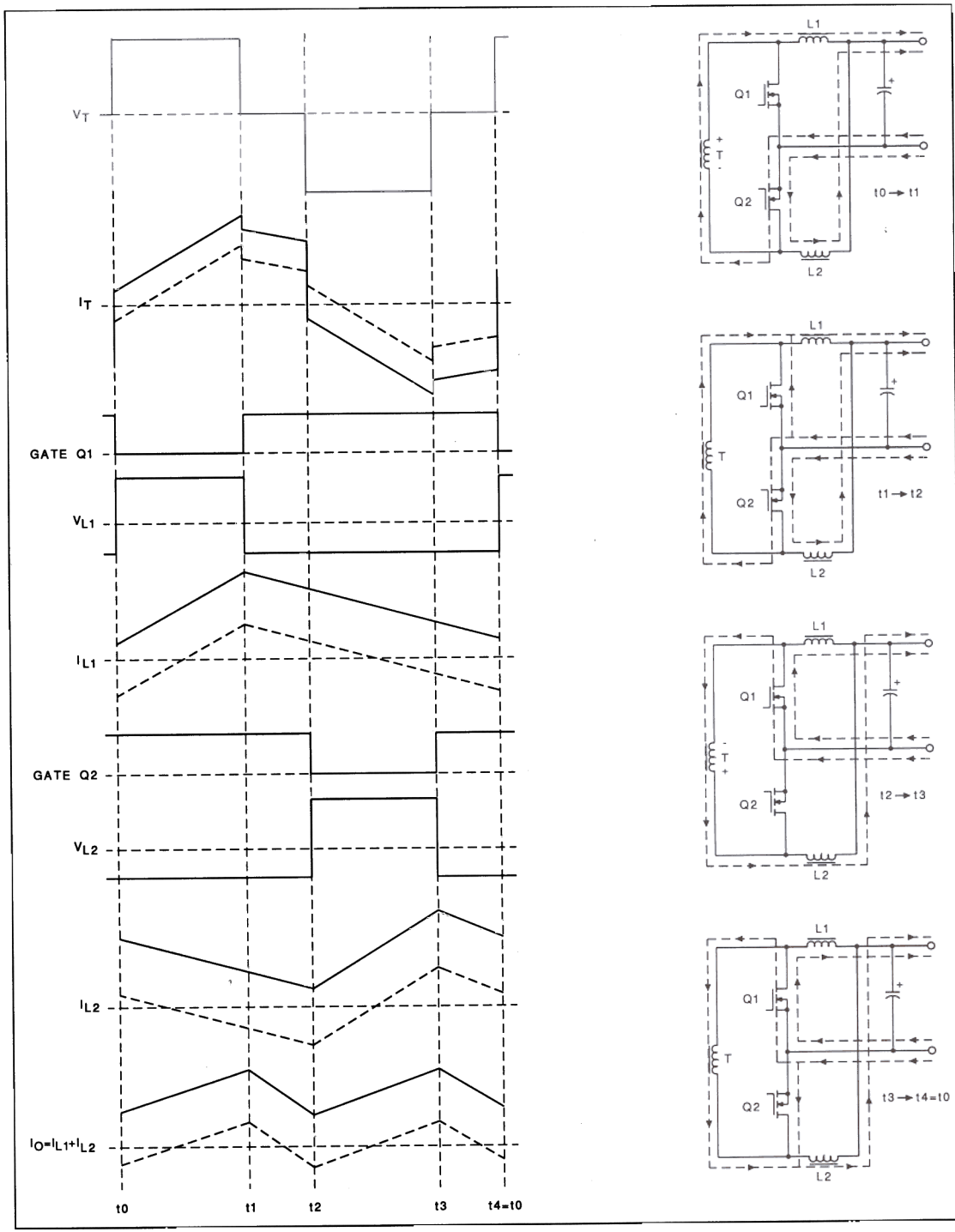


Figure 5. Operation of the Current Doubler Rectifier

The current doubler working under the same conditions as a full wave rectifier will reduce the copper loss in the transformer secondary by approximately 50%, as reported in [4]. Converters using the current doubler rectifier might achieve lower and better distributed power dissipation and smaller overall volume for magnetic components. An integrated magnetic solution for further reduction in size and cost has been also reported in [2], using a half-bridge converter as the primary power stage.

Figure 4(f) shows the two controlled switches for synchronous rectification. The operation of the current doubler rectifier with synchronous rectification is highlighted in Figure 5.

In accordance with the primary side, the switching period is divided into four intervals.

State 1 (t0→t1):

At t0, V_T becomes positive at the dotted end of the secondary. During State 1, Q1 is off and Q2 is on. Current flows in positive direction in both filter inductors. The sum of I_{L1} and I_{L2} supplies the load current. Because of the peak current mode control used on the primary side, the peak values of I_{L1} and I_{L2} must be equal, thus the load current is equally shared between L1 and L2. The current I_{L1} flows through Q2 and the transformer secondary. The voltage across L1 equals V_T-V_O. This positive voltage causes I_{L1} to increase. At the same time, L2 freewheels through Q2 and I_{L2} decreases by the rate of V_O/L2. The current through the secondary, I_T equals I_{L1} and it accounts for half of the total load current.

State 2 (t1→t2):

In this state, V_T is zero and Q1 and Q2 are both on. The voltage across L1 becomes -V_O, producing a negative slope in I_{L1}, which now flows through Q1. The conditions for L2 do not change and both inductors are in freewheeling mode.

State 3 (t2→t3):

During State 3, V_T is negative at the dotted end of the secondary winding, Q1 is on and Q2 is off. A positive voltage, V_T-V_O appears across L2 and I_{L2} starts increasing. In this state, I_T equals I_{L2}, thus only half of the load current flows in the secondary again. L1 freewheels through Q1 and I_{L1} decays by the rate of -V_O /L1.

State 4 (t3→t4=t0):

The full operating cycle is completed by another freewheeling period. The voltage V_T becomes zero and Q1 and Q2 are on simultaneously. -V_O appears across L2 causing its current to decrease and freewheel through Q2 while L1 continues to freewheel as in State 3.

The no load operation of the circuit is illustrated by the dashed lines in the current waveforms. Both filter inductors have bi-directional currents, hence the duty ratio does not change to accommodate the lower output current level. The current doubler preserves continuous conduction mode operation of the converter under all load conditions. There are two significant advantages associated with this effect. One is that the converter gain will not collapse. This phenomena would take place at the onset of discontinuous conduction mode, which is completely eliminated in this circuit. The other advantage is the constant amplitude of the magnetizing current from zero to full load. This represents a significant benefit to ensure soft switching at light loads.

DESIGN SPECIFICATIONS

Input Voltage (V_I):	32V to 72V
Output Voltage (V_O):	5V
Output Current (I_O):	0A to 20A
Output Power:	100W
Efficiency:	>90% at full load
Output Ripple:	100mV p-p
ZVT Range:	0% - 100%
Isolation:	1000V_{RMS}
Switching frequency (f_{CLOCK}):	400kHz (200kHz magnetic components)

DESIGN OVERVIEW

A full bridge converter with current doubler synchronous rectifiers was implemented using standard, commercially available components wherever it was possible. Power to this unit is

supplied from the nominal 48V bus of a distributed power system. Control functions are provided by a UC3879 control IC. A galvanically isolated 5V output is capable of delivering 20A to the load. The feedback incorporates an opto-coupler to cross the 500V isolation boundary between the primary and secondary side of the power supply. Load-sharing capability is added to accommodate higher current loads by paralleling several modules.

Understanding the four major states gives sufficient information about the square wave operating principle of the circuit. Unfortunately, the ultimate performance of the power supply depends upon how well the circuit works during the switching intervals. A resonant transition takes place in the circuit every time the converter advances from one state to the next one. The delay between turning off one switch and turning on its complementary pair in the same bridge leg provides the opportunity for the resonant operation of the parasitic components. In an optimal design, the resonant action aligns all four switches under all operating conditions to zero voltage before the switch is turned on. Only in this case the circuit is capable of delivering high efficiency and low EMI level. The conditions of the successful ZVT operation depend on the power and parasitic component values and the optimization of the delay times, as it will be shown later.

POWER STAGE DESIGN

This section determines the major components and critical operating parameters of the power converter. Trying to use as much off-the-shelf components as possible will require a different way of thinking. In several instances the actual design process is substituted by defining the selection criteria of the components. However, understanding the underlining principles of the component parameters and their effect on the operation of the circuit is imperative to successfully execute the design.

Semiconductors

The MOSFET transistors selected for the primary side switches are MTP33N10E types. These 100V, 58mΩ devices have one of the lowest R_{DSON} values in TO220 package. Several factors had to be considered in the selection process of these components. These are the gate drive power requirements, transition times and their proportion compared to the switching period (loss of effective duty ratio), potentially higher primary circulating current which parameters are functions of the parasitic parameters of the chosen MOSFET device. Valid considerations were given [5] for high input voltage applications, where the lowest R_{DSON} devices do not guarantee the optimum efficiency. Nevertheless, in this low input voltage application which also maintains lossless turn-on of the devices at all operating conditions, conduction loss is the dominant one. It can be minimized by using the lowest possible R_{DSON} devices.

In addition to the extended soft-switching operation of the circuit due to synchronous rectification, the output rectifier circuit employs two MTP75N50HD type 50V, 9mΩ (max. value) devices for more efficient power conversion. The selection criteria for these devices is the lowest possible R_{DSON} value that technology and cost considerations allow.

Transformer Design

Conventional transformer design starts with determining the acceptable temperature rise, the corresponding minimum area product and the maximum flux swing allowed to stay within the calculated core loss limits of the transformer. These parameters will define the number of turns required on the primary side. The secondary number of turns calculated from the turns ratio, is based on the minimum value of the input voltage, the maximum steady state duty ratio and the DC transfer function of the converter.

When off-the-shelf parts are considered, the first step is to calculate the DC transfer function and the required turns ratio. For the phase shifted full bridge converter with current doubler output

stage, the following input to output relationship can be established:

$$\frac{V_{I,MIN} \bullet N - V_O}{L1} \bullet D_{MAX} \bullet \frac{1}{f_{CLOCK}} =$$

$$\frac{V_O}{L1} \bullet \left[(1 - D_{MAX}) \bullet \frac{1}{f_{CLOCK}} + \frac{1}{f_{CLOCK}} \right] \quad (1)$$

Solving the equation for N, the required turns ratio can be calculated as:

$$N = \frac{N_S}{N_P} = 2 \bullet \frac{V_O}{V_{I,MIN} \bullet D_{MAX}} \quad (2)$$

Two important conclusions can be drawn from this result. The current doubler output stage needs twice the number of turns on the secondary side then its full wave counterpart, but only one winding is needed. Otherwise, the transfer function is identical to any traditional full bridge circuit using full wave diode rectifiers. As a result, existing designs with full wave rectification can be easily modified for a current doubler configuration with the present transformer if the center tap termination is not used. Note also that the number of turns on the primary and the secondary side are closer to each other for this design. Consequently, the transformer turns ratio can be adjusted in finer steps, lower leakage inductance can be achieved and the maximum duty ratio can be better optimized in a current doubler configuration.

In this design:

$V_O = 5V$
$V_{I,MIN} = 32V$
$D_{MAX} = 0.8$

therefore:

$$N = \frac{N_S}{N_P} = 2 \bullet \frac{5V}{32V \bullet 0.8} = 0.39$$

After reviewing the available transformers according to the required size, power rating, operating frequency range, temperature rise, mounting considerations and turns ratio, the selected part is a PE68499 type. It is a low profile surface mount transformer from Pulse Engineering. The electrical and mechanical specifications of the transformer are reviewed in Table 1:

PGF Surface Mount Power Transformer	
PULSE part number:	PE-68499
Power rating:	100W convection cooled, 200W
Operating frequency range:	200kHz - 500kHz
Core type:	EE (custom)
Est. core loss:	0.6W
Thermal Impedance:	26°C/W
Est. temperature rise:	27°C
Primary number of turns:	10 (2x5 in series)
L_magnetizing:	186µH
R_dc primary:	14mΩ
R_ac primary:	16mΩ
Secondary number of turns:	4
R_dc secondary:	2.5mΩ
R_ac secondary:	2.8mΩ
L_leakage:	0.26µH
Cp (transformed to primary):	186pF
Hipot:	1000Vrms
Dimensions WxLxH:	1.16"x1.07"x0.032"
Weight:	14.5 grams

Table 1. Transformer Data

For users planning to design their own transformer, the design procedure is given in several references. A conventional transformer design example can be found [12] while detailed consideration for planar transformer structures are also discussed [5]. In general, the phase shifted full bridge converter is very forgiving of the parasitic values of the transformer because these components are utilized beneficially in the operation of the circuit.

Switching Transitions

One goal of this design is to maintain zero voltage switching for the entire load range from zero to 20A output current. To guarantee the soft switching of all four primary semiconductors by design, the conditions of the ZVT operation have to be analyzed [6]. The first observation to make is to realize that the two legs of the bridge converter operate

under different conditions. Switches QA and QB are driven by the clock signal of the controller. Every time a clock signal is generated one of these switches turns off and, after the delay specified in the controller, the other switch turns on. Whenever a switching action takes place in the leg formed by QA and QB, the converter terminates the freewheeling (or passive) state and starts a new active interval, delivering energy from the primary to the secondary side of the power supply. Thus the leg comprised of QA and QB is called the Passive-To-Active (P→A) leg. On the contrary, the other side of the bridge circuit composed of QC and QD is called the Active-To-Passive (A→P) leg. Switching action in the A→P leg is initiated by the PWM comparator when the measured current signal or the ramp equals the actual value of the error signal. At that instant, the power flow from the primary to the secondary side is interrupted and the circuit goes to a passive (freewheeling) state.

A→P leg resonant transition

A typical full bridge converter with all the parasitic components and initial conditions is shown in Figure 6(a). Switching transition starts with turning off QD. The schematic diagrams featured in Figure 6(b) and 6(c) represent the equivalent circuits of the phase shifted full bridge converter during the resonant transition. There are two components which propel the resonant action in this transition. One of them is the contribution of the magnetizing current. The value of the magnetizing current at turn-off of QD (or QC) is constant. It is independent of the input voltage and the load current while regulation is maintained on the output of the converter. This is because the converter operates in continuous inductor current mode from zero to full load and the applied volt-second product is constant. Its value equals:

$$I_M = \frac{1}{2} \cdot \frac{V_I}{L_M} \cdot D \cdot \frac{1}{f_{CLOCK}} \qquad (3)$$

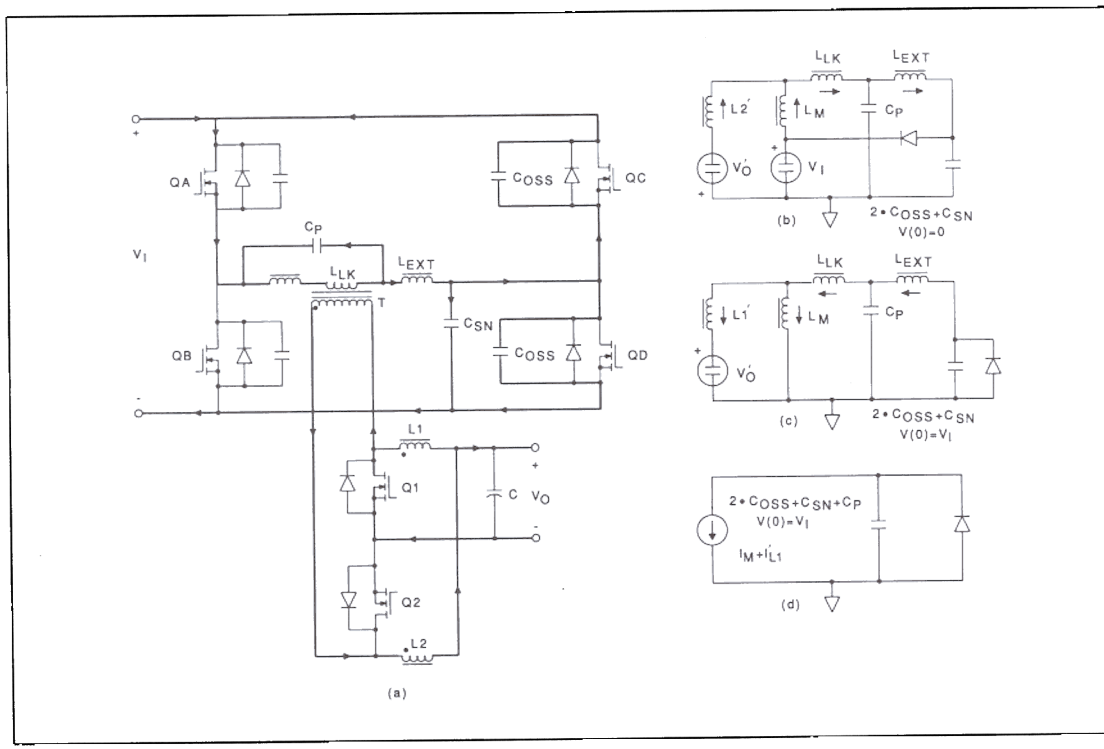


Figure 6. A→P Transition Equivalent Circuits

The other current component driving the transition is the contribution of the load current. Its instantaneous value at the beginning of the resonant action varies with the load current and calculated as:

$$I_{L1,PK} = I_{L2,PK} =$$

$$\frac{1}{2} \cdot \left(I_O + \frac{V_O}{L1} \cdot (2 - D) \cdot \frac{1}{f_{CLOCK}} \right) \quad (4)$$

It is important to note that both currents will actually increase during the transition because of the polarity of their respective voltages. Consequently, this soft transition will take place every time, if enough time is allowed for the resonant action to be accomplished.

The capacitive and inductive energies of the circuit at the beginning of the A→P transition are defined as:

$$E_{C,A\rightarrow P} = \frac{1}{2} \cdot (2 \cdot C_{OSS} + C_P + C_{SN}) \cdot V_I^2 \quad (5)$$

$$E_{L,A\rightarrow P} = \frac{1}{2} \cdot L_M \cdot I_M^2 + \frac{1}{2} \cdot \frac{L1}{N^2} \cdot (N \cdot I_{L1,PK})^2$$

$$\frac{1}{2} \cdot (L_{LK} + L_{EXT}) \cdot (I_M + N \cdot I_{L1,PK})^2 \quad (6)$$

When $E_{L,A\rightarrow P} >> E_{C,A\rightarrow P}$, the currents will not change significantly during the resonant transition and the equivalent circuit of Figure 6(b) can be further simplified as shown in Figure 6(d). The inductive circuit components can be replaced by a current source, therefore, the time required for the switching transition can be calculated by the following simplified formula:

$$\tau_{DELAY,C-D} = (2 \cdot C_{OSS} + C_P + C_{SN}) \cdot \frac{V_I}{I_M + N \cdot I_{L1,PK}} \quad (7)$$

Figure 7 shows the solution of (7) using the following circuit parameters:

C_{OSS} = 600pF	drain source capacitance of the MOSFET transistors,
C_P = 180pF	equivalent parasitic capacitance transformed to the primary side,
C_{SN} = 2.2nF	external snubber capacitance to control dv/dt at the A→P leg,
N = 0.4	transformer turns ratio,
L_M = 186µH	magnetizing inductance,
L_{LK} = 0.26µH	transformer leakage inductance,
L_{EXT} = 2µH	commutating inductance,
L1 = L2 = 3µH	output filter inductances,
V_I = 32V, 48V 72V	input voltage (worst case is $V_{I,MAX}$),
V_O = 5V	output voltage,
I_O = 0A ... 20A	dc output current of the converter,

These results were verified by using the more complicated equivalent circuit and PSpice circuit simulation yielding similar values for the transition time.

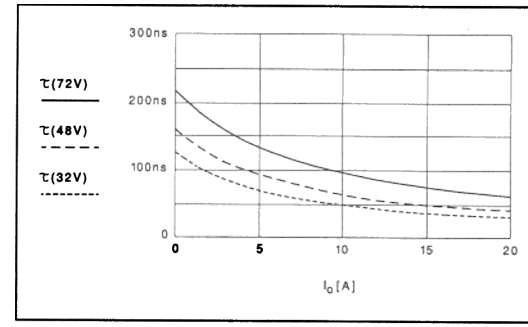


Figure 7. Required Time to Complete Soft Transition in the A→P Leg.

The conclusion of this exercise is to demonstrate that the transitions of the A→P leg in the phase shifted full bridge converter are inherently soft under any load conditions, if the delay time ($\tau_{DELAY,C-D}$) between the turn-off and turn-on of the transistors QC and QD is set properly. In the section describing controller design issues, a simple circuit will be introduced to be able to optimize the delay time of the A→P leg based on the

actual current value propelling the resonant transitions.

P→A leg resonant transition

Initial conditions and equivalent circuits for the P→A leg transitions are shown in Figure 8. The operation of the circuit during this switching interval is rather complicated and has several modes depending on the actual output current value. Modeling the resonant transitions of the P→A leg requires understanding the fine details of the whole power stage.

The switching transition starts with turning off QA. At that instant the magnetizing current and the reflected load current flow through QA, the primary winding of the transformer and QC. The instantaneous value of I_{L1} and I_{L2} at the beginning of the resonant transition can be calculated as:

$$I_{L1} = \frac{1}{2} \bullet \left(I_O + \frac{V_O}{L1} \bullet D \bullet \frac{1}{f_{CLOCK}} \right) \quad (8)$$

$$I_{L2,V} = \frac{1}{2} \bullet \left(I_O - \frac{V_O}{L2} \bullet (2 - D) \bullet \frac{1}{f_{CLOCK}} \right) \quad (9)$$

The capacitances loading the common point of the transistors QA and QB are the C_{OSS} capacitances of the two MOSFETs and the equivalent parasitic capacitance of the transformer. Depending on the values of the parasitic components and the load condition, there are two fundamentally different modes of the resonant transition in the P→A leg. In the first mode, the voltage across the "theoretical" primary winding stays zero during the resonant action, while in the other mode, the voltage across the transformer will start changing.

It is very important to point out here that at the beginning of the P→A leg resonant transition the voltage is applied first across the leakage and any external inductances added in series to the theoretical primary winding of the transformer. The

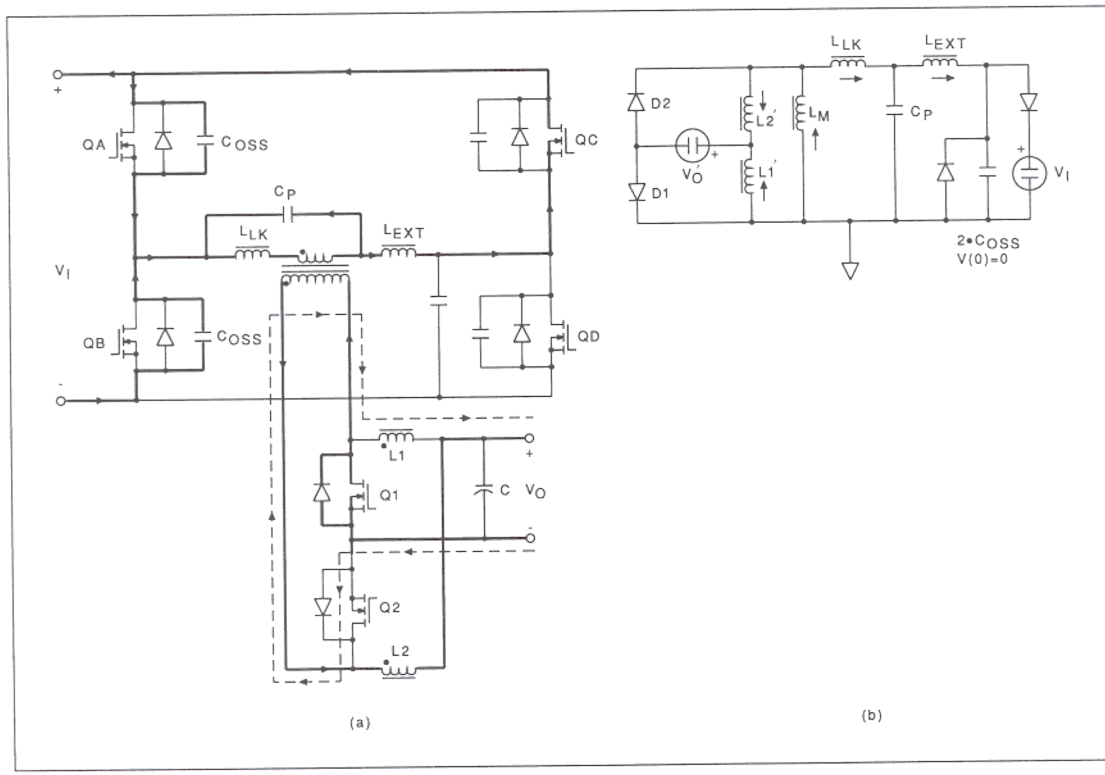


Figure 8. P→A Transition Equivalent Circuits

voltage across the real primary and consequently across the secondary must stay zero until the current in the leakage and external inductors changes direction and reaches the value of the reflected load current.

If the resonant transition can be completed by the energy stored in the leakage and commutating inductances, switching action will be completed before the voltage starts changing across the primary winding of the transformer. For this case, the capacitive and inductive energies of the resonant circuit are given as:

$$E_{C,P\rightarrow A,case1} = \frac{1}{2} \cdot 2 \cdot C_{OSS} \cdot V_I^2 \qquad (10)$$

$$E_{L,P\rightarrow A,case1} = \frac{1}{2} \cdot (L_{LK} + L_{EXT}) \cdot (I_M + N \cdot I_{L1})^2 \qquad (11)$$

and $E_{C,P\rightarrow A,case1} < E_{L,P\rightarrow A,case1}$ (12)

As (11) indicates, the available inductive energy in the P→A transition is much lower than it was in the other bridge leg (6), since the magnetizing and the output inductors do not contribute. That explains loosing the soft-switching operation at the P→A leg, especially at light load and with low leakage inductance, when the energy relationship of (12) is violated. In this situation, there are two cases again, which depend on the magnetizing and reflected load current values. If the magnetizing current has a larger value than the reflected output current, the difference of these two current components still flows in the right direction. The transition is further propelled by the magnetizing inductance (14). Furthermore, if the valley current of the output inductor is negative during the transition, the output inductor also contributes to complete the resonant action (15) and eventually the resonant transition will be completed if the energy relationship in (12) holds true. For these cases:

$$E_{C,P\rightarrow A,case2} = \frac{1}{2} \cdot (2 \cdot C_{OSS} + C_P) \cdot V_I^2 \qquad (13)$$

$$E_{L,P\rightarrow A,case2} = \frac{1}{2} \cdot (L_{LK} + L_{EXT}) \cdot (I_M + N \cdot I_{L1})^2 +$$

$$\frac{1}{2} \cdot L_M \cdot \left(I_M^2 - \left[I_M \quad I \cdot I_{L2,V}) \cdot \frac{I}{N^2 \cdot L} \quad \frac{}{I + L2} \right]^2 \right) \cdot$$

$$\frac{1}{2} \cdot \frac{L2}{N^2} \cdot \left\{ \left[N \cdot I_{L2,V} + (I_M - N \cdot I_{L2,V}) \cdot \frac{L_M}{L_M + \frac{L2}{N^2}} \right]^2 - (N \cdot I_{L2,V})^2 \right\} \qquad (14)$$

or

$$E_{L,P\rightarrow A,case3} = \frac{1}{2} \cdot (L_{LK} + L_{EXT}) \cdot$$

$$\left[(I_M + N \cdot I_{L1})^2 - \left(I_M + N \cdot I_{L2,V} \cdot \frac{L2}{N^2 \cdot L_M + L2} \right)^2 \right] +$$

$$\frac{1}{2} \cdot L_M \cdot \left[I_M^2 - \left(I_M + N \cdot I_{L2,V} \cdot \frac{L2}{N^2 \cdot L_M + L2} \right)^2 \right] + \frac{1}{2} \cdot L2 \cdot I_{L2,V}^2 \qquad (15)$$

For the last possible combination, the energy in the leakage inductance is not sufficient to complete the resonant transition and the reflected load current is larger then the amplitude of the magnetizing current. In this case, the current will change direction in the loop through QA, QC and the primary before the middle point of the P→A leg completes its resonant transition and the chance for lossless switching is permanently lost.

Commutating Inductor

When soft-switching of the P→A leg can not be ensured for all operating conditions because of the low value of the transformer leakage inductance, adding an external commutating aid inductor can extend the soft-switching range of the converter significantly. This inductor has to be selected according the energy requirements of the P→A leg and must be kept at its minimum value in order to achieve optimum efficiency of the circuit. An inductance higher than the minimum required value will lower the effective duty cycle of the power circuit, eventually resulting in lower turns ratio. This

increases the reflected output current value on the primary side and the voltage stress of the secondary side rectifier devices, both leading toward lower overall efficiency of the circuit. Another way to extend the soft-switching range of the converter is to reduce the value of the output filter inductors and/or the magnetizing inductance. This way, it insures that the reflected output current always stays below the actual magnetizing current value. It is usually not possible to sufficiently reduce the value of the filter inductor in a regular full wave output rectifier structure, because of the increasing stress of the filter capacitors and the higher output noise. However, in the current doubler configuration, the ripple currents of the two output inductors cancel each other at the output capacitor, therefore this solution can also be considered.

For example, Figure 9, 10, 11 and 12 show the P→A leg resonant transitions with different combinations of output and commutating inductor values.

These waveforms show that the best result is achieved with 3µH output inductors and by adding an external 2µH commutating inductor in series with the primary winding of the transformer. The value shall be determined for worst case conditions at the maximum input voltage using the equivalent circuit of Figure 8(b) and circuit simulation tools, or by solving the equations given in (10)-(16). Figure 13 displays the common solution of (10)-(16) obtained by MathCAD. When the available energy curve, $E_{L,P\rightarrow A}$ is above the required energy line, $E_{C,P\rightarrow A}$ lossless switching of the P→A leg is feasible.

Because of the complex nature and numerous conditions involved, deriving closed form equations for the transition time of the P→A leg would be rather difficult. Figure 14 shows the required time to complete the transitions as a function of the output current. The optimum value of the commutating inductor value was obtained by varying the L_{EXT} parameter in the MathCAD calculations used to generate Figure 13. The final numbers in Figure 14 were calculated by PSpice simulation, using the equivalent circuits in Figure 8(b).

Output Inductors

Although the current doubler offers significant benefits for the power transformer ([1]-[3]), it requires one additional output inductor. While in traditional full wave output stages the entire output current flows through the filter inductor which

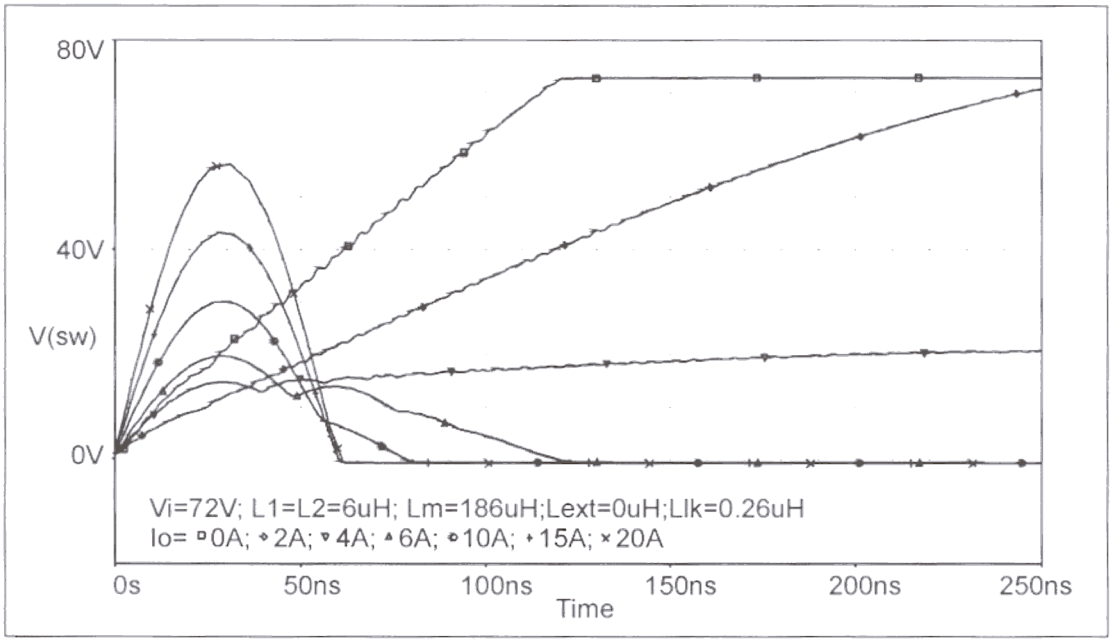


Figure 9. Resonant Transition in the P→A Leg Lo=6µH; Lm=186µH; Lext=0µH.

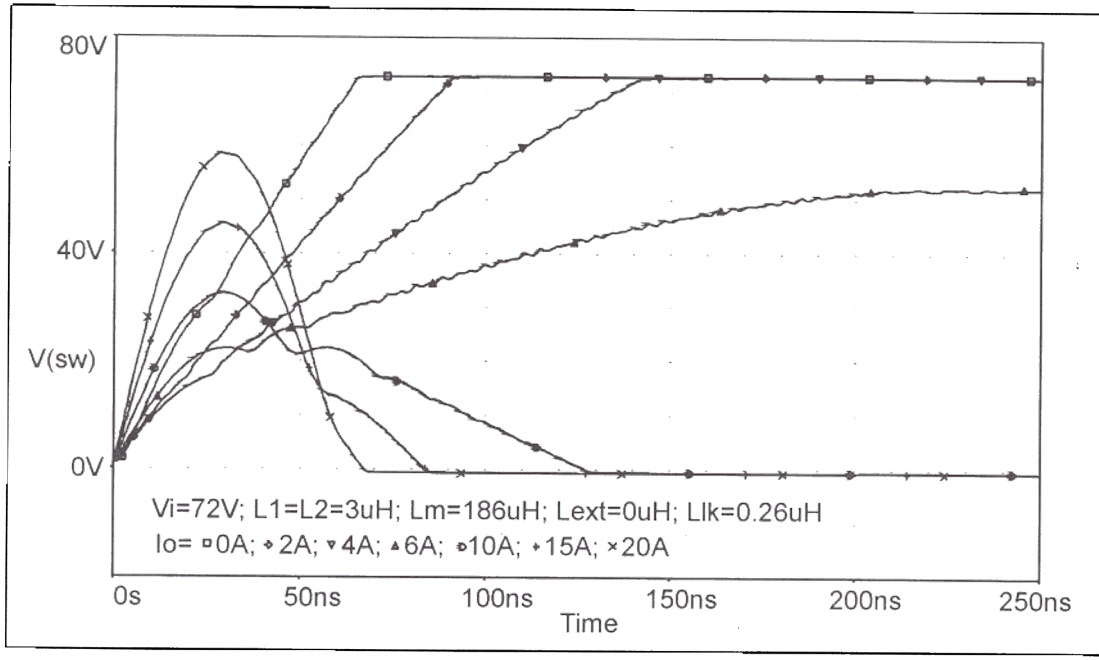


Figure 10. Resonant Transition in the P→A Leg Lo=3µH; Lm=186µH; Lext=0µH.

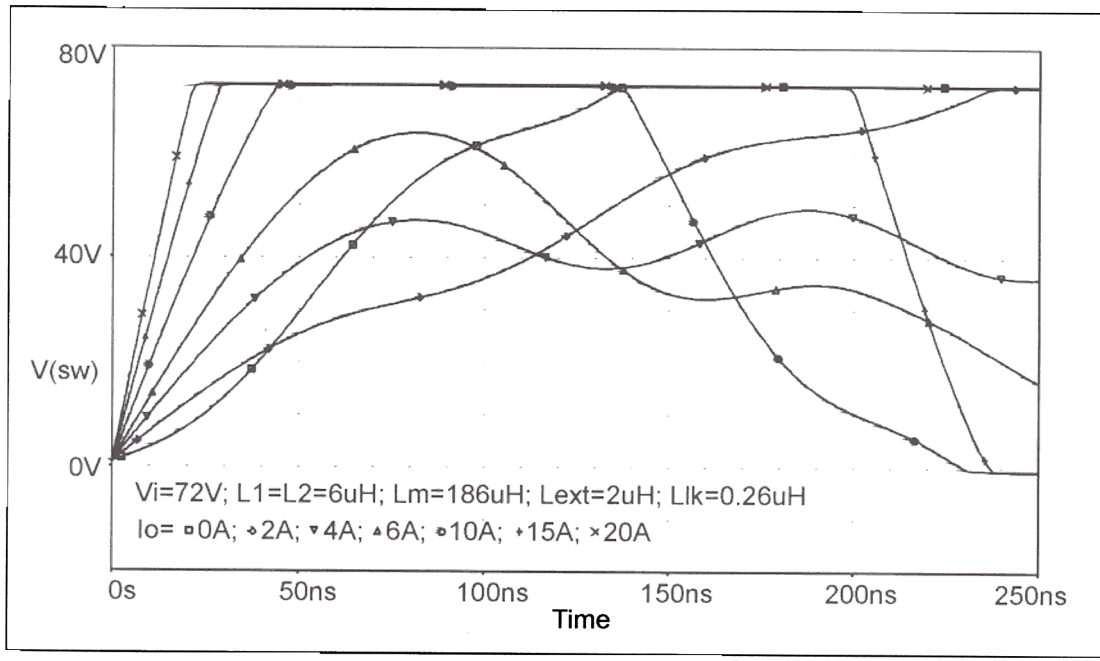


Figure 11. Resonant Transition in the P→A Leg Lo=6µH; Lm=186µH; Lext=2µH.

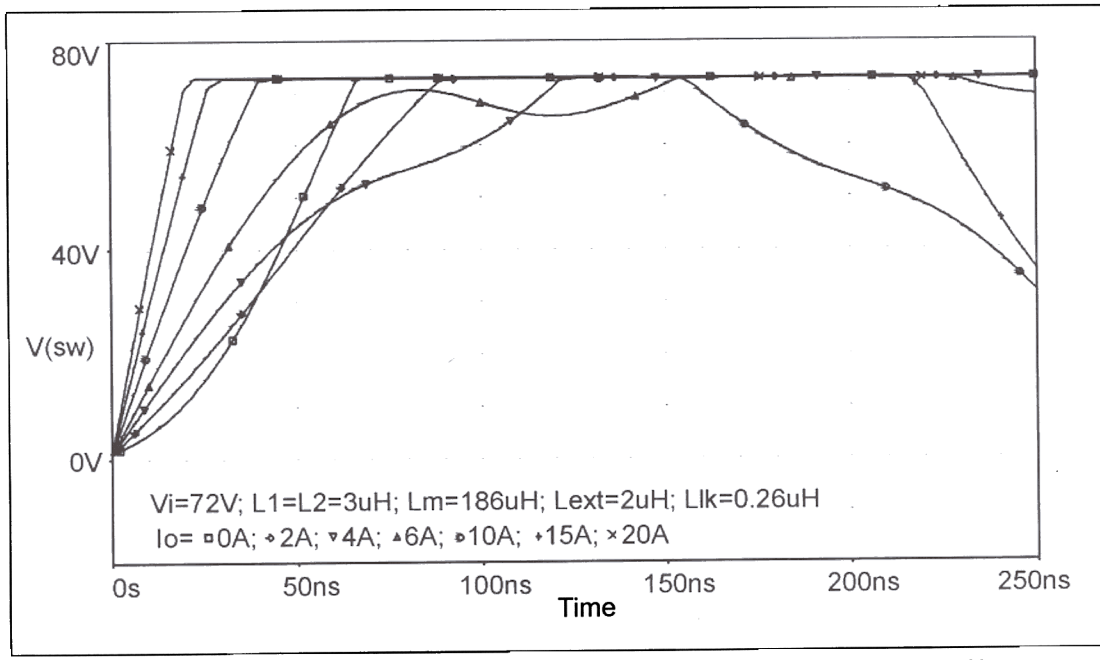


Figure 12. Resonant Transition in the P→A Leg Lo=3µH; Lm=186µH; Lext=2µH.

operates at double the frequency of the isolation transformer, these inductors carry only one half of the load current and they work at half the frequency of their full wave counterparts (same as the operating frequency of the power transformer). The current waveforms are 180 degrees out of phase and the ripple components partially cancel each other in the common output capacitor. For the same equivalent output ripple current that would be generated by a full wave rectifier circuit, the inductance of each output choke has to be doubled. Considering that the physical size of the inductors are proportional to their energy storage capabilities ($I_L^2 \bullet L$), the total core volume of the two output inductors is the same as the single filter choke used in the full wave rectifier circuit.

The two output inductors of the circuit were selected from the same PGF product line offered by Pulse Engineering. Their value is based on the simulation results of the P→A leg resonant transitions and their characteristics are reviewed in Table 2.

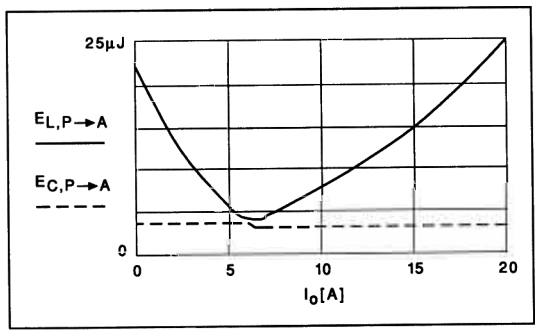


Figure 13. Available and Required Energies of the P→A leg.

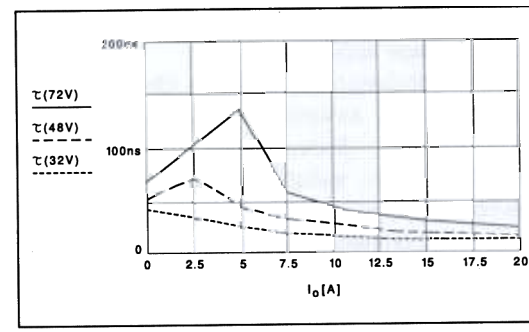


Figure 14. Optimal Timing of the P→A Leg.

PGF Surface Mount Power Inductor	
PULSE part number:	PE-54011
Current rating:	10Adc
Inductance:	2.75µH @ 10A
Operating frequency range	200kHz - 500kHz
Core type:	EFD 15 gapped ferrite
Est. core loss:	80mW
R_dc:	2.7mΩ
Dimensions WxLxH:	0.7"x0.7"x0.032"
Weight:	10 grams

Table 2. Output Inductor Data

For designing your own output inductors, the procedure is given in [13]. There are no additional circumstances which would require special attention. In general, since the inductors of the current doubler circuit work with higher ripple current, ferrite or another low loss material is the preferred choice. Balancing the core and copper losses are also easier with this topology.

Synchronous Rectification

Advancement in high density, low R_{DSON} MOSFET development makes synchronous rectification a feasible and competitive rectification technique for low voltage, high current DC/DC converters. Analysis of the readily available high temperature, low forward voltage drop Schottky rectifiers and high density, low R_{DSON} MOSFET transistors shows that synchronous rectifiers are beneficial below 25A output current. Figure 15 shows the power dissipation of a MTP75N05HD MOSFET transistor and a 32CTQ030 Schottky rectifier as a function of the output current in a low output voltage application.

This comparison is based on identical operating conditions, assuming no conduction of the MOSFET body diodes during the freewheeling period. However, switching losses were added to the conduction losses since body diode conduction can not be completely avoided during the switching intervals. This switching loss was estimated as 25% of the conduction losses of the MOSFET transistors. When Schottky diodes were used, the switching losses were estimated as 5% of the conduction loss of the diode.

Synchronous MOSFET switches are used in this design to achieve higher efficiency and zero voltage transitions from zero to full load. To avoid body diode conduction during the freewheeling period of the converter, the synchronous switches are driven from the primary side.

This technique is called control driven synchronous rectification ([1],[3]) and it offers the capability to reverse the current direction in the output inductors. Similarly to other topologies utilizing control driven synchronous rectification, the turn-off of the appropriate rectifier switch has to precede the switching action on the primary side. The proper timing of the MOSFET rectifiers have an important role in determining the ultimate efficiency of the circuit. Early termination of the conduction interval will force the current into the body diode of the transistors leading to reverse recovery problems and switching losses in the device. Conversely, any delay at the turn-off of the synchronous switches will result in a shoot through situation on the secondary side of the isolation transformer lowering the potential efficiency of the circuit.

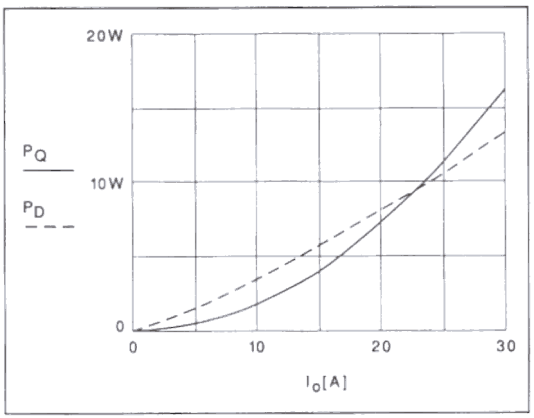


Figure 15. Power Dissipation of Schottky and MOSFET Rectifier Devices

Secondary Gate Drive

Because the timing of the synchronous switches is critical for proper operation, the high current gate drive circuits of Q1 and Q2 are located on the secondary side. Power for these drivers is provided directly from the secondary winding of the main transformer by peak rectification. This way, the drivers are operational even with a shorted output and during start up, when the output pulses are short. The drive signals are transmitted to the secondary side via a signal transformer, a technique which eliminates the delay usually associated with the leakage inductance of the gate drive transformers. Figure 16 shows the logic and the timing relationships between the primary and secondary gate drive pulses.

Adding Parallel Diodes to the Synchronous MOSFETs

This technique is well known, but is not a universal solution to avoid the reverse recovery problem of the body diode in the synchronous MOSFET transistor. The source of the problem is the packaging inductances inherently present in semiconductor packages. Since the body diode is a parasitic component of the silicon structure of the MOSFET device, it is connected in parallel with the channel without any inductance. The current can flow either in the channel or the diode section of the part without overcoming the effect of the bond wire inductance. When the current of the device establishes in the body diode, there is only a very low voltage available to steer the current from the MOSFET diode to any externally paralleled diode. To demonstrate this, assume a very favorable 10nH parasitic inductance for a TO220 semiconductor package. The voltage drop across the body diode is approximately 0.76V at 10A in a MTP75N05HD transistor. On the other hand, a 32CTQ030 type Schottky has a voltage drop of 0.2V at 1A. The maximum rate of change in the current between the two device is:

$$\frac{dI}{dt}_{MAX} = \frac{0.56V}{2 \cdot 10nH} = 28 \frac{A}{\mu sec}$$

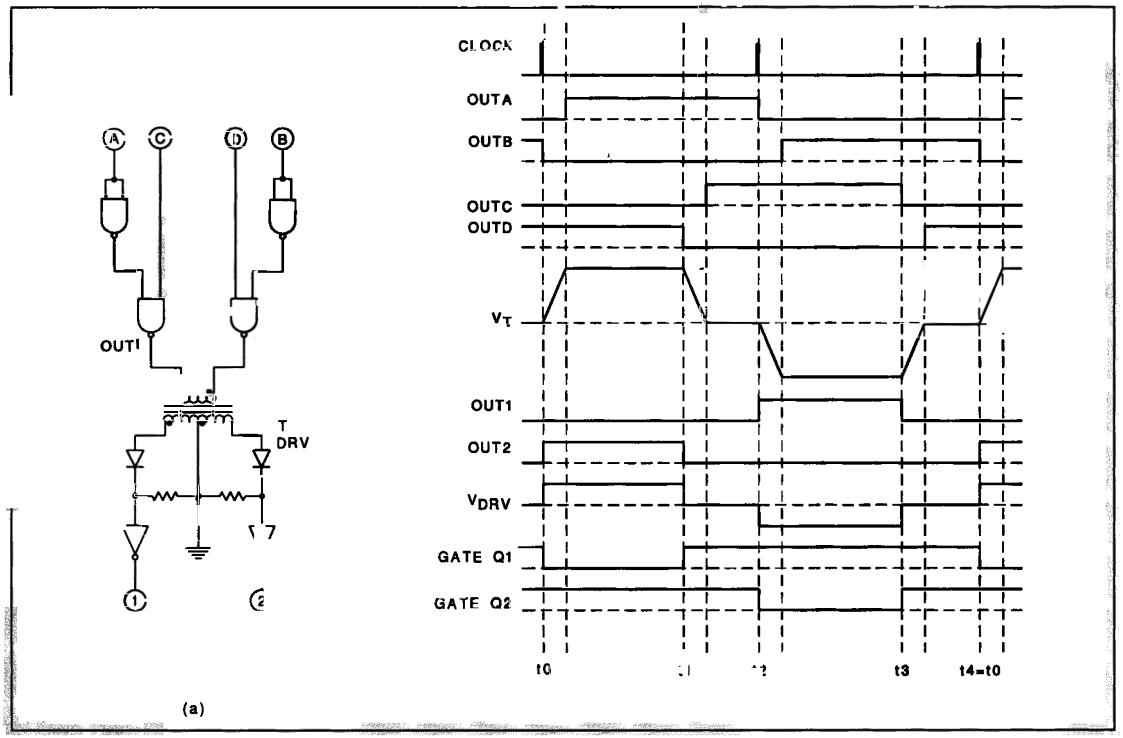


Figure 16. Circuit and Timing Diagram of the Secondary Gate Drive.

That means a minimum of 400ns time interval for the current to be transferred from the body diode to the external Schottky at full load (10A). At higher output currents the situation becomes even worse and the time required to direct the current to an external device very quickly approaches the total duration of the freewheeling period.

Best efficiency results were obtained by slowing down the switching speed of the synchronous switches by placing a 15Ω series resistor in the gate drive path. At turn on, the body diode conducts for a short period of time, but it does not cause significant losses because it will be followed by the conduction of the channel. At the turn off process, the MOSFET operates in linear mode during the switching period preventing a significant portion of the current to flow in the body diode. As a result, body diode conduction and the associated reverse recovery problem is greatly reduced while conduction losses are only slightly increased in the device.

CONTROLLER DESIGN

Controller Setup Using the UC3879

The new UC3879 phase-shift PWM controller is an improved version of the UC3875 family. Below is a list of the improvements and the new features of the IC. Further details on the UC3879 phase shift PWM controller can be found in reference [14]:

- Selectable undervoltage lockout options
- Lower power consumption
- Improved oscillator circuit
- Cycle-by-cycle current limiting
- Flexible delay time circuit with zero delay option
- Low current TTL/CMOS compatible outputs to enhance noise immunity.

In isolated power supplies, where the error amplifier is located on the secondary side of the converter, the controller setup is limited to selecting the appropriate undervoltage lockout option, defining the timing components of the oscillator, determining the proper delay times for the two bridge legs, interfacing the current sense circuit to the controller and calculating the slope compensation if required.

To ensure fast switching speed and fully enhanced operation of the primary side MOSFET transistors, the desired undervoltage lockout is 15.5V for this example. It is accomplished by leaving the UVSEL pin of the UC3879 floating.

Clock frequency of the controller is programmed to 400kHz. In order to maximize the operating duty-cycle of the converter, the timing capacitance is kept at its minimum value, 220pF. Once the CT value is given, RT is defined as:

$$RT = \frac{0.47 + 0.07 \cdot \sqrt{47.17 - 5 \cdot 10^4 \cdot CT \cdot f_{CLOCK}}}{CT \cdot f_{CLOCK}} \quad (16)$$

The time between turning off one switch and turning on the other in the same leg of the full bridge circuit has a profound effect on the circuit performance. One unique feature of the UC3879 is the ability to separately program the delays of the A→P and the P→A bridge legs.

The delay time of the A→P leg is set at the DELAYSET C-D pin of the controller. Figure 7 shows the required time to complete the soft transition in the A→P leg as a function of the load current. According to the graph, the optimum delay varies from 20ns to 165ns depending mainly on the output current and slightly on the input voltage values. Although, using the maximum number will ensure zero voltage switching under all operating conditions, it will reduce the maximum obtainable duty ratio for the converter. For this reason, adjusting the delay time seems desirable. Figure 17 shows a simple solution to adjust the delay time according to the actual load current based on the current information available on the primary side.

The situation is more difficult at the P→A leg. As Figure 14 shows, the longest transition time usually does not coincide with the lowest current level (zero load) in the converter, thus the simple circuit of Figure 17 can not provide the optimal delay under all operating conditions. Nevertheless, it can correct for most of the variations in the transition time above the load current level which corresponds the longest delay time. Below the critical current, the delay time will be somewhat longer than optimum.

When a minimum guaranteed load can be established or the application does not justify the extra complexity of the variable delay time circuit, the delay times can be set to a constant value. For this case, the delay times of the A→P leg shall be set according to the minimum load current, where soft switching is still required, according to equation (17):

$$\tau_{DELAY\_C\text{-}D} = \left(2 \bullet C_{OSS} + C_P + C_{SN}\right) \bullet \frac{V_{I,MAX}}{I_M + N \bullet \left[\frac{I_{O,MIN}}{2} + \frac{V_O}{2 \bullet L1} \bullet (2 - D) \bullet \frac{1}{f_{CLOCK}}\right]}$$

When the delay time is constant, the best approach for the P→A leg is to set the delay time to one fourth of the resonant period of the node capacitance, the leakage and the commutating inductances, as it is given in equation (18).

$$\tau_{DELAY\_A\text{-}B} = \frac{\pi}{4} \bullet \sqrt{(L_{LK} + L_{EXT}) \bullet (2 \bullet C_{OSS} + C_P)}$$

Accurate information of the current flowing through the primary of the power transformer is

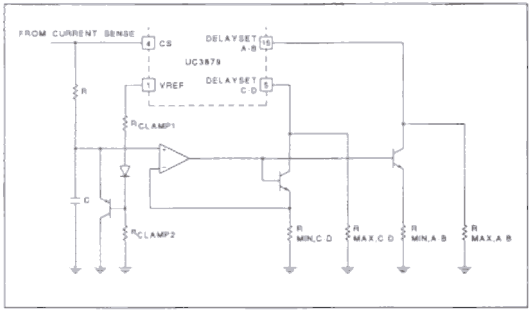


Figure 17.

$$N \bullet \left[\frac{I_{O,MAX}}{2} + \frac{1}{2} \bullet \frac{V_O}{L1} \bullet \left(2 - D_{MIN}\right) \bullet \frac{1}{f_{CLOCK}}\right] \quad (19)$$

needed for this topology, the signal across the resistor at full load shall be set to 2V, which is the maximum signal on the C/S+ pin of the UC3879. Accordingly,

$$R7 = \frac{50 \bullet 2V}{I_{P,MAX}} \quad (20)$$

Primary Gate Drive

There are two different methods to drive the four switches of the full bridge converter in conjunction with the UC3879 controller. One requires high current drivers and two gate drive transformers, each with two secondary windings to drive two MOSFETs in the same bridge leg. The other solution employs integrated high and low side drivers. This design features two IR2110 half bridge MOSFET gate drive integrated circuits from International Rectifier.

Using the integrated half bridge drivers reduced cost, board area and eliminated two additional magnetic components in this application.

Isolated Feedback

This design was intended for modular power architectures where high current loads are often supplied by several, parallel connected power supplies with lower individual current rating. For these applications, the UC3907 load share controller offers a flexible and low cost secondary side solution. This integrated circuit incorporates the precision voltage reference, error amplifier, current sense and load share functions in one 16 pin IC, [15].

Although loop stability is not in the focus of this design review, the following considerations can be useful in closing the feedback loops of the system. From loop stability point of view this circuit operates at 400kHz. It is determined by the controller sampling rate and the output ripple frequency which equal the clock frequency. There are three loops interacting in this power supply. The first loop is the current loop, residing on the primary side. Slope compensation is not required when the current doubler output stage is employed because both filter inductors are working below 50% duty ratio. The gain of the current loop is embedded in the control-to-output transfer function as a constant, below the crossover frequency of the voltage loop. The second loop is the voltage control loop with a crossover frequency of 10kHz in this example. When a third loop, such as the load share circuit, is added to the system, there will be two loops controlling the output voltage. To prevent interaction between the two loops, the designer has to ensure that the crossover frequency of the load share loop is at least one order of magnitude lower than the one of the voltage feedback loop, which is usually adequate in preventing thermal and reliability issues at paralleling modules.

EXPERIMENTAL RESULTS

The final schematic of the power stage and controller section are presented in Figure 18 and 19 respectively.

The example converter was built and tested over all operating conditions. Figure 20 and 21 illustrate the characteristic waveforms of the controller. Figure 20 shows the signal across the timing capacitor (trace 1), the SYNC output of the UC3879 controller (trace 2), the primary current waveform on the secondary of the current sense transformer (trace 3) and the voltage on the COMP pin of the UC3879. As shown, the converter is running closed loop at 400kHz. The four outputs of the controller are displayed in Figure 21. The operating duty ratio is approximately 75%, based on the phase relation between the signals.

The primary side operation of the circuit at 15A and 0A output current is demonstrated in Figure 22 and 23 respectively. The traces in both pictures are A→P leg and P→A leg middle points, transformer current and transformer voltage waveforms. Soft-switching of all four primary switches at no load has been achieved and shown in Figure 23.

Figure 24 and 25 verify the operating principle of the current doubler output stage with respect to the primary waveforms. Shown are the middle points of the A→P and P→A legs along with I_{L1} and I_{L2} at 15A and 0A loads.

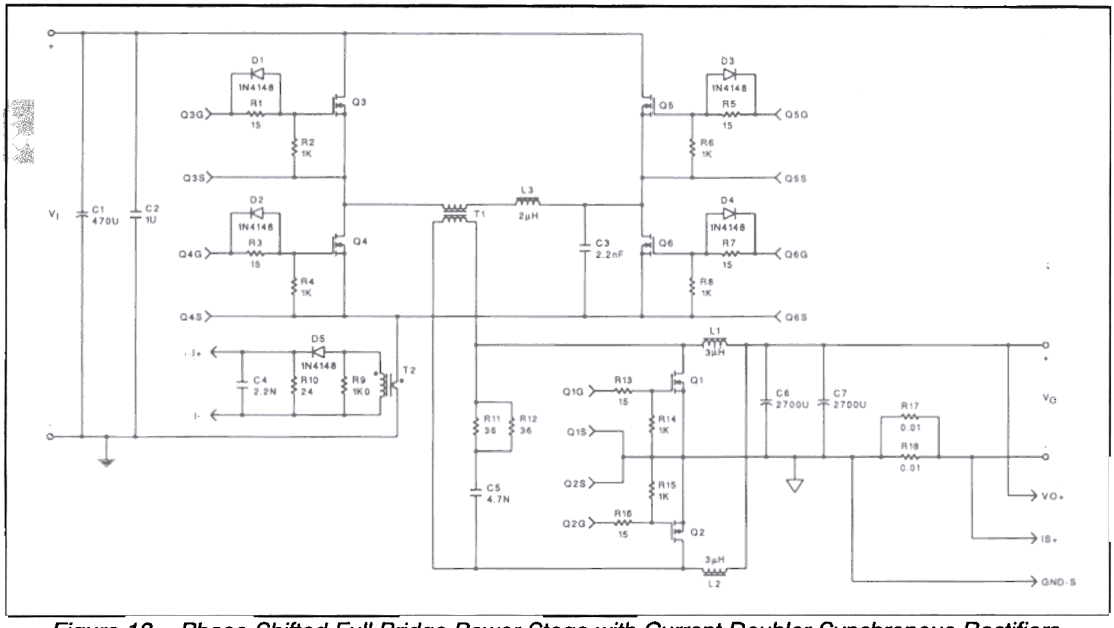


Figure 18. Phase Shifted Full Bridge Power Stage with Current Doubler Synchronous Rectifiers.

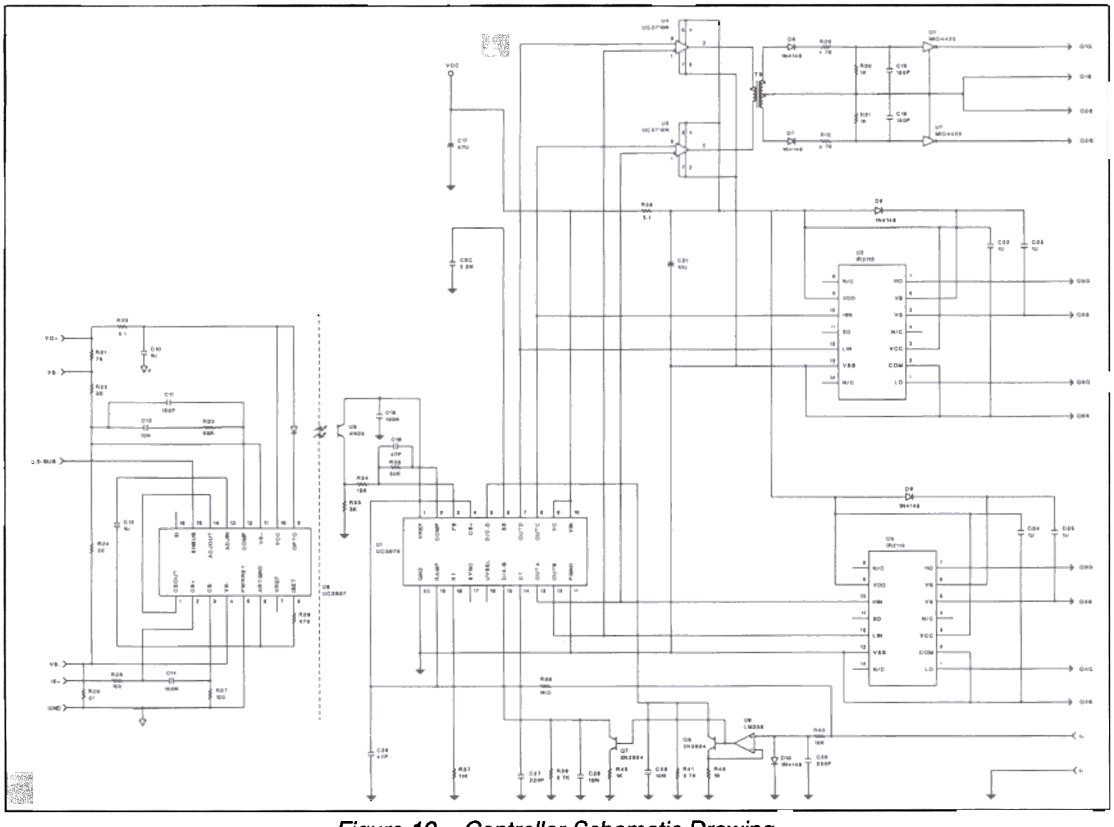


Figure 19. Controller Schematic Drawing.

The next three pictures are dedicated to the resonant transitions of the P→A leg. In Figure 26 the converter is running without load and the resonant transition is completed in a relatively long time, 200ns. The same transition, shown at 10A load in Figure 27, takes only 60ns. Figure 28 was also taken at 10A output current, but the modulation of the delay time was disabled. The comparison of Figure 27 and 28 shows clearly the benefit of the adaptive delay times.

Typical waveforms of the current doubler synchronous rectifier are shown in Figure 29 through Figure 31. The waveforms in Figure 29 and 30 are the voltage of the transformer secondary, the output current before the output filter capacitor and the two individual inductor current at 15A and at 0A load respectively.

Figure 31 completes the tour of the operating waveforms, illustrating the gate drive waveforms of the synchronous switches in respect to the transformer secondary voltage and the unfiltered output current at 15A load.

The efficiency of the circuit measured at nominal input voltage, is shown in Figure 32. The highest efficiency achieved was 92.5% at half load. The circuit operated above 90% efficiency in the range from 4A to 20A load current.

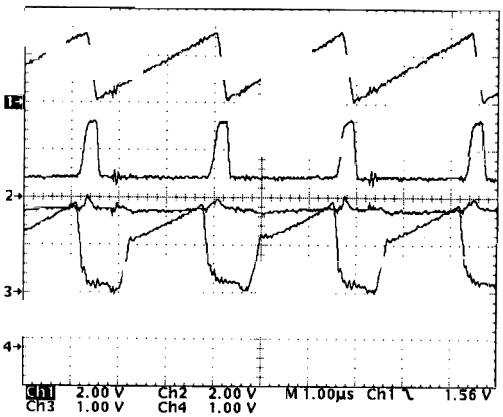


Figure 20. Controller Waveforms; CT (pin 14), CLKSYNC (pin 17), RAMP (pin 19) and COMP (pin 2).

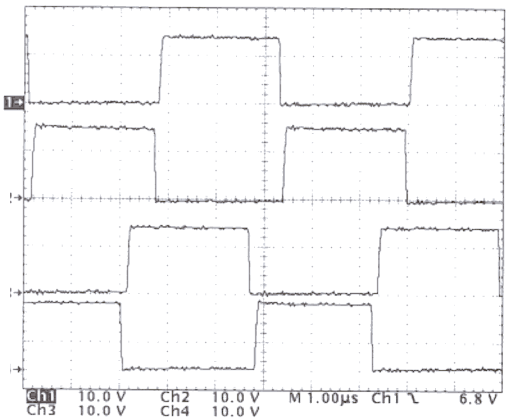


Figure 21. Controller Waveforms; OUT A (pin 13), OUT B (pin 12), OUT C (pin 8), OUT D (pin 7).

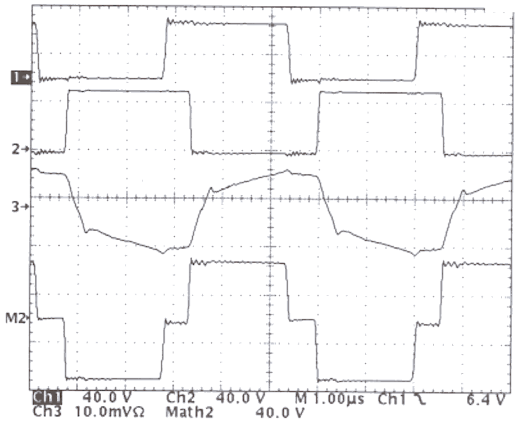


Figure 22. Waveforms of the primary at 15A load; P→A leg, A→P leg, transformer primary current (5A/div), and primary voltage.

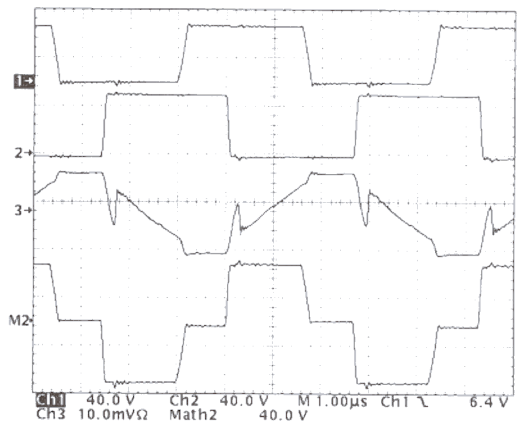


Figure 23. Waveforms of the primary at 0A load; P→A leg, A→P leg, transformer primary current (2A/div), and primary voltage.

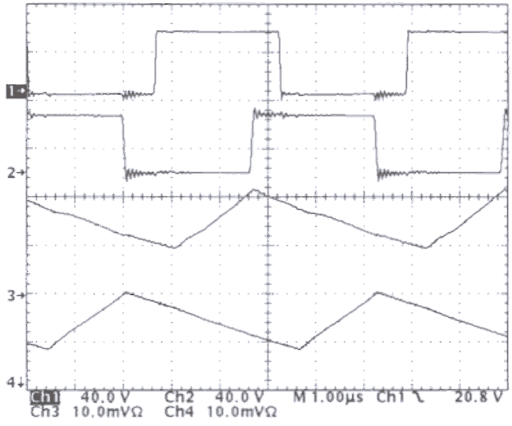


Figure 24. Operating Waveforms at 15A load; P→A leg, A→P leg, I_{L1}, I_{L2}, (both 5A/div).

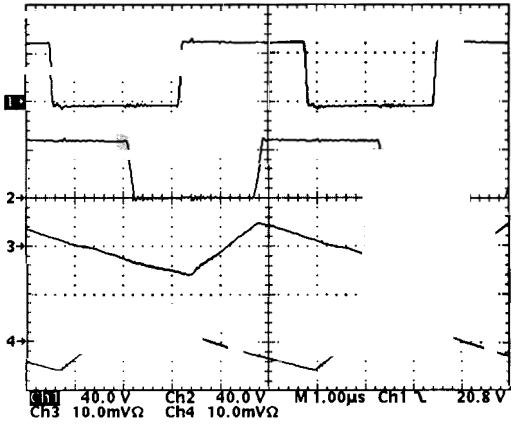


Figure 25. Operating Waveforms at 0A load; P→A leg, A→P leg, I_{L1}, I_{L2}, (both 5A/div).

CONCLUSION

The current doubler topology with synchronous rectification had been presented. This alternative rectification technique simplifies the power transformer and adds one more filter inductor to the output rectifier circuit in push-pull, half-bridge and bridge converters. Superior performance of the circuit had been shown in a 100W, 400kHz, DC-DC converter. The example power supply combines the excellent characteristics of the current doubler rectifier with the superior properties of the phase shifted full bridge converter on the primary side. This combination has proved its effectiveness achieving efficiency above 92% in an isolated 5V output power supply, operating from a 48V distribution bus.

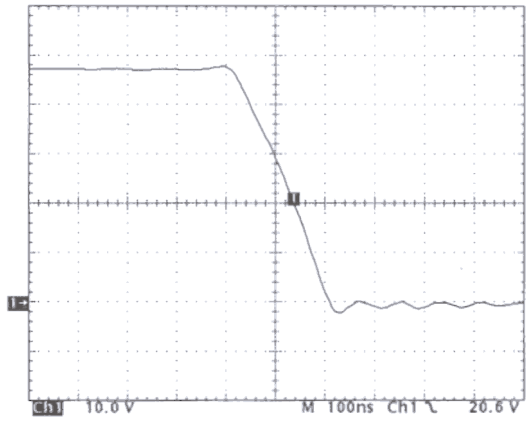


Figure 26. Transition time recorded at OA load.

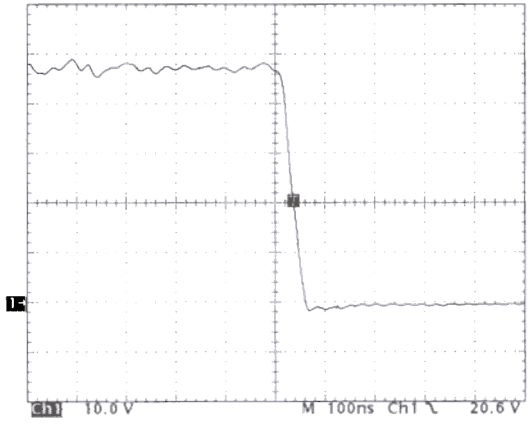


Figure 27. Transition time at 15A using adaptive delay time control.

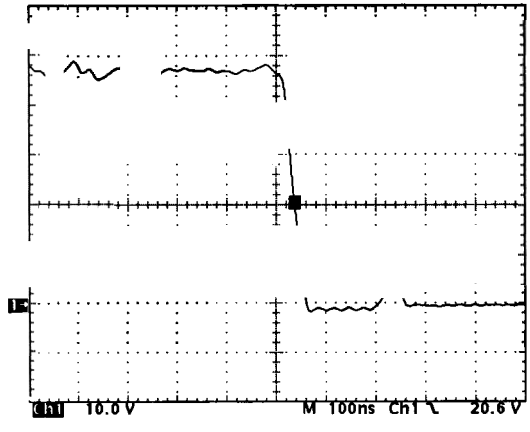


Figure 28. Transition time without the adaptive delay time control.

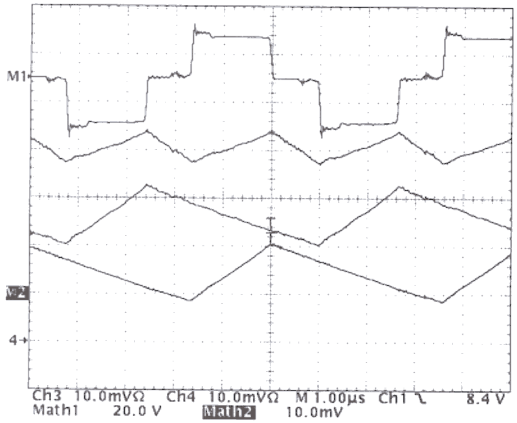


Figure 29. Secondary Waveforms at 15A load; transformer secondary voltage, $I_{L1} + I_{L2}$, I_{L1}, I_{L2}, (all 5A/div).

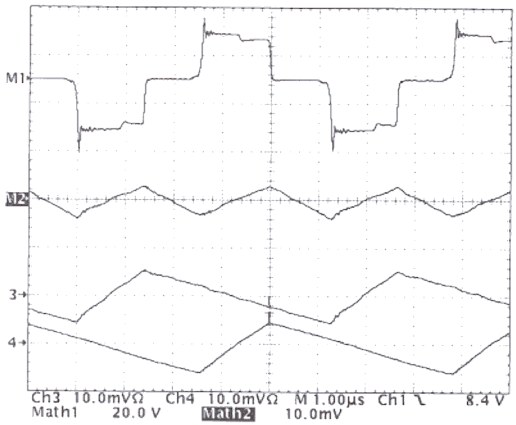


Figure 30. Secondary Waveforms at OA load; transformer secondary voltage, $I_{L1} + I_{L2}$, I_{L1}, I_{L2}, (all 5A/div).

In addition, the component selection criteria and consideration for the critical design steps of the phase shifted full bridge converter had been covered. Soft-switching operation from zero to full load had been demonstrated to verify the design procedure.

REFERENCES

[1] L. Balogh, "The Performance Of The Current Doubler Rectifier With Synchronous Rectification", HFPC '95 Proceedings, pp. 216-225

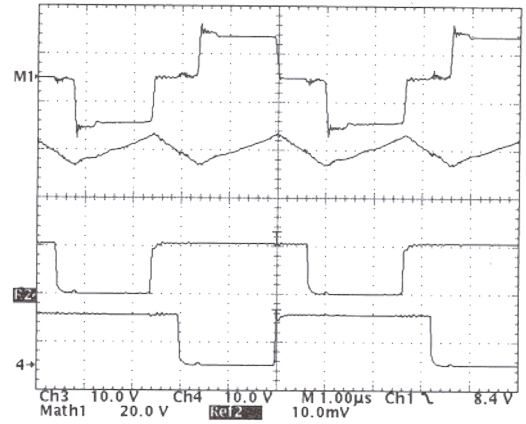


Figure 31. Secondary Waveforms at 15A load; transformer secondary voltage, $I_{L1}+I_{L2}$ (5A/div) and gate signals of the synchronous switches (Q1 and Q2)

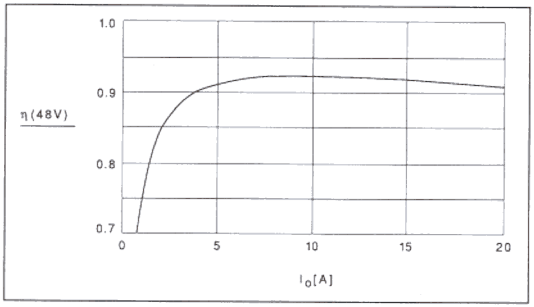


Figure 32. Efficiency vs. Load @ 48V input.

[2] K. O'Meara, "A New Output Rectifier Configuration Optimized For High Frequency Operation", HFPC '91 Proceedings, pp. 219-225

[3] I. D. Jitaru, "High Efficiency DC-DC Converter", HFPC '94 Proceedings, pp. 120-127

[4] L. Balogh, "The Current doubler Rectifier: An Alternative Rectification Technique For Push-Pull and Bridge Converters", Design Note-63, Unitrode Integrated Circuit Corporation, DG-300, pp. 12-14

[5] W. M. Andreycak, "Design Review: 500W, 40W/in3 Phase Shifted ZVT Power Converter", Topic 4, SEM-900 Power Supply Design Seminar Manual, Unitrode Integrated Circuit Corporation

[6] L. Balogh, R. Redl, D. W. Edwards, "Optimum ZVS Full Bridge DC/DC Converter With PWM Phase-Shift Control: Analysis, Design Considerations, And Experimental Results", APEC '94 Proceedings, pp. 159-165

[7] R. Redl, L. Balogh, N. O. Sokal, "A Novel Soft-Switching Full Bridge DC/DC Converter: Analysis, Design Considerations, And Experimental Results At 1.5 kW, 100 kHz", PESC '90 Proceedings, pp. 162-172

[8] W. M. Andreycak, "Designing A Phase Shifted Zero Voltage Transition (ZVT) Power Converter", Topic 3, SEM-900 Power Supply Design Seminar Manual, Unitrode Integrated Circuit Corporation

[9] O. D. Patterson, D. M. Divan, "Pseudo-resonant Full Bridge DC/DC Converter", PESC '87 Proceedings, pp. 424-430

[10] G. Moschopoulos, et al, "A Fixed Frequency ZVS High Power SMR Converter With Zero To Rated Load Variation Capability", INTELEC '92 Proceedings, pp. 351-358

[11] "UC3879 Phase-Shift Resonant Controller", Data Sheet, Unitrode Integrated Circuit Corporation, Product & Applications Handbook 1995-96, pp. 6-357 - 6-361

[12] L. H. Dixon, "Power Transformer Design For Switching Power Supplies", SEM-100 Power Supply Design Seminar Manual, Unitrode Integrated Circuit Corporation (reprinted in subsequent Seminar Manuals)

[13] L. H. Dixon, "Design Of Flyback Transformers And Filter Inductors", SEM-400 Power Supply Design Seminar Manual, Unitrode Integrated Circuit Corporation (reprinted in subsequent Seminar Manuals)

[14] L. Balogh, "The New UC3879 Phase Shifted PWM Controller Simplifies The Design Of Zero Voltage Transition Full Bridge Converters", Application Note U-154, Unitrode Integrated Circuit Corporation

[15] "UC3907 Load Share Controller", Data Sheet, Unitrode Integrated Circuit corporation, Product & Applications Handbook 1995-96, pp. 6-419 - 6-424

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