High Fidelity Pulse Width Modulation Amplifiers based on Novel Double Loop Feedback Techniques

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High Fidelity Pulse Width Modulation Amplifiers based on Novel Double Loop Feedback Techniques

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Abstract

This paper addresses the realisation of high performance, high efficiency audio power amplifiers using Pulse Width Modulation and a novel double loop feedback technique. Using both current and voltage feedback, certain advantages are obtained in comparison to more conventional topologies. Both two level (class AD) and three level (class BD) PWM are analysed in detail to find the optimal modulation method. A 200W/8ohm prototype has shown convincing performance with THD+N<0.1%, a 113 dB dynamic range and an efficiency approaching 90% at higher output powers.

1. Introduction

Pulse Width Modulation has been known for numerous years and has many applications with in power supplies motor drivers etc. The theoretical possibility of realising high efficiency amplifiers is very attractive but several problems has prevented widespread use of this very different principle of power amplification:

- Distortion and noise problems.
- Sensitivity to load variations due to the inherent passive post filter preventing general purpose use.
- Power consumption not satisfying [4].
- Power amplifier cost and complexity [4,6].

This paper addresses these problems with a new approach, based on a double feedback loop configuration.

2. Pulse Width Modulation

The basic principle behind a *PWM amplifier* is shown in Fig. 1. The amplifier principle is also termed a *digital power amplifier* due to the digital operation of the power transistors or a *class D amplifier*. The audio signal is pulse width modulated by comparing it with a reference signal (carrier) which can be performed in either the digital or analogue domain. The resulting small signal PWM is converted to power levels by the power switch. Ideal switching elements operating either 'on' or 'off' is the secret behind the theoretical very high efficiency of the PWM based amplifier.

The carrier is a sawtooth or a triangle signal corresponding to single sided modulation (leading or trailing edge) and double sided modulation, respectively. The modulation process of both modulation strategies is illustrated in more detail in Fig. 2. Further modulation

subclasses are defined by the switching method which can be either AD (two level) or BD (three level). As illustrated in Fig. 2, AD PWM takes two 'digital' values whereas three level switching takes three values.

Clearly, the modulation results in a sampling of the signal. Since the pulse edges coincide exactly with the point at which the signal is sampled the sampling approach is termed *natural sampling* or analogue PWM. The alternative main class of modulation is *uniform sampling* also termed digital PWM. Uniform sampling refers to modulation based on a sampled signal. In recent years, there has been a considerable interest in digital amplifiers based on variations of digital PWM, but several problems as discussed in [1] with the power stage of these amplifiers have prevented a breakthrough. This paper is concentrated on double sided PWM due to the advantages of double sided modulation. Class AD and BD modulation are analysed in detail to find the most suitable modulation strategy for the novel double loop based amplifier topology.

2.1 Double sided AD PWM

Fig. 2a shows a principal diagram of a power stage driven to achieve AD PWM. Each half-bridge voltages are denoted as v_A and v_B, respectively. The voltage across the load impedance (Z) is then given by:

$$v_Z(t) = v_A(t) - v_B(t) \tag{1}$$

Due to the 'inverted' drive of the two half-bridges the voltage across the load impedance takes two voltage levels, either -V or V. The signal is sampled once in each period of the carrier signal, i.e. the sampling frequency is equal to the carrier frequency.

Pulse width modulation of a sine wave has been analysed by Black [7]. Using a double fourier series, a sine wave modulated by double sided AD PWM can be expressed as:

$$\begin{aligned} x_{AD}(t) = {} & M \cdot V \cdot \cos(\omega \cdot t) + 4 \cdot U \cdot \sum_{m=1}^{\infty} \frac{J_0(M \cdot m \cdot \frac{\pi}{2})}{m \cdot \pi} \cdot \sin(m \cdot \frac{\pi}{2}) \cdot \cos(m \cdot \omega_{carr} \cdot t) \\ & + 4 \cdot V \cdot \sum_{m=1}^{\infty} \sum_{n=-\infty}^{n=\infty} \frac{J_n(M \cdot m \cdot \frac{\pi}{2})}{m \cdot \pi} \cdot \sin((m+n) \cdot \frac{\pi}{2}) \cdot \cos(m \cdot \omega_{carr} \cdot t + n \cdot \omega \cdot t) \end{aligned} \tag{2}$$

Where:

M	Modulation index. The signal amplitude relative to the carrier.
V	Power supply level (DC)
ω	Audio signal angle frequency.
ω_{carr}	Carrier signal angle frequency.
J_n	Bessel function of nth order
n	Index to the harmonics of the audio signal
m	Index to the harmonics of the carrier signal

From the double fourier series, the individual components are easily determined. Fig. 3 (left) illustrates the spectral content of a AD pulse with modulated sine wave, with the parameters:

f = 20KHz, f_{carr} = 315KHz and M = 0, -20dB and -40db

The following can be concluded:

- All harmonics of the switching frequency are represented at all output levels.
- The frequency spectrum contains intermodulation components between the audio and the carrier frequency and they occur symmetric around each of the harmonics of the carrier frequency.
- There are no direct harmonic components of the audio signal (the typical characteristic of natural sampling) .

2.2 Double sided BD PWM

Fig. 2b illustrates the signals in an ideal output stage driven to achieve BD PWM. The half-bridges are driven by separate modulators and the B bridge comparator is feed with the inverted audio signal to obtain the desired switching characteristics Fig. 2a illustrates, how the output voltage switches between 0 and V with positive audio signal polarity and between *0* and *-V* with negative audio signal polarity and the maximum output voltage step of the H-bridge is thus V. The zero level in BD PWM is obtained by applying the same level at each half bridge output either $v_A=v_B=0$ or $v_A=v_B=V$. The maximum differential output voltage step is thus halved, which means that the maximum ripple current in the load impedance decreases. But due to the zero level generation, the output contains both differential- and common mode components [1,2].

Fig. 2 also illustrates, that the audio signal is sampled *twice* in every carrier period. The effective switching frequency is thus doubled to $2 \cdot f_{carr}$. This very attractive feature of BD PWM can be beneficial in multiple ways (compared to AD):

- A reduction of the switching frequency and thereby the switching losses by a factor of 2.
- An increase of loop bandwidths without an increase of carrier frequency.

As with AD PWM a sine wave modulated by double sided BD PWM can be expressed as a double fourier series:

$$x_{BD}(t) = M \cdot V \cdot \cos(\omega t) - 4 \cdot U \cdot \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm\infty} \frac{J_n(m \cdot M \cdot \frac{\pi}{2})}{m \cdot \pi} \cdot \sin((m+n) \cdot \frac{\pi}{2}) \cdot \sin(n \cdot \frac{\pi}{2}) \cdot \sin((m \cdot \omega_{carr} + n \cdot \omega) \cdot t - n \cdot \frac{\pi}{2}) \quad (3)$$

Fig. 3b illustrates the spectral content of a pulse width modulated signal, with the same parameters as double sided AD switching. The following special features of BD PWM should be noticed:

- The modulated signal does not contain any harmonics of the carrier frequency. Thus, IM components are placed symmetrically around the even harmonics of the carrier.
- There are no intermodulation components *around odd multiple* of the carrier frequency. Thus, the IM components with the lowest frequencies are located around $2 \cdot f_{carr}$. This corresponds well with the effective doubling of the switching frequency as discussed above.

- The intermodulation component amplitudes *decrease linearly with the audio signal.* Thus, in theory the residual is totally 'noiseless'.

The disadvantages of double sided BD PWM compared to double sided AD PWM are mainly that the output of the H-bridge contains a switching common mode voltage with a peak to peak amplitude of V, and the small increase in modulator complexity. Furthermore, class BD requires a more precise control of the switches of the load to obtain a satisfying distortion performance open loop. The effect of these important differences in respect to the novel feedback topology will be analysed in the following sections.

3. Amplifier topology

Traditional approaches to feedback in PWM amplifiers have certain disadvantages. Single loop feedback after the post filter can not be applied without performance degrading lead compensation [5] due to the phase shift of the filter. Applying efficient feedback before the post filter [1] is a possible solution, but there is no correction of the possible non-linear post filter behaviour, i.e. linear core materials are necessary to prevent filter induced distortion and intermodulation. The dependence between amplitude response and load impedance, prevents general purpose use where the load is unknown. Since the very goal of this work was to invent a non complex amplifier principle with a good insensitivity to load variations an alternative approach have been investigated.

A new feedback topology based on both current and voltage feedback is proposed. The topology, shown in Fig. 4 combines high loop gain bandwidth, load impedance insensitivity and post filter error correction and is therefore very suited for general purpose amplifier applications. The feedback network consist of an inner current loop that converts the output stage and a second order post filter to a first order system with high bandwidth. General purpose voltage feedback can thereafter be applied across the load impedance without performance degrading lead network. The obvious advantages of the proposed double loop topology are:

- The local feedback of the current loop corrects the power stage errors close to their source (the PWM output stage and the modulator is the determining noise and distortion source).
- A double loop results in a double correction of errors.
- Although the current loop increases the output impedance of the inner loop (ideally a current generator), the gain of the outer loop gives a low resulting output impedance.
- The voltage loop reduces the demands of post filter linearity.

The disadvantages of the double loop control is that a resistive measuring of the current leads to extra power losses reducing the efficiency of the system in comparison to e.g. [1]. Furthermore, exact current measurement without introducing unwanted measurement noise is no simple matter [2].

4. Double loop feedback topology

The first order approximation to the current loop is shown in [3] for general control of switching regulators. This basic theory has been extended to audio amplifiers in [2]. The essential elements of the feedback topology is shown in fig. 4.

4.1 The current loop

The closed current loop transfer function, defined as the voltage measured over the equivalent measurement resistance, can be expressed as:

$$H_{cl,c}(f) = \frac{i_L(f) \cdot R_s}{V_{c,in}(f)} = \frac{1}{1 + \frac{Z_t(f)}{H_c(f) \cdot K_{PWM} \cdot R_s}} = \frac{1}{1 + \frac{Z_t(f)}{K_1 \cdot K_{PWM} \cdot R_s}} \tag{4}$$

where:

- $Z_t(f)$ is the total impedance of post filter and load impedance (a second order system).
- R_s is the equivalent current measurement resistance.
- $H_c(f)$ is the current forward path transfer function. In this work $H_c(f)$ is a constant, $H_c(f)=K_1$.

K_{PWM} is the equivalent gain of the PWM-modulator, given by:

$$K_{PWM} = \frac{V}{V_{carr}} \tag{5}$$

$Z_t(f)$ is given by:

$$Z_t(f) = j \cdot 2\pi \cdot f \cdot L + \frac{R_L}{R_L + j \cdot 2\pi \cdot f \cdot R_L \cdot C} \tag{6}$$

Where L and C are the 2nd order post filter components and R_L is the load impedance which here is assumed to be resistive. The following theory can easily be generalised to more typical load impedances with resonant peaks and the typical 3dB/octave rise at higher frequencies. An investigation of the transfer function shows that it can be approximated by a first order system if certain conditions are satisfied:

$$H_c(f) >> \frac{R_L}{K_{PWM} \cdot R_s} \quad \text{for} \quad f \leq \frac{1}{2 \cdot \pi \cdot R_L \cdot C} \tag{7}$$

Under these assumptions the closed current loop can be expressed as:

$$H_{cl,c}(f) = \frac{i_L(f) \cdot R_s}{V_{c,in}(f)} = \frac{1}{1 + \frac{j \cdot 2\pi \cdot f \cdot L}{K_1 \cdot K_{PWM} \cdot R_s}} \tag{8}$$

This is clearly a first order system with the bandwidth

$$f_{bw,c} = \frac{K_1 \cdot K_{PWM} \cdot R_S}{2 \cdot \pi \cdot L} \tag{9}$$

The bandwidth is thus proportional to K_1. The maximum bandwidth of the current loop is obtained with the maximum value of K_1. The constant is limited by the *ripple stability* criteria due to ripple current in the filter inductor. Ripple unstability occurs when the slew rate of the feedback signal is larger than the slewrate of the carrier signal which is:

$$SR_{carr} = 4 \cdot V_{carr} \cdot f_{carr} \tag{10}$$

where V_{carr} is the peak amplitude of the carrier. The maximum SR of the feedback signal is dependent on modulation method and this is one of the factors that influence on the choice of modulation method. The slew rates for the two modulation approaches can be expressed as:

$$SR_{f,AD} = \frac{K_1 \cdot R_s \cdot 2 \cdot V}{L} \tag{11}$$

$$SR_{f,BD} = \frac{K_1 \cdot R_s \cdot V}{L} \tag{12}$$

The maximum values of K_1 that will secure ripple stability are therefore:

$$K_{1,AD} = \frac{2 \cdot V_{carr} \cdot f_{carr} \cdot L}{R_s \cdot V} = \frac{2 \cdot f_{carr} \cdot L}{R_s \cdot K_{PWM}} \tag{13}$$

$$K_{1,BD} = \frac{4 \cdot V_{carr} \cdot f_{carr} \cdot L}{R_s \cdot V} = \frac{4 \cdot f_{carr} \cdot L}{R_s \cdot K_{PWM}} \tag{14}$$

The maximum current loop bandwidth is derived by inserting (.13) and (14) in (9). This leads to the following maximal bandwidths for the two considered modulation approaches.

$$f_{bw,c} = \frac{f_{carr}}{\pi} \quad \text{(AD)} \tag{15}$$

$$f_{bw,c} = \frac{2 \cdot f_{carr}}{\pi} \quad \text{(BD)} \tag{16}$$

From a conventional Nyquist sampling viewpoint the bandwidth of the current loop is also limited by the carrier/sampling frequency:

$$f_{bw} < f_s$$

As explained in the "Pulse width Modulation" section above the sample rate was found to be equal to the carrier frequency for AD PWM and equal to twice the carrier frequency for BD PWM. The limiting factor on loop bandwidth is therefore ripple stability. In short, the use of BD PWM has the very important advantage of doubling the bandwidth of the current loop in comparison to AD PWM.

4.2 The voltage loop

The bandwidth of the voltage loop is limited by the bandwidth of the current loop. It was shown above that the current loop can be approximated with a first order system under given assumptions, which are easily obtained in practical applications. Since the general voltage feedback is applied on this first order system, the feedback potential is increased considerably compared to traditional single loop voltage feedback with variants of lead compensation [4,6].

From fig. 4 and the current loop expression (8) above we get the following open loop transfer function of the voltage loop:

$$H_{ol,v}(f) = \frac{H_v(f) \cdot K}{R_s \cdot \left(1 + j \cdot \frac{f}{f_{bw,c}}\right)} \cdot \frac{R_L}{1 + j \cdot \frac{f}{f_{RC}}} \qquad (17)$$

where $f_{bw,c}$ is given in (9) and f_{RC} is:

$$f_{RC} = \frac{1}{2 \cdot \pi \cdot R_L \cdot C} \qquad (18)$$

From (17) we derive the closed loop expression :

$$H_{cl,v}(f) = \frac{1}{K} \cdot \frac{1}{1 + \frac{R_s}{H_v(f) \cdot K \cdot R_L} \cdot \left(1 + j \cdot \frac{f}{f_{bw,c}}\right) \cdot \left(1 + j \cdot \frac{f}{f_{RC}}\right)} \qquad (19)$$

The audio band closed loop gain is determined by K alone. The closed loop bandwidth is a parameter that can be chosen arbitrarily. Placed under the bandwidth of the current loop the design criteria of 45 degrees phase margin will be achieved.

The following table summarises some of the interesting observations of the previous sections:

Configuration	AD	BD
Effective switching frequency	f_{carr}	$2 \cdot f_{carr}$
Current loop OL BW	$f_{bw,c} = \frac{f_{carr}}{\pi}$	$f_{bw,c} = \frac{2 \cdot f_{carr}}{\pi}$
Load differential noise	-	+
Load common mode noise	+	-

To conclude from the comparison of double sided AD and BD PWM the advantages of double sided BD PWM, in terms of modulation spectrum and possible open loop bandwidths, overcome the disadvantages.

4.3 Loop synthesis

The placement of system singularities can be done in many ways given the bandwidth limitations above as the primary restriction. It has been shown that the loop bandwidths of both current and voltage loop can be chosen close to the switching frequency, especially with BD PWM. It is therefore possible to realise reasonable high bandwidth control loops with modest switching frequencies. The typical control loop design criteria of a 45 degrees phase margin can be achieved with a bandwidth of the closed voltage loop that is equal to the bandwidth of the current loop.

A possible way of loop design is based on the desirable loop response. The loop bandwidth frequency and choice of modulation scheme will determine the carrier frequency by (15) and

(16). To achieve the typical 'dominant pole' integrator characteristic of the voltage loop, a zero can be placed a decade below the current loop bandwidth frequency $f_{BW,c}$. This placement will not influence the phase margin.

The RC pole should be placed at the audio bandwidth limit. A lower placement of the RC pole is desirable in respect to loop gain characteristics and damping of high frequency noise. The problem of this approach is an increase of the maximum peak output current of the power stage. The placement of the RC-pole is thus a compromise between maximum feedback in the audio band and minimum peak output current of the power stage.

5. The implementation of a 200W/8 ohm prototype

A prototype of the double loop topology was developed. Due to the above mentioned advantages of BD PWM this modulation strategy was chosen for implementation. The table below gives a summary of the important parameters:

Power supply level (single)	70V
Carrier frequency	315 KHz
Current loop bandwidth	200 KHz
Voltage loop bandwidth	200 KHz
Current loop gain	20dB
Voltage loop gain	20dB - 40dB

The power supply level of 70V corresponds to a maximum modulation index of 0.85.

5.1 Realisation

The modulator, driver and power stage are crucial elements in the system. A carefully designed circuit and layout are essential to obtain optimal performance of each element and thereby good system performance, in terms of a very low distortion and noise level. The demands rise with amplifier power handling capability. With optimal design an open loop distortion between 0.01% to 1% can be achieved at all frequencies, even at high power 200W-300W amplifiers.

The possibility of realising very high performance amplifiers with high efficiency today, is partly due to the development in Power MOSFET transistors and driver technology in the recent years. Fully integrated H-bridge drivers capable of sourcing and sinking the high peak currents are necessary for a precise control of the bridge transistors. The use of fully capable, integrated driver circuits dramatically reduces the system complexity.

In general, the implemented double loop topology was a non complex low cost construction.

5.2 Results of implementation

Measurements on the implemented prototype are illustrated in Fig. 5-10. Fig. 5 shows bode plots of the amplifier driving load impedances from 4-8 ohm. The Bode plots demonstrate the insensitivity to load variations. The table below summarises the pass band gain and phase variations:

Nom. load impedance	Gain	Phase
8	±0.1 dB	±7 deg
4	±0.7 dB	±11deg

It is important to notice that the small variations in the amplifiers' gain and phase at 8 ohm load impedance are obtained while having a second order passive post filter at 20KHz which effectively suppresses intermodulation components between the carrier and audio signal.

THD+N versus frequency was measured at four output powers levels increasing from 40mW to 200W in a 4ohm and an 8ohm load impedance. Fig. 6 illustrates the equivalent measurements in both 4 and 8 ohms. There is a reasonable independence of load impedance (in terms of maximum distortion). THD+N increases as predicted (corresponding to the shape of the voltage loop) with frequency from 0.007% to 0.15% at higher output powers. Maximal distortion is in the frequency band 5KHz - 7KHz. The decrease in THD+N above 7KHz is mainly due to post filter damping of the primary 2nd and 3rd harmonics. At output powers below 40mW, THD+N are determined by the residual noise of the amplifier. This is confirmed by the flat characteristic at 40mW in both the load impedances, where THD+N is constant around 0.02%.

A 16K 16x averaged FFT-analysis of the residual noise is shown Fig. 7. The measured unweighted audio band noise is 90μV RMS in an 8ohm load. This corresponds well with the noise floor level around 1μV with the given FFT parameters. The residual noise does not contain noticeable spurious tones, and supply hum is well damped. The residual noise is remarkably low when comparing with other amplifiers principles. The low residual noise level gives an unweighted dynamic range of around 113dB.

A 16K FFT-analysis of a 1KHz sine wave at 1W output power is shown in Fig. 8. The harmonic roll-off is seen to be well behaved. Al components above the 3rd harmonic are well damped. The distortion is primarily uneven harmonic, with the 3rd harmonic dominating with 180μV corresponding to a 3rd harmonic distortion of 0.006% relative to the fundamental. There are no significant spurious tones in the output. At higher output powers 100W-200W, the noise floor rises noticeable due to the nature of class BD modulation, but the noise level never gets to be dominating compared to the harmonic distortion.

Fig. 9 illustrates the efficiency versus output power measured with an 8 ohm load. At maximum output powers the efficiency approaches 90%. Due to quiescent power losses in the area of 12W the efficiency decreases with lower output powers and is less than 30% at output powers below 10W. In [1], considerably lower power losses have been achieved (full bandwidth version). The reasons are mainly the necessary higher switching frequency and supply voltage in this topology, the current measurement and the demands of very small blanking time. But even with an idle power dissipation of 12W it is possible to reduce the needed heatsink volume more than 10 times, relative to a similar conventional class B amplifier due to the high efficiency at higher outputs.

The table below summarises the obtained amplifier specifications:

Max. power (continuous)	200W
Frequency response	3Hz - 30KHz / 8 ohm 3Hz - 22KHz / 4 ohm
Load impedance	4 ohms / 8 ohms
Supply voltage (single)	70V
THD+N (20Hz→f_{max} , 40mW→Po_{max})	0.003%-0.15% (4 ohm) 0.006%-0.12% (8 ohm)
Residual noise 20Hz-22KHz (unw)	90μV RMS
Dynamic range (unw)	113dB
Idle consumption - Total	12W
Maximal efficiency	90%

6. Conclusions

This paper has addressed the realisation of high fidelity PWM switching amplifiers for general purpose use based on a novel double loop topology with both current and voltage feedback. The topology has been analysed and the advantages and disadvantages of the topology have been pointed out. A 200W prototype has shown good performance especially in terms of dynamic range, distortion and maximal efficiency.

It is in the authors belief that the achieved performance of this new principle makes it a promising, non- complex alternative to previously proposed topologies based on pulse with modulation and linear amplifiers in general.

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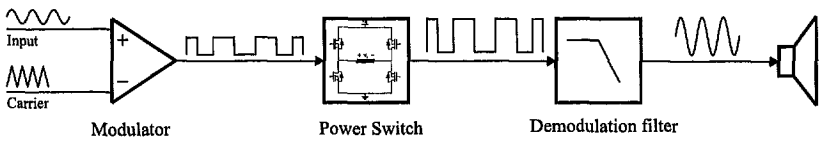

Fig. 1 Basic principle of pulse width modulation

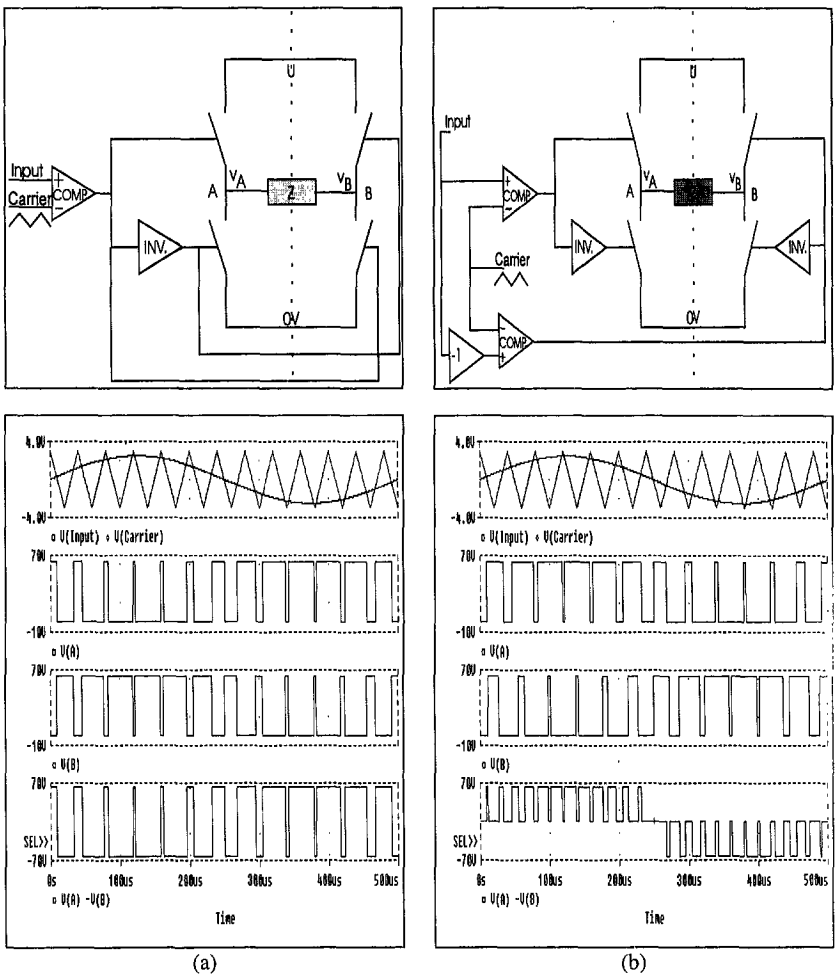

Fig. 2 PWM modulators, and the important output stage signals in AD and BD PWM.

AD. f=20KHz. f_c=315KHz.

BD. f=20KHz. f_c=315KHz.

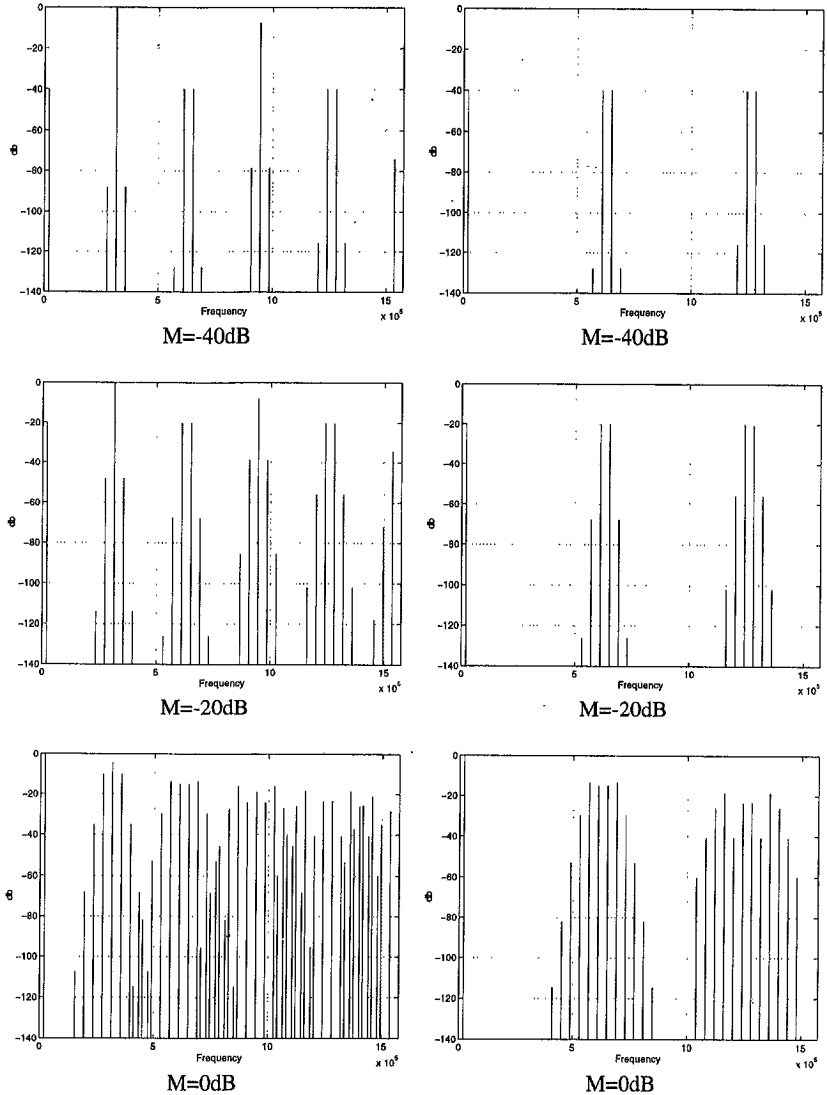

Fig. 3 Modulation spectra of AD and BD PWM with modulation indexes M=-40dB, -20dB and 0dB.

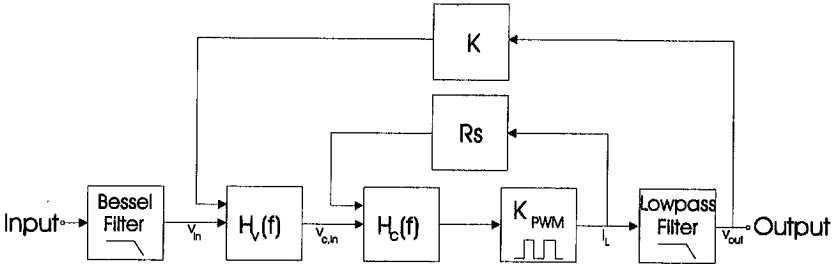

Fig. 4 Blockdiagram of the double loop network.

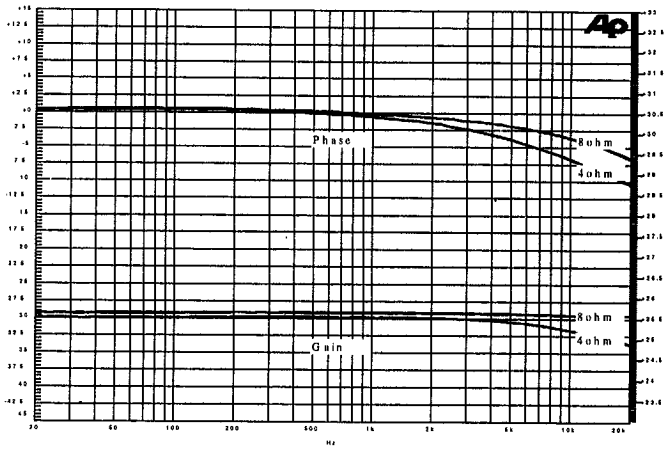

Fig. 5 Relative gain and phase caracteristics for 4 and 8 ohm nomial load impedances.

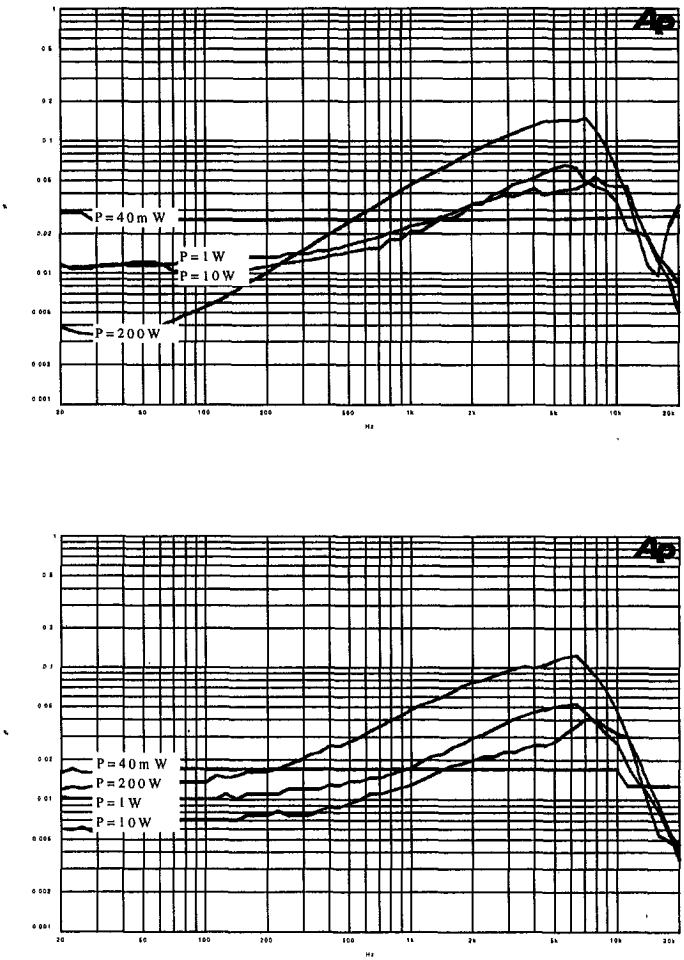

Fig. 6 THD+N versus frequency measured at five representative output levels increasing from 40mW to 200W. The upper curve is with a 4ohm dummy impedance, and the lower curve is with an 8 ohm load impedance.

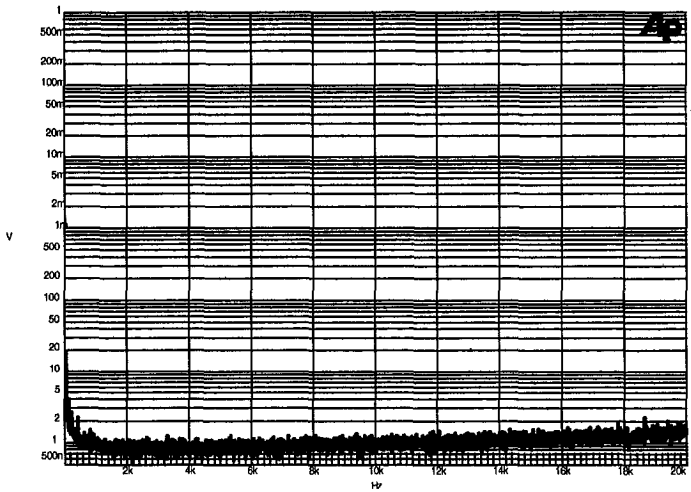

Fig. 7 16K FFT-analysis of the residual amplifier noise . The sampling frequency is 44.1KHz. The resulting inband residual noise is around 90μV RMS, corresponding to a dynamic range of 113dB unweighted.

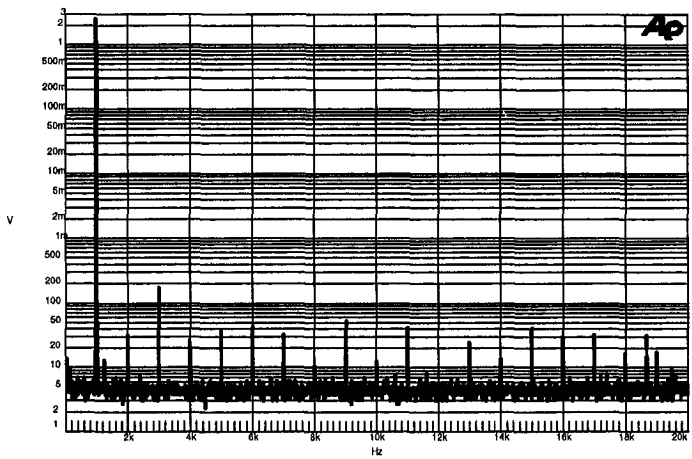

Fig. 8 16K FFT-of a 1KHz sinewave at 1W output power (44.1KHz sampling frequency). The harmonic roll-off is acceptable, with a clear dominance of the 3rd harmonic. (THD+N = 0.02% at 1W/1KHz).

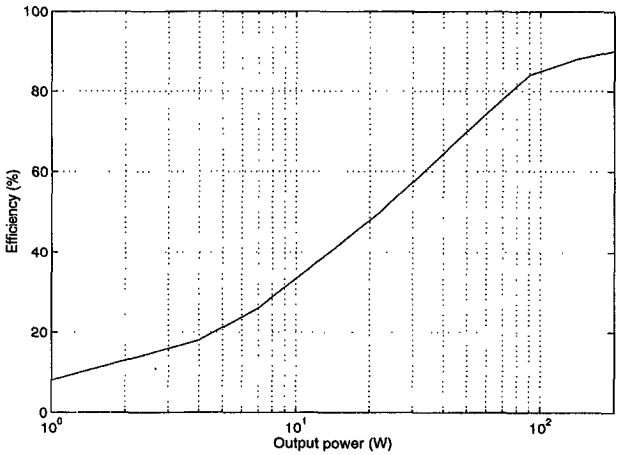

Fig. 9 Efficiency versus output power