Application Note AN4134

Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)

Abstract

This paper presents practical design guidelines for off-line forward converter employing FPS (Fairchild Power Switch). Switched mode power supply (SMPS) design is inherently a time consuming job requiring many trade-offs and iteration with a large number of design variables.

The step-by-step design procedure described in this paper helps the engineers to design a SMPS easily. In order to make the design process more efficient, a software design tool, **FPS design assistant,** that contains all the equations described in this paper, is also provided.

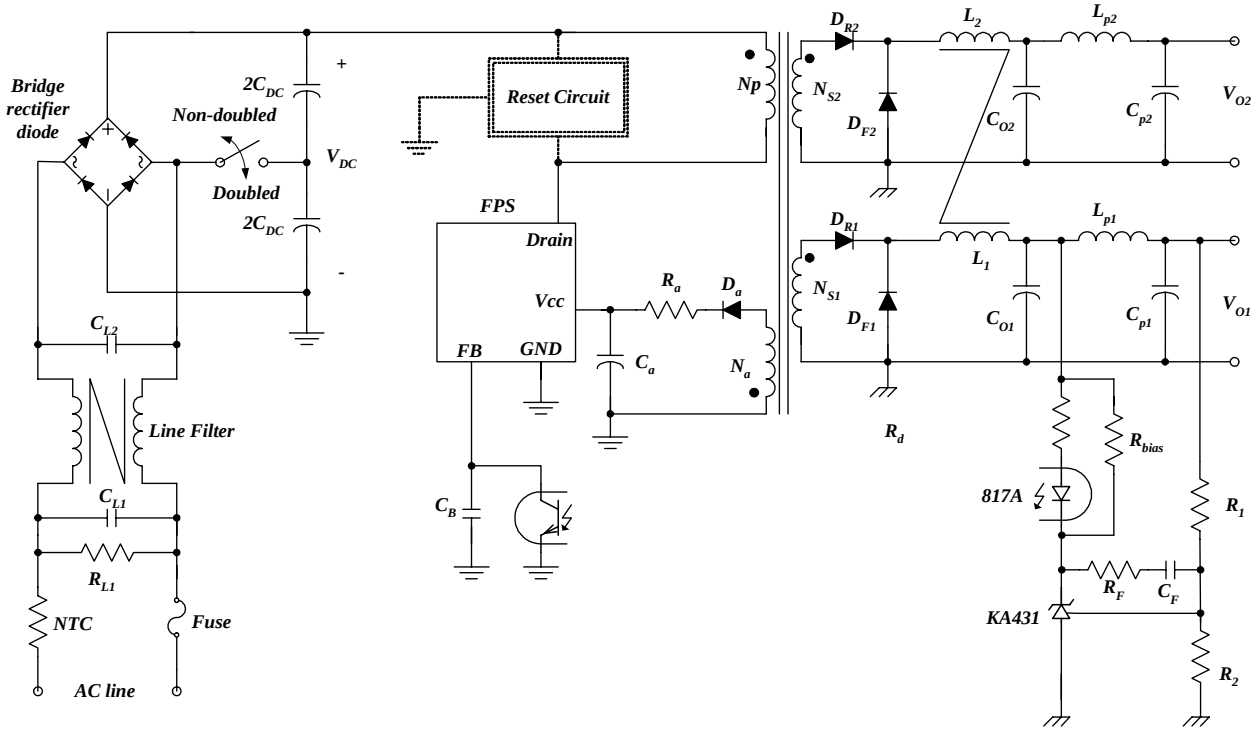


Figure 1. Basic Off-line Forward Converter Using FPS

1. Introduction

Due to circuit simplicity, the forward converter has been widely used for low to medium power conversion applications. Figure 1 shows the schematic of the basic off-line forward converter using FPS, which also serves as the reference circuit for the design procedure described in this paper. Because the MOSFET and PWM controller together with various additional circuits are integrated into a single package, the design of SMPS is much easier than the discrete MOSFET and PWM controller solution.

This paper provides step-by-step design procedure for an FPS based off-line forward converter, which includes transformer design, reset circuit design, output filter design, component selection and closing the feedback loop. The design procedure described herein is general enough to be applied to various applications. The design procedure presented in this paper is also implemented in a software design tool (FPS design assistant) to enable the engineer to finish SMPS design in a short time. In the appendix, a step-by-step design example using the software tool is provided.

2. Step-by-step Design Procedure

In this section, design procedure is presented using the schematic of the figure 1 as a reference. In general, most FPS has the same pin configuration from pin 1 to pin 4, as shown in figure 1.

(1) STEP-1 : Determine the system specifications

- Line voltage range (V_{line}^{min} and V_{line}^{max}) : Usually, voltage doubler circuit as shown in figure 1 is used for a forward converter with universal input. Then, the minimum line voltage is twice the actual minimum line voltage.

- Line frequency (f_L).

- Maximum output power (P_o).

- Estimated efficiency (E_{ff}) : It is required to estimate the power conversion efficiency to calculate the maximum input power. If no reference data is available, set E_{ff} = 0.7~0.75 for low voltage output applications and E_{ff} = 0.8~0.85 for high voltage output applications.

With the estimated efficiency, the maximum input power is given by

$$P_{in} = \frac{P_o}{E_{ff}} \qquad (1)$$

Considering the maximum input power, choose the proper FPS. Since the voltage stress on the MOSFET is about twice the input voltage in the case of the forward converter, an FPS with 800V rated MOSFET is recommended for universal input voltage. The FPS lineup with proper power rating is also included in the software design tool.

(2) STEP-2 : Determine DC link capacitor (C_{DC}) and the DC link voltage range.

The maximum DC link voltage ripple is obtained as

$$\Delta V_{DC}^{max} = \frac{P_{in} \cdot (1 - D_{ch})}{\sqrt{2} V_{line}^{min} \cdot 2f_L \cdot C_{DC}} \qquad (2)$$

where D_{ch} is the DC link capacitor charging duty ratio defined as shown in figure 2, which is typically about 0.2.

It is typical to set ΔV_{DC}^{max} as 10~15% of $\sqrt{2} V_{line}^{min}$ For voltage doubler circuit, two capacitors are used in series, each of which has capacitance twice of the capacitance that is determined by equation (2).

With the resulting maximum voltage ripple, the minimum and maximum DC link voltages are given as

$$V_{DC}^{min} = \sqrt{2} V_{line}^{min} - \Delta V_{DC}^{max} \qquad (3)$$

$$V_{DC}^{max} = \sqrt{2} V_{line}^{max} \qquad (4)$$

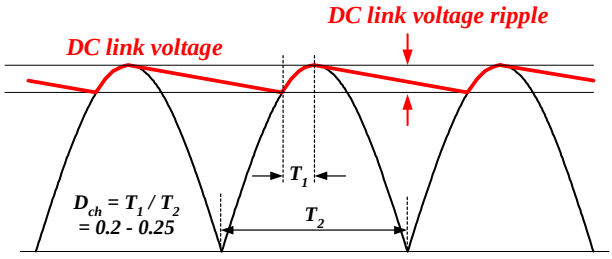


Figure 2.DC Link Voltage Waveform

(3) STEP-3 : Determine the transformer reset method and the maximum duty ratio (D_{max})

One inherent limitation of the forward converter is that the transformer must be reset during the MOSFET off period. Thus, additional reset schemes should be employed. Two most commonly used reset schemes are auxiliary winding reset and RCD reset. According to the reset schemes, the design procedure is changed a little bit.

(a) Auxiliary winding reset : Figure 3 shows the basic circuit diagram of forward converter with auxiliary winding reset. This scheme is advantageous in respect of efficiency since the energy stored in the magnetizing inductor goes back to the input. However, the extra reset winding makes the construction of the transformer more complicated.

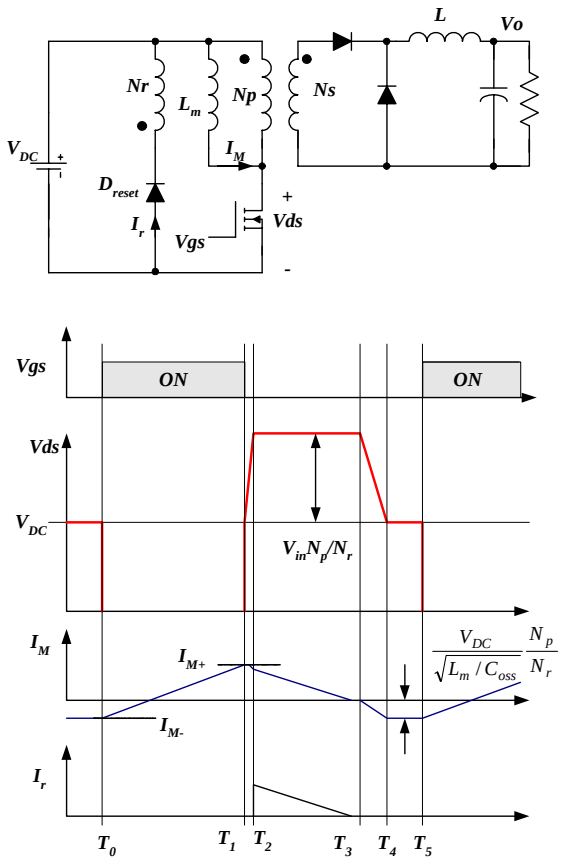


Figure 3. Auxiliary Winding Reset Forward Converter

The maximum voltage on MOSFET and the maximum duty ratio are given by

$$V_{ds}^{max} = V_{DC}^{max}\left(1+\frac{N_p}{N_r}\right) \quad (5)$$

$$D_{max} \le \frac{N_p}{N_p+N_r} \quad (6)$$

where N_p and N_r are the number of turns for the primary winding and reset winding, respectively.

As can be seen in equations (5) and (6), the maximum voltage on the MOSFET can be reduced by decreasing D_{max}. However, decreasing D_{max} results in increased voltage stress on the secondary side. Therefore, it is proper to set D_{max}=0.45 and N_p=N_r for universal input. For auxiliary winding reset, FPS, of which duty ratio is internally limited below 50%, is recommended to prevent core saturation during transient.

(b) RCD reset : Figure 4 shows the basic circuit diagram of the forward converter with RCD reset. One disadvantage of this scheme is that the energy stored in the magnetizing inductor is dissipated in the RCD snubber, unlike in the reset winding method. However, due to its simplicity, this scheme is widely used for many cost-sensitive SMPS.

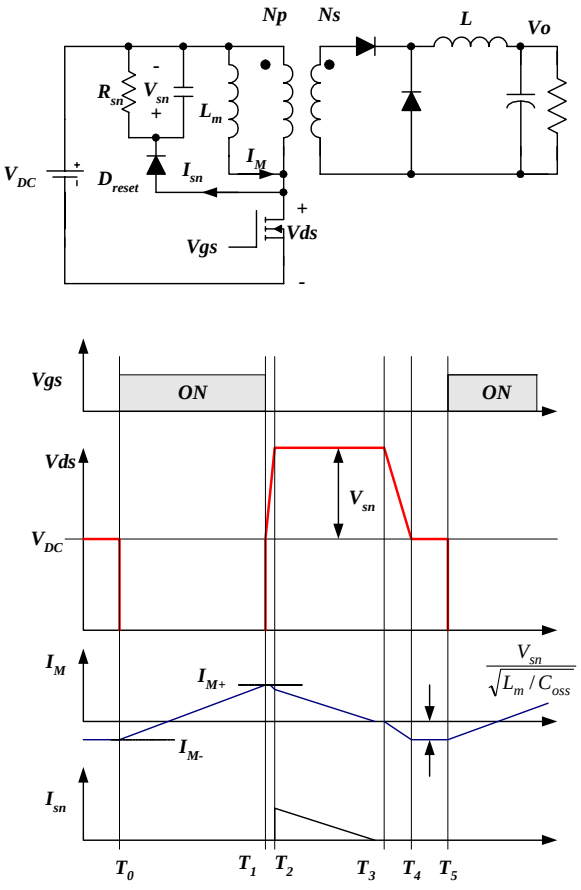


Figure 4. RCD Reset Forward Converter

The maximum voltage stress and the nominal snubber capacitor voltage are given by

$$V_{ds}^{max} = V_{DC}^{max} + V_{sn} \quad (7)$$

$$V_{sn} > \frac{V_{DC}^{min} \cdot D_{max}}{(1-D_{max})} \quad (8)$$

Since the snubber capacitor voltage is fixed and almost independent of the input voltage, the MOSFET voltage stress can be reduced compared to the reset winding approach when the converter is operated with a wide input voltage range. Another advantage of RCD reset method is that it is possible to set the maximum duty ratio larger than 50% with relatively low voltage stress on the MOSFET compared to auxiliary winding reset method, which results in reduced voltage stress on the secondary side.

(4) STEP-4 : Determine the ripple factor of the output inductor current.

Figure 5 shows the current of the output inductor. The ripple factor is defined as

$$K_{RF} = \frac{\Delta I}{2I_o} \quad (9)$$

where I_o is the maximum output current. For most practical design, it is reasonable to set K_{RF}=0.1~ 0.2.

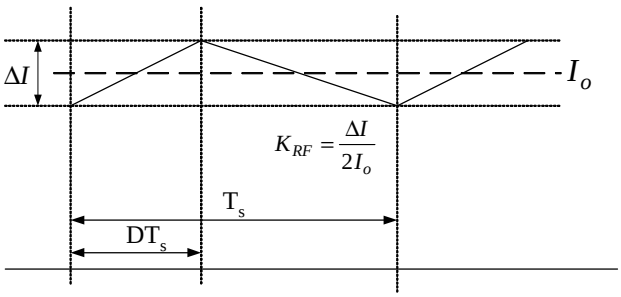


Figure 5. Output Inductor Current and Ripple Factor

Once the ripple factor is determined, the peak current and rms current of MOSFET are obtained as

$$I_{ds}^{peak} = I_{EDC}(1+K_{RF}) \quad (10)$$

$$I_{ds}^{rms} = I_{EDC}\sqrt{(3+K_{RF}^2)\frac{D_{max}}{3}} \quad (11)$$

$$where \qquad I_{EDC} = \frac{P_{in}}{V_{DC}^{min} \cdot D_{max}} \quad (12)$$

Check if the MOSFET maximum peak current (I_{ds}^{peak}) is below the pulse-by-pulse current limit level of the FPS (I_{lim}).

(5) STEP-5 : Determine the proper core and the minimum primary turns for the transformer to prevent core saturation.

Actually, the initial selection of the core is bound to be crude since there are too many variables. One way to select the proper core is to refer to the manufacture's core selection guide. If there is no proper reference, use the following equation as a starting point.

$$A_p = A_w A_e = \left[\frac{11.1 \times P_{in}}{0.141 \cdot \Delta B \cdot f_s}\right]^{1.31} \times 10^4 (mm^4) \qquad (13)$$

where A_w is the window area and A_e is the cross sectional area of the core in mm^2 as shown in figure 6. f_s is the switching frequency and ΔB is the maximum flux density swing in tesla for normal operation. ΔB is typically 0.2-0.3 T for most power ferrite cores in the case of a forward converter. Notice that the maximum flux density swing is small compared to flyback converter due to the remnant flux density.

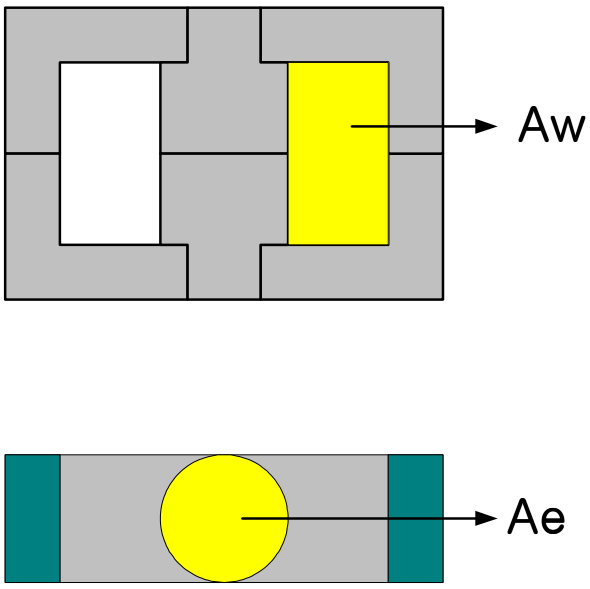


Figure 6. Window Area and Cross Sectional Area

With a determined core, the minimum number of turns for the transformer primary side to avoid saturation is given by

$$N_p^{min} = \frac{V_{DC}^{min} \cdot D_{max}}{A_e \cdot f_s \cdot \Delta B} \times 10^6 \quad (turns) \qquad (14)$$

(6) STEP-6 : Determine the number of turns for each winding of the transformer

First, determine the turns ratio between the primary side and the feedback controlled secondary side as a reference.

$$n = \frac{N_p}{N_{s1}} = \frac{V_{DC}^{min} \cdot D_{max}}{V_{o1} + V_{F1}} \qquad (15)$$

where N_p and N_{s1} are the number of turns for primary side and reference output, respectively. V_{o1} is the output voltage and V_{F1} is the diode forward voltage drop of the reference output.

Then, determine the proper integer numbers for N_{s1} so that the resulting N_p is larger than Npmin obtained from equation (14). The magnetizing inductance of the primary side is given by

$$L_m = A_L \times N_p^2 \times 10^{-9} \quad (H) \qquad (16)$$

where A_L is the AL-value with no gap in nH/turns^2.

The numer of turns for the n-th output is determined as

$$N_{S(n)} = \frac{V_{o(n)} + V_{F(n)}}{V_{o1} + V_{F1}} \cdot N_{s1} \quad (turns) \qquad (17)$$

where $V_{o(n)}$ is the output voltage and $V_{F(n)}$ is the diode forward voltage drop of the n-th output.

The next step is to determine the number of turns for Vcc winding. The number of turns for Vcc winding is determined differently according to the reset method.

(a) <u>Auxiliary winding reset</u> : For auxiliary winding reset, the number of turns of the Vcc winding is obtained as

$$N_a = \frac{V_{cc}^* + V_{Fa}}{V_{DC}^{min}} \cdot N_r \quad (turns) \qquad (18)$$

where Vcc* is the nominal voltage for Vcc and V_{Fa} is the diode forward voltage drop. Since Vcc is proportional to the input voltage when auxiliary winding reset is used, it is proper to set Vcc* as the Vcc start voltage to avoid the over voltage protection during the normal operation.

(b) <u>RCD reset</u> : For RCD reset, the number of turns of the Vcc winding is obtained as

$$N_a = \frac{V_{cc}^* + V_{Fa}}{V_{sn}} \cdot N_p \quad (turns) \qquad (19)$$

where Vcc* is the nominal voltage for Vcc. Since Vcc is almost constant for RCD reset in normal operation, it is proper to set Vcc* to be 2-3 V higher than Vcc start voltage.

(7) STEP-7 : Determine the wire diameter for each transformer winding based on the rms current.

The rms current of the n-th winding is obtained as

$$I_{sec(n)}^{rms} = I_{o(n)} \sqrt{(3 + K_{RF}^2)\frac{D_{max}}{3}} \qquad (20)$$

where $I_{o(n)}$ is the maximum current of n-th output.

When the auxiliary winding reset is employed, the rms current of the reset winding is as follows.

$$I_{Reset}^{rms} = \frac{V_{DC}^{min} D_{max}}{L_m f_s}\sqrt{\frac{D_{max}}{3}} \qquad (21)$$

The current density is typically 5A/mm^2 when the wire is long (>1m). When the wire is short with small number of turns, current density of 6-10 A/mm^2 is also acceptable. Avoid using wire with a diameter larger than 1 mm to avoid severe eddy current losses and to make winding easier. For high current output, it is better to use parallel winding with multiple strands of thinner wire to minimize skin effect.

Check if the winding window area of the core is enough to accommodate the wires. The required window area is given by

$$A_w = A_c / K_F \qquad (22)$$

where A_c is the actual conductor area and K_F is the fill factor. Typically the fill factor is 0.2-0.3 when a bobbin is used.

(8) STEP-8 : Determine the proper core and the number of turns for output inductor

When the forward converter has more than one output as shown in figure 7, coupled inductors are usually employed to improve the cross regulation, which are implemented by winding their separate coils on a single, common core.

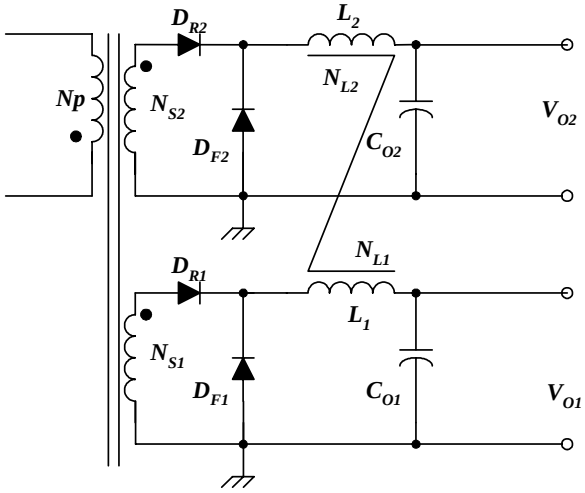


Figure 7. Coupled Output Inductors

First, determine the turns ratio of the n-th winding to the reference winding (the first winding) of the coupled inductor. The turns ratio should be the same with the transformer turns ratio of the two outputs as follows.

$$\frac{N_{S(n)}}{N_{S1}} = \frac{N_{L(n)}}{N_{L1}} \qquad (23)$$

Then, calculate the inductance of the reference output inductor as

$$L_1 = \frac{V_{o1}(V_{o1} + V_{F1})}{2 \cdot f_s \cdot K_{RF} \cdot P_o}(1 - D_{min}) \qquad (24)$$

$$\text{where} \qquad D_{min} = D_{max} \cdot \frac{V_{DC}^{min}}{V_{DC}^{max}} \qquad (25)$$

The minimum number of turns for L_1 to avoid saturation is given by

$$N_{L1}^{min} = \frac{L_1 P_O (1 + K_{RF})}{V_{O1} B_{sat} A_e} \times 10^6 \quad (turns) \qquad (26)$$

where I_{lim} is the FPS current limit level, A_e is the cross sectional area of the core in mm^2 and B_{sat} is the saturation flux density in tesla. If there is no reference data, use B_{sat} =0.35-0.4 T. Once N_{L1} is determined, $N_{L(n)}$ is determined by equation (23).

(9) STEP-9 : Determine the wire diameter for each inductor winding based on the rms current.

The rms current of the n-th inductor winding is obtained as

$$I_{L(n)}^{rms} = I_{o(n)}\sqrt{\frac{(3 + K_{RF}^2)}{3}} \qquad (27)$$

The current density is typically 5A/mm^2 when the wire is long (>1m). When the wire is short with small number of turns, a current density of 6-10 A/mm^2 is also acceptable. Avoid using wire with diameter larger than 1 mm to avoid severe eddy current losses and to make winding easier. For high current output, it is better to use parallel winding with multiple strands of thinner wire to minimize skin effect.

(10) STEP-10 : Determine the diode in the secondary side based on the voltage and current ratings.

The maximum voltage and the rms current of the rectifier diode of the n-th output are obtained as

$$V_{D(n)} = V_{DC}^{max} \frac{N_{S(n)}}{N_P} \qquad (28)$$

$$I_{D(n)}^{rms} = I_{o(n)}\sqrt{(3 + K_{RF}^2)\frac{D_{max}}{3}} \qquad (29)$$

(11) STEP-11 : Determine the output capacitor considering the voltage and current ripple.

The ripple current of the n-th output capacitor is obtained as

$$I_{C(n)}^{rms} = \frac{K_{RF} I_{o(n)}}{\sqrt{3}} \quad (30)$$

The ripple current should be equal to or smaller than the ripple current specification of the capacitor.

The voltage ripple on the n-th output is given by

$$\Delta V_{o(n)} = \frac{I_{o(n)} \cdot K_{RF}}{4 C_{o(n)} f_s} + 2 K_{RF} I_{o(n)} R_{c(n)} \quad (31)$$

where $C_{o(n)}$ is the capacitance and $R_{c(n)}$ is the effective series resistance (ESR) of the n-th output capacitor.

Sometimes it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of the electrolytic capacitor. Then, additional LC filter (post filter) can be used. When using additional LC filter, be careful not to place the corner frequency too low. If the corner frequency is too low, it may make the system unstable or limit the control bandwidth. It is proper to set the corner frequency of the filter to be around 1/10 to 1/5 of the switching frequency.

(12) STEP-12 : Design the Reset circuit.

(a) <u>Auxiliary winding reset</u> : For auxiliary winding reset, the maximum voltage and rms current of the reset diode are given by

$$V_{Dreset} = V_{DC}^{max}\left(1 + \frac{N_r}{N_p}\right) \quad (32)$$

$$I_{Dreset}^{rms} = \frac{V_{DC}^{min} D_{max}}{L_m f_s}\sqrt{\frac{D_{max}}{3}} \quad (33)$$

(b) <u>RCD reset</u> : For RCD reset, the maximum voltage and rms current of the reset diode are given by

$$V_{DR} = V_{DC}^{max} + V_{sn} \quad (34)$$

$$I_{DR}^{rms} = \frac{V_{DC}^{min} D_{max}}{L_m f_s}\sqrt{\frac{D_{max}}{3}} \quad (35)$$

The power loss of the snubber network in normal operation is obtained as

$$Loss_{sn} = \frac{V_{sn}^2}{R_{sn}} = \frac{1}{2}\left[\frac{(nV_{o1})^2}{L_m f_s} - \frac{2nV_{o1}V_{sn}}{\sqrt{L_m / C_{oss}}}\right] \quad (36)$$

where V_{sn} is the snubber capacitor voltage in normal operation, R_{sn} is the snubber resistor, n is N_p/N_{s1} and C_{oss} is the ouput capacitance of the MOSFET. Based on the power loss, the snubber resistor with proper rated wattage should be chosen.

The ripple of the snubber capacitor voltage in normal operation is obtained as

$$\Delta V_{sn} = \frac{V_{sn} D_{max}}{C_{sn} R_{sn} f_s} \quad (37)$$

In general, 5-10% ripple is practically reasonable.

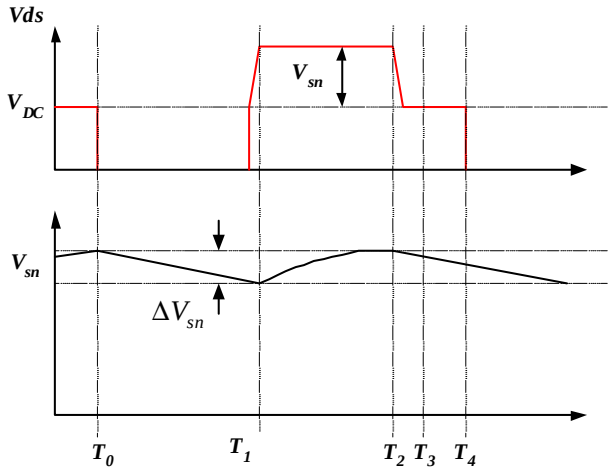


Figure 8. Snubber Capacitor Voltage

(13) STEP-13 : Design the feed back loop.

Since FPS employs current mode control as shown in figure 9, the feedback loop can be simply implemented with a one pole and one zero compensation circuit.

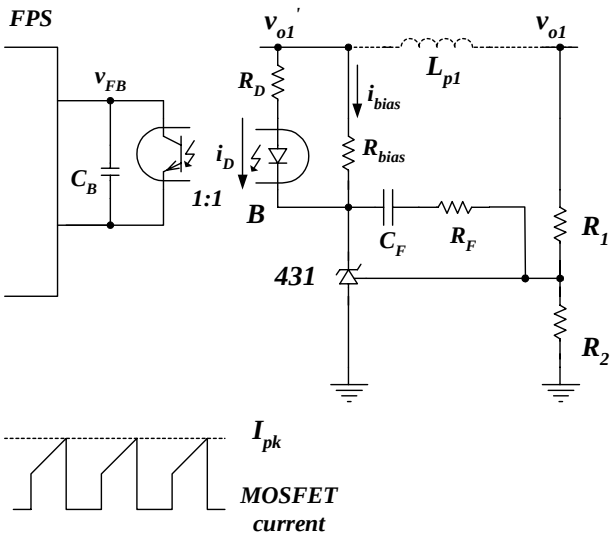


Figure 9. Control Block Diagram

For continuous conduction mode (CCM) operation, the control-to-output transfer function of forward converter using FPS is given by

$$G_{vc} = \frac{\hat{v}_{o1}}{\hat{v}_{FB}} = K \cdot R_L \cdot \frac{N_p}{N_{s1}} \cdot \frac{1 + s/w_z}{1 + s/w_p} \qquad (38)$$

$$\text{where} \quad w_z = \frac{1}{R_{c1}C_{o1}}, \qquad w_p = \frac{1}{R_L C_{o1}}$$

and R_L is the effective total load resistance of the controlled output defined as V_{o1}^2/P_o.When the converter has more than one output, the DC and low frequency control-to-output transfer function are proportional to the parallel combination of all load resistance, adjusted by the square of the turns ratio. Therefore, the effective total load resistance is used in equation (38) instead of the actual load resistance of V_{o1}.

The voltage-to-current conversion ratio of FPS, K is defined as

$$K = \frac{I_{pk}}{V_{FB}} = \frac{I_{lim}}{3} \qquad (39)$$

where I_{pk} is the peak drain current and V_{FB} is the feedback voltage for a given operating condition.
Figure 10 shows the variation of control-to-output transfer function for a CCM forward converter according to the load. Since a CCM forward converter has inherent good line regulation, the transfer function is independent of input voltage variation. While the system pole together with the DC gain changes according to the load condition.

The feedback compensation network transfer function of figure 9 is obtained as

$$\frac{\hat{v}_{FB}}{\hat{v}_{o1}} = -\frac{w_i}{s} \cdot \frac{1 + s/w_{zc}}{1 + 1/w_{pc}} \qquad (40)$$

$$\text{where } w_i = \frac{R_B}{R_1 R_D C_F s}, w_{zc} = \frac{1}{(R_F + R_1)C_F}, w_{pc} = \frac{1}{R_B C_B}$$

As can be seen in figure 10, the worst case in designing the feedback loop for a CCM forward converter is the full load condition. Therefore, by designing the feedback loop with proper phase and gain margin in low line and full load condition, the stability all over the operation ranges can be guaranteed.

The procedure to design the feedback loop is as follows:

(a) Determine the crossover frequency (f_c). When an additional LC filter (post filter) is employed, the crossover frequency should be placed below 1/3 of the corner frequency of the post filter, since it introduces -180 degrees phase drop. Never place the crossover frequency beyond the corner frequency of the post filter. If the crossover frequency is too close to the corner frequency, the controller should be designed to have enough phase margin more than about 90 degrees when ignoring the effect of the post filter.

(b) Determine the DC gain of the compensator (w_i/w_{zc}) to cancel the control-to-output gain at f_c.

(c) Place compensator zero (f_{zc}) around $f_c/3$.
(d) Place compensator pole (f_{pc}) above $3f_c$.

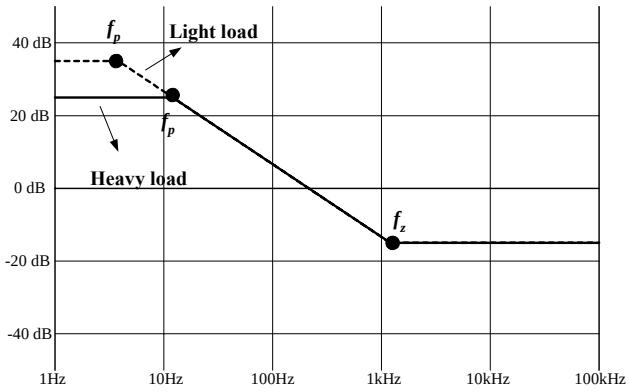


Figure 10. CCM Forward Converter Control-to-output Transfer Function variation According to the Load

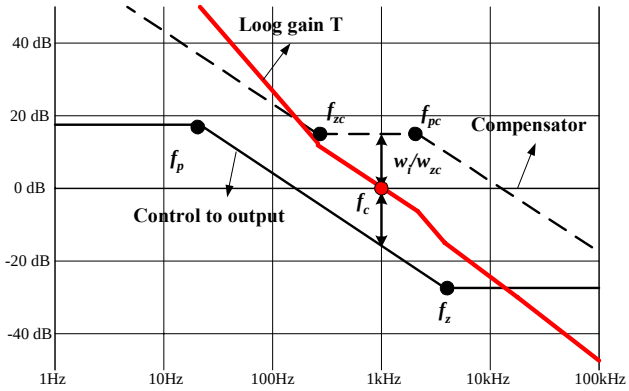


Figure 11. Compensator Design

When determining the feedback circuit component, there are some restrictions as follows.

(a) The capacitor connected to feedback pin (C_B) is related to the shutdown delay time in an overload situation as

$$T_{delay} = (V_{SD} - 3) \cdot C_B / I_{delay} \qquad (41)$$

where V_{SD} is the shutdown feedback voltage and I_{delay} is the shutdown delay current. These values are given in the data sheet. In general, 10~100 ms delay time is proper for most practical applications. In some cases, the bandwidth may be limited due to the required delay time in over load protection.

(b) The resistor R_{bias} and R_D used together with opto-coupler and the KA431 should be designed to provide proper operating current for the KA431 and to guarantee the full swing of the feedback voltage of the FPS. In general, the minimum cathode voltage and current for KA431 is 2.5V and 1mA, respectively. Therefore, R_{bias} and R_D should be designed to satisfy the following conditions.

$$\frac{V_o - V_{OP} - 2.5}{R_D} > I_{FB} \quad (42)$$

$$\frac{V_{OP}}{R_{bias}} > 1mA \quad (43)$$

where V_{OP} is opto-diode forward voltage drop, which is typically 1V and I_{FB} is the feedback current of FPS, which is typically 1mA. For example, R_{bias}<1kΩ and R_D <1.5kΩ for V_{o1}=5V.

- Summary of symbols -

A_w : Window area of the core in mm^2
Ae : Cross sectional area of the core in mm^2
B_{sat} : Saturation flux density in tesla.
ΔB : Maximum flux density swing in tesla in normal operation
C_o : Capacitance of the output capacitor.
D_{max} : Maximum duty cycle ratio
E_{ff} : Estimated efficiency
f_L : Line frequency
f_s : Switching frequency
I_{ds}^{peak} : Maximum peak current of MOSFET
I_{ds}^{rms} : RMS current of MOSFET
I_{lim} : FPS current limit level.
$I_{sec(n)}^{rms}$: RMS current of the n-th secondary winding
$I_{D(n)}^{rms}$: Maximum rms current of the rectifier diode for the n-th output
$I_{c(n)}^{rms}$: RMS Ripple current of the n-th output capacitor
I_O : Output load current
$K_{L(n)}$: Load occupying factor for n-th output
K_{RF} : Current ripple factor
L_m : Transformer primary side inductance
$Loss_{sn}$: Power loss of the snubber network in normal operation
N_p^{min} : The minimum number of turns for the transformer primary side to avoid saturation
N_p : Number of turns for primary side
N_r : Number of turns for reset winding
N_{s1} : Number of turns for the reference output
P_o : Maximum output power
P_{in} : Maximum input power
R_c : Effective series resistance (ESR) of the output capacitor.
R_{sn} : Snubber resistor
R_L : Output load resistor
V_{line}^{min} : Minimum line voltage
V_{line}^{max} : Maximum line voltage
V_{DC}^{min} : Minimum DC link voltage
V_{DC}^{max} : Maximum DC line voltage
V_{ds}^{nom} : Maximum nominal MOSFET voltage
V_{o1} : Output voltage of the reference output.
V_{F1}* : Diode forward voltage drop of the reference output.
V_{cc}* : Nominal voltage for Vcc
V_{Fa} : Diode forward voltage drop of Vcc winding
ΔV_{DC}^{max} : Maximum DC link voltage ripple
$V_{D(n)}$: Maximum voltage of the rectifier diode for the n-th output
$\Delta V_{o(n)}$: Output voltage ripple of the n-th output
V_{sn} : Snubber capacitor voltage in normal operation
ΔV_{sn} : Snubber capacitor voltage ripple
V_{sn}^{max} : Maximum snubber capacitor voltage during transient or over load situation
V_{ds}^{max} : Maximum voltage stress of MOSFET

Appendix. Design Example using FPS design Assistant

Target System : PC Power Supply

- Input : universal input (90V-265Vrms) with voltage doubler
- Output : 5V/15A, 3.3V/10A, 12V/6A

FAIRCHILD SEMICONDUCTOR™

FPS Design Assistant ver.1.0 By Choi
For forward converter with reset winding

Blue cell is the input parameters
Red cell is the output parameters

1. Define specifications of the SMPS

Minimum Line voltage (V_line.min)	180	V.rms
Maximum Line voltage (V_line.max)	265	V.rms
Line frequency (fL)	60	Hz

	Vo		Io		Po		KL	
1st output for feedback	5	V	15	A	75	W	42	%
2nd output	3.3	V	10	A	33	W	18	%
3rd output	12	V	6	A	72	W	40	%
4th output	0	V	0	A	0	W	0	%
Maximum output power (Po) =	180.0	W						
Estimated efficiency (Eff)	70	%						
Maximum input power (Pin) =	257.1	W						

2. Determine DC link capacitor and the DC voltage range

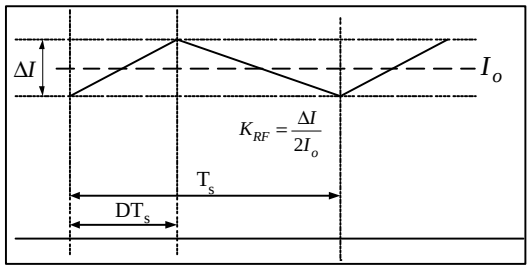
DC link capacitor	235	uF
DC link voltage ripple =	29	V
Minimum DC link voltage =	226	V
Maximum DC link voltage =	375	V

3. Determine the maximum duty ratio (Dmax)

Maximum duty ratio	0.4		
Turns ratio (Np/Nr)	1	>	0.67
Maximum nominal MOSFET voltage =	750	V	

4. Determine the ripple factor of the output inductor current

Output Inductor current ripple factor	0.15	
Maximum peak drain current =	3.27	A
RMS drain current =	1.81	A
Current limit of FPS	4	A



5. Determine proper core and minimum primary turns for transformer

Switching frequency of FPS (kHz)	67	kHz	
Maximum flux density swing	0.32	T	--> EER2834
Estimated AP value of core =	9275	mm^4	AP=12470
Cross sectional area of core (Ae)	86	mm^2	Ae=86
Minimum primary turns =	49.0	T	Aw=145

6. Determine the numner of turns for each outputs

	Vo		VF			# of turns	
Vcc (Use Vcc start voltage)	15	V	1.2	V	3.6 =>	4	T
1st output for feedback	5	V	0.4	V	3 =>	3	T
2nd output	3.3	V	0.4	V	2.06 =>	2	T
3rd output	12	V	0.5	V	6.94 =>	7	T
4th output	0	V	0	V	0 =>	0	T
VF : Forward voltage drop of rectifier diode					Reset winding =	50	T
					Primary turns =	50	T
					->enough turns		
AL value (no gap)	2490	nH/T^2					
Transformer magnetizing inductance =	6.27499	mH			--> EER2834		

7. Determine the wire diameter for each transformer winding

	Diameter		Parallel		Irms		(A/mm^2)
Primary winding (Np)	0.68	mm	1	T	1.81	A	4.98
Reset winding (Nr)	0.31	mm	1	T	0.08	A	1.04
Vcc winding	0.31	mm	1	T	0.10	A	1.33
1st output winding	0.68	mm	4	T	9.5	A	6.56
2nd output winding	0.68	mm	3	T	6.3	A	5.83
3rd output winding	0.68	mm	2	T	3.8	A	5.25
4th output winding	0	mm	0	T	0.0	A	#DIV/0!
Copper area =	33.9262	mm^2					
Fill factor	0.25						
Required window area	135.705	mm^2	--> EER2834 (Aw=145)				

8. Determine proper core and number of turns for inductor (coupled inductor)

Cross sectional area of Inductor core (A	86	mm^2	--> EER2834	
Saturation flux density	0.42	T		
Inductance of 1st output (L1) =	5.7	uH		
Minimum turns of L1 =	6.5	T		
Actual number of turns for L1	6	=>	6	T
Number of turns for L2 =	4	=>	4	T
Number of turns for L3 =	14	=>	14	T
Number of turns for L4 =	0	=>	0	T

9. Determine the wire diameter for each inductor winding

	Diameter		Parallel		Irms		(A/mm^2)
Winding for L1	0.68	mm	5	T	15.1	A	8.30
Winding for L2	0.68	mm	3	T	10.0	A	9.22
Winding for L3	0.68	mm	2	T	6.0	A	8.30
Winding for L4	0	mm	0	T	0.0	A	#DIV/0!
Copper area =	25.4089	mm^2					
Fill factor	0.25						
Required window area	101.636	mm^2	--> EER2834(Aw=145)				

10. Determine the rectifier diodes in the secondary side

	Reverse voltage		Rms Current		
Vcc diode	55	V	0.10	A	-->UF4003
1st output diode	22	V	9.5	A	-->MBR3060PT
2nd output diode	15	V	6.3	A	-->MBR3045PT
3rd output diode	52	V	3.81	A	-->MBR20H100CT
4th output diode	0	V	0.00	A	

11. Determine the output capacitor

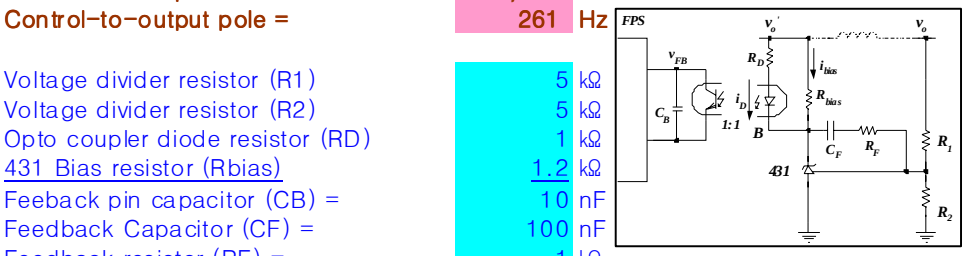
	Capacitance		ESR		Current ripple		Voltage Ripple	
1st output capacitor	4400	uF	20	mΩ	1.3	V	0.09	V
2nd output capacitor	4400	uF	20	mΩ	0.9	V	0.06	V
3rd output capacitor	2000	uF	60	mΩ	0.5	V	0.11	V
4th output capacitor	0	uF	0	mΩ	0.0	V	####	V

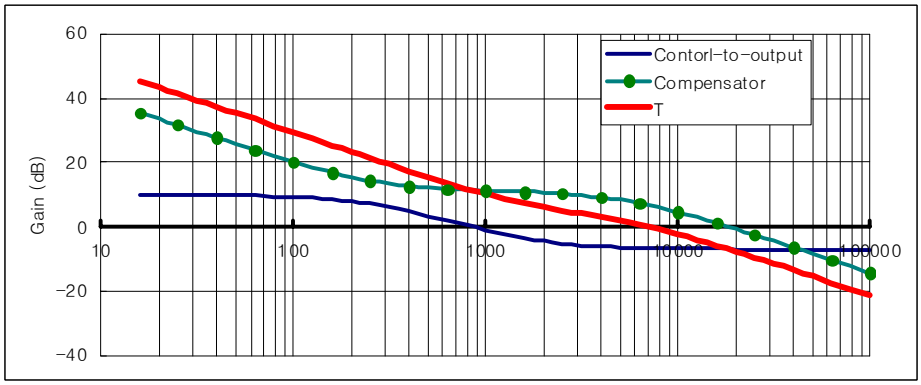
12. Design the Reset Circuit

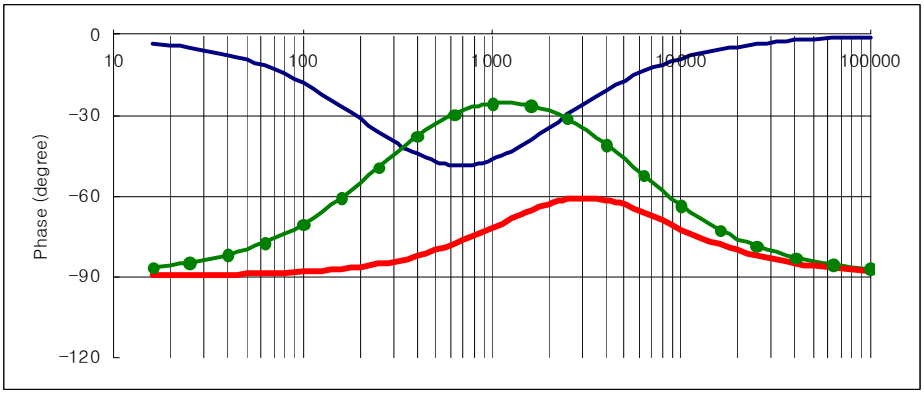
Reset diode rms current	0.08	A	
Maximum voltage of reset diode	750	V	-->UF4007

13. Design Feedback control loop

Control-to-output DC gain =	3	
Control-to-output zero =	1,809	Hz
Control-to-output pole =	261	Hz
Voltage divider resistor (R1)	5	kΩ
Voltage divider resistor (R2)	5	kΩ
Opto coupler diode resistor (RD)	1	kΩ
431 Bias resistor (Rbias)	1.2	kΩ
Feeback pin capacitor (CB) =	10	nF
Feedback Capacitor (CF) =	100	nF
Feedback resistor (RF) =	1	kΩ
Feedback integrator gain (fi) =	955	Hz
Feedback zero (fz) =	265.393	Hz
Feedback pole (fp) =	5307.86	Hz







Design Summary

- For the FPS, FS7M0880 is chosen. This device has a fixed switching frequency of 67kHz.
- To limit the current, a 10 ohm resistor (Ra) is used in series with the Vcc diode.
- The control bandwidth is 6kHz. Since the crossover frequency is too close the corner frequency of the post filter (additional LC filter), the controller is designed to have enough phase margin of 120 degrees when ignoring the effect of the post filter.

Figure 12 shows the final schematic of the forward converter designed by *FPS Design Assistant*

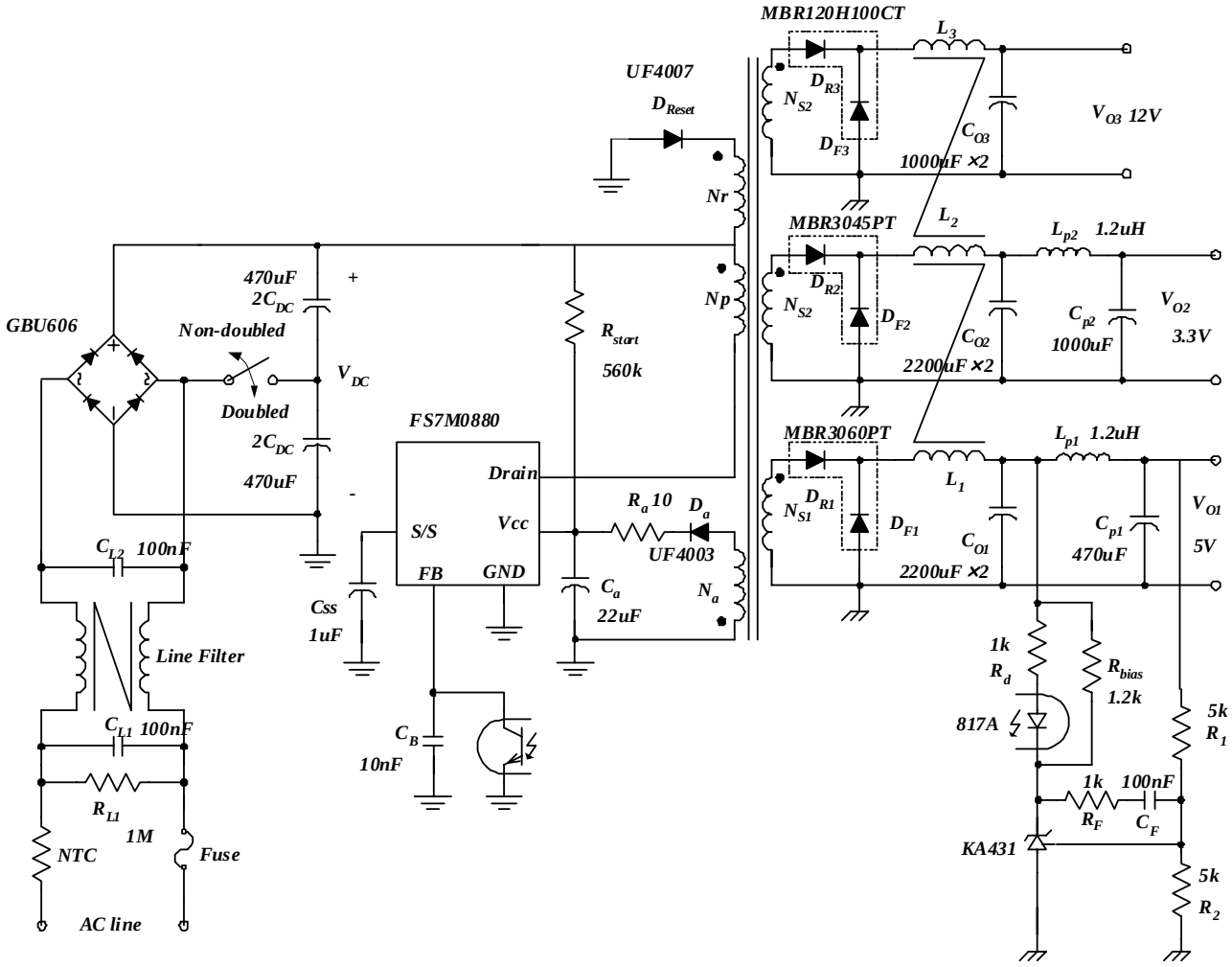


Figure 12. The final schematic of the forward converter

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