Technology of Q 2500 colour TV set

LOEWE.

Loewe Opta GmbH
Postfach 1554
96305 Kronach
Industriestraße 11
96317 Kronach
Tel: (09261) 99-0
Fax (09261) 9 54 11
e-mail: loewe@loewe.de
http://www.loewe.de

231-90415.917

1 Introduction

The Q 2500 chassis is a further development of the tried and tested 100 Hz Q 2400 chassis. The modular design, dimensions and layout have been retained.

In order to improve picture performance even further, several circuit components have either been modified or newly added. For sound signals, IF processing in the main receiver unit is now entirely digital.

The Q 2500 chassis is available in three different versions, Q 2500/H (High End), Q 2500/M (Medium) and Q 2500/B (Basic). The signal board is different for all three versions. It has different equipment in certain areas owing to the different power spectrum of the three versions. All H/M and B signal board versions are electrically interchangeable. Due to the incorporation of 2 or 3 AV sockets (the back of the TV set does not fit) they are not mechanically compatible. Except for the signal board there is no differentiation with respect to all other components for the different versions – High End, Medium and Basic. The Q 2500 chassis therefore supersedes the Q 2400 and Q 4140 chassis completely.

Because of this concept it is now possible to fit a DVB upgrade kit to all 100 Hz TV sets – from the Contur to the Aconda. So far this has only been possible for sets with the Q 2400 chassis and not for sets with the Q 4140 chassis.

The following features have been retained from the previous chassis:

- 8 bit digital signal processing
- ACP (Automatic Channel Programming) for fully automatic programming of stations and sorting of cable and SAT reception, including an update function.
- child protection security-plus with secret code.
- - Sharpness control, photo CD circuit and comb filter (S-PAL).
- SCS (Sharpness Control System) for a picture-dependent velocity modulation of the horizontal (line) sweep.
- DTI Plus (Digital Transient Improvement) for colour edge sharpening.
- 576-line still picture
- Adjustable noise suppression DNC (Digital Noise Control)
- Suppression of interline flicker DLC (Digital Lineflicker Control).
- Digital Line Interpolation (DLI) for full frame picture display for PALplus and also in all zoom modes.
- Digital Motion Interpolation (DMI) ensures continuous movement over all single frame pictures.
- Automatic Movie Detection (AMD) for switching to wide screen format in PAL standard on 16:9 units.
- Automatic PALplus recognition and format switching for 16:9 units.
- Digital Scene Control (DSC) for improved grey scales.
- Various switching modes (4:3, Cinema, Zoom, 16:9 and Panorama Mode for 16:9 units).
- Automatic Volume Control (AVC) for adjusting the volume between different channels and during commercial breaks
- On the front: Headphone output and input with S terminals and three cinch sockets.

- Copy function for re-recording between different inputs and outputs (also in standby mode), and during TV programmes.

- Internal clock synchronized with Teletext.

- EPG function (electronic programme guide).

- Recording timer for video recorder and SAT standby function.

- Operation of Loewe video recorders via the menu.

- Switch-off automation and timer.

- In 81 cm sets a rotary panel is used in order to compensate for the earth's magnetic field. This prevents distortion of the picture no matter where the set is placed.

- Personal Control System (PCS): operation tailored to individual customer requirements. The most frequently used functions may be assigned to four buttons of the remote control. Additionally, the operating manual may be viewed on the screen – On Screen Display (OSD). This includes help instructions on functions currently used, information on the remote control functions and an index, which enables immediate implementation of functions. It is also possible to set limitations to the scope of operation according to customer requirements. The user may, for example, be prevented from making changes to particular settings.

- Automatic Gain Control (AGC) for all video signals shown in the main picture.

- The RGB signals are no longer converted to analogue Y/C signals but are directly digitised instead.

- An Audio-In socket to which, for example, an external digital radio receiver may be connected.

- Some models, e.g. Aconda, may be upgraded

- A Dolby Digital Module can be installed in model versions H and M.

- The EAROM and the DVB software may be directly written to via an external V 24 service interface using a PC and service adapter.

The following features are completely new:

- Depending on version, either two or three AV sockets.

- Depending on version, a Teletext memory with 3000 pages (with active EPG function 2000 pages).

- An own radio menu, accessible over the "speaker symbol" on the remote control.

- Improved Digital Movie Mode (DMM). Feature films are recognized safely. Therefore, accidental switching to camera mode is prevented. Switching effects do not occur anymore.

The following circuit descriptions have been subdivided according to the individual modules. Deviation from this scheme occurs occasionally in order to emphasize relations between circuits more effectively. All component positions in the circuit diagrams are identified by four figures. For the signal board the fully equipped version H is explained. For versions M and B only the differences are noted.

The upgrade kits are explained in a separate circuit description.

1.1 Foundations of 100 Hz technology

1.1.1 Prerequisites for 100 Hz

In order to double the picture frequency at the receiver, the signals have to be read into the relevant memory blocks and then read out twice at double rate.

The following prerequisites must be met:

- The signals need to be digitised.
- The memory modules require at least 3 Mbits storage capacity.
- The software must be able to run a controller, which in turn monitors the read-in and read-out functioning of the memory.
- Suitable frequency-stabilized oscillators for generating the clock frequency must be provided.
- The drive signals for the output stages, line and field deflection, and the E/W correction must also be at double frequency.
- The power output stages for deflection, as well as the deflector itself, need to be designed for the higher frequency and the resulting higher currents.
- The RGB output stages need to be able to process the doubled bandwidth.

1.1.2 100 Hz display modes

When examining display modes the deflection raster and the video raster need to be considered together. In 50 hz operation, the two single-frame pictures A and B are written to the scanning system ‘a’ and ‘b’, i.e. every second line of frame A and the intermediate lines of B. This is achieved in that the flyback of ‘a’ begins in the middle of a line. Trace ‘b’ starts also in the middle of a line but is written to the end of a complete line. The next trace ‘a’ starts again at the beginning of a line. The trace time, however, is always the same.

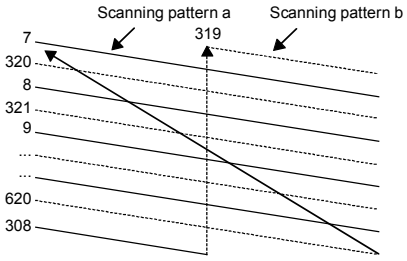
1.1.3 Mode AABB

The simplest case of 100 hz operation involves a simple doubling of single-frame picture display, i.e. field A is displayed twice consecutively followed by field B (AABB).

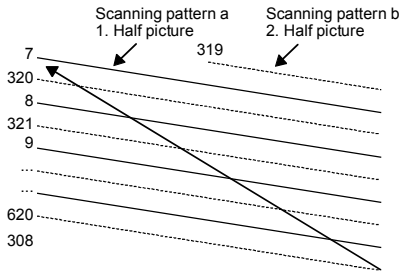
To achieve this the deflection raster must be modified so that ‚a’ is written twice followed by ‘b’ (aabb). Theoretically, this can be accomplished in two ways. Firstly, by adjusting the flyback’s starting time for the 4 single frames. A half-line more is written for ‘a1’ and a half-line less in for the third field. In practice, such a scheme would be quite difficult to implement. In comparison, the second possibility is easier to achieve. This involves shifting the 2nd and 3rd fields (a2 and b1). This can be accomplished by adjusting the current though the deflector by modifying the base resistance. This produces the same time interval for all traces over all fields

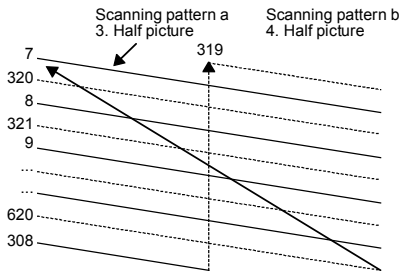
Deflection 100Hz

1. 50Hz

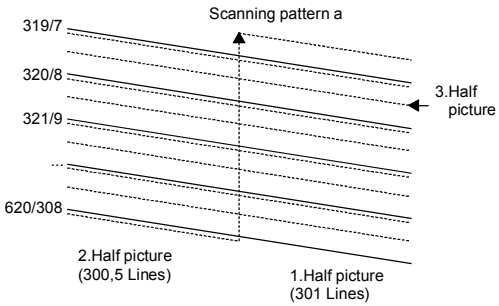


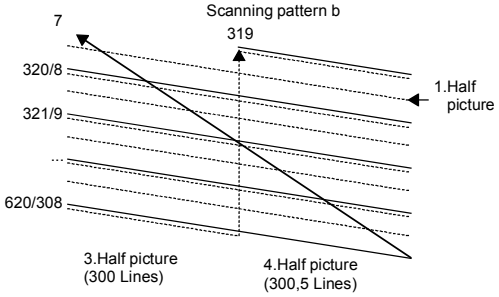
2.100Hz
Scanning pattern a-b-a-b



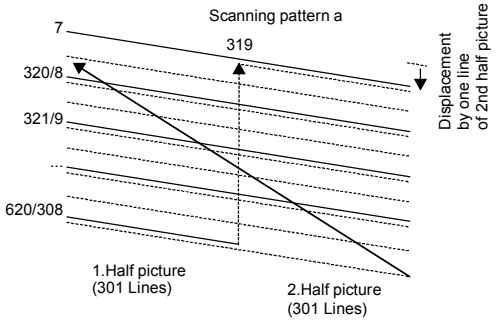


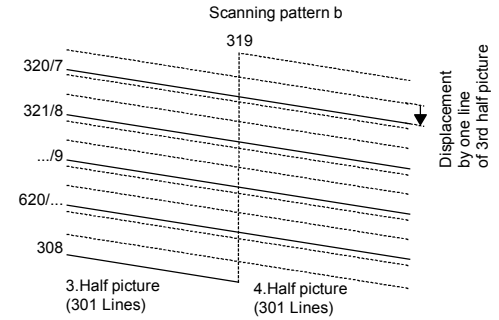
3a 100Hz
Scanning pattern a-a-b-b





3b 100Hz
Scanning pattern a-a-b-b





For AA and BB display, delay lines must ensure that the lines of the 1st and 2nd, and 3rd and 4th fields contain the same picture information when superimposed on one another. This mode of display allows for very effective reduction of large-area flicker. A reduction of interline flicker is, however, not possible, because intermediate lines are only traced after 20ms.

1.1.4 Mode ABAB

This mode, together with the two described below, are only possible in conjunction with a second single-frame picture memory because of the alternating display of A and B. The deflection must also operate in 'abab' raster form. In this display mode, the signals are not modified during deflection or image processing operations. In this case, both interline flicker and large area-flicker can be reduced. However, jerking effects in moving images can arise. This form of display is only suitable for signals where an image is formed from two fields between which there is no relative movement. This mode is therefore of interest only for "Photo CD" or cinema scope films in PALplus.

Reduction of interline flicker without movement interpolation (DLC)

Memory 1	Memory 1 retarded	Memory 2	Output	Deflection Scanning pattern
A	A v	B	A	a
A	A v	A	A'	b
B	B v	A	B'	a
B	B v	B	B	b
A	A v	B	A	a

1.1.5 Mode AA'B'B

In this display mode two single-frame pictures, A' and B', are calculated. By using an interpolation filter the current single-frame, the current single-frame delayed by one line and the signal delayed by one single-frame are compared with one another. If deviations are detected in one of the signals, this signal is eliminated and the values that agree in the other two signals are retained. If all three signals vary, an average is formed.

Interpolation example

Memory 1	10	10	10	x x x
Memory 1 retarded	10	10	9	x x x
Memory 2	10	8	8	x x x
Output	10	10	9	x x x

The deflection proceeds as sweep 'abab'. The calculated A' and B' are written to shifted scanning system of the 2nd and 3rd single frames. A and B are written to the non-shifted system of frames 1 and 4.

This mode is suitable for the display of horizontal motion between frames. Only small jerking effects arise between movements.

The mode is used to suppress interline flicker in normal TV operation.

1.1.6 Mode AA*BB*

In this display mode with respect to the calculated frames A* and B*, the movement between the original frames A and B, and between B and the next A are taken into account. This movement interpolation (DMI – Digital Motion Interpolation) takes into account both horizontal and vertical movements which cover several lines. This means that when suppressing interline flicker, continuous movement over all frames is achieved.
For full frame pictures (films) it is also assured that no movement between two single-frame pictures takes place (DMM – Digital Movie Mode).

In this display mode the deflection is also 'abab'.

Movement interpolation

Pcture 1

Picture 2

Picture 3

Picture 1

Picture 1*

Picture 2

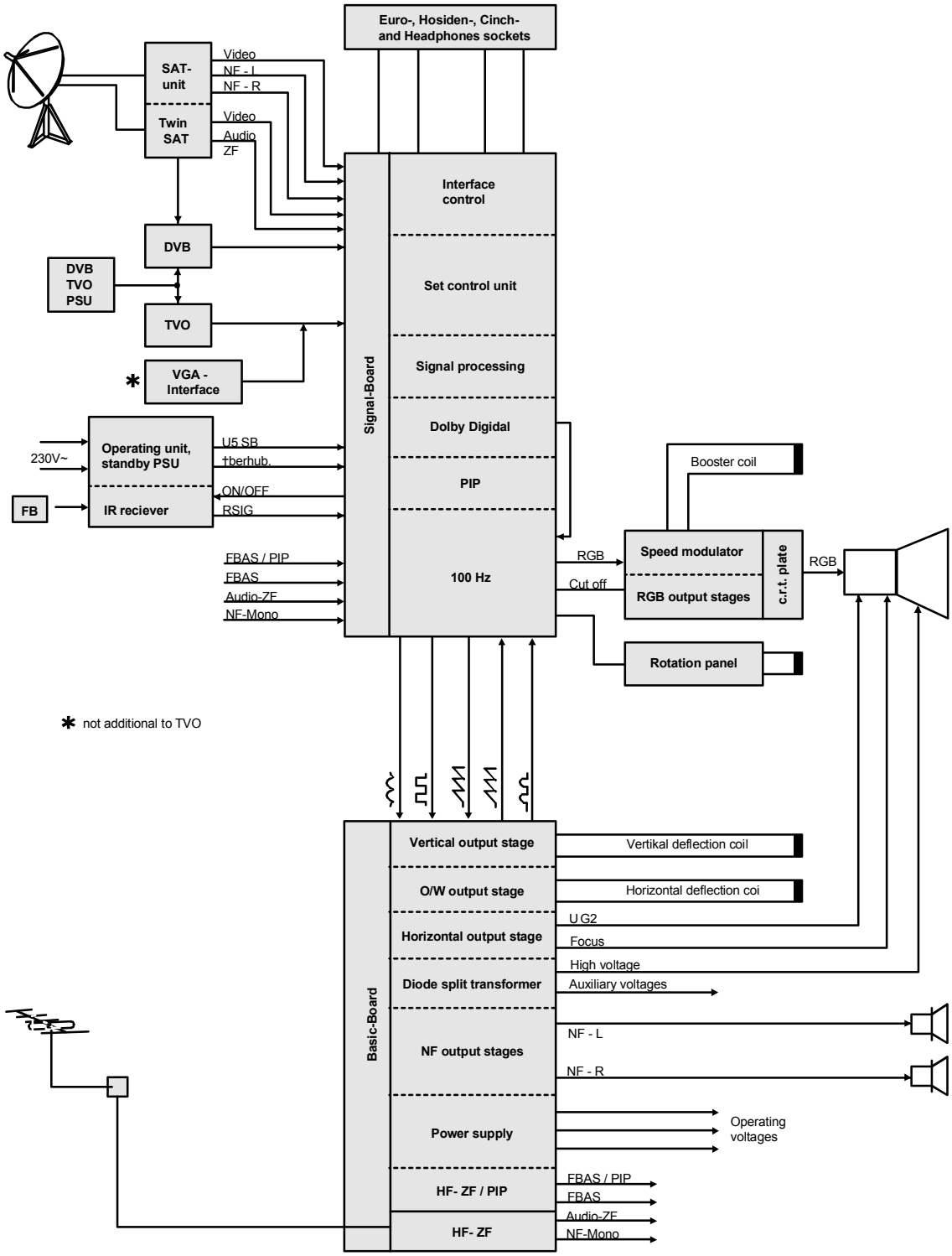
Picture 2*

Picture 3

Picture 3*

Display mode 100Hz

No.	Picture change frequency	Video scanning pattern	Deflection scanning pattern	Mode	Advantages
1.	50Hz	A-B	a-b		
2.	100Hz	A-A-B-B	a-a-b-b	DLC off	-Reduction of large area shimmer
3.	100Hz	A-B-A-B	a-b-a-b	-Photo CD on -PAL plus Cinema Scope	-Reduction of large area shimmer -Reduction of interline shimmer in full picture setup
4.	100Hz	A-A´-B´-B	abab	DLC on	-Reduction of large area shimmer -Reduction of interline shimmer in full picture setup with movement
5.	100Hz	A-A*-B*-B	abab	DMI	-Reduction of large area shimmer -Reduction of interline shimmer in full picture setup with movement -Movement interpolation


Euro-, Hosiden-, Cinch- and Headphones sockets
SAT-unit
Twin SAT
Video
NF - L
NF - R
Video
Audio
ZF
DVB
DVB TVO PSU
TVO
VGA - Interface
Operating unit, standby PSU
230V~
FB
IR reciever
U5 SB
†berhub.
ON/OFF
RSIG
FBAS / PIP
FBAS
Audio-ZF
NF-Mono
Signal-Board
Interface control
Set control unit
Signal processing
Dolby Digidal
PIP
100 Hz
Booster coil
Speed modulator
RGB output stages
c.r.t. plate
RGB
RGB
Cut off
Rotation panel
* not additional to TVO
Basic-Board
Vertical output stage
Vertikal deflection coil
O/W output stage
Horizontal deflection coi
Horizontal output stage
U G2
Focus
High voltage
Diode split transformer
Auxiliary voltages
NF output stages
NF - L
NF - R
Power supply
Operating voltages
HF- ZF / PIP
FBAS / PIP
FBAS
Audio-ZF
HF- ZF
NF-Mono

2 Basic board

This main heading covers the analogue stages from the power supply circuit through the power output stages to beam current limitation, irrespective of whether or not they are contained on the basic board. In order to maintain consistency, several smaller stages on the basic board are also described.

2.1 Standby power supply

The Q 2500 receiver once again contains a standby power supply circuit, thus limiting current consumption in this mode to < 2 Watt.

The use of a new CCU SDA 6000 on the signal board increases the standby power consumption from 1 W to 2 W, compared to the older model. To meet the requirements of increased power consumption, there is now a small, blocking oscillator type power supply attached to the operating control, which supplies the U5 SB.

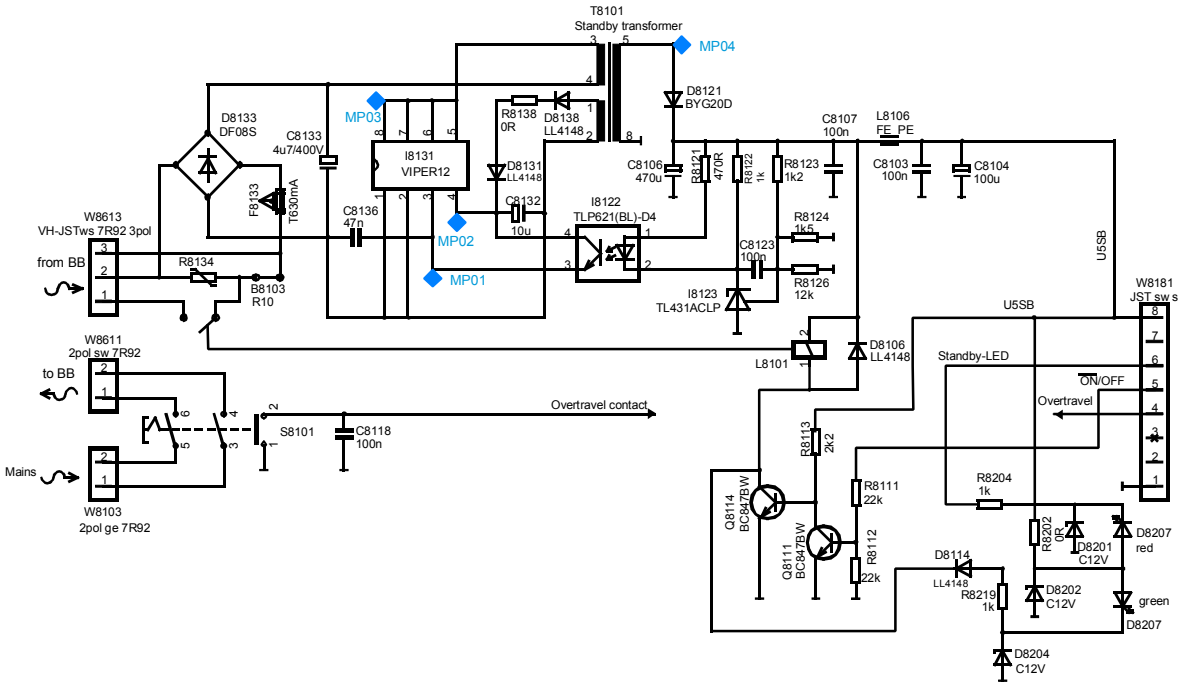
Siemens Corporation has announced a new index of the SDA 6000, that needs only 1 W power in standby operation. This will be implemented on the signal board, but the standby power supply will not be changed.

The circuit itself is mounted together with the IR receiver and the LEDs on its printed circuit board. It supplies the U5 SB, which maintains functioning of the IR detector, the processor circuit and the operating software. The last two circuits operate in standby mode, i.e. the clock frequency is reduced internally so that only those stages required to recognize a switch-on command are maintained in operation. Because of the NexTView function with U 3.3 the TV RAM is retained in self refresh mode. All of this contributes to the standby mode's low power consumption.

2.1.1 Standby power supply circuit

The main voltage is fed via W 8103 the switch S 8101 and W 8611 to the basic board and continues via the line filter (C 612, T612,C 613) and the 3-pole pin connector W613/BB back to pin 2/3 of operating control W 8613. The 220V is rectified by the bridge rectifier D 8133 and smoothed by C 8133. The blocking oscillator type power supply consists essentially of the control circuit I 8131, in which the switching transistor for the primary blocking oscillator winding is integrated, the transformer T 8101 and the opto-coupler I 8122. An operating voltage of about 18V is led from winding T 8101 pin1/2 via D 8138/D 8131 and C 8132 to I 8131 on pin 4. Control input I 8131 pin 3 is supplied with secondary side current control information by opto-coupler I8122. This control circuit stabilises the secondary side output voltage derived from the winding pin 5/8 of T 8101 at 5V. This is then fed via W 8181 pin 8 to the signal board. I8122 is fitted with an internal excess temperature, excess current and excess voltage switch protection. The blocking oscillator type power supply operates at a switching frequency of about 50 kHz.

Q2500 Operating Control



The rectified secondary voltage is applied to pin 2 of the relay winding L 8101. via protective resistor R 106. The cold end is open since Q114 is non-conducting and the receiver is in standby mode. This is indicated by illumination of the red LED.
Transistor Q 8114 is blocked, if the working contact is open, the device is in standby, which is indicated by illumination of the red LED.

If the processor receives an ON command from the infrared detector it sets its appropriate switch output to low level. This is then fed to the base of Q 8111 via pin 5 in plug W 8181 which is blocked. Via R 813, U5 SB makes transistor Q 8114 switch. The cold end of the relay coil is earthed, the working contact is closed and the main voltage flows to the main power supply circuit via pin 1 of W 8613, thereby switching the receiver on.

2.2 Blocking oscillator type power supply

The voltage supply in the Q 2400 chassis is drawn once again from a free-running blocking oscillator type power supply. TDA 4605 is used as the control and regulating circuit. In terms of its function, this IC resembles the well-known TDA 4601.

It has, however, a different type of output stage. The 4605 is designed to control a field effect transistor.

This circuit uses a BUZ 91 MOS-FET as the switching transistor. Since control of field effect transistors requires virtually no current, reducing the need for heat dissipation, it has been possible to eliminate the heat sink in the TDA 4605 control IC and house the circuit in a dual-in-line package.

On the secondary side, BUZ 71 A V-MOS transistors are used to stabilise U3.3, U5 and U12 in order to keep power dissipation to a minimum.

The converter transformer, which also provides the standard VDE power distribution, has a primary working winding and a secondary winding to supply voltage to the IC and to generate a control voltage.

Secondary windings also generate the following voltages:

UB to supply the line output stage

U 25 to supply the line driver stage

U 3.3, U 5 and U 12
predominantly to supply an operating voltage to the digital control

U9 for the interface switching ICs

U8 for the video ICs

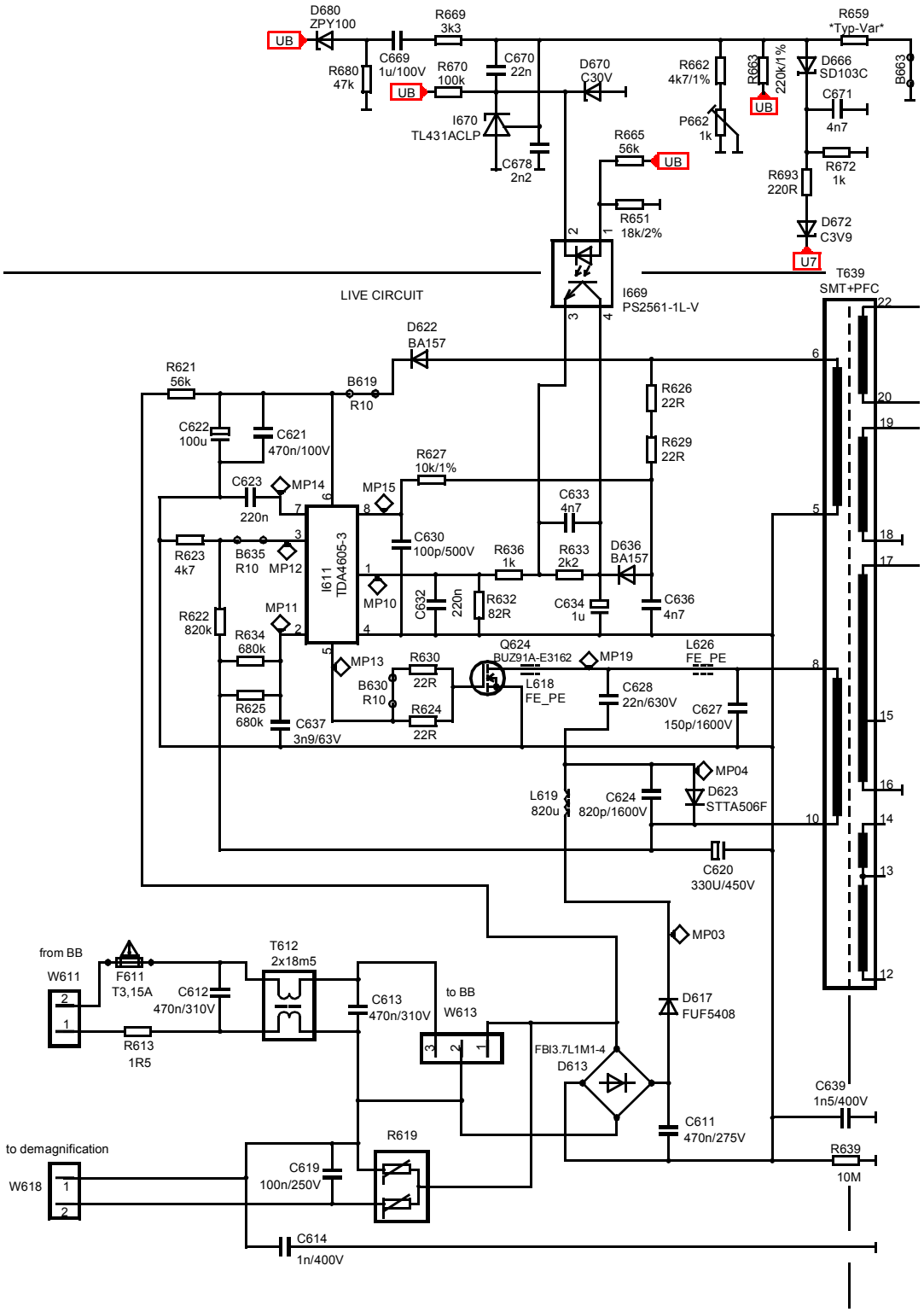
UNF+ and UNF-
used to supply a floating voltage to the VF output stages, approx. ± 18 V

2.2.1 Primary side

The mains voltage flows through the mains power switch, the working contact of the standby relay and the mains RFI suppression filter to the degaussing coil, and via the start-up current limiter R 613 to the bridge rectifier D613.
A voltage of approx. 310 V very rapidly builds up at charging capacitor C 620. This is applied to the drain terminal on the switching transistor via the working winding in the converter transformer.

Since the gate BUZ 91 is not driven at this time, there is no load on the operating voltage.

Q2500 blockingo oscillator type power supply, primary side



2.2.2 Start-up

The power supply section is started up by an additional starting circuit. The required voltage is rectified using a diode path in the bridge rectifier. It is fed via resistor R 621 to pin 6 in TDA4605 where capacitor C 622 is then slowly charged. During this charging phase, capacitor C 637 is charged to 6.6 V on pin 2 via an internal IC path. A reference voltage of 1V that is required during the start-up phase and later during normal operation is also generated in the IC.

If the voltage at pin 6 reaches 12 V the IC operates and makes the switching transistor conducting via pin 5. A current flows through both the transformer working winding and the switching transformer drain source path. During this period, magnetic energy is being stored in the transformer. During this conductive phase, a drain current simulator C 637, integrated in the IC, is charged on pin 2. If the internal reference value of 1 V is reached the IC blocks the switching transistor. The magnetic field in the transformer breaks down and this induces voltages in the windings.

The start-up procedure recommences and the system swings/oscillates to normal operation. This is arrived at when a voltage of 400 mV has built up at pin 1.

2.2.3 Normal and control operation

A static state is set in normal operation at constant load. The operating voltage for the IC is drawn from the transformer winding pin 5-6 and rectified with D622. The voltage at pin 6 in the IC is then 11 V. The control input at pin 1 is 400 mV and the duty cycle for the zero passage detector at pin 8 in the IC is set.

The switching transistor is controlled with a fixed frequency of between 20 and 40 kHz, which corresponds to the instantaneous load.

If the load changes, the duty cycle at pin 8 in the IC also changes. The negative edge indicates to the IC when the energy stored in the transformer has been dissipated. If the load increases, this occurs more quickly and the IC reduces the control frequency. If the load decreases, the control frequency increases. This means that load variations between approx. 40 and 260 W and mains voltage fluctuations between 180 and 270 V can be compensated for.

In order to achieve a higher UB voltage stability, regulation on the secondary side is now used which influences the primary circuit's I 669 opto-coupler. The I 669 opto-coupler is controlled via I 670. The control mechanism is influenced via several paths:

- With d.c. voltage via R 663
- Alternating, by coupling to the R 680 diode.
- When not under load, via D 672

The operating voltage is set with the P662 potentiometer. A small resistance here indicates a high value of UB. Correspondingly, a high value of R means a low value for UB.

If UB increases, e.g. due to a smaller load on the line output stage, UB exerts a stronger influence via R 663 at the input of I 670. This results in the I 670 cathode outputting a smaller voltage. The photodiode in I 669 receives more current through R 665. The path between pin 3/4 of I 669 has a lower resistance allowing for a higher voltage on pin 1 of I 611. Component I 611 then regulates output voltage until a value of 400 mV on pin 1 is reached again. If the value of UB becomes lower, then the regulation process is exactly the inverse of that described here.

Via D 680, R 669 and C 669, ripple voltage components are coupled into the regulating circuit. In particular, this branch prevents a low 50 hz ripple voltage arising on UB. With 60 hz signal sources (NTSC, PAL 60 Hz or VGA operation), this would result in humming interference in the picture.

Without secondary-side regulation, e.g. in SAT standby operation, UB would increase to approx. 180 V. In this mode of operation, other voltages (e.g. the bias voltages for the U 5, U 12 branch) do not alter significantly. Stabilization is also guaranteed for these voltages in this mode of operation.

Due to the secondary-side stabilization with UB as stabilization factor, UB without any load would naturally remain constant. In this case, the power supply would regulate down from approx. 180 V (without secondary-side regulation) to the previously set value of UB, typically 146 V. This would also result in all other voltages being reduced. The bias voltages for the stabilized voltages would be too low and they would no longer be stabilized. The digital electronics would search for errors.

In order to prevent this, the regulation acts via U 7. This is accomplished via components D 672, R 693 and 666.

U 7 also drops when the line-output stage is disconnected. When this has reached a value of approx. 6V, the D 666 Schottky diode voltage has also fallen sufficiently for it becomes conducting. A further drop in operating voltage is prevented by the I 670 input. Stabilization of secondary side voltages, e.g. for U 5 and U 12, still operate properly in this mode of operation.

2.2.4 Protective operation

The IC contains a protective circuit to prevent the control frequency from entering ranges where it would otherwise damage the switching transistor during over- and underload. In such cases the system is shut down.

The indicator for this is the voltage on pin 6 in TDA4605. During normal operation this voltage is approx. 11 V. If the load increases, due to a short circuit on the secondary side, for example, the voltage on pin 6 drops. If it drops below 7V, the logic circuit switches off. The same occurs if the voltage on pin 6 exceeds 15 V due to complete discharge or a fault in the control circuit. There is also a second protective circuit to safeguard against overloading. If the current flowing through the working winding in the transformer and therefore also through the switching transistor is so great that the voltage on pin 3 drops below 1 V, the power supply also cuts out.

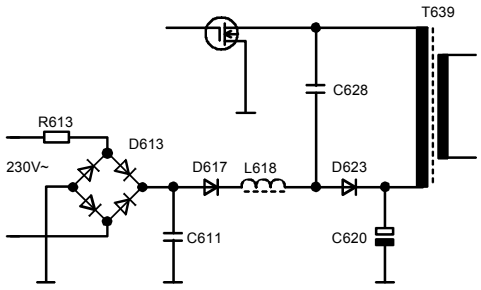
In addition, integrated thermal protection switches the system off at chip temperatures of over 150°.

2.2.5 Power Factor Control

All TV sets with power consumption of more than 75 W, and delivered after 01.01.2001, must be fitted with a Power Factor Control (PFC) circuit.

The circuit power supplies used up to now overlay a pulsed current on the sinusoidal mains alternating voltage. The Power Factor Control circuit ensures current extraction is almost completely sinusoidal. This function is implemented by changing the power supply's input range

Power Factor Control



The alternating voltage from the mains is rectified by the D 613 bridge rectifier. When in resonance, C 620 is loaded to approx. 310 V. Without PFC this means that mains current will only be drawn when the sinusoidal half-wave exceeds 310 V. Sinusoidal current extraction is therefore not guaranteed. With the PFC circuit, C 620 is not directly charged from the mains. Charging of C 620 is via the C 628 current pump. When the Q 624 switching transistor is conducting, C 628 is connected to earth. C 628 is charged via D 617 and L 619. If Q 624 is now switched off, a voltage of approx. 400 V is set on the drain.

The energy stored both in C 628 and in the coil can now charge up C 620 via D 623. C 628 will naturally also be charged when the sinusoidal mains alternating voltage just crosses zero and has a low value.

Q 624 is switched with a frequency between 20 kHz and 40 kHz, depending on load conditions. This also means that C 620 is charged with a current at the same frequency. The current drawn from the mains would also correspond to this frequency, but will be harmonized by the mains input filter.

2.2.6 Secondary side

Although the secondary side voltages are relatively stable, and fast and transient changes in load can be compensated for by the field effect transistor in the primary side, stabilisation of voltages in the digital component is still required.

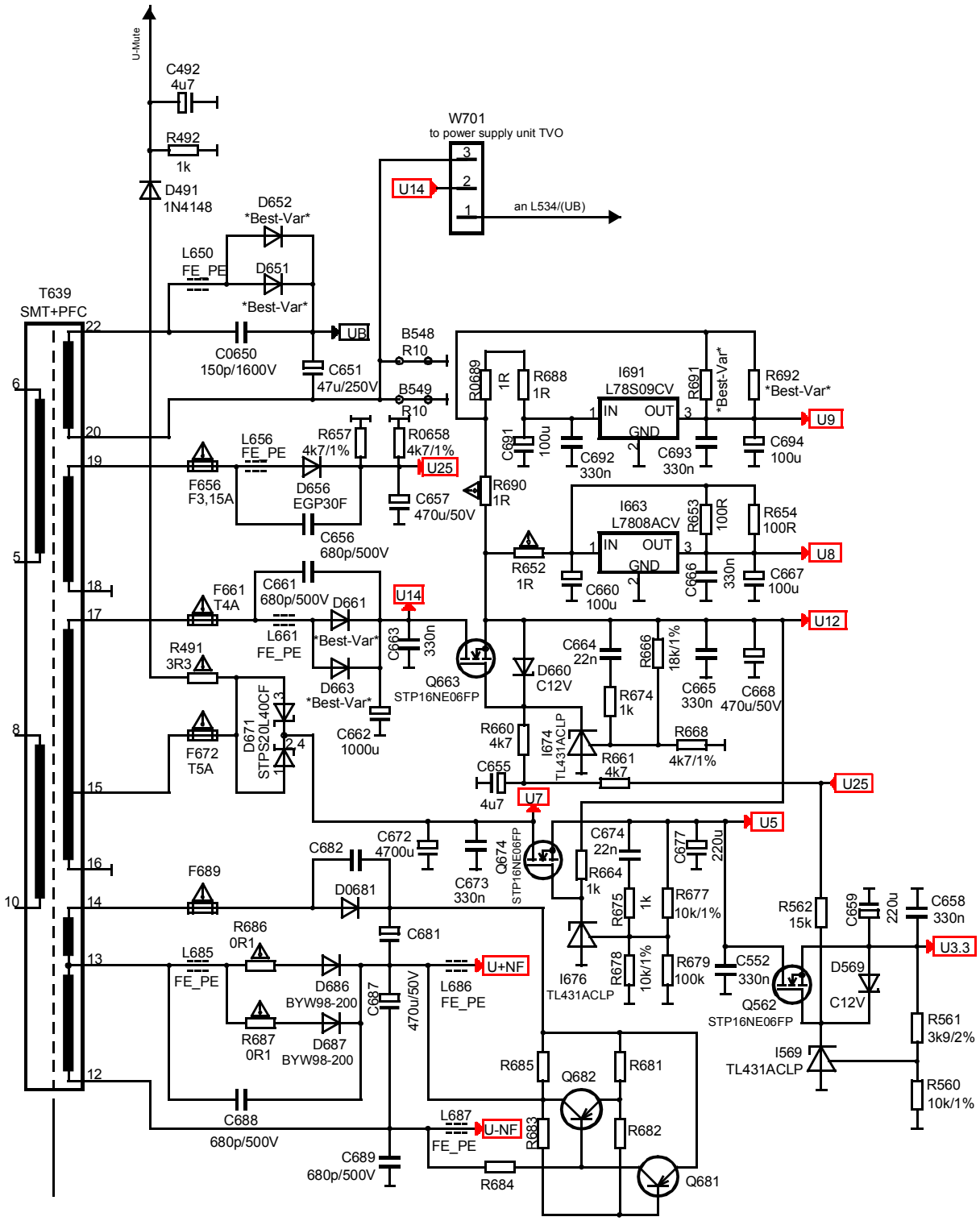
The two secondary voltages U 3.3, U 5, U 8, U 9 and U 12 are stabilised

For the other secondary voltages:

- UB for the horizontal stage
- U 25 for the horizontal driver stage
- UNF+ and UNF- for the VF output stage

Stabilisation is not required, as no current is drawn from these non-controlled levels.

Q2500 blocking oscillator type power supply, secondary side



2.2.7 Voltage stabilisation

For each of the operating voltages U 3.3, U 5 and U 12 a V-MOS transistor is used as a horizontal controller for stabilisation. Their gate voltages are kept constant by the connected IC's I 569 for 3.3 V, I 676 for 5 V and I 674 for 12 V. In addition, their control input is connected to the voltage distributor by the respective output voltage.

If the output voltage falls under high load, the IC's become high resistant causing the gate voltage to increase and the horizontal controllers are controlled upwards further, whereupon the output voltage increases again. If the load decreases the opposite occurs.

In addition, voltages U8 for the video control and U9 for the interface with the fixed voltage controllers L 7808 and. L 78S09 are stabilised. The controllers I 663 and I 691 are now also located in the power supply. The input voltage is U 12.

2.2.8 Voltage increase

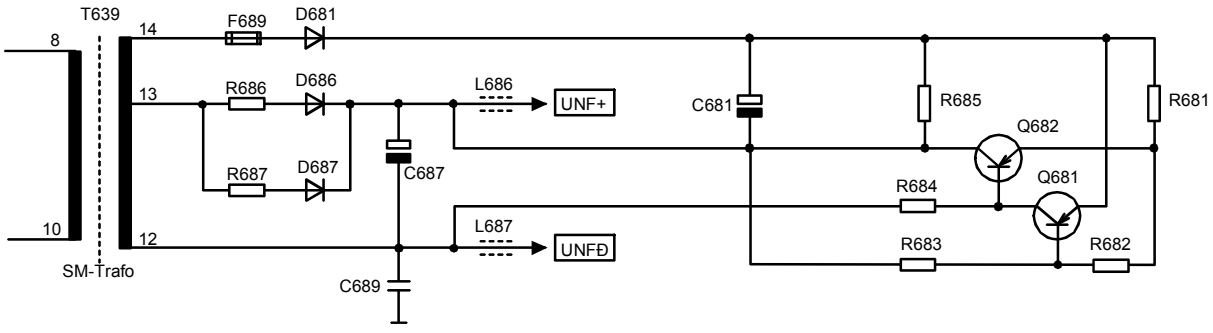
To avoid overloading the VF output phases, they are supplied with a load-dependent operating voltage. The control range of the circuit for this lies between ±18 V in no-load operation and ±13 V at full load.

The pulses taken from pin 14 of the transformer are rectified by D 681 and applied to the emitter connections of transistors Q 682 and Q681. For no-load or low-load operation no voltage is felt across current measurement resistor R 681. This means that Q 681 is blocked and Q 682 is switched through to its base with L level via R 684. The voltage from pin 14 of the transformer increases the VF operating voltage to +18 V.

If the noise level is increased, more current is drawn accordingly. There is a corresponding voltage drop across R 681, which means the base of Q 681 goes more negative, the transistor switches and as a consequence with base Q 682 going positive, a greater or lesser degree of blocking is achieved. The VF operating voltage is reduced accordingly.

Harmonic distortion is therefore kept low. thus preventing overheating of the output ICs. In this way a noise-level dependent video pumping can be prevented.

Voltage increase for VF



2.2.9 Servicing information

For repairs and fault-finding in the power supply unit the following should be noted:

Always connect the unit via an isolation transformer, especially when fault finding the primary side.

The load on C 620 remains active long after the unit has been switched off. Discharge the load if necessary via a low-resistance resistor.

Operation of the power supply unit without the digital unit is possible. For this pin 5 on pin connector W 8181 is connected to earth, but not until a voltage is applied to the standby power supply. For specific failures, this test can also be done with an integrated digital component.

A check of the horizontal output stage cannot be made by withdrawing the deflection plug. For this test L 534 must be unsoldered. An extra load is not required.

A separate test of the power supply unit function without interference from the chassis can be achieved by unsoldering one side of the secondary side rectifier diodes. The rectifier branch for the UB (D 651) and U7 (671) must be available. The UB can then be loaded with a 100 Watt LED.

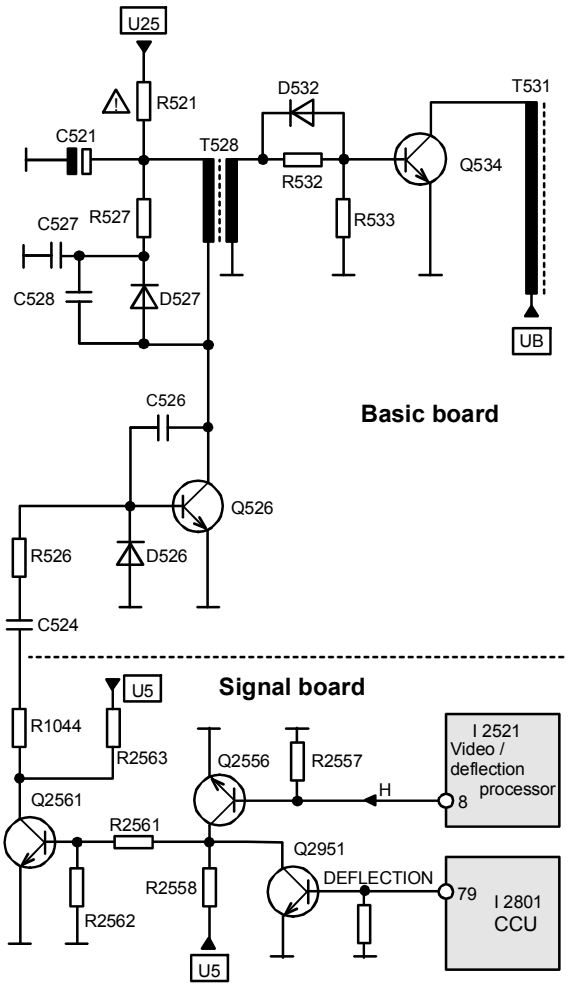
U 7 and UB are necessary for power supply control, so do not deactivate them.

2.3 Horizontal deflection and high voltage production

On the 100 Hz Chassis Q 2500 the horizontal driver, horizontal output stage and high voltage production are essentially the same as the predecessor.

2.3.1 Horizontal driver

The horizontal driver stage is controlled from I 2521 on the signal board via pin 13 from connector W 1511. The pulse at this point is 2.5 Vss.



Capacitive control via C 524 prevents driver stage Q 526 being held conductive continuously if components are faulty or there are no control pulses. Diode D 526 enables rapid discharge of C 524, if Q 526 is controlled in the blocking phase.

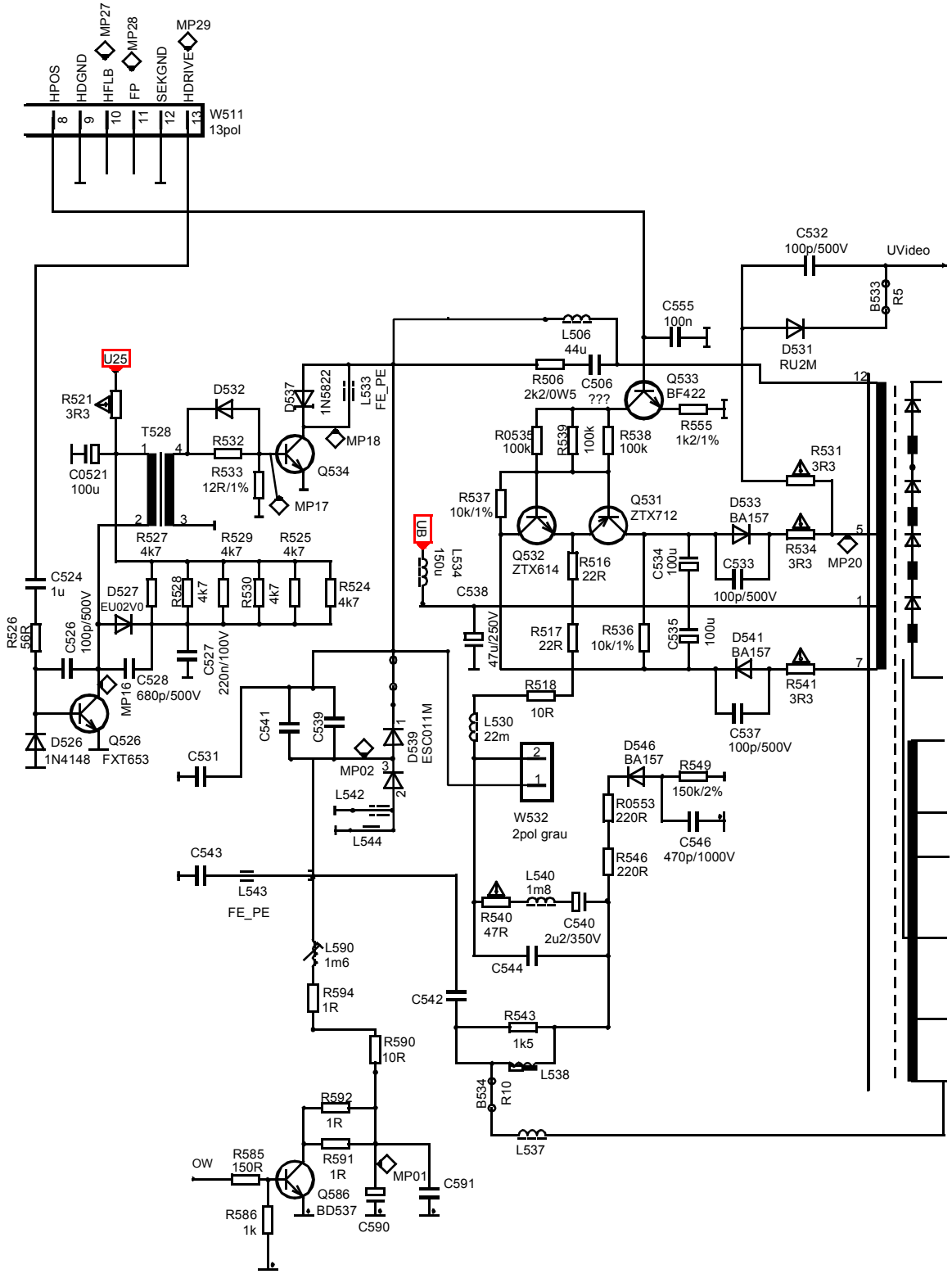
It can be clearly determined from the line driver circuit, as from the control of the line output stage, that this is a case of low-resistance current control. The driver stage is equipped with a transistor, which supplies for the drive transformer T 528 (conversion ratio 7:1) output stage the required base control current of up to 0.9 Ass. To limit inductive switching peaks an R/C combination is connected, a.c. to earth, to the collector of Q 526 after diode D 527. The driver stage operates with respect to the output stage in alternating operation, i.e. if Q 526 is conducting, then Q 534 is blocked and vice versa.

2.4 Horizontal output stage

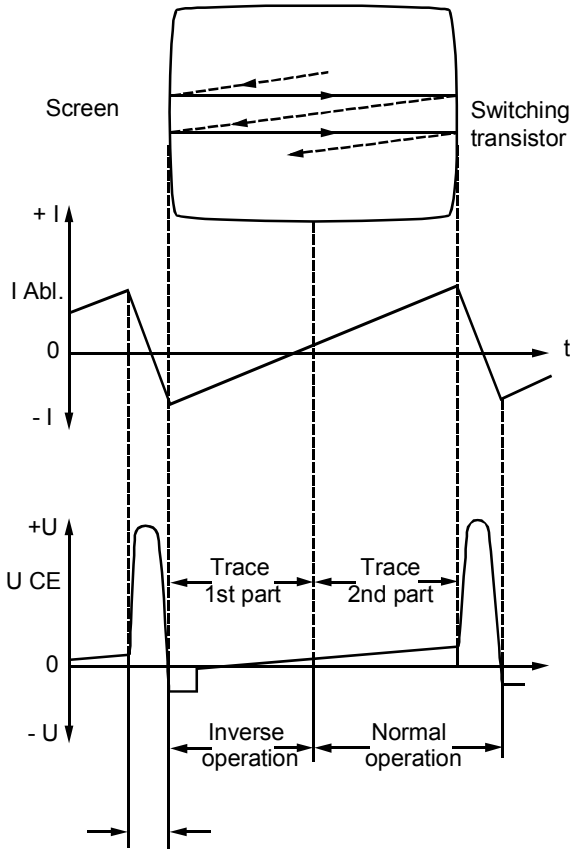
As mentioned in the previous section control of the horizontal output stage, or more precisely the horizontal switching transistor, alternates according to the switching regulator principle. Essentially the base resistance consists of R 532 and the series secondary winding of the driver transformer T 528. The parallel arranged resistor R 533 dampens switching peaks arising in the inductivity.

An additional anti-parallel diode from collector Q 534 to earth, which was used as a booster diode in earlier forms of thyristor deflection switching, is not required, as in this switching concept the collector-base route of the switching transistor Q 534 fulfils the function of the booster diode by a process of inverse operation. In practice the parallel O/W-modulation diodes cause a perceptible load reduction of the switching transistor. The drawing below shows that this inverse operation of the transistor occurs during the first half of the trace, until about the middle of the line. In the second half of the run the transistor operates as normal with conducting base-emitter diode. Only during the relatively short flyback time is the switching transistor blocked. The low resistance base switching already described enables the base peak current between +0.9 A and –0.9 A in both directions to be dissipated quickly.

Q2500 horizontal output stage



It is conceivable that the essentially higher emitter currents (IE max. = 4.5 A) will invoke enormous "flooding" of charge carriers in the N-P- and P-N-transitions of the semiconductor. In order to guarantee rapid switching behaviour and to ensure rapid discharge of the charge carriers in the base zone, the base control is correspondingly low resistance.



In this respect it must be mentioned that the control pulses are specially formed for the dual functionality of Q 534 normal and inverse operation. In principle the trace relationship of the base control of 6 µs flyback and 26 µs trace time is changed to 14 µs flyback and 18 µs trace time. In this way it is possible, to process unavoidable production dispersion of the driver transformer. By means of prompt control the switching transistor has sufficient time to prepare for the following operational phase.

The operating voltage of the horizontal output stage is taken from the switch mode power supply and is 146 V for 33“/4:3 and 32“/16:9/RF c.r.t.s, 142V at 21,24,28“/4:3 and 136 V for all other c.r.t.s. The exact control and switching rhythm during a line period corresponds to the principle of the switched resonant circuit. For this the line switching transistor operates via its three operating conditions - conduction, inverse conduction and blocked – in such a way that the charge and discharge procedures of the collector capacity C 531 and inductivity T 531 determine the exact trace and flyback intervals.

Only during the horizontal flyback time is Q 534 blocked for 6 µs. By charging the operating voltage the capacitor of the parallel resonance circuit C 531 forms the positive half wave of a sinusoidal oscillation. C 531 and T 531 are dimensioned in such a way that they create horizontal flyback pulses. The natural desire of a parallel resonance circuit to convert the stored charge in the capacitor into inductance as magnetic energy leads to reversal of polarity of the current.

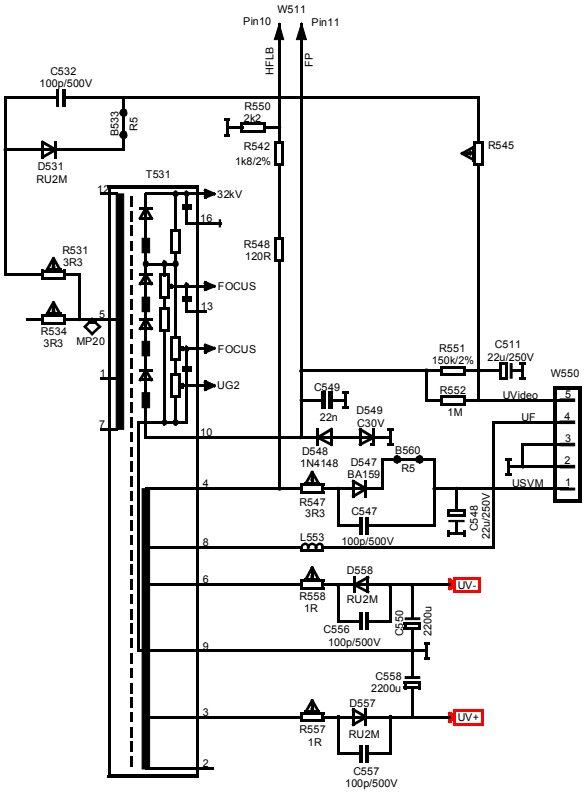
Normally the negative component of the sinosoidal oscillation is felt on the collector of Q 534. This attempt is however prevented by the collector-base diode path of Q 534.

On reaching the start up voltage the diode path becomes conductive and cuts the negative components. In these cases the E/W modulator diodes support this function, whereby in the switching transistor the power dissipation of the transistors is reduced

The horizontal deflection pulses are detached directly from the collector of the switching transistor on the parallel deflection winding. Between the base point of the horizontal deflector and the E/W diode modulator the east/west correction information is coupled in accordance with the dual generator principle. This procedure is almost non-reactive with respect to the primary winding of the high voltage transducer.

2.4.1 High voltage production

Q2500 secondary H output stage



The high voltage transducer also contains the cascade. The secondary winding of the step up transformer is divided into four and the high voltage rectifier diodes are connected between the individual winding sections. This form of high voltage production is possible without the highly charged capacitors used up to now, which increases the reliability of high voltage production and makes possible a space-saving compact solution.

The resistance voltage divider and the potentiometer of the focus and G2 adjustment is integrated mechanically into the splitting combination for units with 4:3 c.r.t.s.

The filament voltage of the c.r.t. is assigned to pin 9. On pin 4 the flyback pulse for the synchronisation of the control is assigned to pin 4. At the same time this pulse is rectified by D547 and fed to the c.r.t. plate via connector W 549. The 60V occurring here is required by the c.r.t. PCB for the speed modulator. The UV+ and UV- for the vertical stage (approx. ± 13 V) occur in the windings between pin 6 and 9 and pin 3 and 9.

Just like the amplitude of the radiation current a corrective voltage for the stabilisation of the horizontal amplitude can be tapped at the base, connection 10 of the high voltage winding.
This radiation current dependent voltage is led to the signal board via pin 11 of connector W 511. The radiation current fuse and limiter are found here.

The operating voltage U 200 for the video output stage is tapped on the primary side of the pin 5 of the diode split transformer and rectified by D 531. In addition on connection 5 another voltage UB -10 V and on pin 7 a voltage of UB +10 V are produced, which are felt on capacitors C 535 and C 534. On UB = 136 V there are 126 V and 146 V. These voltages are required for the offset correction of the horizontal deflector.

2.4.2 Horizontal- offset deflector

The deflector pulse is formed in such a way that through the deflection and S-correction a linear deflection results. This only functions however when the deflection is exactly central. As the Q 2500 chassis could also be used as a VGA monitor, high demands are placed on linearity. For this reason the possibility of offset correction is created.

A free DAC in I 2271 is used for horizontal offset correction. The d.c. voltage felt on pin 55 can be set in the servicing mode. This is fed via connector W 511 /W 1511, pin 8, to the base of transistor Q 533 on the basic board. Q 533 together with R 555 represents a current source for the push-pull stage Q 531 and Q 532. The operating point for the push-pull stage is set with R 537 and the parallel circuit of R 535/538/539. At rest the operating voltage of the line output stage is applied to the base connections of Q 531/532 and both transistors are blocked.

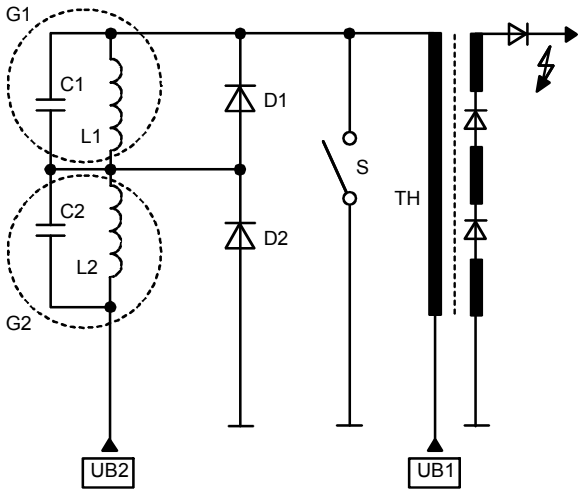
If I 2271 increases the base voltage of transistor Q 533 and this then conducts, the base voltage of the push-pull stage drops and Q 531 conducts. This means the d.c. current is made more negative by resistors R 516, R 517 and R 518 and coil L 530, whereby the deflection shifts to the left.

If, on the other hand, the voltage on pin 27 of I 2271 drops, transistor Q 533 becomes high resistance and the base voltage on the push-pull stage increases. This means Q 532 conducts and L 530 increases the voltage on pin 2 of the deflection coil. This leads to a shifting of the d.c. current component in a positive direction and deflection to the right. Coil L 533 serves as d.c. current coupling for the deflection.

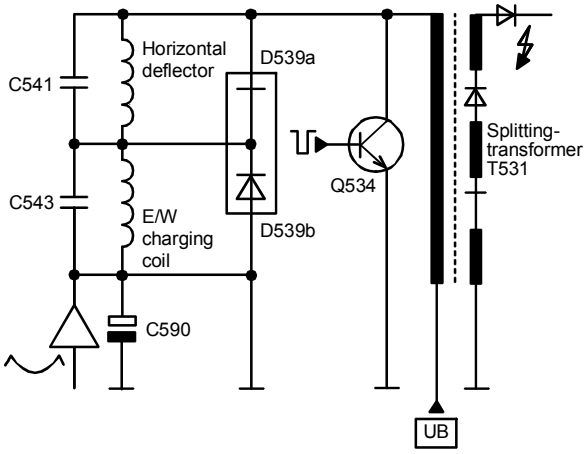
2.5 East/west correction

In order to compensate for the pincushion (distortion) in 110° units in an east/west direction, the horizontal deflection current in the vertical centre must be increased with respect to the vertical start and vertical end. The right degree of correction is achieved by influencing the horizontal deflection current with a vertical frequency parabola in the east/west diode modulator.

Two generators connected to each other by a bridging circuit provide the correction signal for the E/W modulator for the horizontal deflection current.



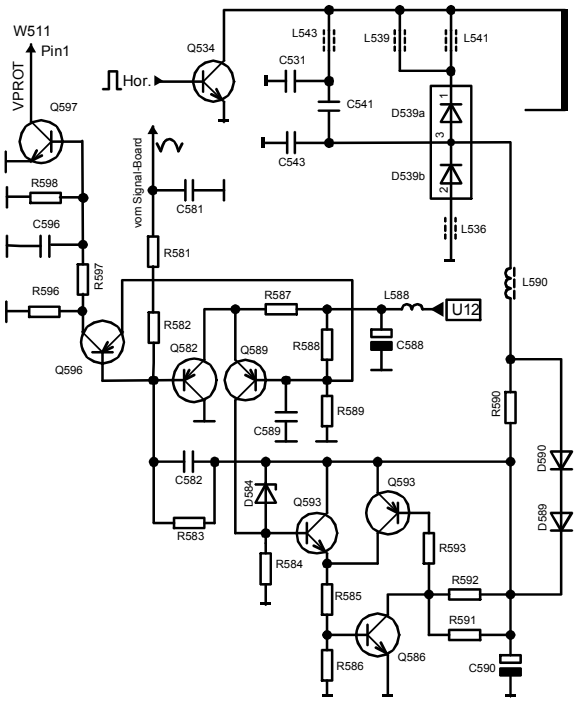
In the above drawing the two generators, G1 = horizontal generator, and G2 = east/west generator, are represented only by their resonant circuits. The deflection current in the deflection coil L1 is supplied by both generators. So that the high voltage is not influenced by the E/W modulator, the voltage on transformer TH is determined only by the horizontal generator G1. Therefore, for correct bridge compensation during the line trace, only E/W modulation of the deflection current takes place in an almost non-reactive fashion on the horizontal output level. For improved clarity the conceptual flow diagram above is shown in the following drawing with the actual component locations.



2.5.1 Circuit

The components of the east/west output stage, as well as the diode modulator are located on the basic board.

E/W correction



The video/deflection processor TDA 9332 applies a d.c. underlying parabola type voltage to pin 3. This Information contains all corrections for picture width and east/west. The following amplifier stage, consisting of transistors Q 582 to Q 589, could therefore be implemented simply as a conventionally based differential amplifier.

Control is via low-pass filter R 581, C 581 and R 582 on the base of transistor Q 582. The low-pass filter suppresses any noise components from the pulse width generator in I 2521.
The base of transistor Q 589 is determined by the voltage divider R 588/R 589 in d.c. and thereby determines the operational point of the differential amplifier.

The amplification of the differential amplifier is determined essentially by the relationship of the negative feedback resistance R 583 and the output resistances R 581/582. The parabola type voltage, amplified to 12 V by output stages Q 585 and Q 586, is fed via the E/W charge coil to the diode modulator. Dual diode D 539 superimposes the deflection current on it and the E/W correction is implemented.

Transistor Q 593 was incorporated to protect the output stage transistor Q 586 in the event of the deflection connector being withdrawn. Normally Q 593 acts as positive feedback to Q 586. If the deflection connector is withdrawn the current increases through Q 586 and therefore also through resistors R 591 /R 592. This causes Q 593 to conduct and the power loss in Q 586 to be returned to a normal level. In the event of a fault the two transistors Q 596 and Q 597 ensure that the unit switches to protective operation. Q 596 is conductively controlled by a reduced base voltage. Q 597 conducts and controls VPROT at low level. The CCU protective circuit responds and switches the unit off.

2.6 Vertical output stage

In comparison with earlier models the Q 2500 generation of chassis does not have an a.c. coupled, but a d.c coupled vertical output stage. This has the advantage that the vertical deflection coils can be supplied with current directly and the large coupling capacitor can be dispensed with. This means that vertical correction information can operate directly, without vertical distortions caused by the deflection coil coupling capacitor.

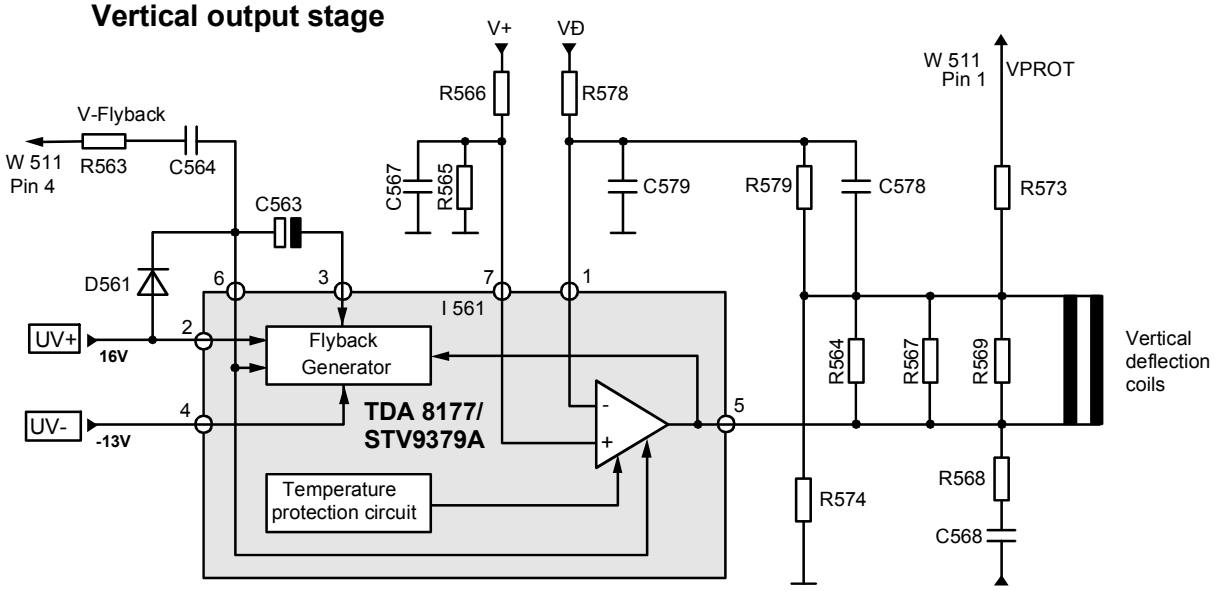
As we know, a positive and a negative deflection current flow through the vertical deflection coils. In order for the d.c. coupled output stage to produce this negative current, it must be supplied with a +/- voltage.

The two possible variants of the vertical output stage IC´s (TDA 8177/STV9379FA) incorporated into the 100 Hz Q 2500 chassis are housed in a Heptawatt plastic housing.

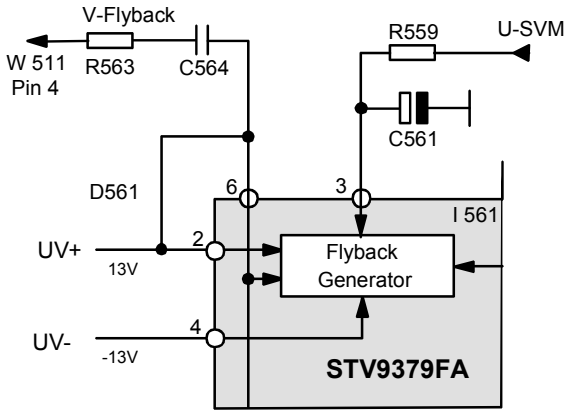
The following functional groups are incorporated into the IC´s as circuit components:

- A power operational amplifier that is able to drive the vertical deflection coils with a peak deflection current up to 3 Ass.
- A flyback generator, that generates the voltage charge for the vertical flyback.
- A temperature protection circuit that limits the deflection current on overload.

The power operational amplifier is controlled symmetrically and inversely on its non-inverting and inverting inputs. Therefore, the video/deflection processor outputs two inversely symmetrical vertical control signals.



Vertical output stage



These two control signals contain all vertical correction information. This means that output side S correction, which is necessary for a.c. coupled output stages, can be dispensed with completely. The component insert at the output of the V output stage is also considerably reduced. Symmetrical control almost fully suppresses interference that can affect the two V control signals due to the very high common mode rejection ratio of the V-power operating amplifier. The two V control signals V+/V- are applied to the pin connector W 511, pin 2/3 and reach the series resistors R 566 /R 578 via the inputs on pin 1/7 of the V output stage I 561. The sawtooth, which is amplified about 10 times, is output by pin 5 of I 561 and forces the current through the vertical deflection coils.

The R/C combination 568, from the output of pin 5 to earth, prevents the tendency of the output stage to oscillate and protects it from switching peaks that can be caused by the deflection coins. To stabilise the V output stage, part of the sawtooth from the base of the deflection coils is fed back via resistor R 579 to the inverted input pin 1 .

Picture formation is normally established by the d.c. current component of the deflection current. This means that for a d.c. coupled V output stage, by simply changing the d.c. components of the control sawtooth, the d.c. component of the deflection current can be changed, and with it the picture formation.

2.6.1 Flyback generator

The job of the flyback generator is to provide, the switching voltage for the voltage increase during the vertical flyback. The problem with this is as follows:

The energy requirement of the vertical output stage is at its highest during the flyback, as the electron stream has to be directed rapidly from the lower right corner of the screen to the top left corner.

This transitory additional energy requirement is achieved by doubling the operating voltage, which is only available for the vertical output stage. During the vertical trace, the bootstrap capacitor C 563 is charged to approx. 26 V via D 561. The output of the flyback generator at pin 3 of I 561 at this point is UV-/-13 V. At the time of flyback start, the flyback generator is switched by the output stage output at pin 5 and applied to the output at pin 3 UV+/ +13 V. Due to the d.c. shift on the minus pin of capacitor C 563, the operating voltage for the output stage on pin 6 increases by the voltage in C 563. At the same time, D 561 is blocked, which prevents the charge in the power supply leaking away. This means that for rapid flyback there is a transitory +40 V (approx.) operating voltage available.
For many c.r.t. types the flyback pulse is not sufficient to fully return the deflection beam, so that flyback lines are visible.

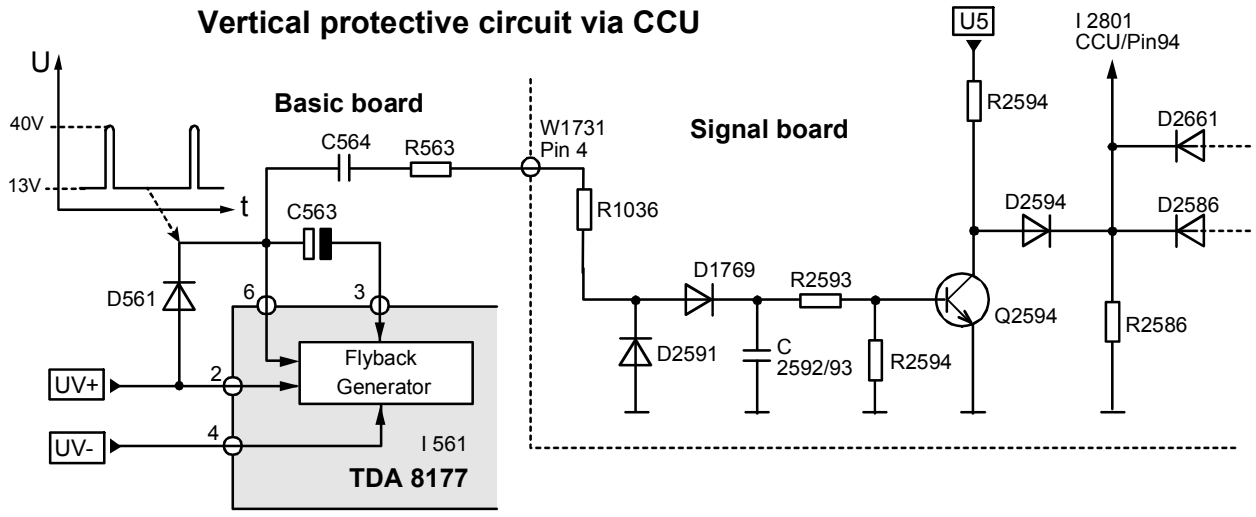
In these devices the V output stage of STV9379FA is used. For the flyback generator this has an independent voltage supply. A USVM/60V is used that is fed to the I 561 via the fused resistor R 559 on pin 3.
If the V output stage is changed during service then ensure it is replaced with the same type. The two IC variants are not compatible.

2.6.2 Vertical protection circuits

Protection circuits are used to protect the c.r.t. against burning if the vertical deflection fails.

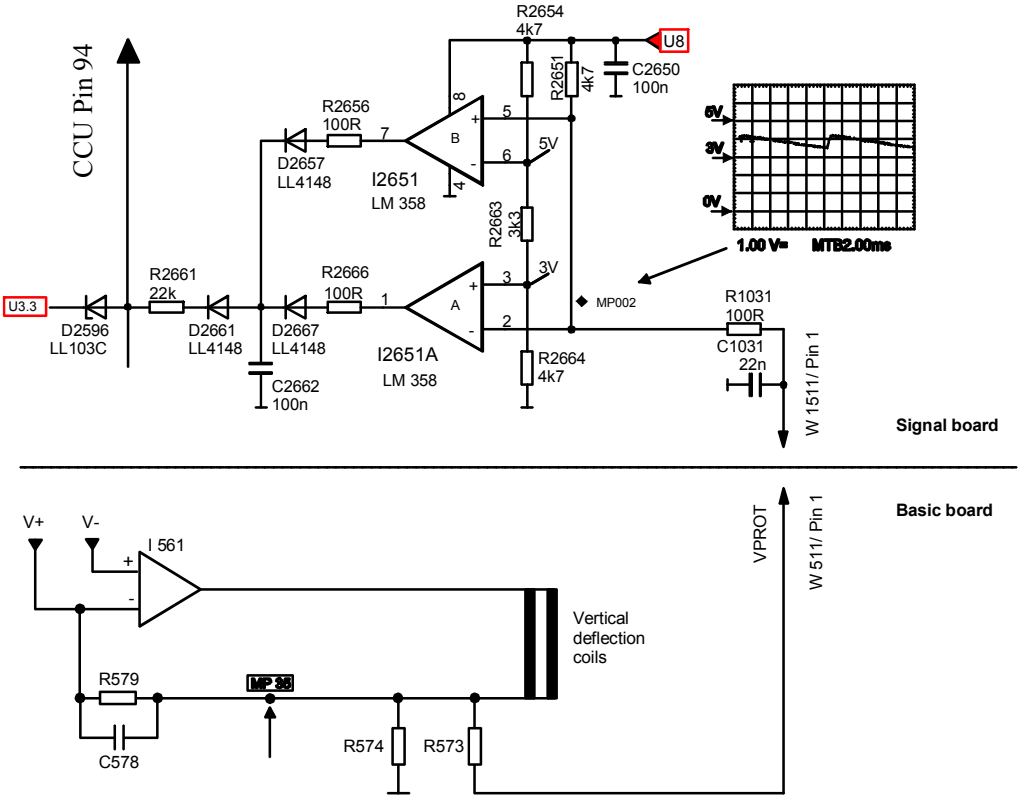
For a d.c. coupled V output stage a fault situation can theoretically occur in which the deflection saw tooth appears to be available, but a faulty d.c. component directs the electron beam to the upper or lower end of the c.r.t. neck. This could cause the c.r.t. neck to melt and lead to destruction of the c.r.t. neck.

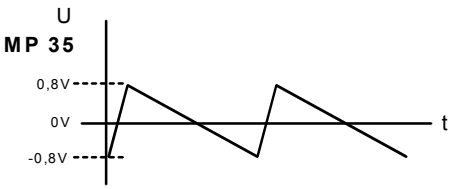
To prevent this a V saw tooth is taken from the base of the V deflection coils with R 573 and a d.c. voltage is applied to the signal board with R 2651.

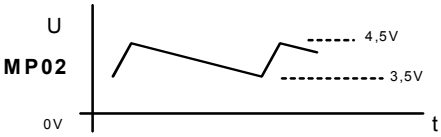


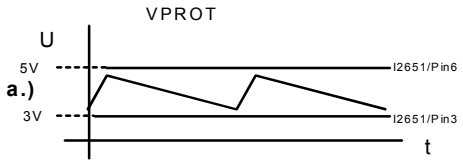
This VPROT signal is fed to the protective circuit that consists of the dual operational amplifier I 2651. Operational amplifier A works on its non-inverting input pin 3, with reference voltage of 3 V and operational amplifier B on its inverting input pin 6 with 5 V. If the VPROT signal - Diagram A – does not fall below or exceed the reference values of 3V and 5 V, then the V deflection and the vertical d.c. component through the deflection coils is correct. If the d.c. component is too positive or too negative - Diagrams B + C – this is interpreted as a fault. If, for example, the d.c. component of the VPROT signal is too small (<3V Diagram C), OP A controls its output on pin 1 to H level. This is fed, via the two D 2667/2661, to CCU pin 94. H level on pin 94 represents a fault and the CCU switches the device within about 2 secs to standby operation. If the d.c.level is too positive (>5V Diagram B) pin 7 goes from OP B to H level and the CCU switches the device off.

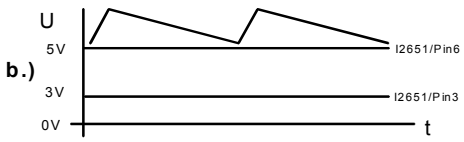
Vertical protective circuit via CCU



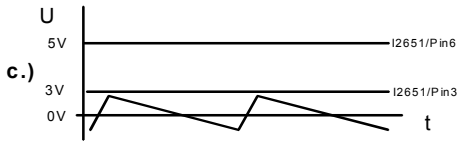




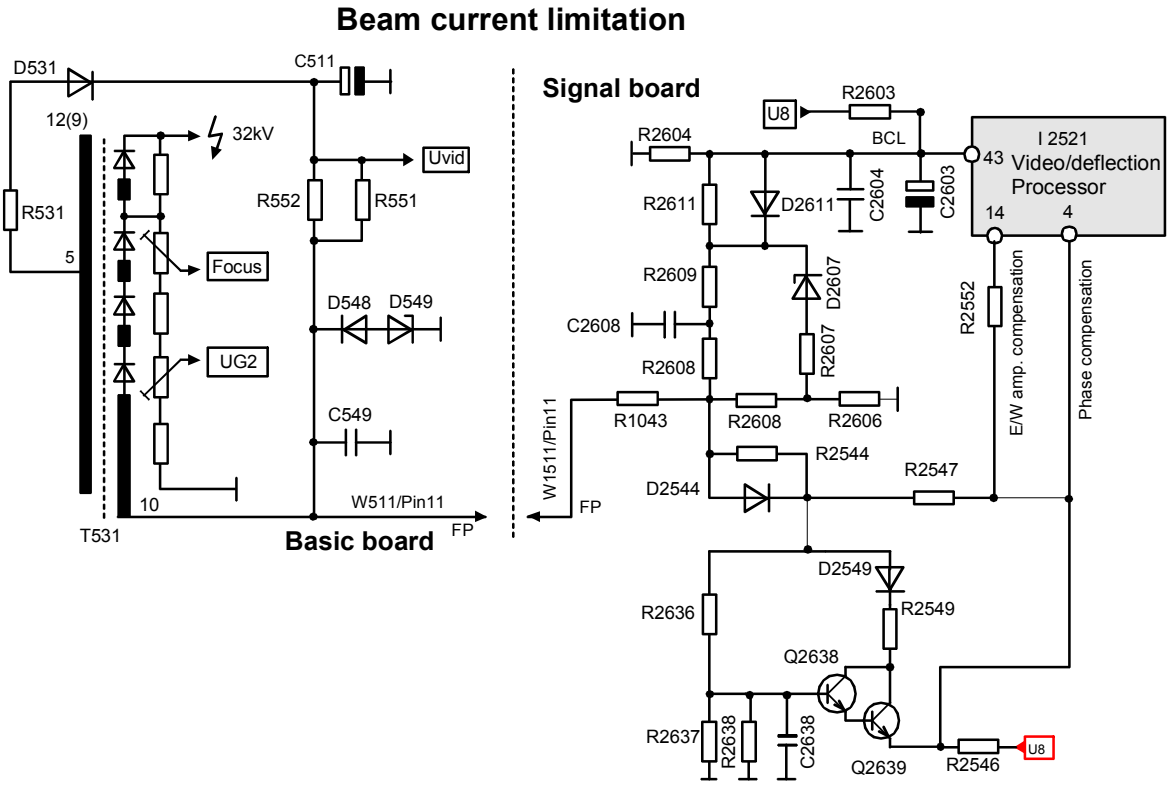




d.c. current component much too positive



d.c. current component much too negative



The second protective switch monitors the V flyback pulse that is fed from I 561 /pin 6 via R 563 to the pin connector W 511 /pin 4. On the signal board this V flyback pulse is rectified by diode D 2591/1769 and integrated with capacitor C 2592/2593. With the voltage available on capacitor C 2992/2593, Q 2594 conducts. The collector of Q 2594 is then at the same potential as L, and diode D 2594 is blocked.

If there is no flyback pulse due the absence of a V output stage, no voltage can build up on capacitors C 2592/2594 and Q 2594 blocks. Pin 94 of the CCU is set to H level via diode D 2594.

If pin 94 of C 161 is set to H level by the absence of a V flyback pulse in the operating condition of the unit, as described, after 2 seconds the CCU switches the device back to standby operation. This permits safe shut down of the device with a faulty deflection controller.

2.7 Beam current limitation

To limit the beam current the Q 2500 chassis is provided with an average value control. The limit switch is integrated into TDA 9332.

The switch to limit the contrast and brightness is controlled with a d.c value via pin 43.

The switch is designed in such a way that for a voltage of >3.3 V there is no limitation on contrast and brightness.
For a voltage between 3.3 and 2.2V the contrast is reduced in proportion to the voltage. If the voltage drops below 1.8 V the brightness as well as the contrast is reduced. At approx. 1 V on pin 15 the brightness and the contrast are reduced by 100%, whereupon the screen is black.

To achieve beam current limitation the base of the diode split transformer influences the d.c. value on pin 43 of TDA 9332. Inversely proportional voltage information on the beam current can be obtained at the base.

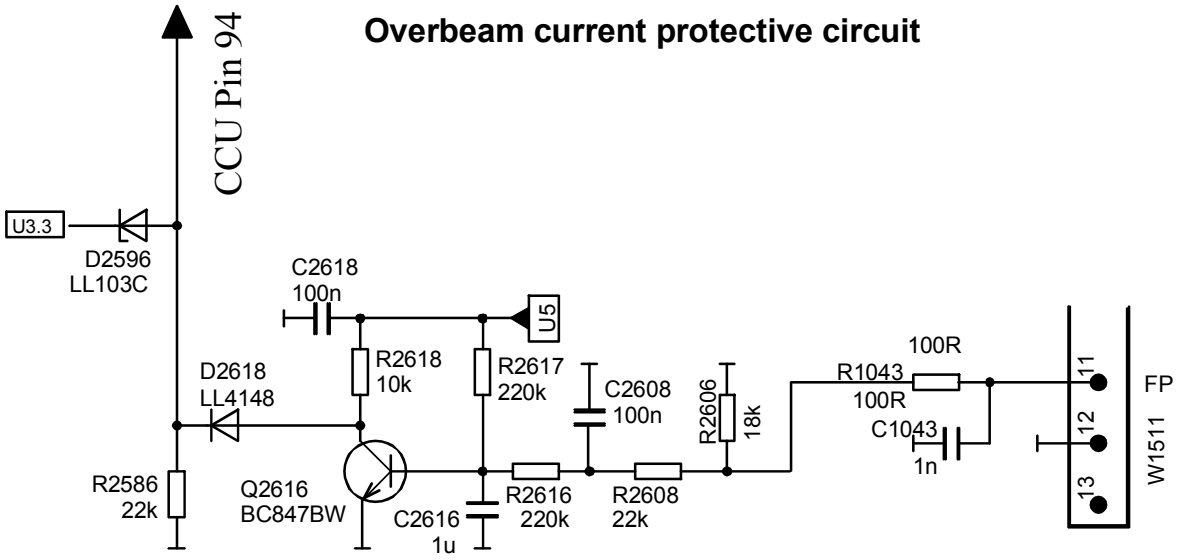
In order for the TDA pin to be at >3.3 V with a beam current of zero, the base of the transformer is connected to U 200 via R 551/552. The positive voltage in this operational state is charged via resistors R 2608, R 2609 and R 2611 of Elko C 2603 and on pin 43 of the TDA there is a voltage of >3.3 V; there is no beam current limitation.

As the high voltage winding in the diode split transformer operates with a virtual earth, the base becomes negative with increasing beam current, whereby C 2603 via R 2608, R 2609 and R 2611 can be correspondingly discharged to a greater or lesser degree and the beam current controlled.

Diodes D 2607 and D 2611 are provided so that the circuit can also react to jumps in beam current. They ensure the rapid discharge of C 2603.

In addition, for a 4:3 display in a 16:9 TV set, from pin 113 of I 2311 via Q 2612 and R 2601, the voltage on C 2603 drops. This corrects the beam current limitation for the smaller screen area. (see also signal board deflection).

Overbeam current protective circuit



2.7.1 Overbeam current fuse

In correct operation the beam current measurement input on pin 43 of TDA is at a d.c. level of 2 to 4 V. According to the level, the RGB output amplifier in this IC is controlled to a greater or lesser extent, which ensures that the beam current limitation is implemented.

If the c.r.t. is controlled upwards to the full extent, even though the gain of the amplifier has been fully reduced , which can occur if there is a fault in the RGB output stage or its

power supply, then the c.r.t. could be damaged if no protective measures are taken.

To prevent this, transistor Q 2616 is connected to the beam current data. In normal operation the transistor conducts and L level is applied to its collector thus making the circuit inoperative.

If the described fault occurs, the base of the diode split transformer becomes negative due to the high beam current, Q 2616 blocks and due to the 5 V on its collector diode D 2618 conducts.

Pin 94 of the CCU is set to H level and switches the device to standby.

2.7.2 HFLB protective circuit

If the line output stage is too strongly overloaded by a fault, the protective circuits discussed cannot respond in any way. Excessive overloading of the H output stage causes the line flyback pulse to reduce in amplitude. The HFLB pulse on pin 10 of W 1511 is therefore monitored by a protective circuit. In normal operation this pulse has an amplitude of approx. 35 V. Via the 20 V zener diode D 2581 this pulse makes Q 2581 conductive in rhythm with the line frequency. Capacitor C 2584 is switched to earth cyclically with the line frequency via Q 581 and cannot therefore charge up. This means that L level is felt on C 2584l. If a fault in the deflection circuit causes HFLB to fall below 20 V, zener diode D 2581 and Q 2581 block. C 2584 charges to H level. This H level is fed via D 2586 to pin 94 of the CCU, which switches the device back to standby operation.

2.8 Speed modulator

The device is also equipped with a speed modulator. It is located between the RGB outputs of the digital unit and the RGB output stages on the c.r.t. board. It controls the speed of the electron beam in the horizontal direction, which increases picture sharpness and prevents a defocusing effect at high contrast on vertical, very bright areas of the picture.

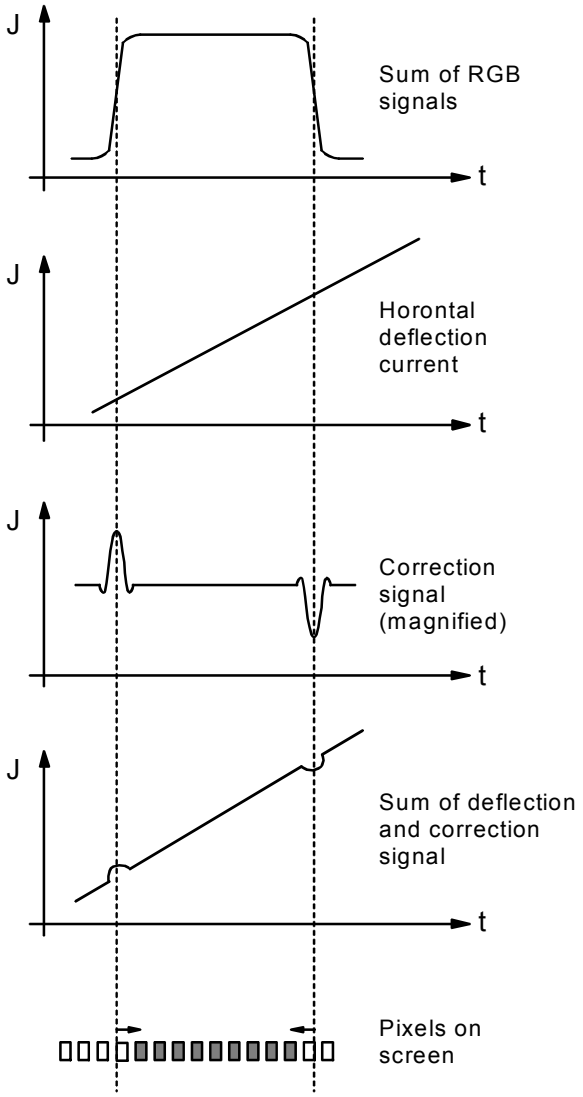
2.8.1 General

The speed modulator evaluates high frequency changes in the picture signal and sends them to an additional winding in the deflector. The resulting magnetic field overlays the normal field produced by the deflection winding. By this method, the deflection speed is adapted to the picture content, which leads to a definite improvement in picture sharpness.

A picture change in a positive or negative direction produces a signal, as shown in the following drawing and thereby supplies the additional winding in the deflector.

The amplitude of the signal and the modulation level of the contrast are therefore dependent on the setting and the slope of the signal change.

One could also modulate the deflection current directly, which would however, be more expensive than the second winding.

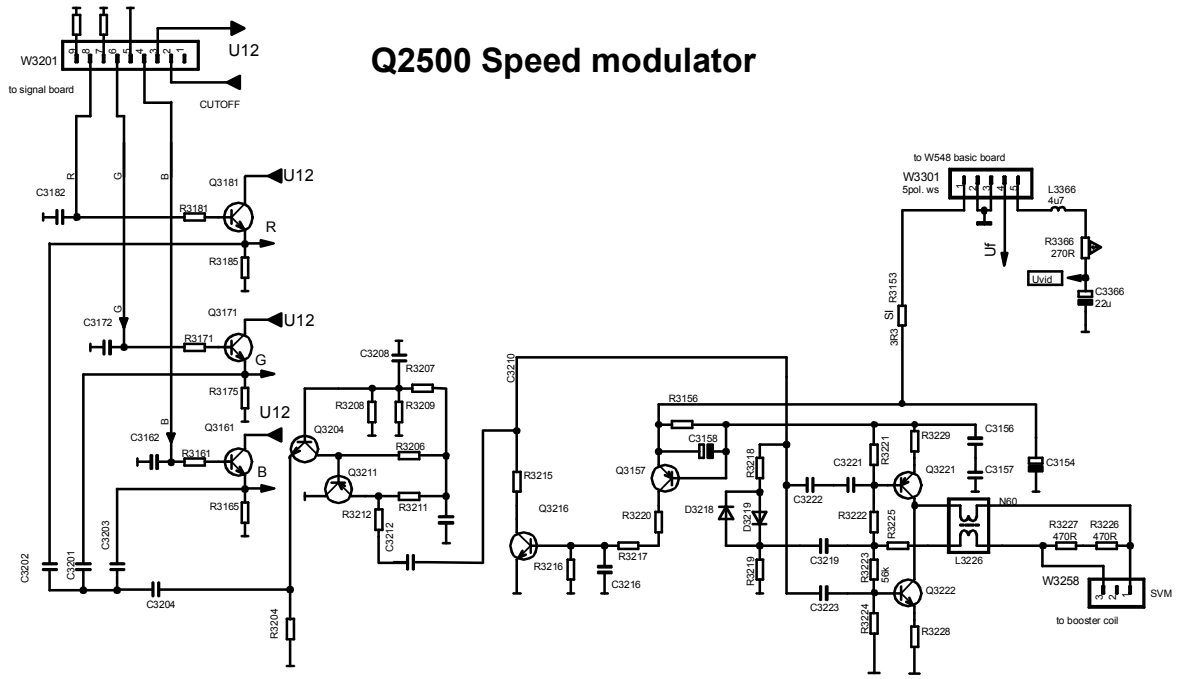


To really understand the operation of the speed modulator we must look at the light characteristics of the pixels on the c.r.t. The longer a pixel is irradiated, the more intensively it shines, and the persistence of the fluorescent image is also longer.

If the signal jumps from dark to light, the deflection is initially accelerated briefly and thereafter remains mainly on one point. In this way the first “bright“ pixel is irradiated for longer and therefore shines more brightly. At the same time the last “dark“ pixel has more time to fade and is irradiated for a shorter time.

If the signal jumps from light to dark, however, this initially causes braking and then deceleration of the deflection in the speed modulator. This means the last “light“ pixel is irradiated longer and therefore shines more brightly. On the other hand, the first “dark“ pixel is irradiated for a shorter period.

In both cases another, simultaneous effect occurs. The signal change occurs while the electron beam, without almost any further deflection, remains on the last “bright“ pixel.



2.8.2 Switching of the speed modulator

The circuit is located on the c.r.t. PCB and is supplied with RGB signals from TDA 9332 via pins 40/41/42.

The RGB signals are applied to connector W 3201 pins 4, 6, 8 at 3 Vss and are then fed via impedance converters Q 3181, Q 3171 and Q 3161. To detect changes in all three colours, the signals are decoupled by capacitors C 3201, C 3202 and C 3203 together. The resulting signal is differentiated with C 3204, R 3204. Control via the RGB signals offers the advantage that this circuit also works with Teletext and OSD operation.

This means that when steep signal changes occur there are only oscillation packages with max. 0.3 Vss on the emitter of transistor Q 3204 for processing.

The input for the circuit of transistor Q 3204 has a low resistance input, so that it can process steep slopes. From the collector the 4 Vss signals are led to the impedance converter Q 3211. This supplies the signal at 6 Vss to the push-pull output stage Q 3221 and Q 3222.

The two transistors are current counter coupled and amplify the signal to a maximum 50 Vss. All voltage data refers to a black/white change and maximum contrast.

Via the voltage dividers R 3221, R 3222, R 3223 and R 3224 one end of the correction coil on pin 1 of W 3258 is set to 30 V.
The two transistors Q 3221 and Q 3222 are blocked without control, so that the other end of the coil is hanging free and no current flows through the coil. Deflection occurs only via the horizontal deflection coil.

For a positive pulse transistor Q 3221 is blocked and Q 3222 conducts. This causes a current to flow via R 3221 and R 3222 through the booster coil and via Q 3222 to earth, which accelerates the deflection.

If, however, a negative pulse is felt, then Q 3221 conducts and Q 3222 is blocked. The

current now flows via Q 3221 through the coil and then on via R 3223 and R 3224 to earth. The reversed direction of current causes the deflection to be arrested.

The deflection coil is controlled directly from the collector connections. Two resistors are connected in parallel to the deflection winding to stabilise the system and using L 3226 in the control lines a throttling of clock faults is achieved.

To prevent overshooting and overloading of the output stages a protective circuit is provided on the PCB. It affects the level of the input signal.

For very steep positive or negative flanks diodes D 3318 and D 319 conduct via C 3319. Positive flanks at the output reduce the input signal via D 3218, as the signal on the output is rotated by 180°. Negative flanks on the output reduce the input signal, as the input signals are directed to earth via D 3319. The circuit specification is such that it does not operate for small signal flanks, thereby ensuring secure operation of the speed modulator over a wide spectrum.

If there is no picture signal, but only noise, the output stages have become overheated. A protective circuit is therefore provided for this case as well.

If the current in the output stages increases, there is a larger voltage drop across current resistor R 3156. The base of Q 3157 goes negative and the transistor conducts. Elko C 3158 ensures that transient, but high currents for steep flanks are possible. Using transistor Q 3157 in conjunction with transistor Q 3216 the input signals of the output phase are reduced and overloading thereby prevented.

As there is a time difference of approx. 80 ns with respect to the RGB signals in the speed modulator circuit up to modulation of the deflection speed, the RGB signal circuit must be retarded by 80 ns after decoupling from the modulator if it is to function correctly. For this reason the 80 ns time lag lines, consisting, for example, of L 3392/3393, C 3392/3398/399 and R 3391/3393 are incorporated into the RGB lines.

2.9 Colour stages

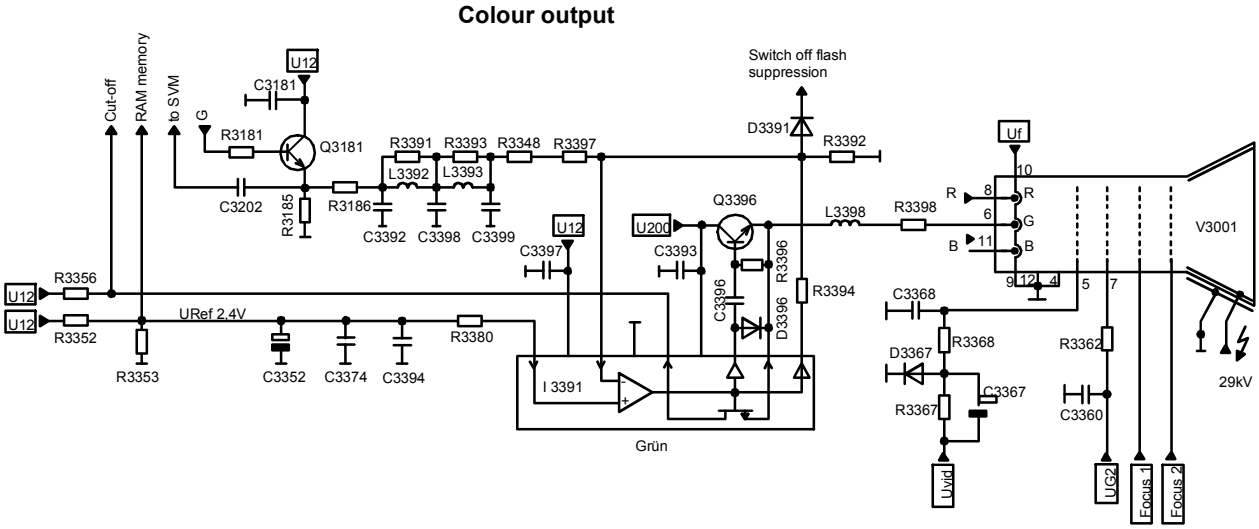
In order to avoid damaging capacitive charges caused by, for example, long cathode wires, which could lead to the frequency response being cut, the RGB output stages have been re-incorporated into the c.r.t. circuit board.

For each colour channel there is an IC whose signal bandwidth of >12 MHz guarantees a high resolution even for rapid signal changes in both directions.

The circuit for the three colour channels is identical. By using ICs the components in the output stages could be reduced to a minimum.

The output stages are energised by the speed modulator with a max. 3 Vss. Via an RC combination the respective signals reach pin 3 of the ICs and are passed on in the IC to the inverting input of an operational amplifier. The non-inverting input and thereby the work point is set via pin 1 of IC .

The resistance between pin 9 and pin 3 provides the negative feedback for determination of the amplification factor.



For control of the c.r.t. cathodes the signals are applied at a maximum 160 Vss via pin 7 and 8. Control is via pin 8 with a corrective signal on pin 7, in order to achieve an automatic blanking current control. The emitter follower on the output of the output stage permits rapid blocking of the cathodes on transition from bright to blank. This permits the delaying effects that are otherwise present to be reduced.

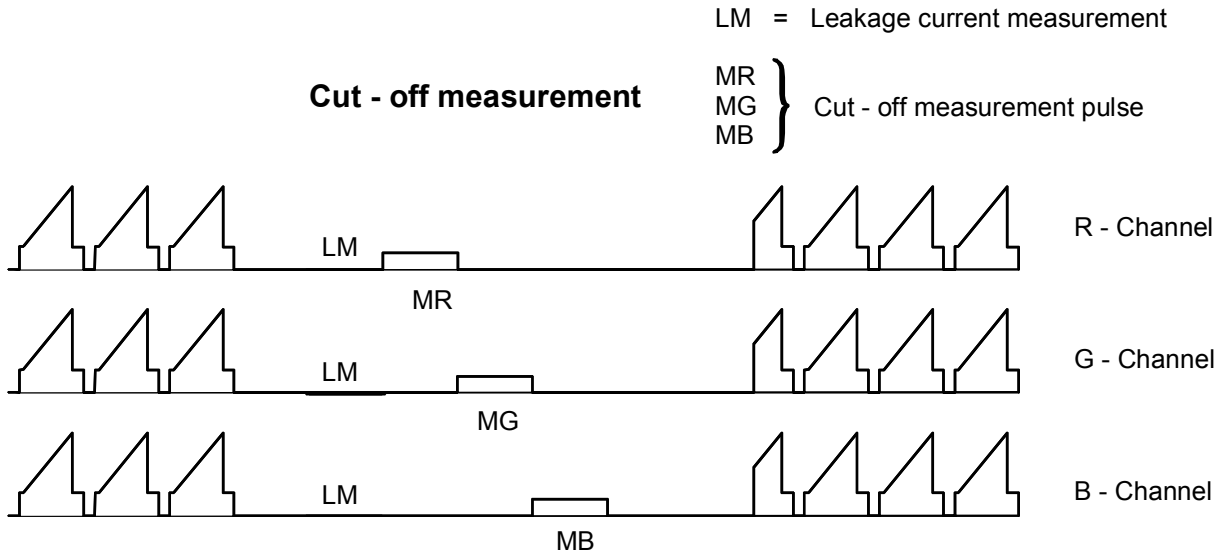
The IC's also contain a component for temperature drift compensation, as well as a circuit via which the transient current can be decoupled. Current information is taken from pin 5, and so with an additional sensor control circuit an automatic blanking value control (cut off control) can be established.

2.9.1 Cut off control

The cut off control is basically a sensor control circuit. It controls electronically dynamic component tolerances and signs of wear, e.g. of the c.r.t.s.

It also has the following advantages:

- automatic blanking value equalisation.
- Avoidance of colour distortion during c.r.t. warm up time and control of above average ageing in the initial operating hours.



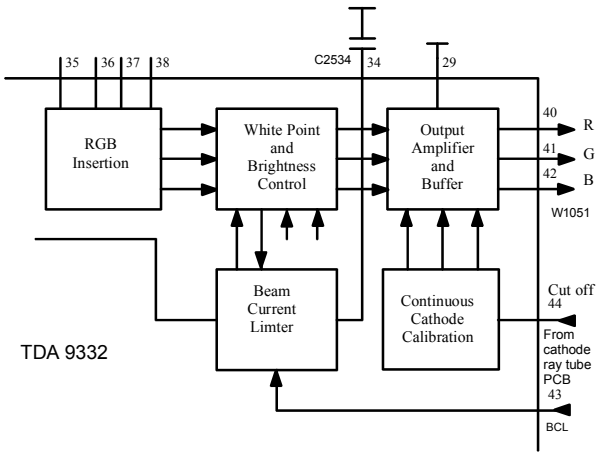
This means that the traditional adjustment controller and the associated adjustment work is no longer required.

Directly after the vertical picture return, measurements are taken of the leakage current of the c.r.t. systems at ultra blank and then, one after the other, the cathode currents of the three systems after input of a specific blank value.

These pulses are fed with the respective RGB signals via the output stages of the c.r.t. systems. From the output stage IC's the respective blank currents of the control circuit in video IC I 2521 on the signal board are supplied via its pin 44.

From a comparison between the established blank current and a reference value, which represents the specified current, a difference is obtained, which controls the cathode current via the video output stages as a controller output. It is dynamically stabilised just above c.r.t. blocking current, up to control tolerances. As small leakage currents in the output stages of the c.r.t.s could lead to distortion of the cut off control, measurement of the leakage current is carried out during the vertical flyback before measurement of the three blanking currents.

Cut - off circuit principle



A consequence of a change to the UG2-voltage is that the cut off control opposes this change. Only a transient effect can be detected on the screen, as long as the control

range of the cut off control is not exceeded. This means an optical comparison of the raster 2 voltage is ruled out. A comparison using a voltmeter is also very unreliable, as the voltage source with approx. 500 MOhm is very resistive.
A comparison of the raster 2 voltage is therefore made in service mode.

2.9.2 Switch off flash suppression

Transistors Q 3341 and 3343 are responsible for suppressing fluorescent flashes on switch off, caused by c.r.t. charges that are not discharged quickly enough via the bleeder in the DST. On start up and during operation they have no function, as the base and emitter of Q 3341 are at the same level it is therefore blocked, as is Q 3343.

On shut down the base of Q 3341 via R 3341 very quickly becomes zero volts. Due to Diode D 3342, that is blocked in the direction of the power supply, Elko C 3342 cannot discharge. Q 3341 switches through and that in C 3342 can switch through via the emitter-collector the output side connected transistor Q 3343. In this way the RGB signals that control the output stage IC's are directed to earth.
Fluorescent image persistence is thus avoided.
Until Elko C 3342 is discharged and the circuit becomes ineffective, the c.r.t. discharges via the bleeder.

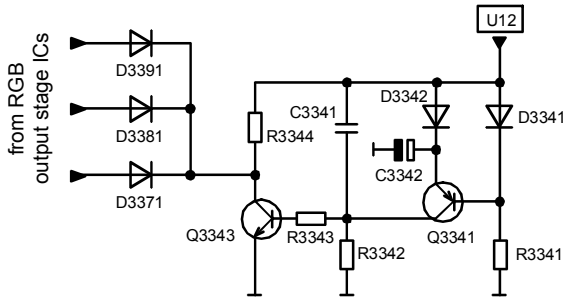
2.10 Rotation panel

2.10.1 Raster correction

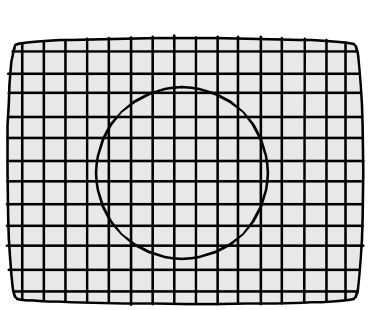
So as the earth's magnetic field affects the colour uniformity of the c.r.t.s, it also influences the picture raster. For a geometrical comparison, a definite alignment towards east ("face to east") is therefore prescribed.

If the device is turned towards another point of the compass, rotation of the picture on the screen occurs according to the type and size of c.r.t. and local characteristics.

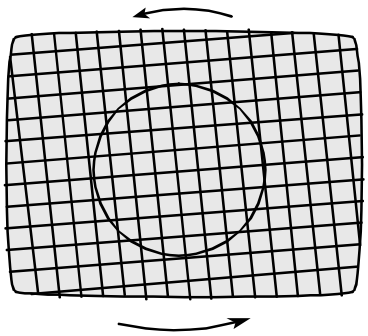
Switch off flash suppression



Raster correction

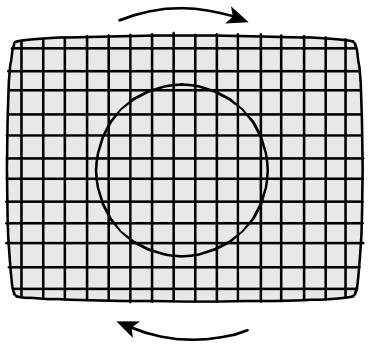


"Face to East" comparison



Raster rotation

"Face to North"



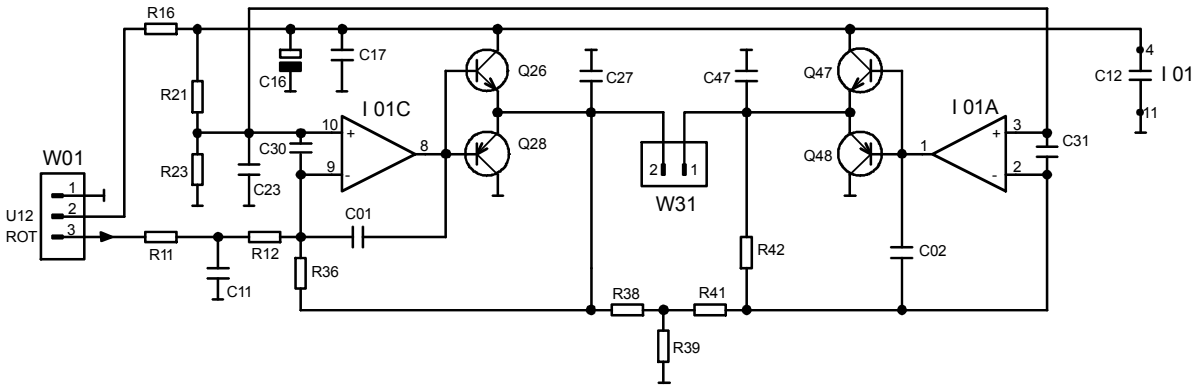
Correction of raster rotation by rotation panel

To compensate for this a rotation panel (raster correction) is incorporated into the 81 cm device with chassis Q 2500. As the effect on the raster is less on smaller and 4:3 tubes the rotation panel is not required.

For the raster correction a circular coil is attached to the cone of the c.r.t. If a uniform current flows through it, the electron beam rotates around its own axis. As the created magnetic field overlays the field of the deflection coils, the picture can be rotated about its central point.

2.10.2 Circuit

For raster correction the DAC on pin 25 of the video/deflection processor TDA 9332 is used. The voltage produced can be adjusted by the user via “rotate picture“ and in service mode. It flows via W 1021, pin 3 to the rotation panel W 1, pin 3.



In this way the inverting input of the operational amplifier on pin 9 of I1C is controlled on the rotation panel. At maximum anticlockwise rotation approximately 3.2 V is applied and at maximum clockwise rotation 3.3 V. The operational point is adjusted on pin 10 by R21 and R23. According to the voltage difference between pin 10 and pin 9 the push-pull stage Q26 and Q28 is controlled. On the base connections there is a voltage of 0.6 to 10.6 V. The output voltage of the push-pull stage is applied to pin 2 of the correction coil and at the same time is fed to the inverting input of operational amplifier I1A via R 38 and R41. This also controls the second push-pull stage Q 48/Q 47. The two OPVs and push-pull stages counteract each other. This means that a current can flow to earth via Q 26, through the correction coil (from pin 2 to pin 1 on W31) and via Q48. On pin 8 of the OPV there is a voltage of 10.6V at maximum clockwise rotation and on the other output pin 1, 0.6 V. Otherwise the current flows via Q 47 through the correction coil (in this case from pin 1 to pin 2 on W 31) and via Q28 to earth.

In this way the current can be adapted to the required correction with respect to direction and size. This correction can, however, also act in reverse, if the coil is rotated on the deflector.

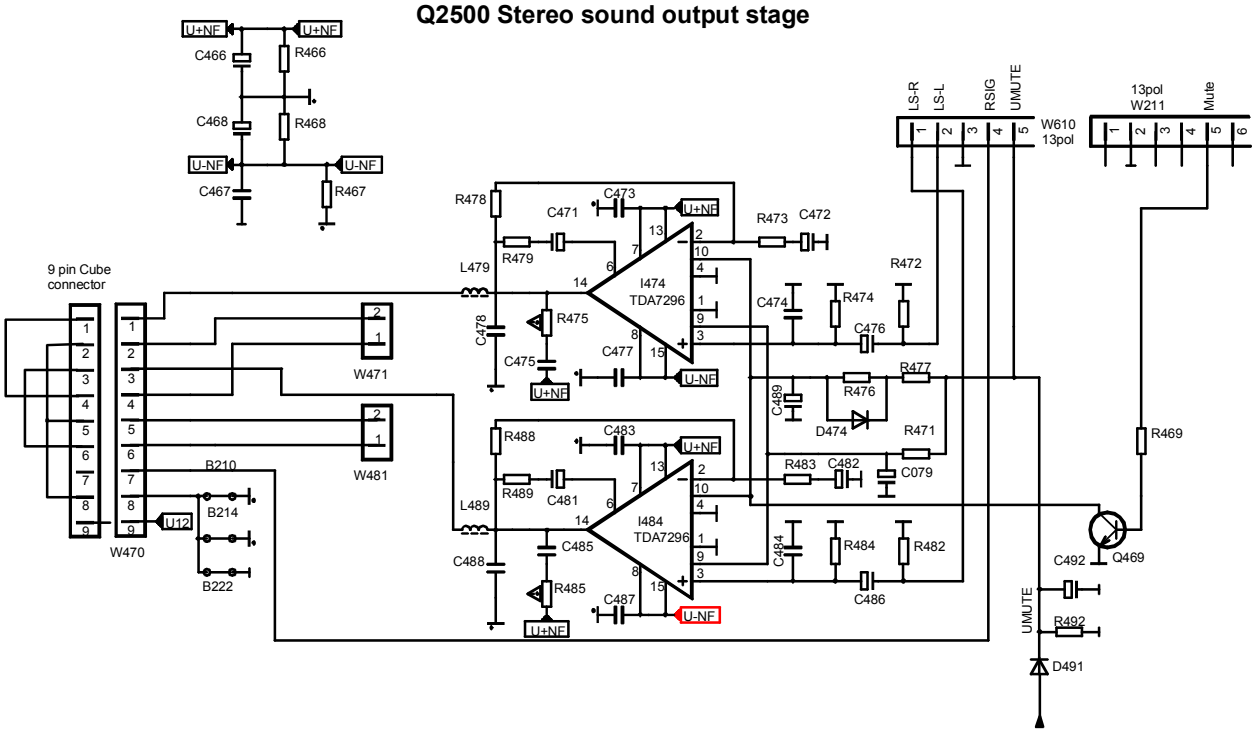
The control electronics for the rotation coil is fixed firmly to the Q 2500 chassis. However, the rotation coil and control electronics should be considered as a unit. In the event of a fault the coil is then changed as a complete unit.

2.11 NF output stages

The two amplitude controlled VF signals are output from pins 56 and 57 of MSP 3411 on the signal board. The signals are applied to the base of transistors Q2081/2083. The transistors are switched as impedance converters to prevent, as far as possible, the coupling of interference pulses on the VF wires between MSP and the output ICs.

The VF signals reach the two output stages via the coupling capacitors C 2082/476. In between are the two mute transistors Q 1586/88. (See signal board).

Q2500 Stereo sound output stage



The output stages are implemented easily as all control processors (volume, tone, balance) as well as base width switching are processed in the MSP.

Compared to previous models the Q 2500 has new output stages. TDA 7296 is equipped with an internal mute function that removes any residual on and off switching interference that is not fully suppressed by the additional mute switching.

The internal mute switching is controlled on pins 9/10. If the voltage on the pins is <3 V, then the output stages is muted. These two pins are controlled via R/C combinations via UMUTE. On start-up the two capacitors C 479/C 489 are charged slowly via the load resistors R 471/R 476 and R 477. The mute function in the IC is achieved via a voltage differential on pin 9 and pin 10. As long as pin 9 is more positive than pin 10, then the output of IC internal is muted. This is achieved on start-up/ shutdown by the R/C combination with various time constants.

On start-up C 479/22 µF is very quickly charged up by R 471/22 k. For C 489/22 µF charging occurs more slowly via R 477/10 k and R 4476/33 k. This means that in the charging phase pin 9 is more positive with respect to pin 10. On shut down C 489 discharges rapidly via D 474 (which releases R 476) and R 477. Pin 9 is again more positive with respect to pin 10 and mute is implemented again internally.

TDA 7296 can be considered to be an operational amplifier. It is controlled by its non-inverting input pin 3. The amplification is calculated from the negative feedback combination R 478/473.
This results in

$$V = 1 + \frac{R\ 478}{R\ 473} = 1 + \frac{22\ k}{0.68\ k} = 33$$

The amplified signal is felt on pin 14 and for the left channel is fed to the loudspeakers via L 479.

The R 479/C 471 combination is necessary for an internal bootstrap. In addition, the output phase is equipped with an overload and temperature protection circuit.

The two output stages are supplied with voltage symmetrically. It is taken from the transformer at zero potential and rectified and smoothed by D 686/687 and C 687. With the help of the R/C combination 466 and 468 it is split into +/- 18 V (see also power supply).

This measure achieves a halving of the peak current by the rectifier diodes D 686/687 and a higher undistorted output performance, especially for low frequencies.
An output stage without any electrolytic capacitors contributes to this.

3 Receiver components

3.1 HF/IF unit

Four receive components can be used in devices with Q 2500 chassis. One is the terrestrial tuner, or HF/IF component, which processes frequencies from 47 MHz to 860 MHz. This hyperband tuner is located on the basic board.

Second is the single SAT or dual SAT receiver for the first IF from 950 MHz to 2150 MHz. This is partly a standard feature or can be retrofitted for certain sets.

In addition, for full IP sets a PIP-HF/IF unit for the reception of terrestrial signals is incorporated into the hyperband range. In this case, however, the audio band is dispensed with, as picture for picture only video signals are required. This is also built into the basic board.

With this equipment the set is able to process all television signals, irrespective of whether they are received by terrestrial antennae or via cable units, and even when derived from parabolic antennae.

3.1.1 HF/IF components

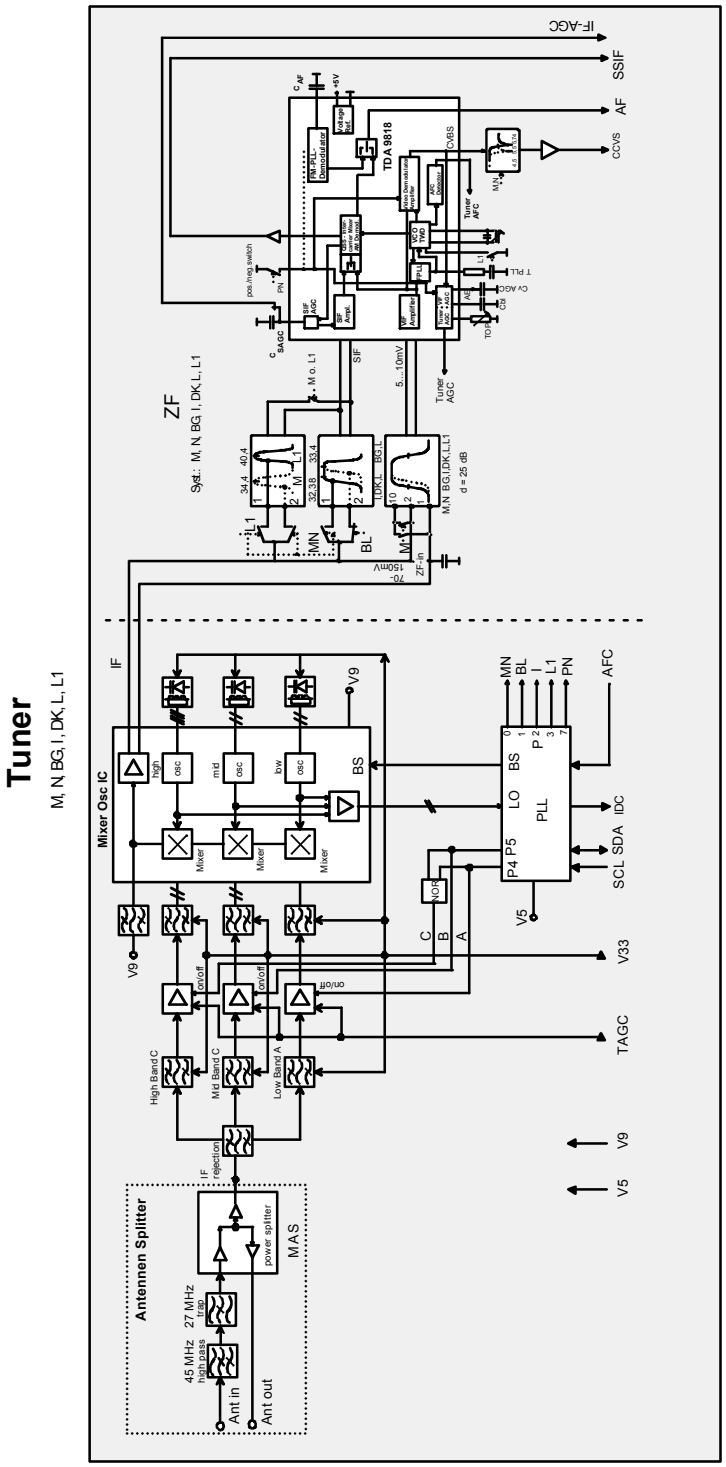
A HF/IF combination is also used. All functions for current European television standards are located in one housing, with two provisos. The IF consists of only one picture IF. The audio demodulation takes place in the audio IC on the signal board. From the IF component only the sound IF is supplied as broadband.

This means that the ceramic transducer and an expensive sound/IF switch are not required. Secondly, for lower price models not destined for export HF-IF, designed only for PAL and SECAM BG, is used. In this case, the change-over to SECAM L and NTSC and the components necessary for this are not required.

This means the two designs are hardware and software compatible.

The following block circuit diagram shows the multi-standard design. Some of the components are not fitted to the BG version.

As in earlier models, the electronics is housed in an HF proof folding housing.

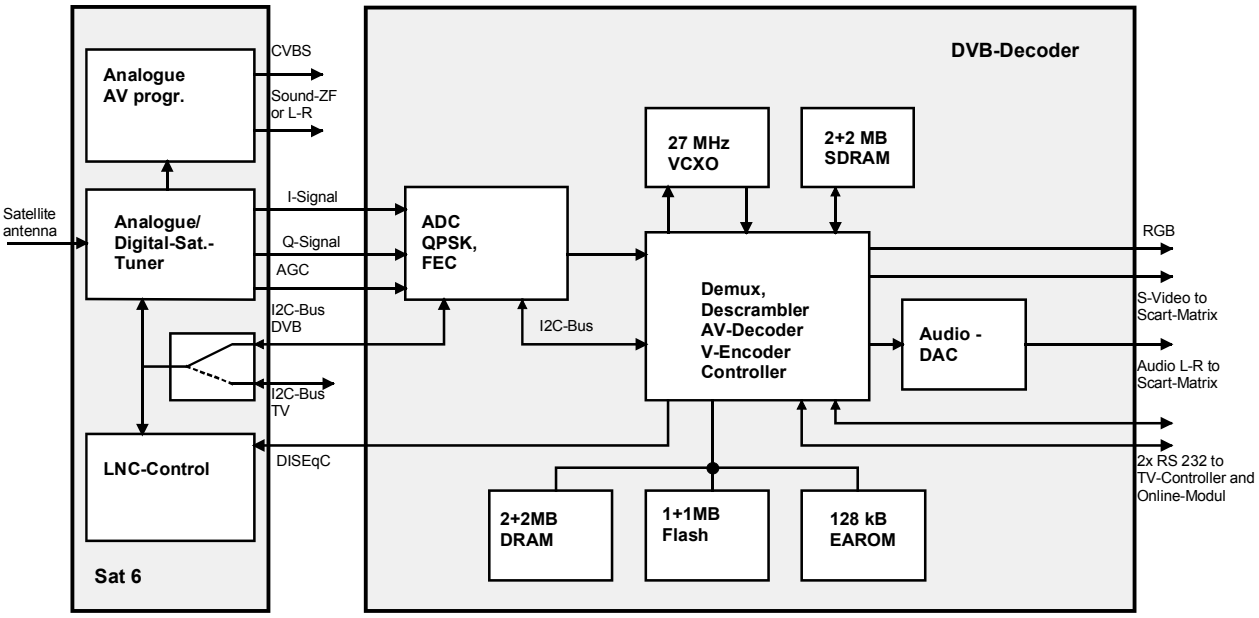

Tuner
M, N, BG, I, DK, L, L1
IF-AGC
SSIF
AF
CCVS
TDA 9818
ZF
Syst.: M, N, BG, I, DK, L, L1
SIF
Tuner AGC
Mixer Osc IC
IF
V9
BS
MN
BL
I
L1
PN
AFC
PLL
LO
P5
P4
SCL
SDA
IDC
V5
V33
TAGC
NOR
A
B
C
high
mid
low
osc
Mixer
on/off
High Band C
Mid Band C
Low Band A
IF rejection
Antennen Splitter
power splitter
MAS
45 MHz high pass
27 MHz low pass
Ant in
Ant out

3.2 DVB Board

3.2.1 Overview

The DVB decoder is able to convert DVB signals that are transmitted free to air via satellite into the appropriate analogue audio and video signals, which are then fed to the signal processing of the TV chassis.

For the conversion of the L band signal derived from LNC or a multiswitch, the combituner of the satellite unit Sat 6 is designed as an assembly set or retrofit set for the Q 2500 chassis. It also supports the interface to an integrated online module.



The following block diagram shows the principal architecture of the Sat 6 and DVB decoder. The interface between Sat 6 and the DVB decoder is formed from quasi-analogue I and Q signals, the AGC signal, the IIC bus and a port used for DISEqC. The IQ signals are derived in the satellite tuner by quadrature mixing of the second IF (479.5 MHz) in the base band. The AGC signal provides amplitude control of the IQ outputs of the tuner. As the Sat 6 unit is able to process analogue and digital signals, both the DVB controller and the TV controller have access to the tuner and the LNC supply. The switching of the IIC buses used for this is achieved by the TV controller driven by the Sat 6 unit.

The processing of DVB signals from the tuner base band interface to the analogue output is achieved by two high integration chips. The first is the front-end component STV0299B (ST microelectronics) that digitises the IQ signals coming from the tuner by means of dual ADCs, demodulates them (carrier and pulse extraction) and carries out Forward Error Correction. The second component is the MPEG-2 demultiplexer-, decoder-, backend- and controller chip STi5500 (ST Microelectronics), which demultiplexes the MPEG-2 transport beam, feeds the selected audio and video components to the MPEG-2 decoder for decompression, decodes them and then converts them into analogue output signals. The STi5500 also has an integrated 32-bit RISC

controller that forms the core of an independent processor subsystem. It is responsible for the control and diagnosis of the other functional units of the DVB decoder module. Commands and data are exchanged via a serial interface to the TV controller. In addition, the DVB is responsible for applications such as the Electronic Program Guide for DVB programmes. In this case the on screen display from the OSD component of the MPEG-2 video decoder is produced. For communication between the TV controller and the controller of the online modules, the data is transferred transparently between the two serial interfaces.

3.3.1 DVB internal features

3.3 Features and parameters

Feature	*Standard/value range*	*Notes*
General		
Receiving and decoding of DVB compatible free to air signals via satellite		
Implementation as integrated module for incorporation or retrofitting in Q 2500	Q2500 basic, medium, high end	
Operational control integrated into the Personal Control System		
Electronic Programme Guide based on standard DVB-SI		
Pre-programming	ASTRA 19.2° East and Eutelsat 13° East	
MPEG-2 main Profile@Main level	720x576 Pixel, 25 Hz	
Support for 4:3 and 16:9 source format (letterbox filtering) and 4:3 display format (16:9 display format by scaling in TV up converter)		Pan&Scan is not used
Teletext processing to DVB teletext standard	ETS 300 472, s. [5]	Reinsertion in the Y signal
Support for DVB radio programmes		

Feature	*Standard/ value range*	*Notes*
Satellite front end		
Demodulation and channel decoding to DVB satellite standard		
Use of the combituners (analogue/digital) of the Sat-6 satellite unit		
Input level area	45...80 dBμV	to 75 Ohm
Input frequency level	950...2150 MHz	
Input socket	F female, 75 Ohm	
IF wideband	36 MHz	-3 dB
Demodulation	QPSK	
Demodulation	QPSK	
Symbol rate	15...30 Mbaud	1...30 Mbaud adjustable 15...30 Mbaud guaranteed
Forward Error Correction	Viterbi, De-interleaving and Reed Solomon	
Use of the LNC voltage generation of the Sat 6 satellite unit or an optional switch fitted directly on the DVB module		
Option for antenna control	13/18 V, 0/22 kHz, DiSEqC Tone Burst, DiSEqC 1.1(partial)	
LNC current	400 mA	

Feature	*Standard/ value range*	*Notes*
Audio/video backend		
Interfaces to chassis	FBAS/audio input (SAT6), RGB output, S video/FBAS output, audio output (Stereo)	
Controller and graphics		
Controller	32 bit RISC controller, 50 MHz clock	
Working memory	4 Mbyte DRAM, 2 Mbyte Flash ROM	
MPEG and video memory	4 Mbyte SDRAM	
Graphics	Internal OSD with 720x576 pixel resolution; to 8 bit/pixel, 4 bit/pixel used	
OSD comparison in service mode (background brightness)	Y_nominal+/-6 levels	

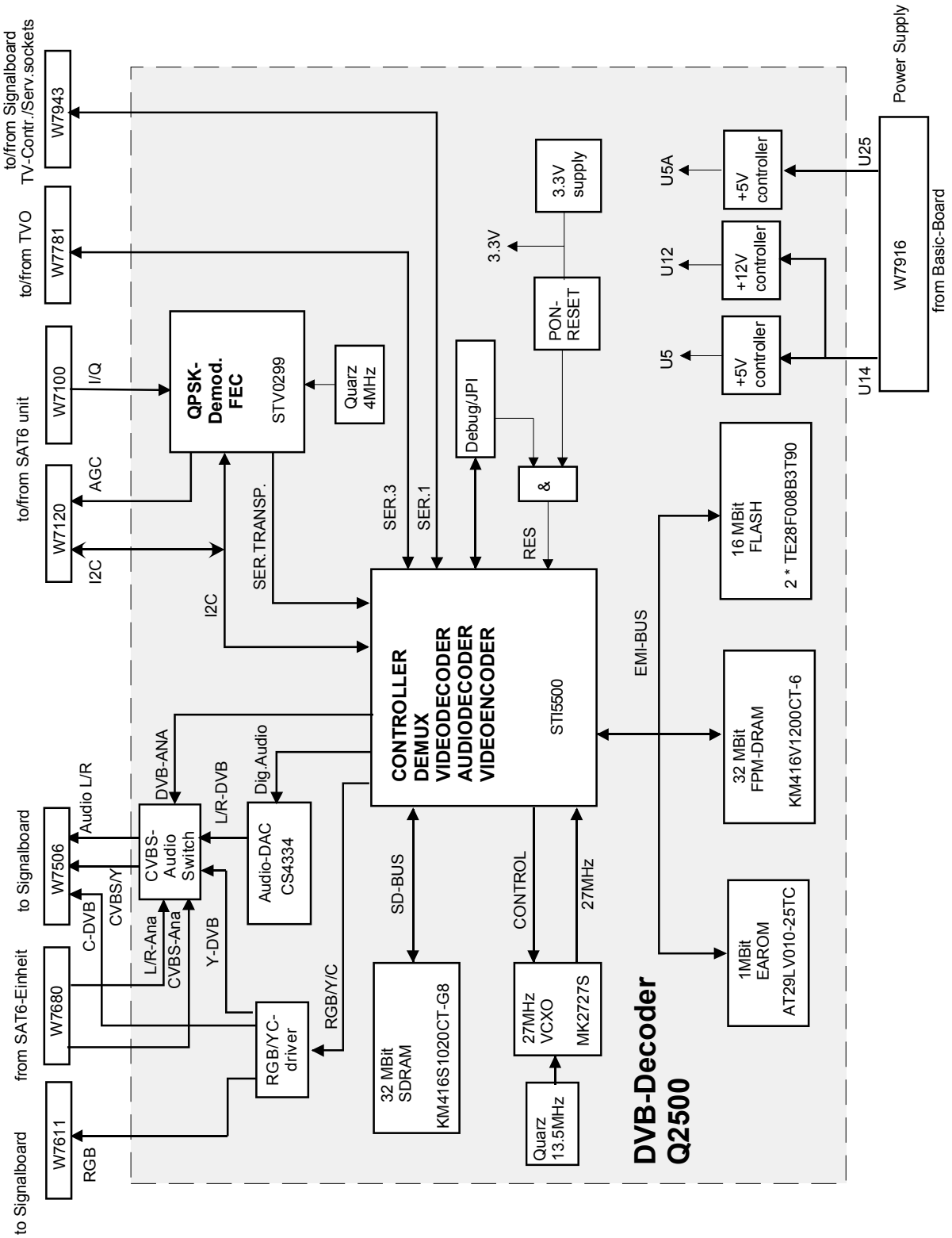
Feature	*Standard/value range*	*Notes*
Software		
Local update of operating software	DVB module: via service socket (RS232-Interface, 5 V)	
Generation and update of programme list via various options: pre-programming, frequency search procedure, semi-automatic programme search (manual setting of carrier currents and automatic search for carrier current levels)		
Separate search procedure for DVB television and radio programmes		
Automatic setup of audio channels (default: configuration in menu language) and display of options (menu tree: sound/voice)		
Programme information: Decoding and display of Present_Event and Following_Event via DVB-SI and Teletext		
Generation of an SI database for freely selectable preferred programmes		
With Next-View harmonised Loewe Digital EPG		
Separate Radio EPG		
Detection of encrypted programmes		
Detection of inconsistent data, robust reaction and generation of messages on fault detection		
DVB Service Mode for comparison (VCXO), diagnostics (Test picture) and deletion of DVB-EAROMs		

3.3.2 DVB/TV features

Feature	*Standard/Value range*	*Notes*
PIP: DVB in TV or VGA, TV in DVB		Satellite: 2 independent leads and Sat 6 twin fitting necessary!
Automatic picture format switching		
Creation of a common programme list with analogue and digital programmes with special recognition of the digital programmes	„D“	
Separate radio mode with radio programme list		

3.3.3 Architecture

The following block diagram shows the architecture of the DVB decoder for Q 2500.


DVB-Decoder
Q2500
CONTROLLER
DEMUX
VIDEODECODER
AUDIODECODER
VIDEOENCODER
STi5500
QPSK-
Demod.
FEC
STV0299
Quarz
4MHz
Debug/JPI
PON-
RESET
3.3V
supply
3.3V
&
RES
SER.3
SER.1
SER.TRANSP.
I2C
I2C
AGC
I/Q
EMI-BUS
SD-BUS
CONTROL
27MHz
16 MBit
FLASH
2 * TE28F008B3T90
32 MBit
FPM-DRAM
KM416V1200CT-6
1MBit
EAROM
AT29LV010-25TC
32 MBit
SDRAM
KM416S1020CT-G8
27MHz
VCXO
MK2727S
Quarz
13.5MHz
+5V
controller
+12V
controller
+5V
controller
U5A
U12
U5
U25
U14
Power Supply
W7916
from Basic-Board
W7943
W7781
W7100
W7120
W7680
W7611
W7506
to/from Signalboard
TV-Contr./Serv.sockets
to/from TVO
to/from SAT6 unit
from SAT6-Einheit
to Signalboard
to Signalboard
DVB-ANA
L/R-DVB
Dig.Audio
Audio L/R
CVBS-
Audio
Switch
Audio-DAC
CS4334
CVBS/Y
C-DVB
L/R-Ana
CVBS-Ana
Y-DVB
RGB/Y/C
RGB/YC-
driver
RGB

3.4 Components

3.4.1 Satellite front end

3.4.2 Functional distribution

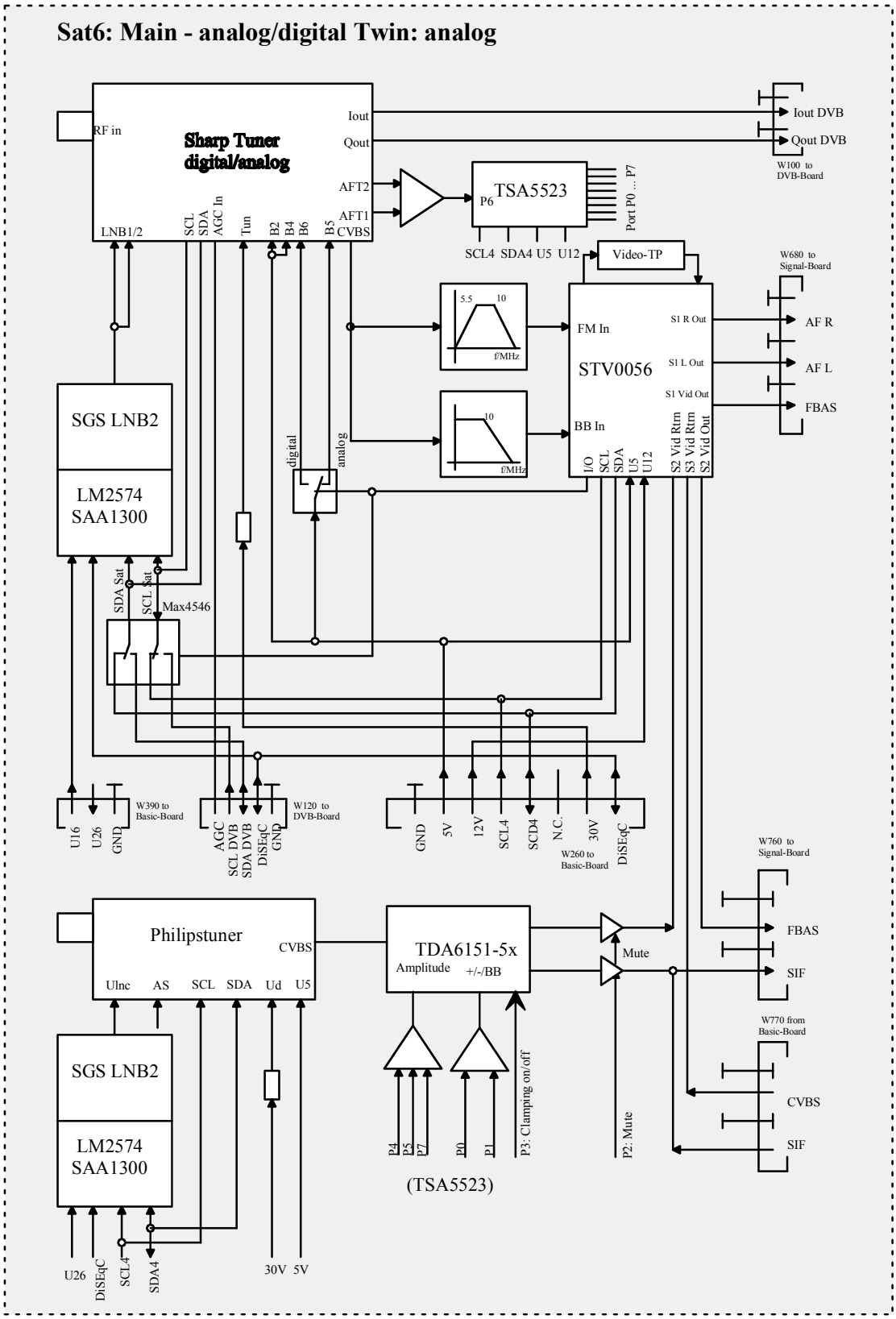
The satellite front-end processes the signal of the 1. satellite IF coming from the Universal-LNC or Multiswitch up to the MPEG-2 carrier current, fed to the MPEG-2 demultiplexer/decoder. It also houses the components for the supply and control of the antenna units. The functions mentioned are distributed to blocks of the Sat 6 (Tuner, LNC supply) unit DVB decoder (AD conversion, demodulation, forward error correction). The separation is implemented via an analogue/digital satellite tuner in order to be able to use redundancy free processing of TV and DVB signals. The reasons for the choice of interfaces are:

Fewer requirements for the screening of the Sat 6 unit and low-interference quasi-analogue baseband interface to DVB decoder.

Due to the functional unity, the relevant parameters for DVB reception of the Sat 6 unit are specified in the following.

3.4.3 Tuner

The tuner converts the signal of the 1. satellite IF in the base band. Signal processing for analogue and DVB signals is distinguished only in respect of demodulation, and is therefore almost identical with respect to the prefiltering and amplification stages, mixing on the 2. IF, channel selection and amplification. For this the implementation of an analogue/digital combi-tuner is advised.
The Sat 6 unit incorporates the BS2W7VG2002 (Sharp) analogue/digital satellite tuner


Sat6: Main - analog/digital Twin: analog
RF in
Sharp Tuner digital/analog
Iout
Qout
AFT2
AFT1
CVBS
LNB1/2
SCL
SDA
AGC In
Tun
B2
B4
B6
B5
Iout DVB
Qout DVB
W100 to DVB-Board
TSA5523
P6
Port P0 ... P7
SCL4 SDA4 U5 U12
Video-TP
W680 to Signal-Board
5.5
10
f/MHz
FM In
STV0056
BB In
S1 R Out
S1 L Out
S1 Vid Out
AF R
AF L
FBAS
I/O
SCL
SDA
U5
U12
S2 Vid Rtrn
S3 Vid Rtrn
S2 Vid Out
SGS LNB2
LM2574
SAA1300
digital
analog
SDA Sat
SCL Sat
Max4546
U16
U26
GND
W390 to Basic-Board
AGC
SCL DVB
SDA DVB
DiSEqC
GND
W120 to DVB-Board
GND
5V
12V
SCL4
SCD4
N.C.
30V
DiSEqC
W260 to Basic-Board
W760 to Signal-Board
FBAS
SIF
Philipstuner
CVBS
Ulnc
AS
SCL
SDA
Ud
U5
TDA6151-5x
Amplitude
+/-/BB
Mute
W770 from Basic-Board
CVBS
SIF
SGS LNB2
LM2574
SAA1300
P4
P5
P7
P0
P1
P3: Clamping on/off
P2: Mute
(TSA5523)
U26
DiSEqC
SCL4
SDA4
30V
5V

3.4.4 DVB demodulation and fault correction

Additional signal processing comprises:

- AD conversion of the quadrature signals from the tuner,
- QPSK demodulation and channel decoding in the form of Forward Error Correction.

Demodulation and channel decoding are compatible with ETS 300 421. In practice an in-house chip solution is used for all three functions. For reasons of interface compatibility with the MPEG decoder, the STV0299B module from ST Microelectronics is used. There then follows specification of the practical implementation, as well as parameters, which in ETS 300421 are only partially set.

Parameter	Value/algorithm	Notes
Chip	STV0299B	Manufacturer: ST Microelectronics
ADC		
ADC-Type	Dual	
Resolution	2*6 bit	
Sampling Clock	Variable, dependent on symbol rate	Generated by on chip PLL
IQ input voltage	1 Vss	
Demodulation		
Procedure	Coherent grey coded QPSK demodulation	
Symbol rate range STV0299B	1...45 Mbaud	
Symbol rate over all (including tuner) without neighbouring channel assignment	1...30 Mbaud	Lower limit: Phase noise of tuner Upper limit: IF bandwidth of tuner
Symbol rate over all with neighbouring channel assignment	15...30 Mbaud	
Preferred value for symbol rate	27.5 and 22 Mbaud	Used in frequency search procedure
Other symbol rates	Decoding from NIT (delivery system descriptor) of Barker Channel or manual selection	
Roll off filtering	Half Nyquist	
Roll off factor	0.20 (20 %); 0.35 (0.35 %)	
Used roll off factor	0.35 (35 %)	
Carrier recovery	Digital PLL with internal de-rotator and hardware lock-in detector	
Pulse recovery	Internal digital PLL	
Processing of the normal or inverting spectrum		

Parameter	Value/algorithm	Notes
Chip	STV0299B	Manufacturer: ST Microelectronics
AGC	AGC analogue/digital tuner with PWM output. Internal digital AGC on power optimisation within the signal bandwidth.	
AFC	digital software AFC	
Forward Error Correction (FEC)		
1. FEC stage	Viterbi decoder	
- Constraint length	7	
- Rate	½	
- Other code rates	½, 2/3, ¾, 5/6, 7/8	
- Rate selection	Automatic or manual	
2. De-interleaver		
- Synchronous word extraction		
- Convolutional interleaver		
- Depth	12	
3. Reed Solomon Decoder		
- Number of parity bytes	12	
- Block length	204	
- Correctable byte error	8	
- Energy dispersal de-scrambler		
Other		
- Carrier current output	Parallel or serial	
- Used mode for output	Serial	
- Control	IIC bus	
- On Chip Error Monitoring		

3.4.5 LNC supply

The components for LNC supply located on the Sat 6 unit or optionally on the DVB module. The control of the circuit on Sat 6 is by DVB operation via the IIC bus and a free port (DISEqCWR) of the DVB decoder/ controller chip STi5500. In TV operation the TV controller assumes control of the Sat 6 unit. This achieves better decoupling of the software module.

Parameter	Value	Note
LNC voltages	0/14/18 V	
LNC current	max. 400 mA	
Current limitation	Electronic	
22 kHz signal	yes (modular)	
Amplitude pf 22 kHz signal	1 Vss	
Duty cycle	(50 +/- 10) %	
DISEqC version	1.0 and partially 1.1	Write only

4 Signal board

Mounted on the signal board, which is linked to the basic board via connectors, are all the necessary building blocks for device control, interface switching, video, audio and videotext processing.

These are:

- The device control with computer circuit, operating software and the EAROM for the storing of system data and customer specific calibration values.
- Production of system cycle frequency necessary for a digital design.
- The digital IC's necessary for picture signal processing.
- The video/deflection processor for the production and synchronization of control pulses.
- Digital audio processing for analogue transferred information and NICAM decoding.
- The teletext decoder, integrated into the SDA 6000, with page memory, in which up to 3000 text pages, according to design, can be saved and which also generates the OSD for the user control.
- The signal and interface selection by corresponding IC's controllable via the I²C bus.
- Optional IC's for video processing, picture in picture.

4.1 Device control

Full device control is implemented by a Siemens 16 bit processor (SDA 6000) together with Loewe operating software. The teletext function is also integrated into the SDA 6000. A standalone teletext processor is therefore not necessary.

All processes in the digital signal preparation, in the tuners and interface selection are checked and controlled via a microcomputer integrated into the SDA 6000. The processor is also known as the CCU (Central Control Unit).

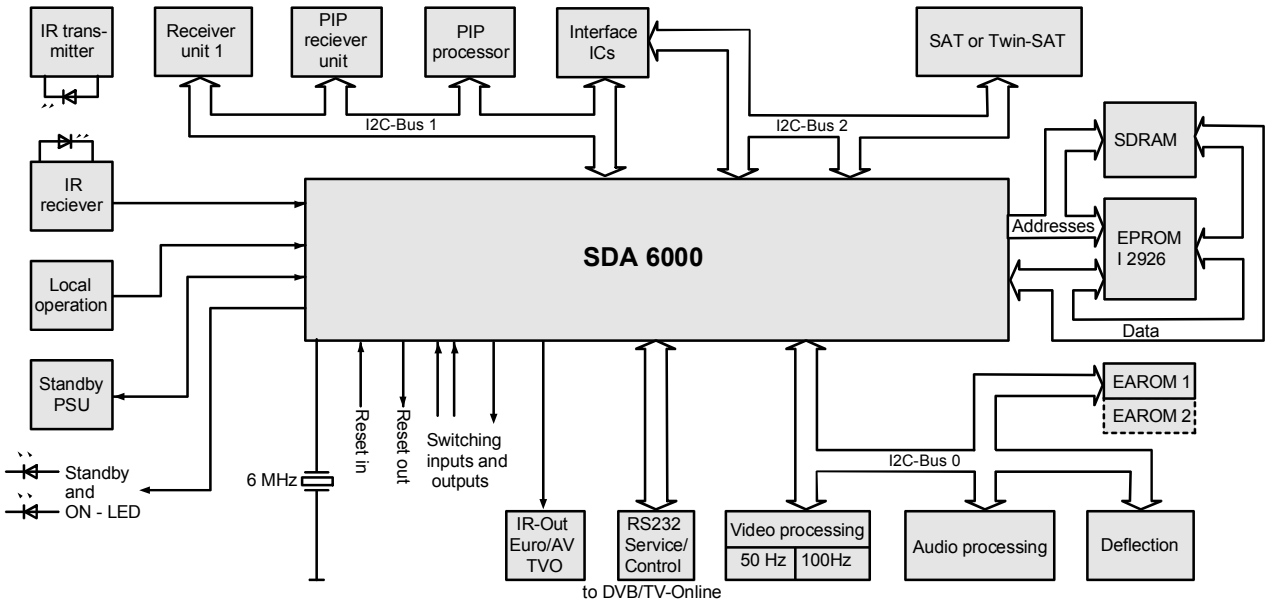
It also supports the operating, tuning and storage system on the frequency synthesis principle. Without the DVB module there are 220 programme storage locations, and with the DVB board there are 1470. The programme locations are available for TV and also for radio operation. The total number of stored programs must not exceed 220 (1470). For the AV inputs six additional places are reserved.
Operating software is held in an external EPROM. For the storage of c.r.t. and system specific data there is an EAROM for device control. The latter also contains programme location information.

All three modules, CCU, EPROM and EAROM are mounted on the signal board.

The remote maintenance sensor permits control of possible device functions. The chassis tuning is also carried out by remote maintenance.

For this, the sensor IC generates a serial data word for each command that is transferred to the receiver with a delay. This signal is demodulated by the IR receiver and prepared in such a way that it can be sent directly to the CCU as an RSIG signal.
The CCU detects the local operating commands on a line by the different voltage levels.

Block diagram - Device control



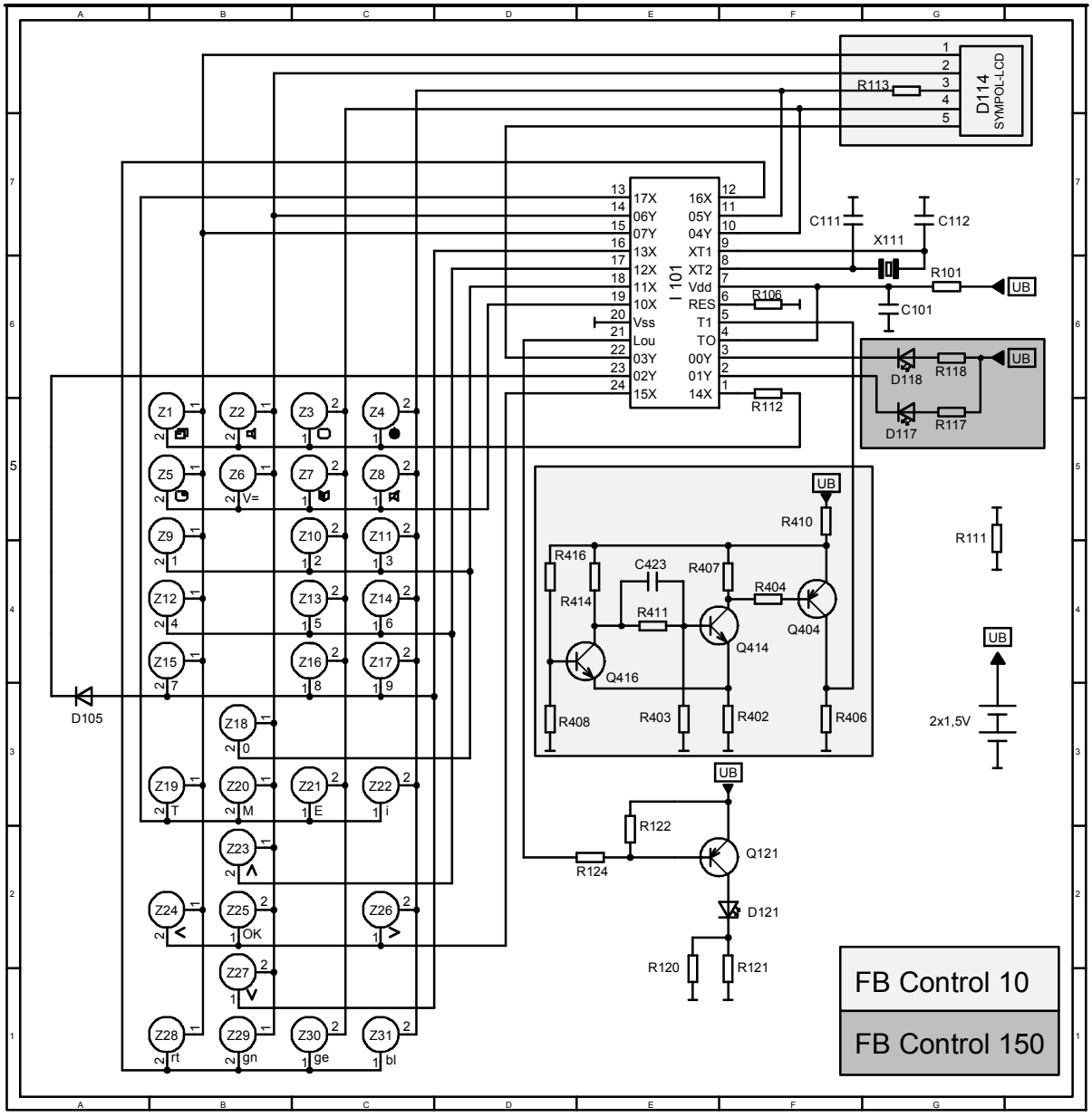
The CCU operates as a central control and information module. The software is held in as external EPROM. It concerns data necessary for the control of the digital IC's, tuning, OSD's etc.

For control of all processes in the device the C 161 bus system:

- generates I²C bus 0
  transmits data to and from the EAROM. In addition it controls the picture and audio signal processing.

- generates I²C bus1
  controls the 1st and 2nd receiver unit on the basic board, the switching IC's for the audio and video signals on the signal board and the optional PIP processor.

- generates I²C bus 2
  controls the satellite units and partially controls the switching IC´s for audio and video.



4.1.1 The infrared sensor

With the state-of-the-art IR transmitter all device functions, with a few exceptions, can be controlled remotely. Starting with on/off via control functions such as volume/contrast, to control of the satellite antenna.

To ensure remote control of all functions, buttons must have double or extended switching functionality.

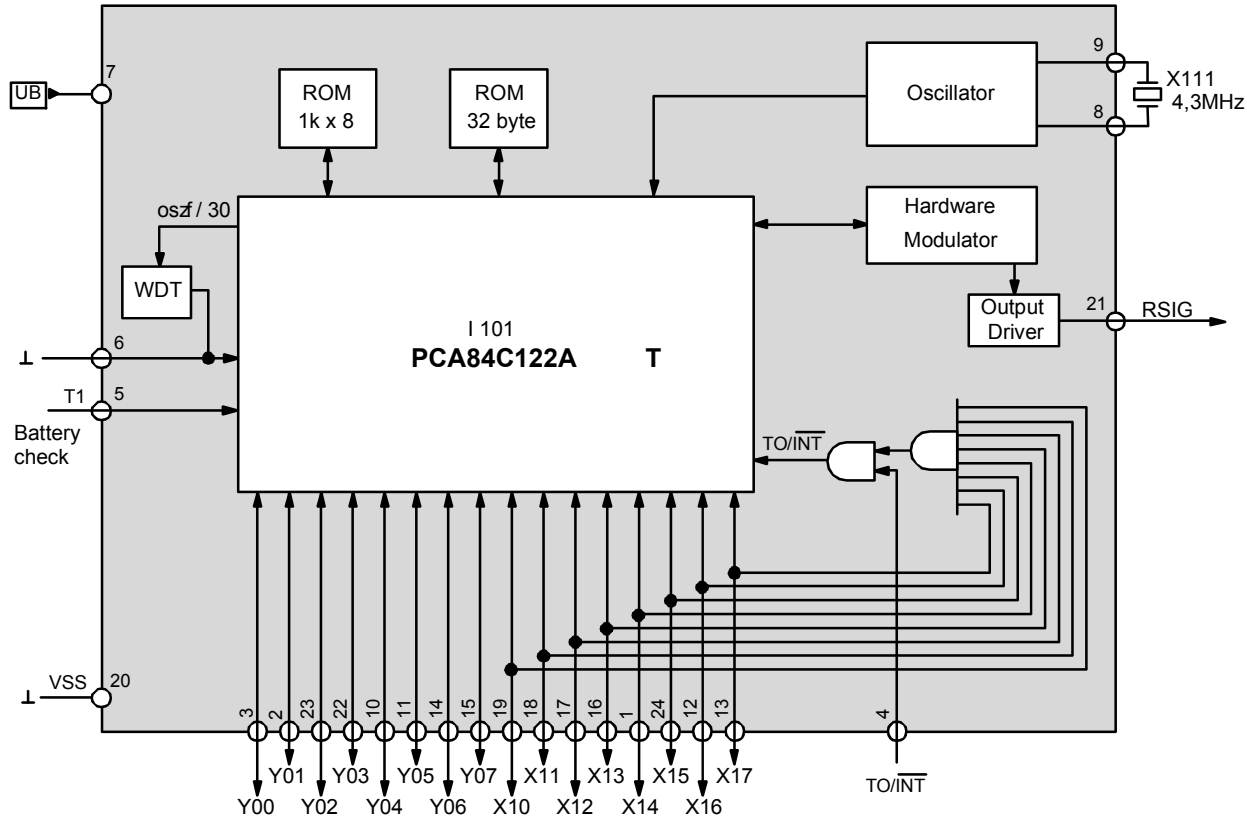
Operation is via a well-organised menu structure. For this a cursor cross is provided on the remote control. In addition, frequently used functions can be assigned to the four colour keys. This does not set the command in the remote control, but a corresponding value in the device software. In the high-quality system

range device the various functions are supported by an LCD display.

An 84 C 122 Philips microprocessor is used in the remote control for the Q 2500 chassis (Control 10 for Loewe Systems and Control 150 for Loewe.). This is an 8 bit standalone microcontroller, especially designed for use in infrared remote controls. It has very little external wiring and is able to control the transmitter diode directly via an amplifying transistor. The modulator is incorporated into the IC. The processor is equipped with Loewe specific software, which is mask programmed. To operate the Q 2500 chassis, commands are issued as RC 5 code, level 0.

The operating commands are formed on the transmitter keyboard by linking a Y input (Y4 Y7) with an X input (X10 X17).

Internal circuit 84C122



The operating commands for videotext are specified as a sub-program in "Level 0".

The transmitter IC produces a code word for each command and adds two start bits and a control bit. The two start bits are always H, and the control bit changes each time the button is pressed. It indicates to the central control unit, whether a new command is present, or the current command is still valid.

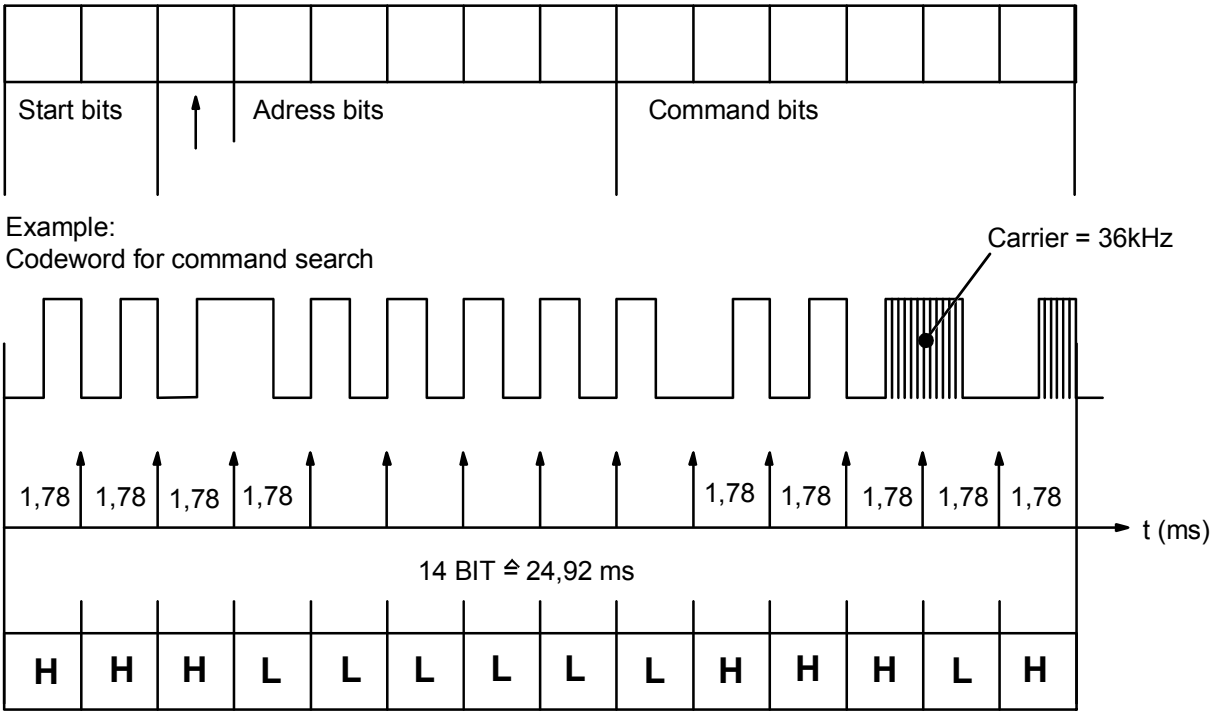
This 14 bit codeword is modulated with a 36 kHz carrier and applied serially to pin 21 of 84 C 122.

The digital Information is expressed by the step direction within the bit (Biphase).

If the button is pressed for a long time on the report control the codeword is repeated after 114 ms.

This signal is supplied to T 121 via resistor R 124, amplified and radiated via infrared diode D 121. The transmitter diode is now no longer covered by a dispersion window. This means the current can be reduced to f 900 mAss. The current can be taken directly from the battery, which means that no additional Elkos are necessary on the operating voltage.

14 BIT - Codeword



On pins 8 and 9 of 84 C 122, the ceramic oscillator X 111 is the component that determines the frequency of the pulse oscillator for the synchronisation of the system and for the production of the carrier frequency (fTr = 1/12 fCycle). Using the ceramic oscillator X 111 means that tuning of the cycle frequency is not needed.

The circuit is functional at an operating voltage of 2.5 – 3.5 V and draws a normally energised circuit current of = 1 uA and an operating current of 35 mA. The transmitter thereby achieves a range of >10 m.
The voltage source is two micro-alkali-manganese batteries.

After switching to the service mode, chassis tuning is implemented with the FB transmitter. The service mode is called up by pressing the functional button “?“ four times, so that the “Service“ display appears, and then pressing the “M“ button on the remote control within one second. Then using the curser buttons, the individual tuning functions can be called up. Tuning is also carried out using the cursor keys. The data is initially stored in the working memory C 161 and is only transferred to the memory on operation of the "ok" memory button. Once returned to normal FS operation, use the "E" button to return to remote operation.

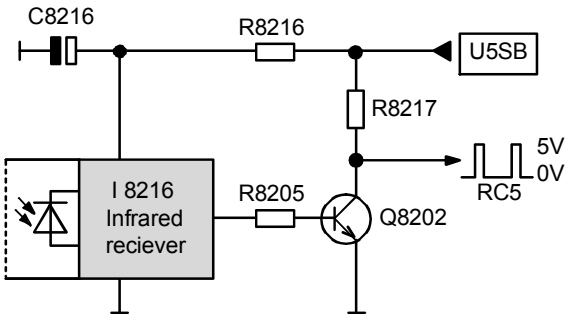
Pressing the Z 1 button switches the remote control processor to another mode. This means that the transmitter can be used for both a videorecorder and DVD player from Loewe. For the videorecorder, however, control is only possible with Korythso code, as used by Panasonic. For the DVD player we use the RC 6 code.

If the remote control is not used in the videorecorder or DVD mode for 20 sec, then it automatically switches back to the TV mode. The video or DVD mode is displayed for Control 10 by the LCD and for Control 150 by an LED on pin 2 (Y1) and pin 3 (Y0).

For Control 10 the LCD is controlled from ports Y3 to Y7. Up to Y3 these are also used to query the button matrix.

The operating voltage is also monitored in Control 10 and displayed correspondingly in the LCD. Measurement of the battery voltage is carried out by transistors Q 416, Q 414 and Q 404 on pin 5 of 84 C 122.

4.1.2 Infrared receiver



The IR receiver on the local control unit is a thick film circuit and is fully encapsulated.

The IR signal from the transmitter is converted into an electrical signal by the receiving diode, amplified and prepared in such a way that it is available on the output as 2 Vss.

With the next transistor Q 8202 on the local control unit the signal is amplified to 5 Vss. In this way the IR decoder in SDA 6000 can be safely controlled via pin 5

Via IC I 2716 and transistors Q 2721, Q 2731 and Q 2741 the IR signal is applied to pin 8 on each of the three Euro sockets. This allows hidden videorecorders to be remotely controlled via the IR receiver of the television set and the AV switching voltage line (see AV operation).

Via Q 2823 the signal reaches transistor Q 2862 on pin connector W 1076. Via W 1076 the IR signal is supplied to a connected online-box.

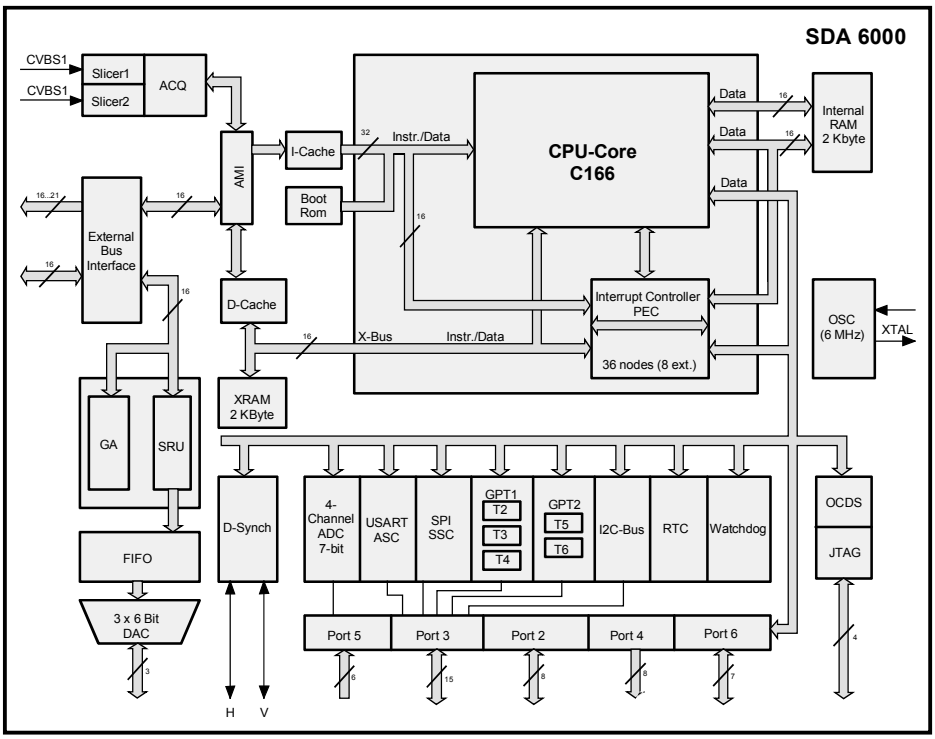
The pulse width for the RC 5 code of the remote control is about. 900 µs. If a connected Multi Media Component is operated with the Control@media IR keyboard, the data is not transferred with the slow RC 5 code, but with an RC MM code (MM-Multi Media) designed for fast data transfer. The pulse width for the RC MM code is 167 µs.

The pulse width of 167 µs requires an IR-receiver with a very short time constant. Therefore, in Multi Media devices a special IR receiver is used, which for operational pur-

poses cannot be replaced by one from a normal TV set.

4.1.3 The SDA 6000 central control unit

A Siemens SDA 6000 is used in the Q 2500 chassis for control of device functions. This 16 bit processor is a development of the C 166 family of single chip CMOS microcontrollers. It combines excellent CPU characteristics of up to 8 million computation operations per second with high functionality, flexibility and high capacity input and output ports. The SAD 6000 has 5 Ports (Port 2 – Port 6) with a total of 44 inputs and outputs. It was designed especially for applications, where cost plays a critical role. This makes the processor suitable for use in colour TV sets.



In the Q 2500 chassis the processor must fulfil the following functions:

- Oscillator for generation of the CPU cycle frequency.
- Generation of the clock frequency for the bus systems.
- Processing of the RSIG signals and local operation commands.
- Generation of the I²C bus systems for control of the HF/IF units, processing of pictures, video text, PIP and audio, for communication with the memory IC, the SAT receiver unit and the interface selection.

- Control of LED's for operating and standby display.

- Creation of further switching processes, e.g. ON/OFF, AV transfer, etc.

- Simulation of a clock synchronised by VPS-information.

- Timer function for programmable disconnect time and recording timer.

- Code converter for IR commands for the remote control of a video recorder via the AV voltage switching line and the Dolby surround unit.

- RS 232 for communication with the online as well as the DVB module.

- Digital Link Plus Control for the 3 Euro/AV sockets

In order to fulfil the required tasks the following circuit components are combined in one chip:

- C 16 core with CPU and interrupt controller

- 2 kByte XRAM as working memory

- Interface for the external ROM

- Quarz controlled clock generator

- Interface for the three I2C buses

- Multifunctional timer

- IR decoder

- ON/OFF Flip-Flop

- Reset circuit for internal reset

- Reset circuit for external IC's.

- Ports P2 to P6 with 44 input and output pins.

Many of these functions are implemented not by the hardware of the processor, but by the Loewe-specific software.

4.1.4 Reset

For correct functioning of the device, various reset pulses are necessary. The first required is a reset on pin 73 for the SDA 6000, as soon as its operating voltage U3.3 is available and the 6 MHz system cycle has run. This reset is produced by I 2941. After this reset the SDA 6000 starts to operate and implements and emits control commands.

The microprocessor also has a reset on pin 8, produced by I 2946, if the circuit power supply has run and all IC's have an operating voltage. This reset is retarded in SDA 6000 and then emitted from pin 100 to the digital IC's.

RESET digital component input pin 8
The reset for this input is formed by a steep positive flank. As U3,3 is the last voltage switched by the power supply unit, this reset is coupled to the voltage. The reset pulse is created in I 2946 and is present on pin 8 of the microprocessor, if all IC's in the chassis have an operating voltage. SDA 6000 can then begin controlling the IC's. In addition the processor also reacts, if the reset is not present on pin 8 or during operation. Normally 5 V is always felt on a reset input, provided the device is fully switched on.

RESET digital component output pin 100
Via this pin the microprocessor sends the reset to the other circuits. This is coupled to input pin 8. In this way the processor can monitor the reset, and for transient voltage failures can prevent, the level on the reset line collapsing. On the other hand, the circuit also makes it possible for the SDA 6000 to emit a software controlled reset on pin 50 during operation

In standby and on start up L level is initially felt on pin 100. Not until the SDA 6000 switches pin 100 to H level, does the L/H flank produce the reset for the IC's. During operation the reset inputs must be held permanently at H level, otherwise the working register will be deleted.

This reset reaches MSP 3410 /pin 21, and the two VCP 3230/33 /pin 15.
All other IC's either do not need a reset or generate it on switching on the operating voltage.

4.1.5 Creation of cycle frequency

The internal oscillator of SDA 6000 is synchronised with a 6 MHz quarz on pins 108 and 109. The cycle frequency for the bus systems is obtained from this frequency by internal distribution. They are from 70 to 400 kHz respectively for the I²C bus systems. The cycle frequency is transferred under software control depending on the current function.

4.1.6 Operational commands

The SDA 6000 receives operational commands as serial data information by RSIG signal on pin 9. The local operating commands are applied to the CCU on pin 126 as various voltage values.

Pin 126 operates as an ADC with 6 bit resolution. By various voltage dividers on the three operating unit buttons, various voltage levels are produced.
The voltage levels are digitised by the ADC, and based on the measured values the CCU issues the appropriate commands.

The following voltages are produced by manipulation of the various buttons:

-
- "+" button - 0.5 V
- "-" button - 1.1 V
- " " button - 1.8V

The overtravel contact is connected to pin 93 of the CCU.

4.1.7 LED display

The red standby LED is controlled via pin 96 of the CCU. In operation the remote control commands in RC5 code are acknowledged by transient illumination of the LED. For standby operation the pin is set to the H level and transistor Q 2853 thereby conducts, whereupon the LED illuminates. The ON LED is controlled via pin 78 with the ON/OFF-command. When the power supply is switched on this line is set to the L level, whereby the green ON LED also illuminates. SAT standby operation is indicated by illumination of the two LED's.

4.1.8 ON/OFF function

If a switch-on command is present, the output ON/OFF, pin 78 of the CCU is set to L level. This blocks transistor Q 8111 in the standby power supply, whereupon Q 8114 conducts and attracts the relay. The system voltage is able to reach the main power supply, which begins to operate.

The device starts operating at the selected program location. The output is once again set to H level by an off command.

With an ON/OFF command the two transistors Q 2961 and Q 2966, which form part of the mute circuit, are switched, thus suppressing input and output noises.

4.1.9 Protective circuit

In order to avoid excessive high voltage, c.r.t. defects or other serious damage due to faults in the vertical deflection, caused by excessive beam current, the device is switched to standby. In addition, pin 94 of the CCU is set to H level. In normal operation L level is present (see description basic board Section 5.2 – 6.2).

If an error occurs – H level on pin 94 of the CCU - the CCU swtiches the device after 2 seconds to standby operation.

4.1.10 AV operation

The circuit is designed so that AV operation with switching voltage on programme locations can be programmed.

Setting is implemented in the menu under connect AV device.
The menu makes clear the exact procedure for setting up or you can refer to the overview in the operating instructions. Monitoring of the switching voltage on pin 8 of the AV socket is implemented via transistors Q 2737/Q 2726 and Q 2746 for AV1/AV2 and AV3. The three emitter followers are connected respectively via voltage dividers to pins 125/124 and 127 of the CCU.

In accordance with the Euro/AV standard, pin 8 of the AV socket is defined as 6V (16:9 operation) and 12 V (4:3 operation) AV operation.

The CCU monitors these voltages on its AV pins. By division of the respective voltages 6V = 1.3V and 12V = 2.6V on the pins of the CCU. If a switching voltage is detected by the CCU, this switches over to AV operation on corresponding menu selection.

- **IR signals**

For the remote operation of VTR devices via the TV-IR receiver the RSIG signal is applied to the Euro sockets pin 8.

For this two signal paths are provided. In normal and standby operation SDA 6000 pin 9 at H level switches transistor Q 2823, and pin 97, which is also on the signal path, is made high-resistant from SDA 6000, to avoid interference. Via Q 2823 and I 2716 the RSIG signal is passed on to the transistors for socket selection. Use of the recorder remote control is necessary for this.

There may be applications, however, for which the video recorder remote control is not available and the TV remote control emits another code that the recorder does not understand. For this a video menu is provided in chassis Q 2500, which is called up in the remote control with “V=“. This allows the basic functions of the recorder to be used. If for “Connect video devices“ three devices are selected, they can all be controlled independently of each other.

In this operating mode the RSIG signal present on pin 5 of the CCU is controlled internally via a code converter and then output via pin 97 of SDA 6000, which is now low resistant. The other signal path is identical with the first possibility.

The code converter changes the RC 5 data words of level 0, as they are delivered to the IR receiver, to those of level 5, with which the video recorder operates. Secondly, the code converter changes the RC 5 command into the corresponding data word of the NEC code. Thirdly, the RC 5 commands are converted into the Korythso code.

The three data words, both RC 5 of level 5, as well as the NEC code word and the Korythso code word, are emitted serially by SDA 6000 pin 97. This means that remote control of recorders that operate with RC 5, NEC or Korythso code is possible.

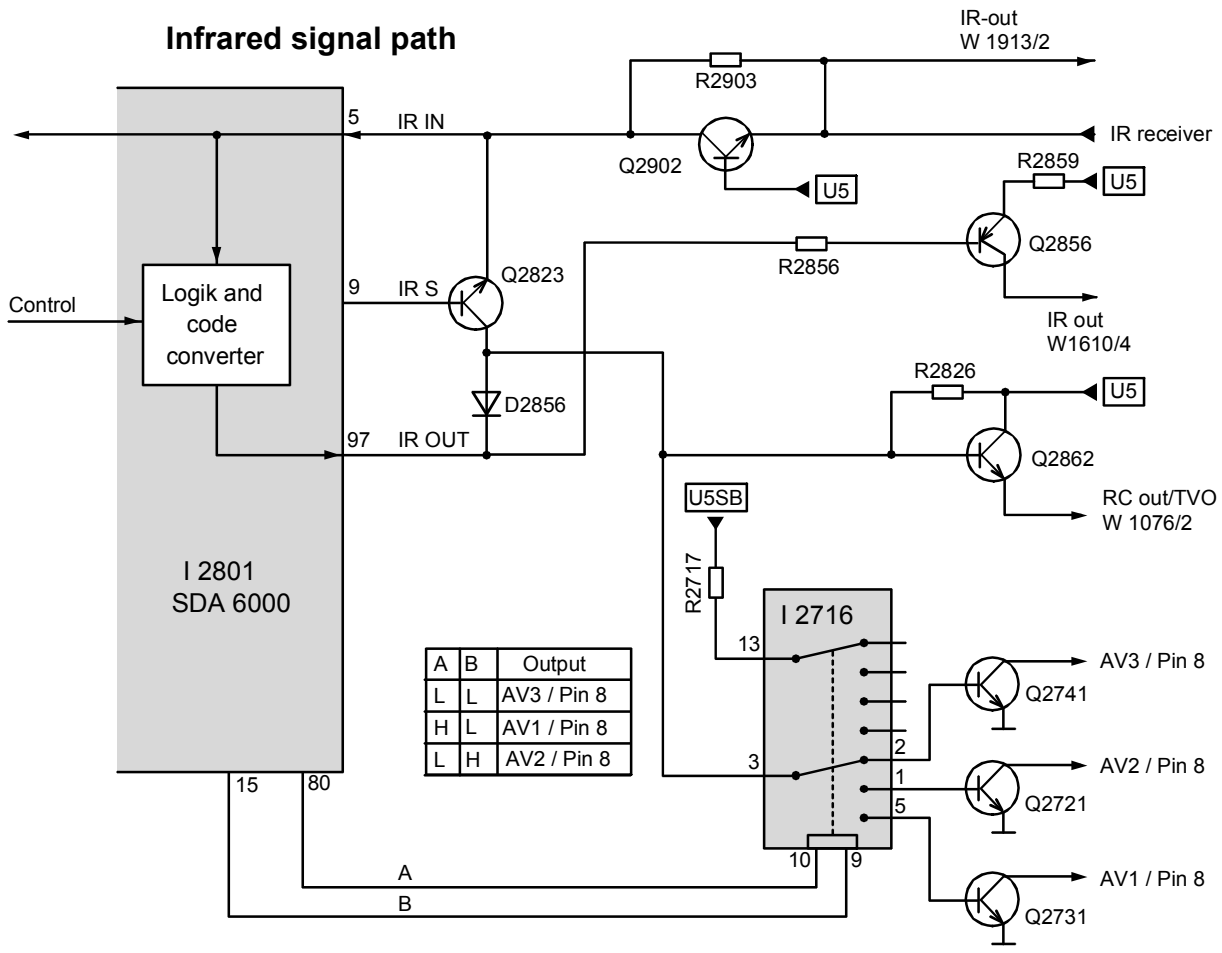
Of course, a recorder must be used that can process the remote control signal coming from the AV switching voltage line. For this most Loewe recorders have a converter.

During output of the converted IR commands transistor Q 2823 is blocked with L level on pin 9 of the CCU. This prevents these signals being affected by IR signals from the receiver on the operating component.

In order to achieve separate operation of the three devices connected to the two Euro sockets, the circuit also contains RSIG signal switching controlled by the CCU.

This switching is implemented by multiplexer I 2716. The IC is controlled by the CCU via the outputs pin 15/80. According to the status, see table, the IRIN/IROUT signal is switched to the respective Euro/AV socket.

An optional online module can be controlled by transistor Q 2862.



The software for the RSIG signal switching is fitted with a load memory function. If there is no information about which socket should be used RSIG is applied to AV 1. If another socket is selected, the signal is then applied to this socket. If no socket is selected, the signal is applied to the one last used. This is true also for standby.

4.1.11 SAT standby

In order to create a situation where a video machine can also receive signals from the SAT receiving unit, which is integrated into the unit, without the TV set needing to be in operation, the horizontal output stage in this operating mode is switched off. This is achieved by an H level emitted via pin 79 of the CCU. This switches transistor Q 2951 and the horizontal control pulse from the video/deflection processor TDA 9332 is lead to earth.

As both the vertical and the RGB output stage obtain their operating voltage from the diode split transformer, this allows the entire c.r.t. to be switched off and the power input in this mode to be reduced. In normal operation pin 79 of the CCU is at L level and transistor Q 2951 is high resistance.

The c.r.t. is switched off when:

a) a timed recording for a video recorder is being processed in the TV set.

b) on switch off using the remote control, if previously, via the video menu, a recorder has been set to record.

c) on switch off using the remote control, if previously overplaying between the sockets of the TV has been activated.

d) Radio – operation is activated (after 20 sec.).

In all these cases all other stages of the chassis are fully operational. Except for d) the sound in the MSP 3410 is switched off via the I²C bus.

4.1.12 SAT unit control

Control of the Sat/TwinSat unit is implemented by the CCU via the I²C-Bus 2.

The SAT unit VI used is also able to control appropriately equipped switch boxes or LNCs via DiSEqC Level 1 (Digital Satellite Equipment Control). In this system pulse modulation of the 22 kHz signals allows data to be exchanged between receiver and peripheral devices. This means that the current different LNC supply voltage switching information, 22 kHz and control function will be replaced and simplified by separate control lines.

In the standard, a logical 1 is defined as 11 periods of 22 kHz signals (0.5 ms) followed by a 1 ms pause (22 periods). The logical 0 is represented in reverse, i.e. 22 oscillations (1 ms) and then a 0.5 ms pause (11 oscillations). For this, each bit requires 1.5 ms for the transfer, which corresponds to a maximum transfer speed of 666 bits per second. After each transferred telegram, there must be a pause of at least 6 ms (132 periods).

Control is implemented according to the Single Master - Single/Multi Slave principle. Master is always the SAT receiver, and the external components (LNC multiswitch, etc.) are the slaves. Therefore, each communication from the receiver is started and the external components can only transfer data, after they have been requested to do so by the master.

A command from the master contains a 1 byte frame, a 1 byte address, a 1 byte command and 1 or more bytes of data. The responses consist of a 1 byte frame and 1 or more bytes of data. Each byte is always followed by a parity bit (P) for error checking.

The frame byte determines, whether the data is sent by the master or the slave. The address byte contains the information that determines which peripheral module (switchbox, LNC ....) is addressed. The command byte determines which switching function is to be implemented (selection LNC, level switching ....). In the data byte additional information can be exchanged. There is still enough free space in the DiSEqC command set for future requirements. This means that the system has built in futurability.

For the DiSEqC control the SDA 6000 has an input and output respectively. Communication with the SAT unit in the device is via a common line on connector W 1211, pin 7 on the basic board and from there via W 250, pin 8 on the SAT unit.

Pin 90 of the CCU is used as an output for the control of peripheral devices. The 22 kHz-signal on the SAT unit is switched using the H level. By switching between the L and H level the 22 kHz is switched by the SAT unit for the required period and a command is then issued via the coaxial cable.

If the SDA 6000 is waiting for data from a peripheral device, then the 22 kHz must be switched at L level on pin 90. The device addressed dampens the 22 kHz signal for the required period by changing the input impedance, so that the data can be transferred to the SAT unit of the TV set. The SAT unit changes this signal into L and H pulses of the same duration, which are applied to connector W 1211, pin 7 on the signal board. The signal is inverted in transistor Q 2831. The DiSEqC information is then made available to the SDA 6000 on pin 7.

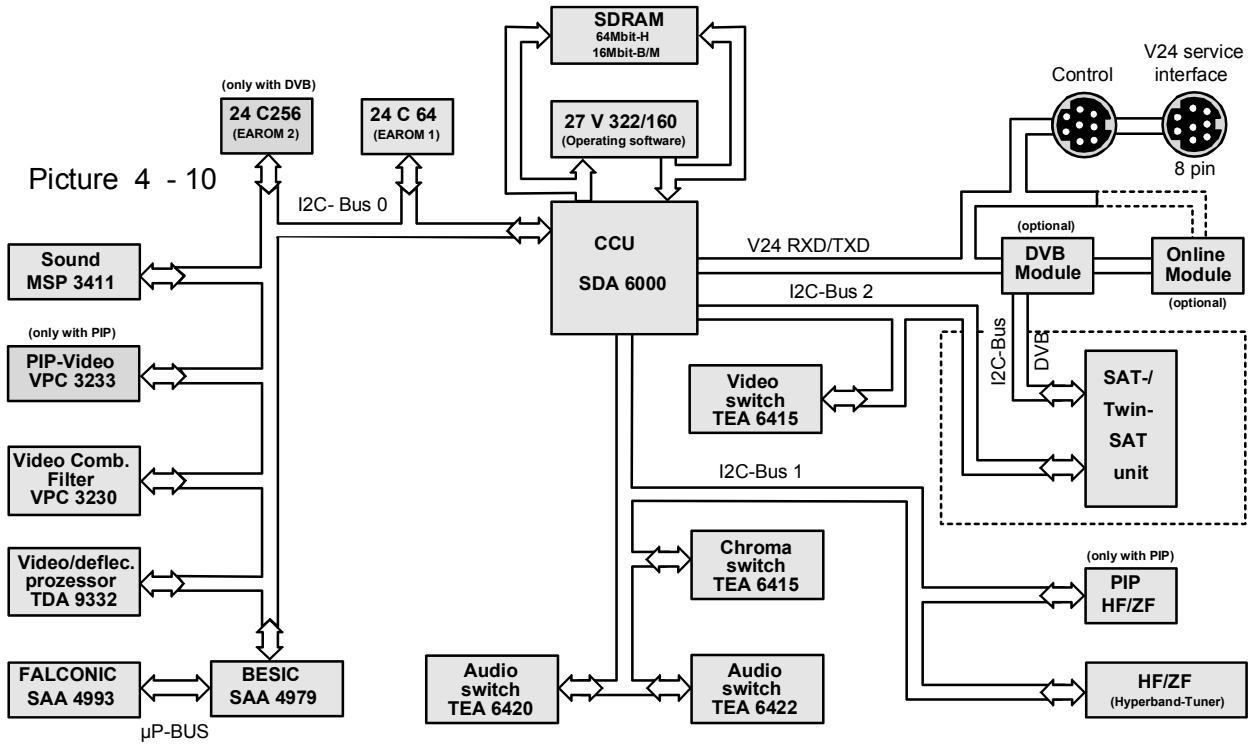
4.2 Bus systems in Q 2500 chassis

Several bus systems are used in order to implement the large number of switching and control functions of the Q 2500 chassis in a reasonable time, and for error-free addressing of the ICs.

For this the SDA 6000 generates three I²C-bus systems with which the memory IC, the control ICs for the HF/IF component, the ICs on the SAT unit, the converter for video and audio, the building levels in the video section, for PIP and multi-sound processor are controlled
The I²C bus systems 1 and 2 on the other hand operate with a common clock line and separate data lines. The I²C bus system 0 operates as usual with separate data and clock lines.

In all I²C bus systems there is constant data traffic. If the Bus Stop command is issued or the device is started with the Power On command, the bus lines are then set to 5 V d.c.

Q 2500/H bus systems

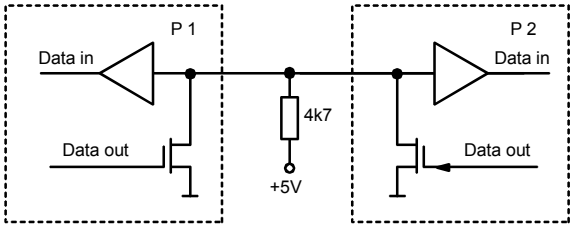


4.2.1 I²C bus systems

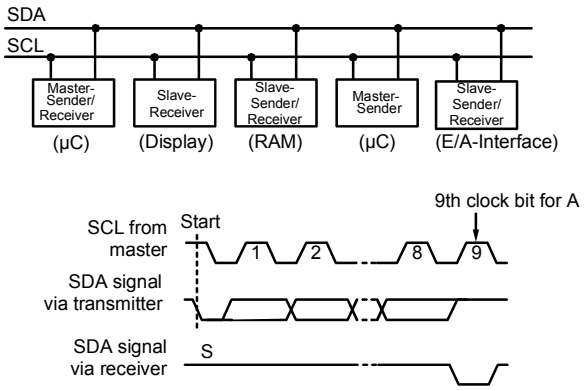
The I²C bus is a two-wire bus system consisting of a DATA line and a clock line. This bus system permits the serial and bi-directional exchange of communication between several microprocessors and peripheral ICs that possess an I²C bus interface. This means that the number of connections is reduced, which results in a simplified switching structure, and increased reliability (fewer solder points, connections, contacts, etc.).

Via pull-up resistors, both lines are in a state of rest (i.e. no data transfer) at H level. Data transfer starts if a clock line is "High" and a negative flank (H > L) appears on the DATA line (Start condition). Evaluation of the data occurs during the H level of the clock pulse.

Data inputs/outputs in I2C bus



The end of data transfer (Stop condition) occurs on signalisation of a positive flank (L > H) on the DATA line and concurrent H level on the clock line.



Up to 400 kbit/s can be transferred via the I²C bus interface of the SDA 6000. The data and clock impulses are switched by software switching logic to the respectively required bus connections.

The CCU operates on its I2C bus outputs with a level of 3.3 V. The other ICs and components operate with TTL level. Adaptation of the CCU level to the TTL level is by transistors Q 2883/86/88/91 and Q 2893.
The following functions are controlled via the I²C bus systems:

I²C bus 0 with SDA 0 and SCL 0

Only the EAROM I 2931 is connected to the I²C bus 0. This memory contains all start values and customer specific values. The data is selected here on start up and when making adjustments or writing to the EAROM on shut down and for memory processes.

If a DVB module is retro-fitted the second EAROM I 2936 is also used. Programme data from 220 to 1470 is stored here.

- Multi-sound processor MSP 3410 to IF- and VF processing.
- The video processor VPC 3230, I 2271 for digitising of input signals and processing in the main signal path. It conducts the digital Y/UV signals to the I 491 memory.
- SAA 4979 for conversion of the digital Y and C signals into analogue Y, R-Y and B-Y signals and for the control of the digital 100 Hz processing with the two half picture memories and the SAA 4993.
- The video/deflection processor TDA 9332 for generation of the RGB control signals for the c.r.t. plate and for generation of the deflection pulse
- Video processor VPC 3233, I 2151 for PIP signal processing. The digitised Y/UV-signals are fed to the two PIP synchronous memories I 2161/71.

The I²C bus has a maximum cycle rate of 400 kHz.

I²C bus 1 with SDA 1 and SCL 1

Just like the I²C bus 0, fixed pins are also provided for the I²C buses 1 and 2 in the SDA 6000. Buses 1 and 2 operate with a common clock line and separate data lines. Data is switched to the respective line for the required bus in an internal transfer switch.

The following are connect to the I²C bus 1:

- The tuning and transfer IC's on the receiver units in the basic board.
- The transfer IC's for video (1 x TEA 6415) and audio (TEA 6422 and TEA 6420) for the interface on the signal board.

The I²C bus 1 operates with a cycle frequency of 100 kHz.

I²C bus 2 with SDA 2 and SCL 1

The Sat or Twin Sat unit is controlled from the SDA 6000 via the I²C-Bus 2.

There are tuning ICs in the receiver unit. Generation of the tuning voltage and control of the band and standard transfer or LNC supply on the SAT receiver.

4.2.2 IC 24C64 memory

A 24C64 64 kbit memory is used. To distinguish this EEPROM from the similarly sounding EPROM it is given the designation EAROM.

In addition to system data for the digital ICs the EAROM also contains user specific data. This is programme related location data such as channel, reception range, standard, etc., as well as customer specific tuning values for brightness, volume and contrast, for example.

The 24C64 has a memory capacity of 65536 bits, and is organised into 8192 x 8 bits. The memory life is at least 10 years, with more than 1 million write and read actions guaranteed. Inputting and outputting of data is controlled by the SDA 6000 and implemented via the I²C bus 0. For this the CCU generates an 8-bit address word preceded by a start bit. The 8-bit value is composed of a 7-bit word for the IC address and one bit, containing the on or off command.

This address word is checked by the IC's connected to the system for conformity with the address words they hold, and receipt is acknowledged by an acknowledge bit from the appropriate IC. In the socket the master IC (SDA 6000) transfers the storage location address. This address consists of two 8-bit words, receipt of which is acknowledged by an acknowledgement bit for each bit respectively. If this occurs, the 8 data bits are transferred to or from the memory IC and receipt is confirmed by the appropriate IC.

Transfer of the data described is implemented via line SDA 0 and is synchronised by the clock on line SCL 0. After transfer of the last acknowledgement bit, the command "Input" sets the save procedure in motion. During the save procedure the inputs SDA and SCL of 24C64 are locked, in order to prevent any external interference with the memory during this time.

After the start up routine the system data is read from the memory by the SDA 6000 via the I²C bus and and then the data is transferred via the I²C bus systems to the appropriate digital IC's.

To prevent inadvertent deletion or overwriting of the memory on start up or shutdown, the Write Protect line pin 7 of the two EAROMs is connected via Q 2943 to the Reset line. In the start up and shut down phase, pin 7 of both EAROM`s is switched to the L level. Inadvertent deletion or overwriting is thereby prevented. In the operating state H level is applied to pin 7.

4.2.3 EPROM M 27 C 322

Device specific software is held in EPROM I 2926 as non-volatile data.

An IC with 32 Mbit memory is used. The memory is divided into 2097152 x 16 bit areas.

Data transfer from the EPROM to the computer is implemented via connections D0 to D16. The memory addresses, from which the data is recalled, are transferred previously via lines A0 to A 20.

4.2.4 SRAM

Data that is necessary for the functioning of the CCU is temporarily saved in the 64MBIT DRAM I 2916. Owing to additional functions in the EPG and DVB the internal RAM area in the CCU is no longer sufficient to store all the data required. Up to 3000 videotext pages are stored in this DRAM.

4.2.5 Search functions

On implementing the search function by pressing the appropriate button the SDA 6000 permits the SAA 4979, via the I²C bus, to output permanent blank in the blank stages. In this way the picture is sampled and using another command from the MSP, the sound as well.

The required frequency is communicated as a whole number multiple of 62.5 kHz from the SDA 6000 via the I²C bus to the tuning IC. From the tuner each set oscillator frequency is present as the actual value. It is sub-divided in the IC and compared to a reference frequency. The sub-multiple ratio is determined by C 161.

Using internal UP and DOWN pulses the tuning voltage is delayed until compatibility is reachd. The PLL engages and communicates this to the SDA6000 via the I²C bus. It then requests the VPC via the I²C bus for the available standardised synchronous signals. If synchronous pulses are present, the permanent blank is lifted. In the event that there are no synchronous signals, the SDA 6000 communicates to the tuning IC the next highest sub-multiple and the tuning procedure begins anew. The search procedure only stops when a transmitter is found. The SDA 6000 determines this by querying the VPC about the synchronous pulses present.

During the search procedure the channels are searched in ascending order within the selected standard. For the PAL B/G, SECAM East, NTSC Europa and SECAM L standards, cable channels are also searched.

On transfer from one FS band to another, the corresponding band switching information is automatically switched at the same time. Depending on the device settings changing of standards is carried out either automatically or manually.

If no transmitter is detected in the selected channel on the normal frequency, the channel is searched from its lower limit in 1 MHz steps. If a transmitter is still not found, the system jumps to the next highest channel.

4.2.6 Storage

If a channel has been found and the correct standard set by the search procedure or direct input of a channel, it can be saved to any programme location between 00 and 220. In addition, all tuning and switching information is written to the EAROM via the I²C bus.

4.2.7 Programme recall

For programme recall the required programme number is input to the SDA 6000 via the remote control. Via the I²C bus it requests the EAROM to communicate the details of this storage location (division ratio, fine tuning, FS standard). This Information is passed via the I²C bus from the memory to the SDA 6000, which then passes it to the tuning IC in the tuner. The IC sets the band switching outputs to the required band and required standard and moves the tuner oscillator to the allocated frequency. The fine-tuning value is also considered with respect to the oscillator frequency and corrected by the AFC. The tuning remains on the required frequency, even when no transmitter is available.

4.2.8 System clock

A realtime clock is integrated into the SDA 6000 to enable timer functions for transmitters without videotext and timed SAT standby programming.

It consists of a computer-integrated time switch and the associated software forming part of the operating software. The synchronisation and setting of this internal clock is implemented by the appropriate videotext information.

It is therefore necessary on starting up the device to select a transmitter with videotext, otherwise clock setting has to be carried out manually.
In standby operation the clock continues to run.

The following logic is provided for setting the time:

- On switching on using the mains button the clock is set to 0.
- On reception of a videotext transmitter the clock is set within one minute.
- In operation the clock is permanently synchronised with the videotext time, so long as time is running in the text.
- If the time deviates by ± 1 or 2 hours, it is only on selection of program locations 1, 2 or 3 that it is set to the videotext time, to avoid time zone errors.

Note
If during operation the time is corrected manually, synchronisation with videotext time is no longer implemented. The time is then running free and after a few days large deviations could occur. Synchronisation of the clock with the videotext can then only be implemented by re-setting the processor, i.e. after switching off and on the mains switch.

The system clock controls the recording of a connected videorecorder, i.e. the switch off and switch on time. For these functions it is important that the system clock is correctly set. If no transmission with videotext is received, the time and date can be manually set.

Note:
The switch off timer can only be completely deactivated with “--:--“. If “00:00“ is set, then at 24.00 the device switches to standby.

4.2.9 Control of signal processing

The SDA 6000 microprocessor controls and monitors all signal processing. To do this it is linked to the signal processors via the I²C bus system. Each processor has an integrated I²C bus interface and a working memory. The content of the working memory is deleted on shut down. This means that the data required by the processors must be reloaded during the start up routine.

This data is stored ex-works in a non-volatile form in the memory IC of the EAROM 24C64. This tuning data is also already stored in replacement EAROM's and therefore only requires minor corrections if an IC is changed. The cost is about the same as current tuning costs after a change of chassis and can be implemented via the FB sensor. A computer can be used for tuning, as detailed in number of specialist magazines, but does not save any time.

On start up C 161 reads the tuning values from the memory via the I²C bus and enters them into the working memory of the appropriate processors via the I²C bus. Apart from the static data that the system requires for functioning, data for the picture amplitude, picture geometry, picture width, etc. is contained in this entered information. It also includes the customer specific tuning information such as brightness, colour saturation, volume, etc. The latter can be changed at any time by the customer, and by using the memory function the changed values can be entered into memory in a non-volatile form.

Changes to these values will be communicated via the I²C bus to the appropriate processors during the adjustment procedure and can then be adjusted to the required values. All data read in on start up as well as data changed by the customer during operation, is checked during operation by continuous communication between the SDA 6000 and the signal processors. If deviations occur these are corrected immediately.

This is particularly the case for time-dependent tuning values such as, for example, white value, black value and c.r.t. leakage current. For this reason in devices incorporating the Q 2500 chassis, ageing of, for example, the c.r.t. only becomes apparent when the scope of control is exhausted and the c.r.t. is totally worn out. In our chassis these dynamic tuning values are therefore subject to special treatment. The values for these functions held in the memory are automatically updated to the current values on each save procedure. In this way updating of the current wear-determined values on start up is not necessary, which the end user will surely notice.

For control and adjustment procedures via the remote control and local operating buttons the changes are initially made only in the working memories of the appropriate IC's and in the register of the SDA 6000. Normally the saving of values in EAROM must be implemented by an additional command (usually the OK button). If the remote control is used to switch the device to standby, then the data in the register of the SDA 6000 is available when the unit is restarted. The data within the unit, such as the last volume level set is retained.

When the unit is switched off at the mains the microprocessor register is deleted, and on the next start up only the EAROM data is available. So that specific settings are retained, the EAROM has an area for "Last memory" data. On shut down the data is saved to this area (e.g. last programme location). In addition, a few seconds after programme location change the set programme location is saved in the Last Memory data area.

4.2.10 Service mode

In order to carry out chassis tuning the device must be placed in the required service mode. The remote control can then be used to call up all the necessary functions for chassis tuning, with a few exceptions. After successful tuning the new values must be saved.
The exact functions available in the service mode can be found in the service instructions for the appropriate device.

4.2.11 Video text

In the 100Hz TV set system the videotext function and the production of overwriting OSD is now the responsibility of the CCU SDA 6000.
For this reason the FBAS signal is fed to pin 117 of the CCU. The CCU controls full data separation and memory administration internally. The VT pages are then stored in the SDRAM I 2916.
The VT information as also the OSD overwriting are applied to pins 112/113/114 of the CCU as RGB signals.

4.2.12 Picture signal processing

Picture signal processing is implemented by highly integrated modern circuits that have been used for the first time by Loewe, in similar IC variants, in the Q 2300 chassis generation. The highly integrated IC's mean that for the two 100 Hz generation chassis Q 2100 and 2200, the 100 Hz module necessary for the signal board can be dispensed with. All the ICs necessary for signal generation can be fitted without problem on the component side of the signal board. This also provides much simpler faultfinding, which is also favoured by the clear signal flow.

The picture signal processing is mainly in digital form, with ICs from different manufacturers being used. The video processor VPC 3230 developed by Intermetall is used in the front end. A Philips IC set is used for the 100 Hz processing. This IC set was reduced by higher integration to two chips and the two half picture memories. The new SAA 4993 in the Q 2500 chassis is used for the latter. The microcontroller, the memory controller, the 50/100Hz memory and the DAC are all combined in the SAA 4979 (BESIC). In the back end of the Q 2500 chassis there is a new processor that contains both the video and the deflection function. The Philips TDA 9332 video/deflection processor has the item number I 2521.
In addition, the Q 2500 chassis can also be optionally equipped with picture in picture processing. This enables one or three small pictures to be inserted (see picture in picture). A split screen is also possible for the first time.

4.2.13 Components for signal processing

The following is a short overview of the components and their functions as used for signal processing. The signal path, pin-assignments and the exact functioning is explained later. The processing is also described in detail later.

- VPC 3230
  Video processor
  8-bit ADC for FBAS and Y/C signals
  4-line comb filter
  Multi standard colour decoder for PAL/ NTSC and SECAM
  20.25 MHz clock generator
  Letterbox detector
  Line compression and decompression for zoom modes

- 2 x MSM SAA 4955 HL
  Half picture memory

  The two half picture memories are necessary for the picture
  signal intermediate storage and processing.

- Philips SAA 4993
  (Falconic: Field and line rate converter with noise reduction IC)

  Dynamic noise suppression set by user.
  Suppression of intermediate line flickering DLC (Digital Lineflicker Reduction).
  Suppression of motion in horizontal movement, DMI (Digital Motion Interpolation).
  Suppression of motion in movies, DMM (Digital Movie Mode).
  Line interpolation, in order to display 576 lines in all zoom functions, DLI (Digital Line Interpolation).

- SAA 4979
  (BESIC: Back End System control IC)
  The integrated half picture memory is for 50/100Hz conversion.
  Control of 100 Hz signal processing
  Synchronisation of 32 MHz
  Peaking and CTI (Colour Transient Improvement) to improve Y and chroma interfaces.
  Horizontal sampling
  DAC for Y, R-Y and B-Y

- TDA 9332
  (Video/deflection processor)
  Inputs for two separate RGB signals.
  PAL/SECAM and NTSC matrix for production of RGB signals.
  Colour saturation, brightness and contrast settings.
  Automatic Cut Off and leakage current control and setting.
  Beam current limitation circuit.
  RGB output amplifier.
  Production of V/H deflection control signals

4.2.14 Signal path

All FBAS or Y/C signals delivered by the receiving units, the three Euro/AV sockets of the front interface, are directed via the video matrix switch to the video processor VPC 3230. The FBAS or Y signal is led from pin 17 of I 1711, via the impedance converter Q 1814 to pin 73 of the video processor I 2271. The filter in the Y/FBAS path consisting of L 2259/57 and the associated capacitors has low pass characteristics. Frequency components over 7 MHz are efficiently suppressed by the filter. This prevents floating effects in the video signal, that may arise from the cycle rate of the ADC and residual signals from neighbouring channel. For Y/C operation the chroma signal moves from pin 14 of I 1721, via the emitter follower of Q 1824 to filter L/C 2266, which suppresses noise components, and then to chroma input pin 72 of 2271.

VPC 3230 is also equipped with two RGB input interfaces.

Pins 1-3 of I 2271 are connected directly to the Euro/AV socket 2 via the corresponding input filter. The associated fast-blank signal is applied to I 2271 on pin 79.

Q 2226 prevents the FB voltage exceeding 2.2 V and thereby damaging the videoprocessor. RGB operation via the Euro/Avc socket 2 is therefore also fast blank compatible. Y/U/V operation is also possible from the second RGB input from pin 4 of I 2271 , 5 and 6. The RGB signals are fed from the optimum DVB module or from the Euro/A socket 3 via this input. The same goes for the Y/U/V signals of the Euro/AV socket 3. The inputs 4, 5 and 6 from I 2271 are not fast blank compatible.

The video processor VPC 3230 digitises and fully processes the FBAS analogue input signals or Y/C signal. On the output there is a digital 8-bit wide luminance and an 8-bit wide demodulated chroma signal with its U/V components. The luminance and chroma signals are transferred in multiplex procedures via eight LM0-7 lines. The amplitude on the lines is 3.3 Vss. The associated cycle frequency is 27 MHz and is output from pin 27 on I 2271.
In SAA 4979 the luminance and chroma signals are led to a demultiplexer and read into the internal half picture memory. Selection results with the 100 Hz cycle rate of 32 MHz.

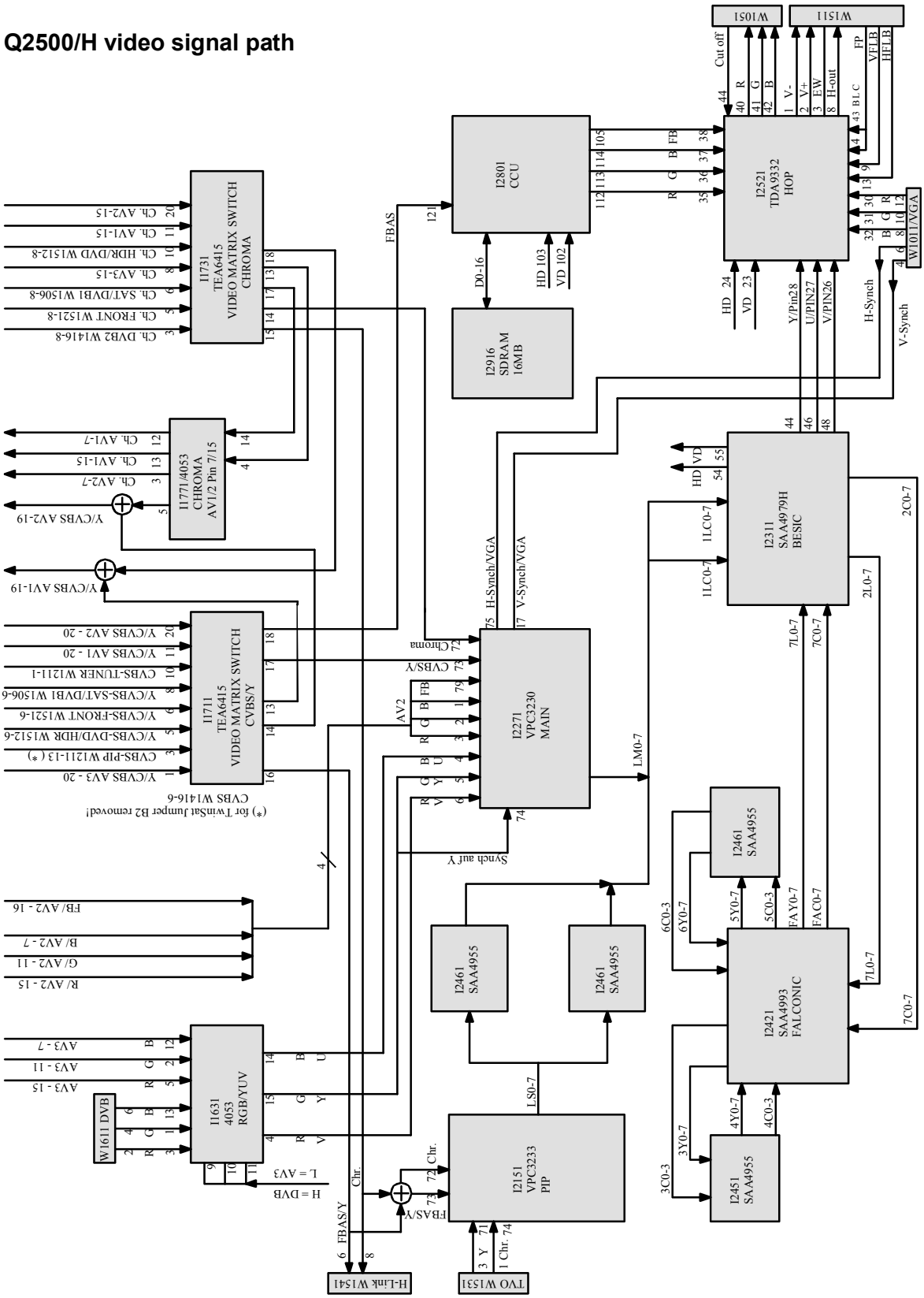
With 3 Mbit, slightly more than a half picture can be stored in intermediate memory, which permits continuous single and dual selection.
The next IC in the signal path, SAA 4993, is responsible for noise suppression and various interpolations. Noise suppression is implemented by signal from the output, which has already been processed, being delayed for a half picture by the second half picture memory and then mixed with the currently applied signal.

In addition, this IC suppresses the intermediate line shimmer. Line interpolation also occurs, so that 576 lines can be displayed in all zoom functions. Movements between the pictures are also interpolated, to ensure a continuous movement process over all half pictures.

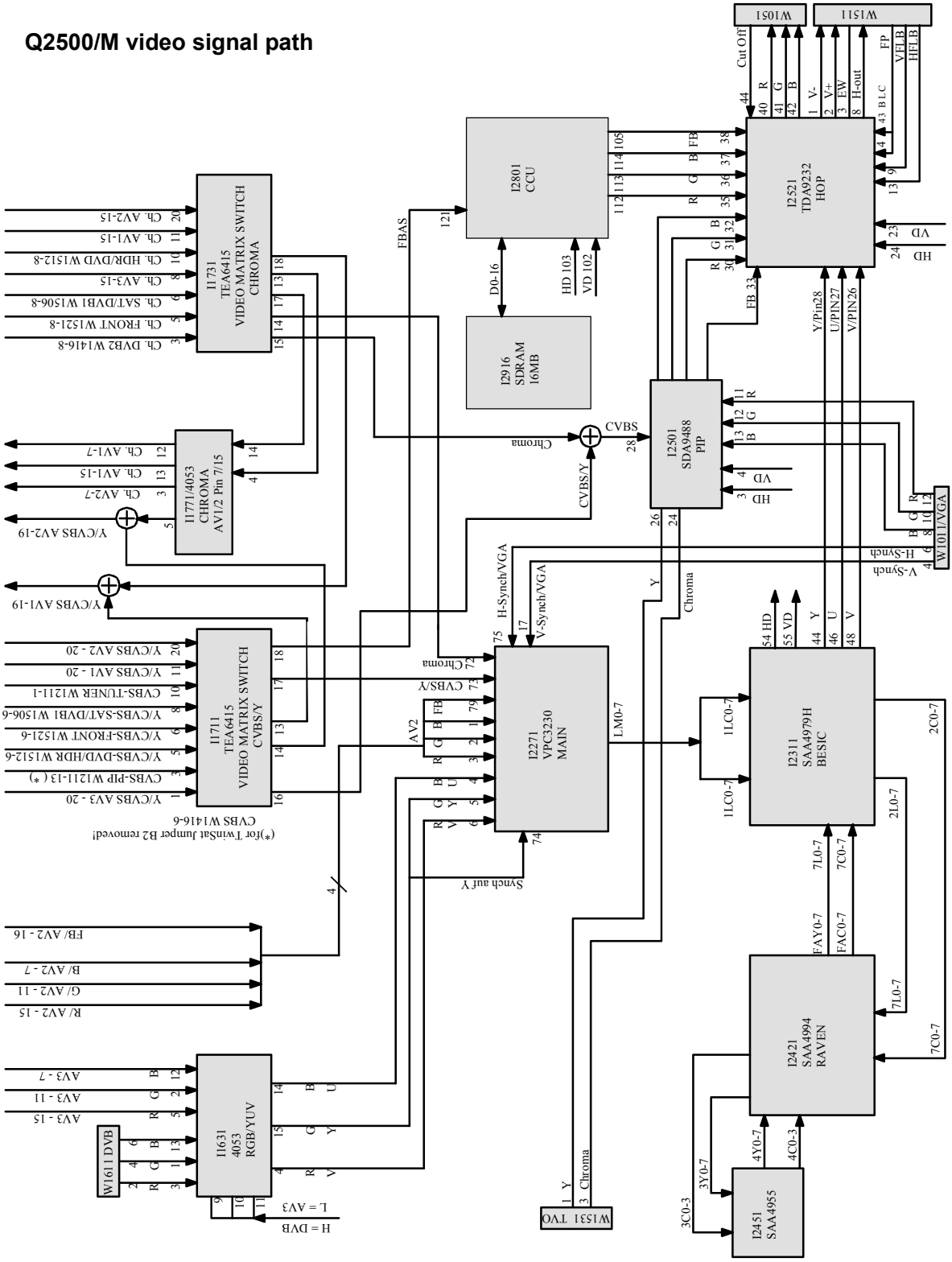
SAA 4979, which is the next IC in the signal path, is used mainly as a DAC and for the control of the digital 100 Hz video processing in the circuit.

In the chroma branch there is a circuit for improving colour transitions. It is used to increase the slope of the colour transition flanks in the differentiation and adder stages.

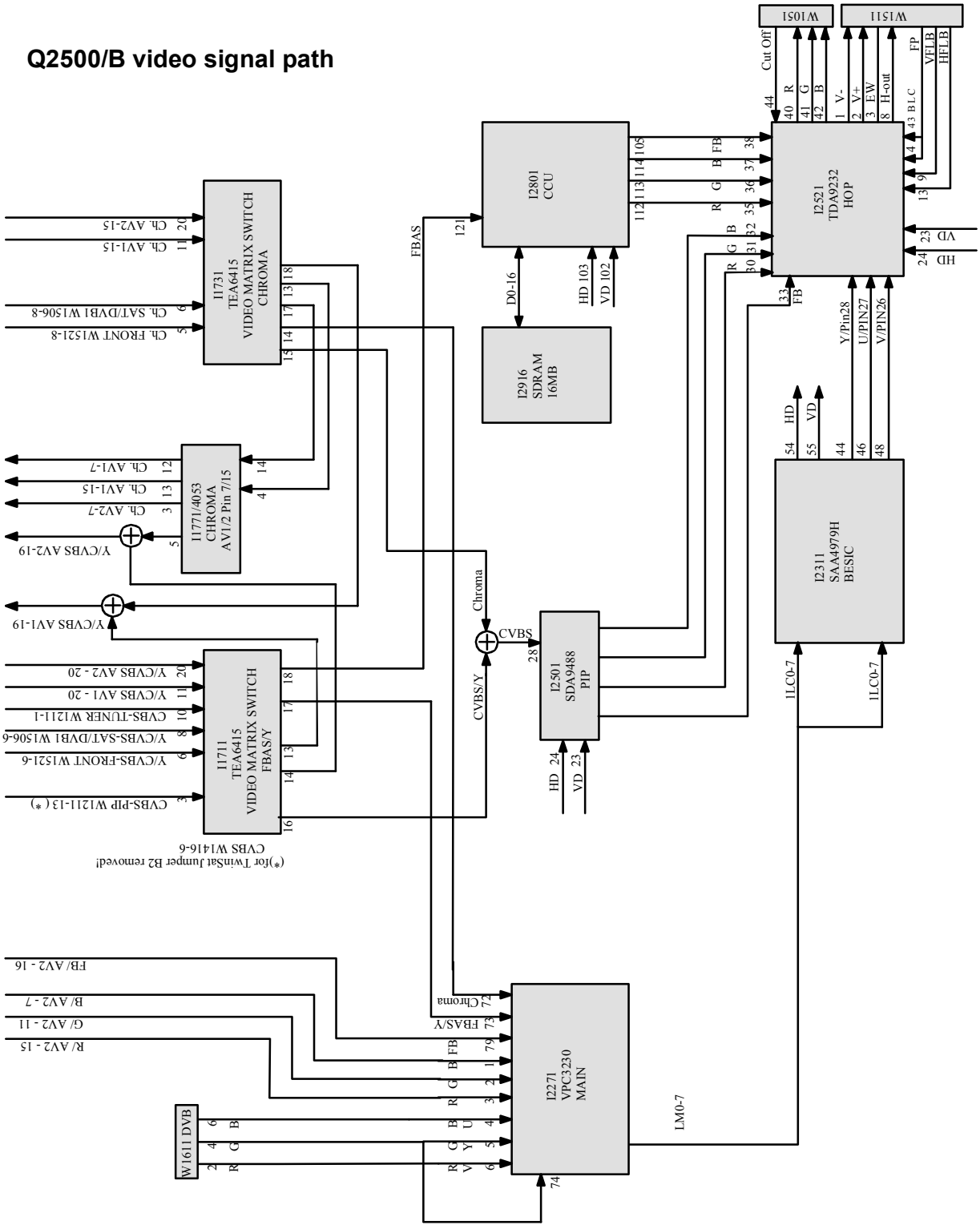
Q2500/H video signal path



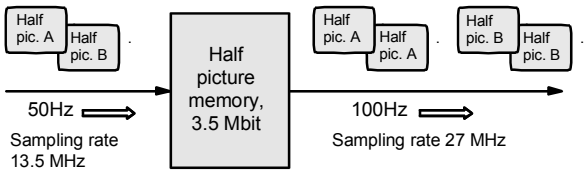
Q2500/M video signal path



Q2500/B video signal path



100 Hz principle



In the Y signal path there is a peaking circuit. It is used to produce black/white edges on overshoots, which increases the sharpness of the picture. The height of the overshoot can be adjusted with the "Sharpness" operating function.

With three output side DACs analogue Y-, R-Y- and B-Y- signals are produced, which are then output on pins 44, 46 and 48.

Finally the Y- and colour difference signals are fed through low-pass filters to filter out interference pulses and the residue of digitisation.

The last IC is the TDA 9332 for the 100 Hz colour signal processing. It controls the RGB power output stages to the c.r.t plate.

The Y-, R-Y- and B-Y signals output on pins 26, 27 and 28 produce RGB signals using analogue matrix circuits.

The IC carries out further processing of analogue RGB signals (twice), CCU signals (once) and signals from the optional VGA interface or online module. Depending on the associated blank information, both the internally produced and the two RGB signals from a selection circuit are switched.

The following integrated modules are responsible for colour saturation, brightness and contrast setting. Control is via the I²C bus from the CCU. The same is true for the white and black value setting. An automatic black value setting is also available. With this cutoff control, signs of ageing, e.g. the c.r.t, are corrected (see description of the RGB output stages).

The signals reach pins 40, 41 and 42 via the RGB output amplifier and are held there at 4 Vss for control of the speed modulator and the RGB output stages.

4.2.15 IC functions

The following paragraphs give a more detailed description of the functions of the ICs used for picture processing.

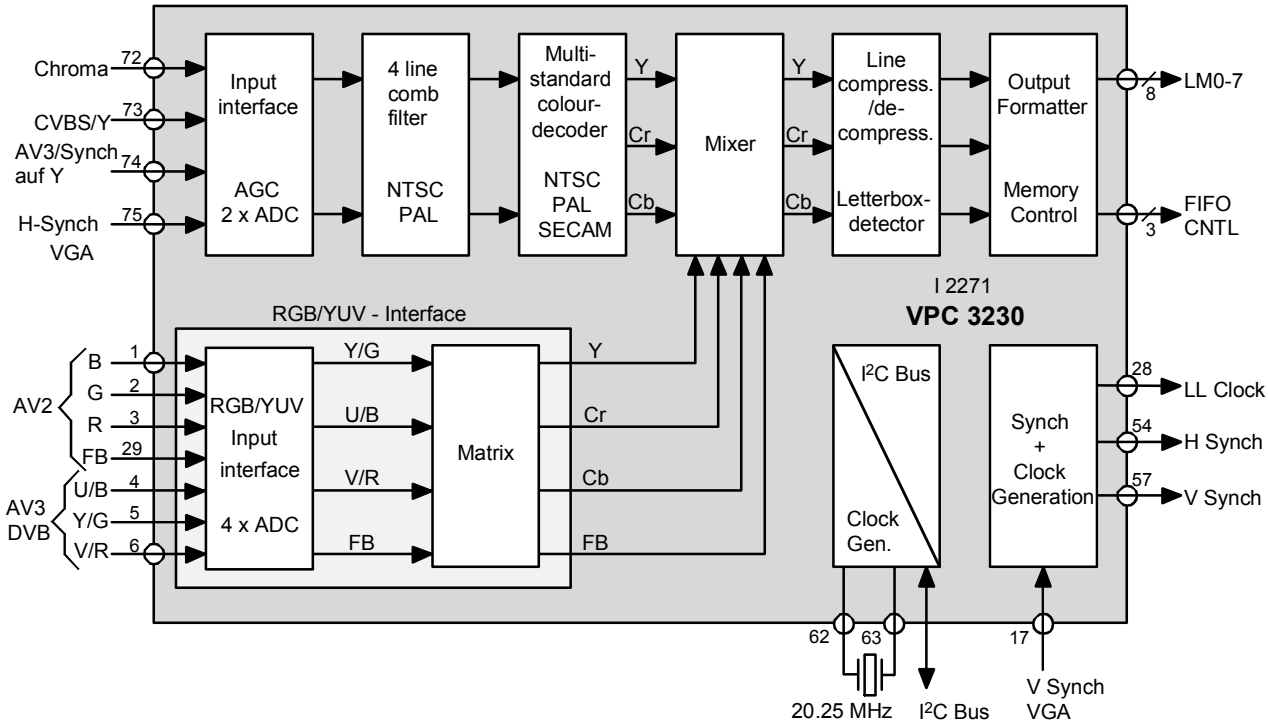
In the descriptions, the processes are shown in a much-simplified form. The operations necessary for the execution of the functions are inevitably much more complex.

4.3 VPC 3230

Video processor

The VPC 3230 is a recently developed video processor from Intermetall in 0.8 µ CMOS-technology. The functions are contained in an 80 pin PLCC housing.

VPC 3230 block diagram



The functions in the VPC 3230 can be roughly summarised into 9 blocks:

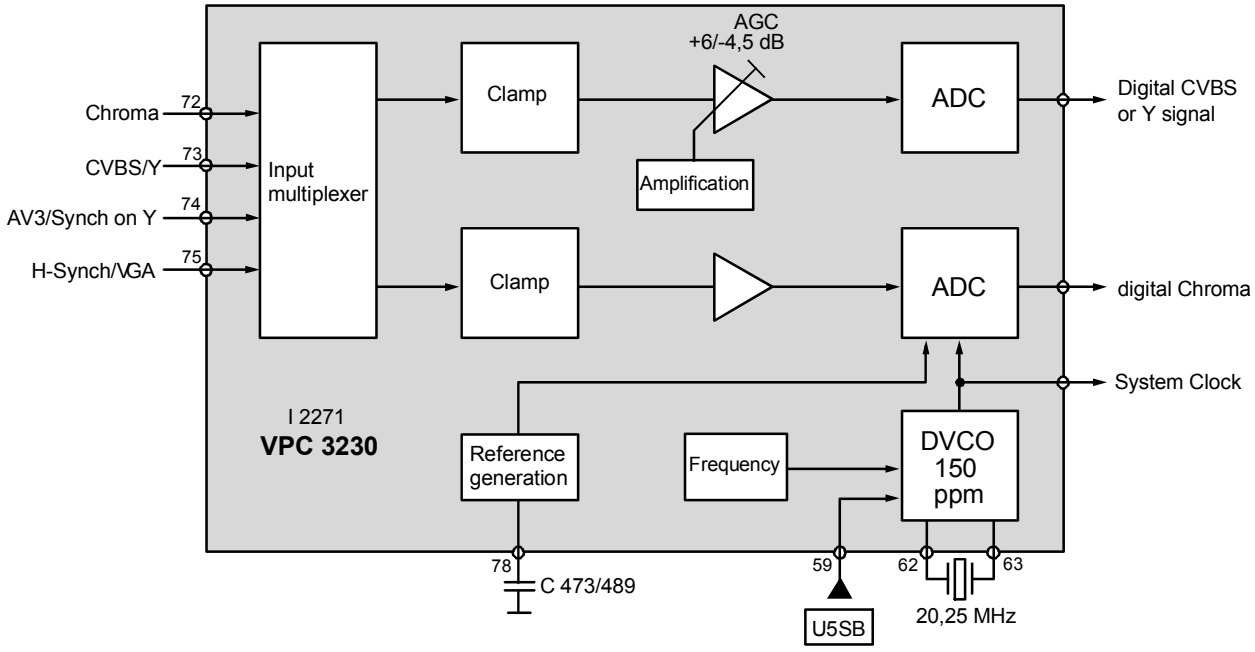
- Input interface with signal selection and two precision 8 bit A/D converters
- 20.25 MHz clock generator
- high quality, adaptive 4 line comb filter
- Multistandard colour decoder for PAL, NTSC and SECAM
- Letterbox detector
- Output format conversion (Output formatter)
- I²C bus interface
- Synchronisation block
- RGB/YUV interface

4.3.1 Input interface

On signal board Q 2500, the input multiplexer is switched in such a way that a choice can be made between two pairs of signals. If an FBAS signal, for example, is supplied by a receiver unit or a Y/C signal is fed to an interface, pin 73 for the FBAS/Y signal and pin 72 for the chroma signal are switched.

So that the signals from the ADC can be correctly digitised, two conditions must be fulfilled. The d.c. level and the amplitude of the signals must be adapted to the ADC . The d.c. level is defined by a signal clamp. For this there is a clamp circuit in the FBAS/Y path that clamps the signal to the rear black shoulder.

Block diagram, VPC 3230 input interface

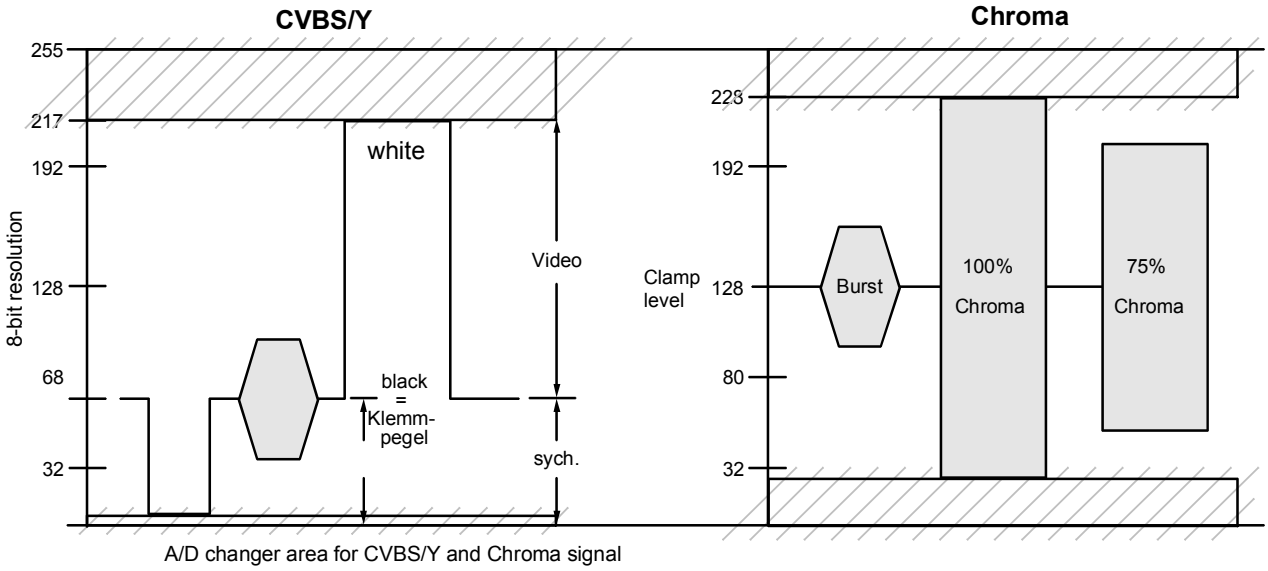


The chroma signal is clamped to its middle value. The following automatic amplifier control in the FBAS/Y path has a control range of -4.5 dB to +6 dB and ensures that even for different input levels the FBAS/Y signal is always optimally adapted to the ADC. In the chroma branch a fixed amplification is sufficient.

The FBAS/Y signal, as also the chroma signal for Y/C operation are digitised at a cycle rate of 20.25 MHz. The resolution of the two ADCs is 8-bit. Therefore, at the output of the input interface there is an 8-bit wide FBAS or Y data stream and for Y/C operation also an 8 bit wide chroma data stream. Both ADCs need a corresponding reference value. This is produced internally in the reference generation and stored externally on pin 78 by C 488/489.

4.3.2 20.25 MHz clock generator

The frequency determining 20.25 MHz Quarz X 2283 is connected to pin 62/63 of VPC 3230. The clock generator is controlled from the synchronisation block. In normal operation the clock generator is line frequency coupled. In the VCR mode, the line frequency coupling is switched off.



4.3.3 Comb filter

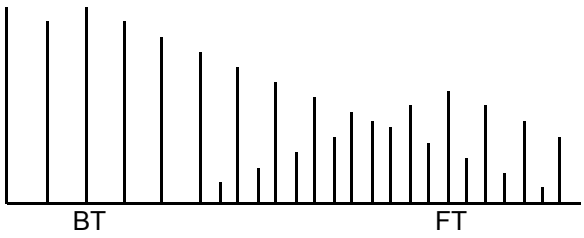
In this area of VPC the normally unavoidable Cross Colour and Cross Luminance interferences in the PAL system are eliminated.

In addition, the use of a comb filter even for colour transmissions permits the full 5 MHz Y resolution to be achieved. Without a comb filter it would be limited to approx. 3.8 MHz by the chroma trap, which would otherwise be required.

This function can be switched off, as it is the case that for all receiver-side circuits for picture improvement, even using a comb filter, there are some rare picture presentations which are not good. Switching off is implemented automatically via the analysis circuit. As this has error-free functioning, the user does not need to worry about switching off.

- **Function of a comb filter**

Let us consider the transfer method of the PAL signal. The brightness information determines that the full video bandwidth is not occupied for all frequencies, but only in specific areas. The colour information is inserted into these energy gaps.

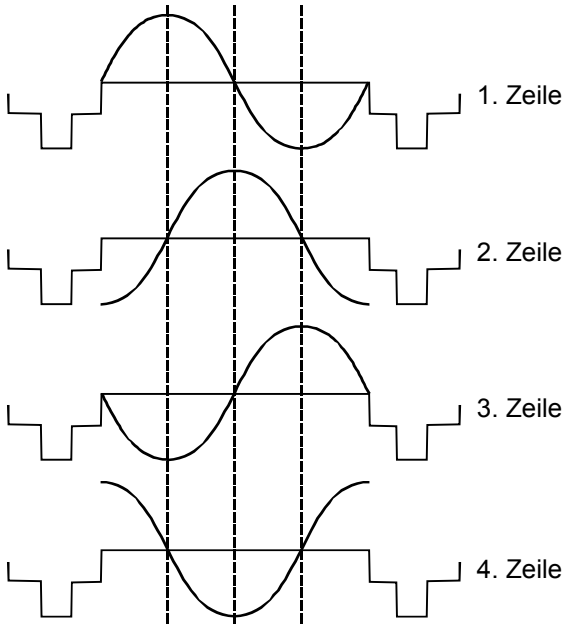


If the colour carrier is in one of these energy gaps, then all sideband frequencies are in the gap as well. For this the picture and colour carrier frequencies must be firmly coupled. The product of these two frequencies is an overlapping frequency. The sine waves cause light and dark pixels on the screen, which have a fixed position from line to line, so that on the screen these form a vertically placed light-dark pattern. The higher the colour car-

rier frequency the less pronounced the Moiré becomes.

In order to keep interference with the picture as low as possible, the phase position of the colour carrier frequency from line to line is shifted forward by 90°. In this way, bright and dark pixels only overlap after four lines. At normal distances the eye cannot detect this interference.

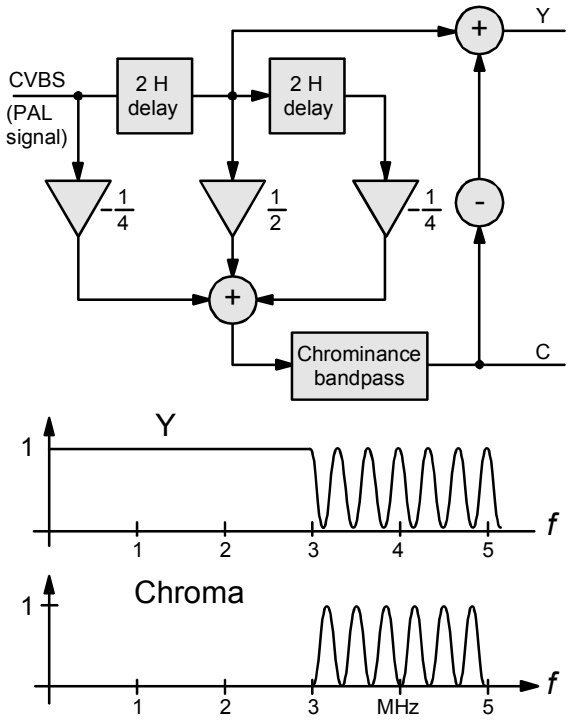
This compensation is known as "Fourth Line Offset Procedure".



This fourth line offset now permits the filtering out of colour components from brightness information, and the reverse. The phase shift from line to line causes a counter phasing of the colour carrier every two lines.

If a two-line delay line is inserted into the circuit and the direct and delayed signals are added together, the colour information is removed and the brightness information is present on the output at double the amplitude.

If one subtracts the two signals from one another, the brightness information is eliminated and the colour information is present at double the amplitude on the output of the circuit.



Theoretically this circuit supplies error free results. A condition for this, however, is the phase and amplitude equality of the chroma signal over 3 lines, which is only the case for the same and equally saturated colours. In practical terms picture joining can occur, in which cross colour and cross luminance interference cannot be removed by the comb filter. Therefore, another circuit is integrated, in which three lines in sequence, from the point of view of both phase and amplitude, are compared.

If a deviation is detected that goes beyond a specific difference, the comb filter function is automatically switched off and the separation of the two components is implemented traditionally with chroma trap and band pass.

As VPC 3230 requires four lines to determine whether the comb filter is to be switched off, the filter operates more efficiently and more frequently than for a two line comb filter.

4.3.4 Multi-standard colour decoder

This block executes demodulation for all TV standards - PAL, NTSC and SECAM. Additional external components are no longer required. On the output of the colour decoder there is an 8 bit wide luminance and chrominance signal respectively in 4:2:2 format.

The VPC monitors the Auto S-VHS detection by means of the colour decoder for the separate chroma line of the colour burst. If signals are fed in from a VHS video recorder, then no burst is present on a separate chroma line. This is in turn communicated to the CCU. The CCU switches to VHS operation. If an S-VHS recorder is connected then a colour burst is measured on the chroma line on playback and the CCU switches the VPC to S-VHS operation via the I²C bus.

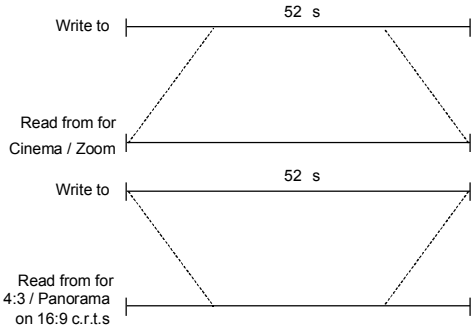
4.3.5 Line compression and decompression

To reproduce 4:3 pictures on a 16:9 c.r.t., and also for the various zoom modes, the video signal must be lengthened, or stretched, horizontally. For this the VPC 3230 has a line memory. Selection occurs at a slower speed, with the line beginning and end not being read (zoom, cinema)

However, quicker selection is also possible. For this the start is delayed with respect to the deflection and the selection is ended before the line end of the deflection (4:3 and Panorama for the 16:9 c.r.t).

The vertical correction of the signal is achieved by the line interpolation in SAA 4991.

Line compression/decompression

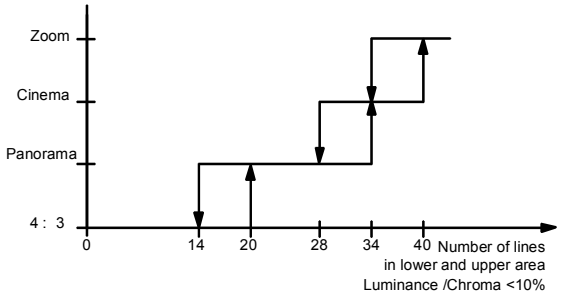


Letterbox detector

For Cinemascope or other film standards upper and lower black bars of various thickness are visible. These black bands can be removed by various zoom functions or at least reduced. Devices with 16:9 c.r.t.'s are also fitted with an automatic format conversion. Depending on the thickness of the black bars this automatic movie detection - AMD – switches between three different zoom modes. For this the Letterbox detector measures the luminance and chrominance components in the upper and lower area.

If, within defined lines, luminance and chrominance values of less than 10% are measured, the CCU switches the deflection controller and the display processor to the appropriate geometrical format. As programme logos are often placed on the right and left of the black bars, no measurement takes place in this area.

Automatic format conversion for 16:9 devices.



As 4:3 picture presentation with upper and lower black areas can lead to false results, the analysis occurs 4 sec. before switching occurs. If, however, undesired conversion processes occur, the function can be switched off with the remote control.

4.3.6 Output format conversion

Up to now luminance and chroma signals have been processed IC internally at a cycle rate of 20.25 MHz. For additional processing by the 100 Hz Philips IC set, an output cycle rate of 13.5 MHz is required. In the Output Formatter, therefore, the output data is converted from 20.25 MHz to 13.5 MHz. The YUV output format is also converted at this stage to 4:2:2 and output by a multiplex procedure to 8 lines. The multiplex cycle rate must therefore have the double cycle rate of 13.5 MHz. The multiple cycle rate on pin 27 of I 2271/ therefore has a frequency of 27 MHz.

4.3.7 Synchronisation block

The synchronisation block generates all the synchronous, sampling, cycle and clamp signals that are necessary for internal and external signal processing.

Before the digital video signal reaches the horizontal and vertical synchronous separation stage, it passes through a 1 MHz low-pass. With the low-pass, video and noise components >1 MHz are suppressed. All signals that are required for the various processing steps in the VPC are controlled via an internal PLL stage and counter.

No special synchronous signals are used for other external signal processing. The SAA4979 detects picture and line start from the data delivered by the VPC, and for further signal processing produces independent V/H synchronous signals. The VPC 3230 supplies the 27 MHz multiplex cycle to pin 27 for the digital luminance/chroma signals.

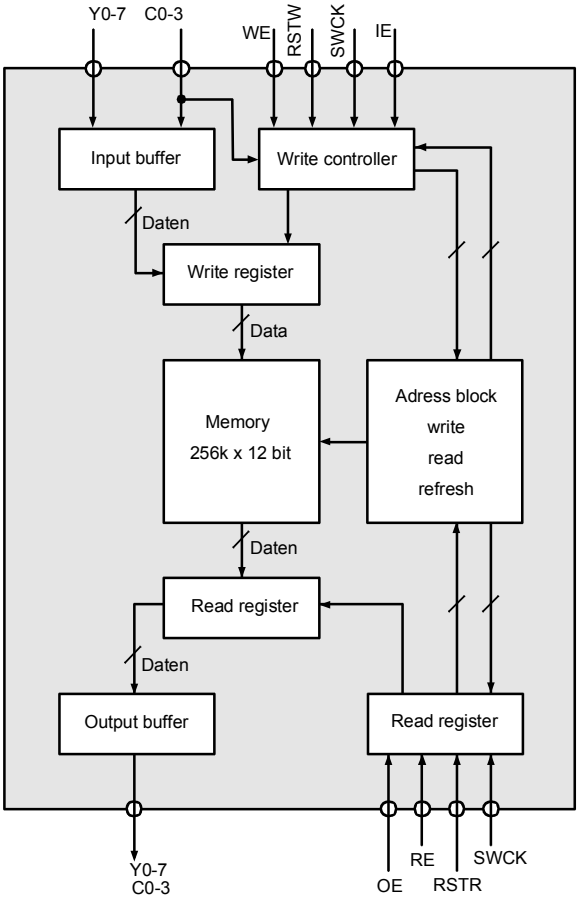
4.3.8 I²C bus interface

Communication between C 161 and VPCm is via the I²C bus interface. The register in the VPC is loaded via this interface after start up and the status in operation is selected via it.

4.4 Half picture memory SAA4955HL

The two memory IC's and the memory integrated into the SAA 4979 are functionally identical, their tasks , however, are different.

SAA4955HL block diagram



The picture memory in SAA 4979 is for the actual 100 Hz function in the circuit, whereas picture memories 2 and 3 I 2451/ I 2461 facilitate noise suppression, the suppression of line quivering, interpolation and a full line freeze frame by a delay of 1 half picture.

Data writing and reading for the two memories take place completely independently of each other.

Inputting and outputting for a single memory is also separately controlled. Data is therefore written to one area of the memory, whilst it is read from another area.

4.4.1 Storage space

The IC is organised into in 256 k words each of 12 bit. Two independent clock signals for writing and reading allow these functions to be carried out concurrently and independently.

A total of 3 072 000 bits can be stored, which corresponds to a little more than one half picture.

This comprises the following:

Sampling rate 16 MHz at a line frequency of 15.625 kHz

$$\frac{16\ \text{MHz}}{15.625\ \text{kHz}} = 1024 \text{ sampling values per line}$$

As the synchronous pulse and the front and rear black shoulder are not required, there are 832 sampling values per line for the actual picture signal. A sample value corresponds to one displayed pixel on the screen.

The sampling gap is not required in the vertical direction either. There are therefore 290 lines per half picture.

832 pixels x 290 lines = 241 280 pixels

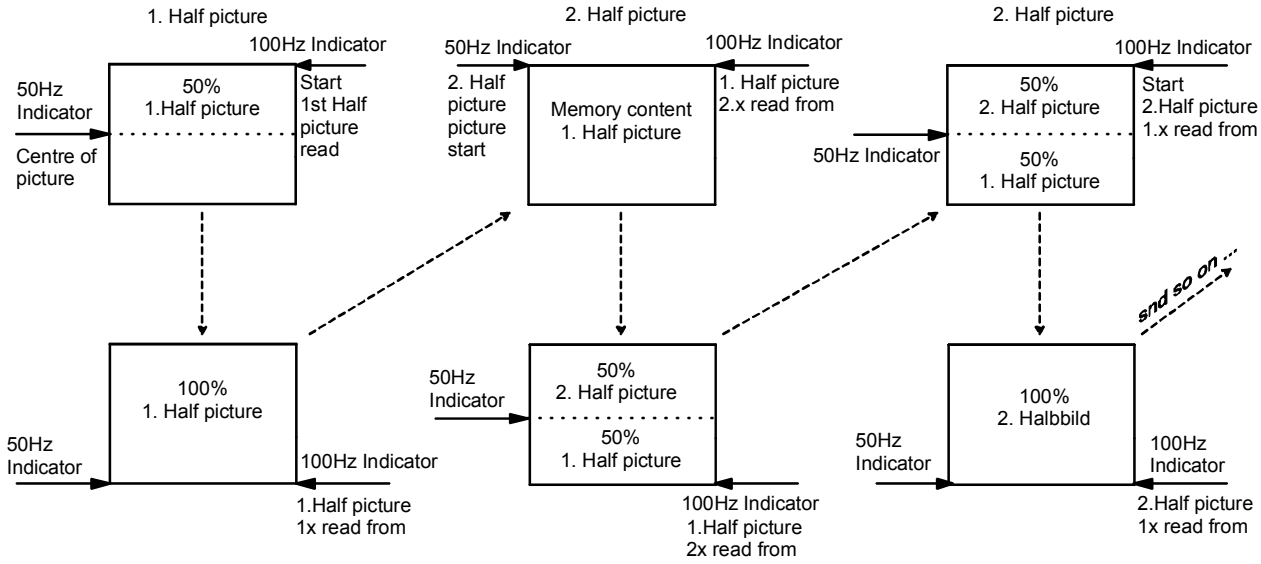
Therefore for each half picture 241 280 pixels must be stored. At a resolution of 8 bit Y and 4 bit chroma

241,280 pixels x 12 bit = 2,895,360 bit

are required for half picture storage capacity.

The 3 Mbit is sufficient for the separate, continual inputting and outputting of this function.

50/100Hz write/read cycle



4.4.2 Conversion of signals in 100 Hz in memory 1

Frequency doubling takes place in the half picture memory 1 (in I 2311), as it is read at double speed. This means it is possible to read the memory twice, whilst it is only written to once. The first reading of a half picture always starts when a little over half the picture is in memory. Due to the double speed, writing to and reading out end at about the same time. As the return times at 100 Hz are also twice as fast, reading out starts before writing to. The picture is therefore read out for the second time and during this time up to half of the next half picture is written to memory.

4.4.3 Half picture memory 2 and 3

In this half picture writing to and reading out of memory take place at the same speed. The half picture is read to memory a second time and so delayed by a half picture. This means that half picture A can be written to and read from memory, whilst the same is happening in memory 1 for half picture B.

4.4.4 Control pulses

The memory is controlled by the following pulses:

pin 22: SWCK (Serial Write Clock)
Cycle for reading in the Y/C signals to the memory.

pin 23: RSTW (Reset Write)
The address counter for writing at the start of the memory area is set at H level.

pin 24: WE (Write Enable)
So long as H level is present, the address counter continues counting to write with WCK.

pin 25: IE (Input Enable)
Data inputs for Y/C signals are released at H level.

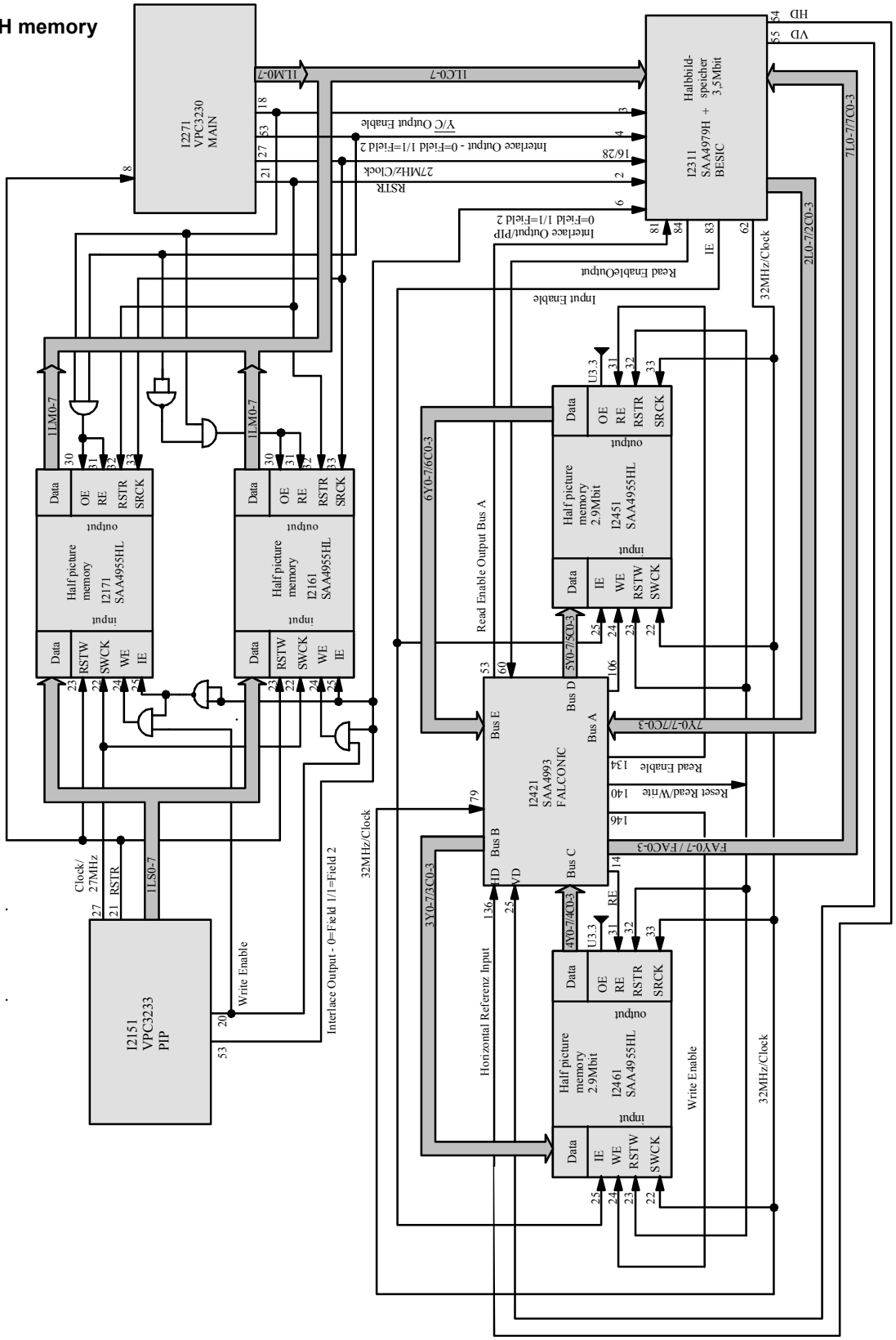
pin 30: OE (Output Enable)
Data outputs for Y/C signals are released at H level.

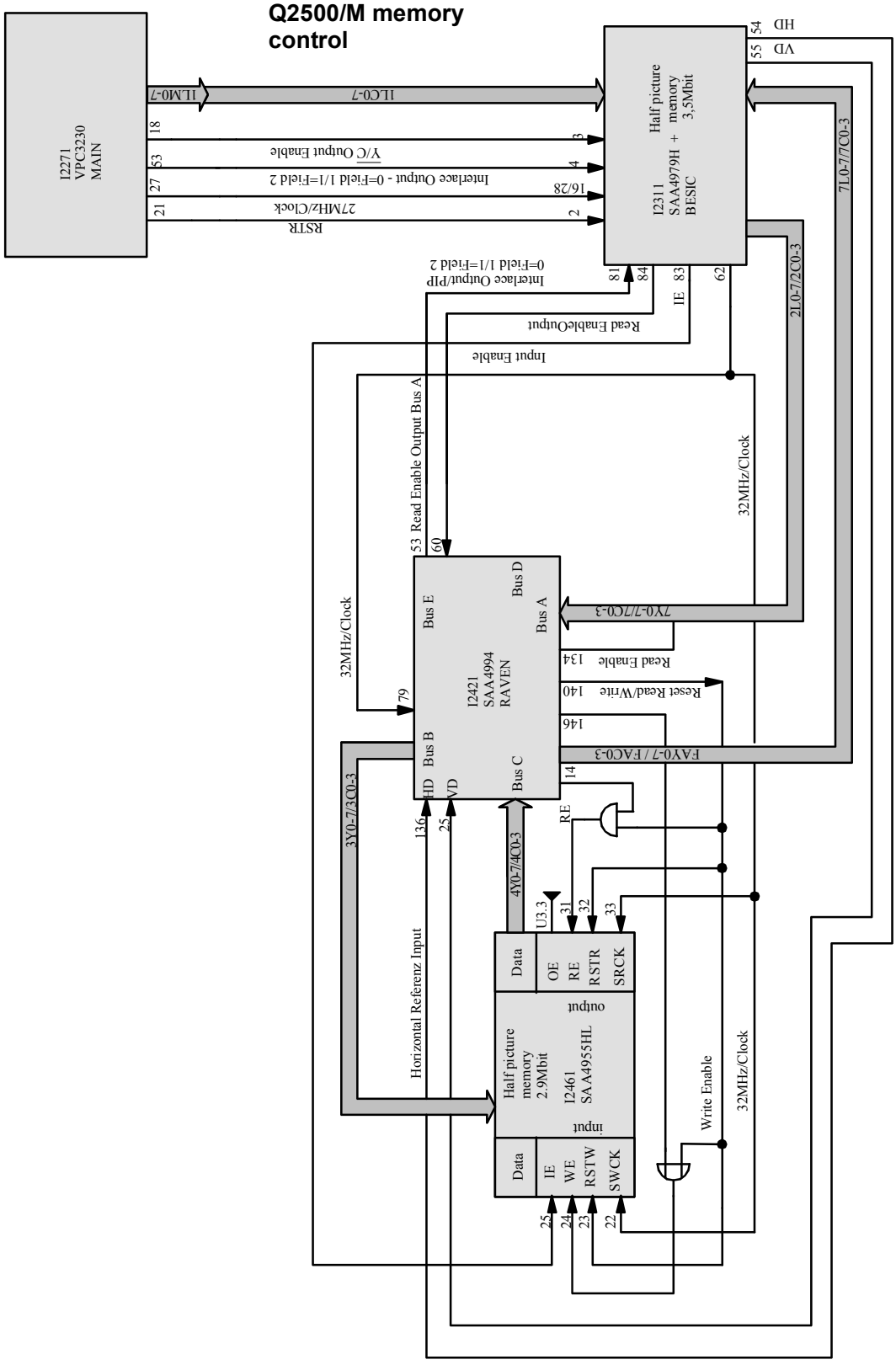
pin 21: RE (Read Enable)
So long as H level is present, the address counter continues counting to read with RCK.

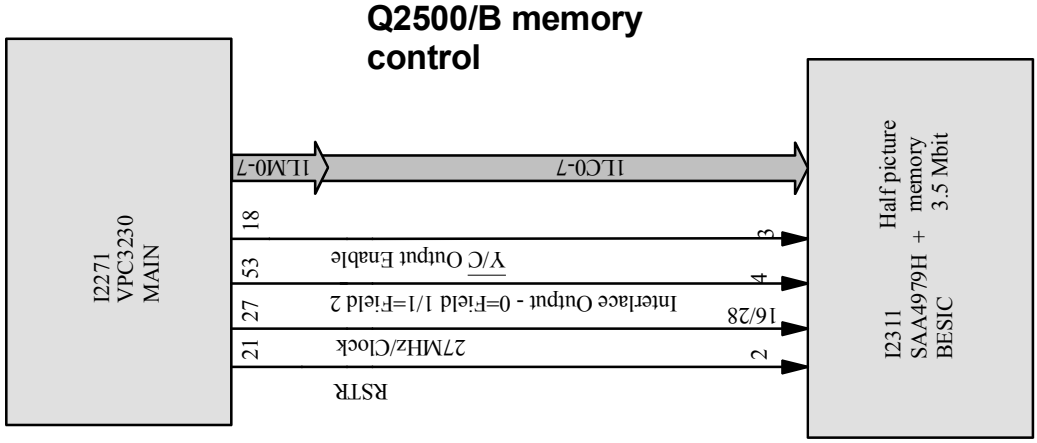
pin 32: RSTR (Reset Read)
H level sets the address counter to read at the start of the memory area.

pin 33: RCK (Read Clock)
Cycle for reading the Y/C signals from the memory.

Q2500/H memory control




Q2500/M memory control
I2271 VPC3230 MAIN
ILM0-7
ILC0-7
18
53
27
21
Y/C Output Enable
Interlace Output - 0=Field 1/1=Field 2
27MHz/Clock
RSTR
I2311 SAA4979H + BESIC
Half picture memory 3,5Mbit
HD
VD
54
55
7L0-7/7C0-3
2L0-7/2C0-3
16/28
Interlace Output/PIP 0=Field 1/1=Field 2
81
84
83
62
IE
Read EnableOutput
Input Enable
32MHz/Clock
53 Read Enable Output Bus A
60
I2421 SAA4994 RAVEN
Bus E
Bus D
Bus A
Bus B
Bus C
7X0-7/7C0-3
Read Enable
134
Reset Read/Write
140
146
FAY0-7 / FAC0-3
14
79
HD
VD
136
25
3Y0-7/3C0-3
4X0-7/4C0-3
RE
U3.3
31
32
33
Horizontal Referenz Input
Data
OE
RE
RSTR
SRCK
output
Half picture memory 2.9Mbit
I2461 SAA4955HL
input
Data
IE
WE
RSTW
SWCK
Write Enable
32MHz/Clock
25
24
23
22



4.5 Falconic module SAA 4993

With the conversion of a picture signal to a line coupled sampling and level adaptation at 3.3 V, 100 Hz is achievable with a 3 Mbit picture memory and a memory controller

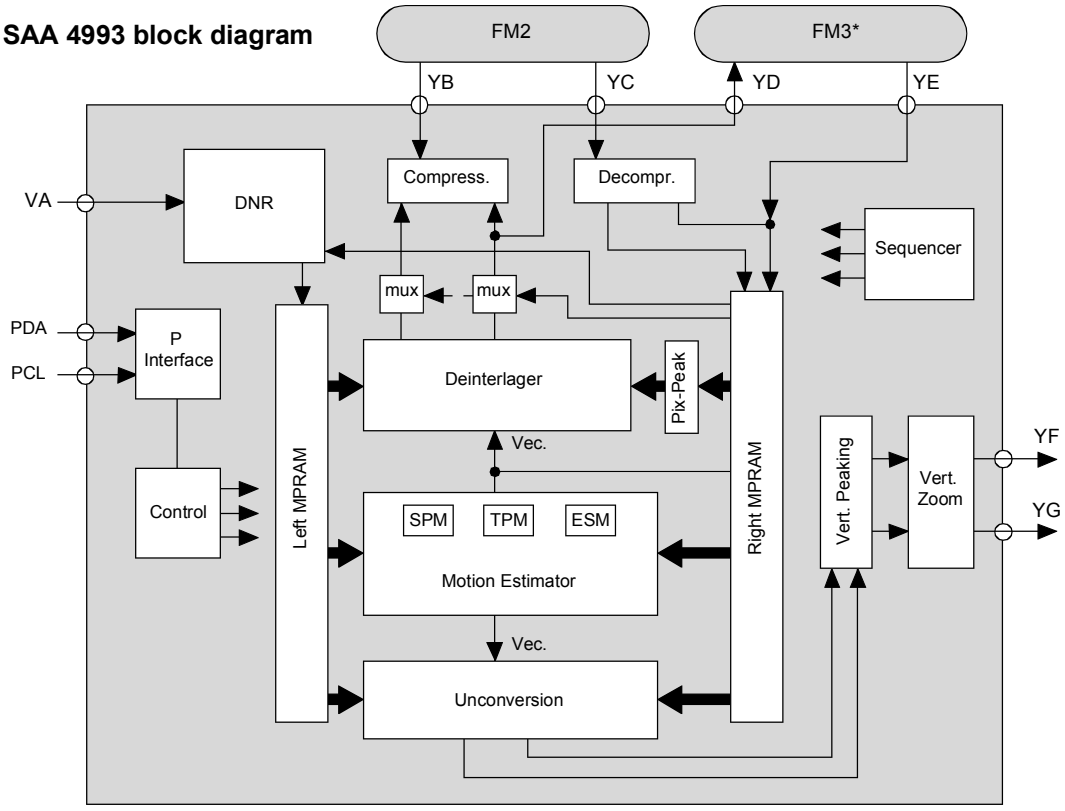
As doubling of the picture change frequency, depending on picture quality and picture presentation, can lead to undesired side effects, a number other features are provided on the Q 2500 chassis. This means that the side effects can be compensated for.

4.5.1 Noise reduction

Together with a second picture memory, SAA 4993 is able to eliminate some of the picture noise that occurs owing to an inadequate antenna signal.

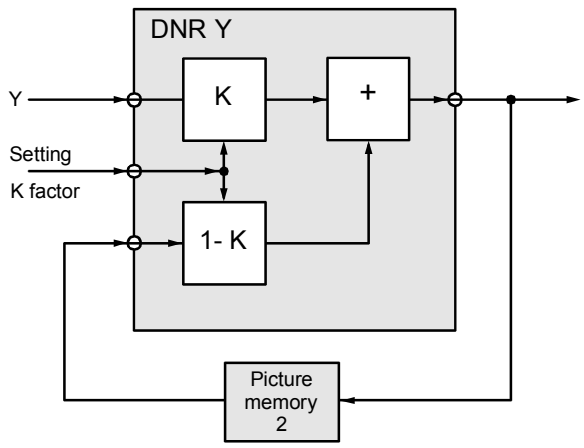
Internally the IC has two separate signal paths, one for the Y and one for the chroma signals. Functionally they are both identical. In the chroma path is a demultiplexer on the input and a multiplexer before the output.

SAA 4993 block diagram



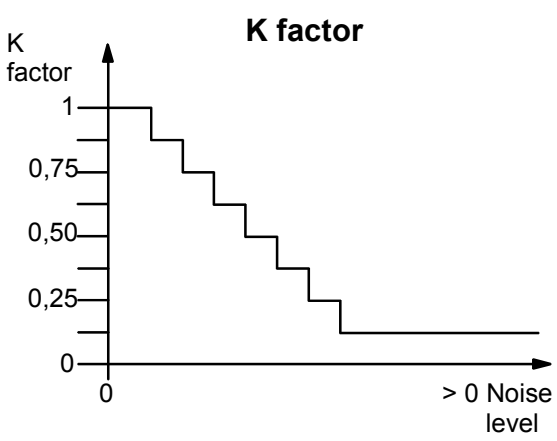
* (SAA 4994 does not control FM3)

Principle noise suppression



Simply expressed the noise suppression system consists of the current half picture signal, in which components of the previous signal are mixed. The composition of the output signal, that is the number of components of the direct and the number of components of the delayed half picture, are determined by the so-called K factor. This K factor is determined by integrated automation.

When using the automation the K factor is dependent on the movement between the half pictures. If there is a lot of movement, noise suppression is not very effective.



Information about the size of movement is provided by the movement detection. This occurs only in the Y branch, with which the K factor is set simultaneously for chroma and Y.

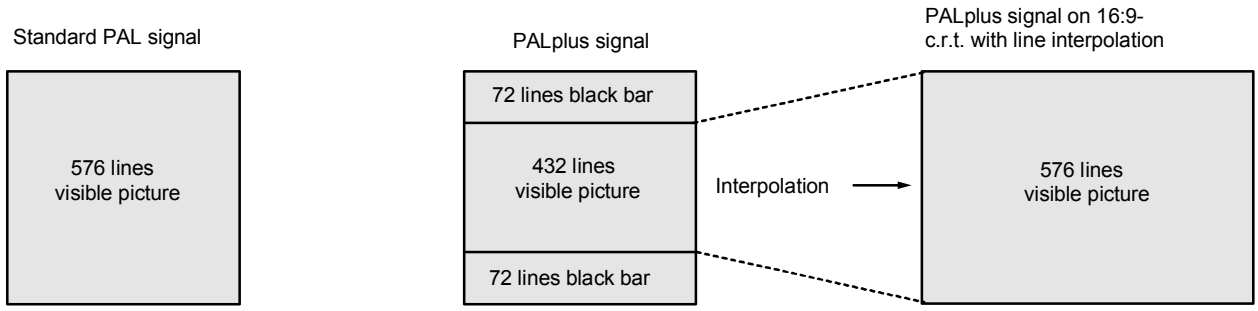
The drawing shows the DNR principle for the Y path. As already mentioned the circuit in the chroma path is identical. The K factor can have a value from 0 to 1. At K = 1, 100% of the direct signal and 0% of the delayed signal is switched to the following "And". No noise suppression is therefore available.

In the other extreme case K = 0, only the delayed signal would be switched, which would correspond to a freeze frame. To avoid this the K factor in our TV sets can never be 0.

Otherwise it would only be programmes with a weak signal that would be incapable of being displayed.

4.5.2 Line interpolation

The line interpolations circuits allow a situation to be achieved in which a full-line picture is written for PALplus signals . The advantage with respect to a PALplus decoder is that even without a PALplus signal, the interpolation in all zoom modes delivers a full-line picture. This function is explained in the following paragraphs for PALplus, in the zoom functions the circuit operates similarly only with other factors.



A standard PAL signal consists of 576 visible lines. For PALplus, 144 of the lines are dark sampled and only 432 lines are transferred as a visible picture. In 16:9 c.r.t's these signals are shown in the ZOOM mode. In order to display 576 lines the information for 4 lines must be determined by 3 lines respectively. This computer operation is very complicated and will therefore not be explained here.

Line interpolation must be carried out both in chroma as in the Y branch.

4.5.3 Movement detector

In the Y branch there is a movement detector. Here current and previous half pictures are compared with each other. An assessment is made of whether it is a question of full pictures in Cinema Scope format. The CCU receives this information via the microprocessor for the Automatic Movie Detection (AMD). The movement detector is also responsible for the setting of the noise suppression K factor.

In addition, using the movement from the previous to the current half picture an assessment is made of how the movement between the two half pictures could behave. In this way, in the movement compensation stage immediately following a new half picture can be calculated. At the same time it must be taken into account that the two half pictures, contain the intermediate lines for the other half picture respectively. In this way a continuous process of movement over all half pictures is achieved, both for horizontal as well as vertical movements. The DMI (Digital Moving Interpolation) function is active for both full picture presentation and for standard video signals.

The operation of this switch is largely error free. Nevertheless, under unfavourable conditions negative effects can occur, therefore the DMI function can be switched off. Instead, the DLC (Digital Lineflicker Control) function is switched on.

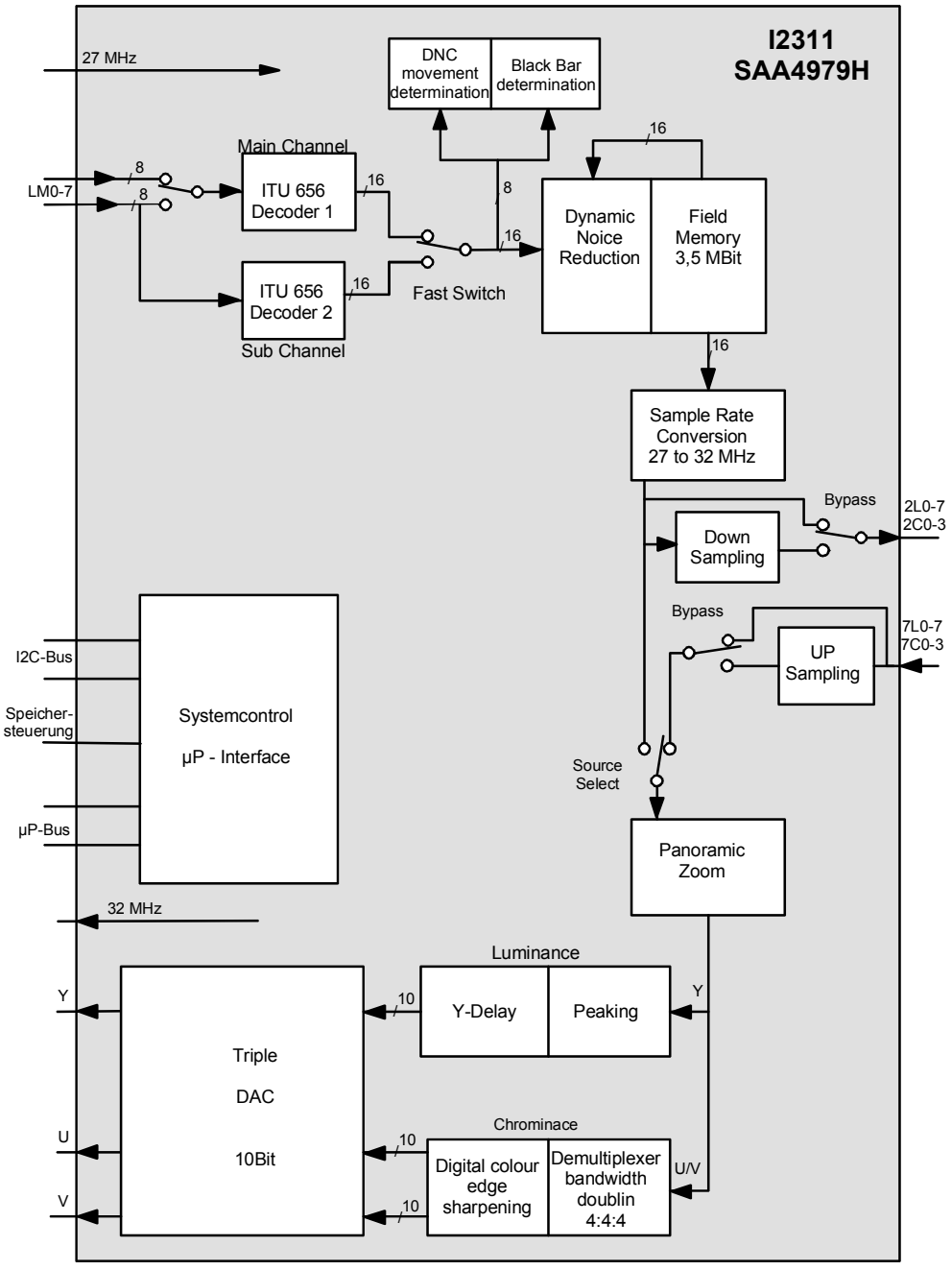
4.5.4 Memory control

Control of the SAA 4993 is implemented via the µP interface from I 2311. The µP bus is assigned to pins 26 (DA) and 27 (CI). In addition it is here in conjunction with the Memory Controller that writing to the 2nd picture memory and reading from the two memories is determined.

4.6 SAA 4979 (BESIC)

The next IC in the signal path, the SAA 4974, is designed for the following functions.

- Demultiplexer for luminance/chroma separation
- 3.5Mbit memory for 50/100Hz conversion
- Cycle rate converter from 27MHz to 32MHZ
- Two signal paths for the separate processing of the Y and chroma signals
- Demultiplexer for the chroma signals
- Band width doubling and digital CTI circuit for improved colour transfer
- Peaking circuit Y branch to increase picture sharpness
- Three blank stages for dark sampling
- Three 10 bit DACs for the generation of analogue R-Y-, B-Y- and Y-signals, I²C bus interface and timing control for the control of the individual processes through the microprocessor.
- Microprocessor bus for the control of the SAA 4993.
- Control of write and read processes in the half picture memory, as well as the total digital 100 Hz video signal processing.
- Generation of a 32 MHz cycle.
- Generation of H and V synchronous pulses for the TDA9332 video/deflection processor.

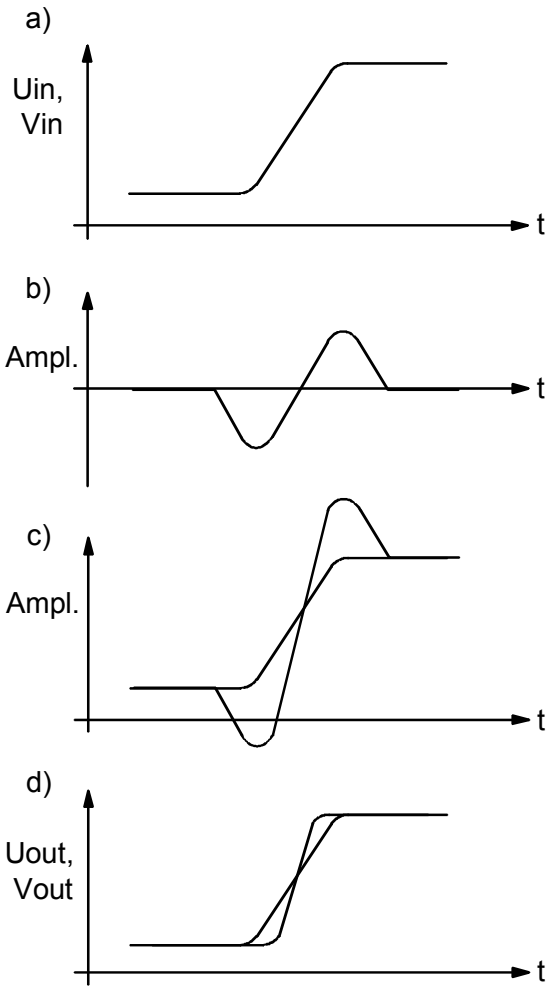


4.6.1 Chroma branch

In the design of the colour television transmission the compatibility with normal black/white systems must be observed, in order for colour transmissions to be received by black and white sets. For this reason the colour information must be integrated into the available frequency spectrum used for the brightness information.

Secondly, to prevent interference the bandwidth for the colour signal must be kept as narrow as possible. For this reason a bandwidth of only 1.2 MHz was selected and the carrier frequency set at 4.43 MHz.

Owing to the narrow bandwidth the rise times for colour change are very long, which appears on the screen as "washed out" transitions.



a) U, V input of SAA
b) U, V Correction signal
c) U, V input + Correction signal
d) sharpend and limited U, V

To compensate for this deficiency, two circuit components are incorporated into the SAA 4979, with which short rise times can be achieved artificially, thereby improving the colour transitions.

In the circuit before these components is a demultiplexer, with which 8-bit wide parallel R-Y- and B-Y signals respectively are derived from the supplied signals.

4.6.2 Band width doubling

In order to increase the effectiveness of the colour flank increase on the supply side, a doubling of the bandwidth from 4:1:1 to 4:2:2 is implemented.
Using a linear phase interpolation filter additional sampling values are calculated from the available chroma sampling values.

These calculated sampling values are inserted respectively between two available values, by which means the bandwidth is doubled. In this way, steep flanks can be transmitted more easily.

4.6.3 Colour flank sharpening

An improvement of the colour transition is achieved by a dual differentiation of the original chroma signal and the ensuing subtraction of the derived correction signal of the chroma signal.

The changes in these signals are evaluated in separate circuits for U and V, and if a threshold value specified by the software is exceeded a correction value is calculated. After the two derived correction signals have been cleaned of noise components, they are subtracted from the available chroma signals U and V. The subtraction is implemented by inversion of the correction signals and subsequent addition with the original signal.

To avoid colour phase errors by the overshooter, it must be blocked by limiter stages.

Here analogue signals are produced from the respective 8-bit wide digital R-Y and B-Y signals, which are then output at 1.8 Vss on pins 46 and 48.

4.6.4 Y signal path

The peaking circuit is not used. The signal is led directly to the sampling stage. This operates in the same way as the sampling stage in the chroma branch.

Via the sampling circuit, the digital Y signal, which is now 9-bits wide, reaches a DAC, which generates an analogue signal. This is then output on pin 44 at 1.5 Vss.

4.6.5 Microprocessor interface

All processes in the SAA 4979 are controlled by SDA6000 via the I²C bus 0 (pin 1 = SDA, pin 2 = SCL). In addition, information for the SAA 4993 and the memory control is also transferred.
The SAA 4993 is controlled by the BESIC via the microprocessor bus to pins 108 (µP DA) and 107 (µP CL).

Switching outputs 4 are used for the switching of the VGA synchronisation. If a switch is made to the VGA programme location, then pin 4 is switched from I 2311 to L level. With this logic state the vertical synchronous pulse of the VGA interface W 1011 pin 4 is switched directly to the video/deflector controller I 2521 via the four Nand gates I 2361 A/B/C and D. The VGA synchronous pulse is, in addition, monitored by I 2271 on its pin 17. If no synchronisation or false synchronisation is detected, I 2311 resets its output on pin 4 and thereby switches over to internal V synchronisation.

4.6.6 Control of the 100 Hz processing (Display)

This stage synchronises the read out from the half pictures and the writing to memory in the second memory. As the signals in the SAA 4993 are written to and read out, it has direct control and is only synchronised by the BESIC.

Via pulse RE (pin 84) the Falconic module controls the reading from both half picture memories and the writing to the second memory.
With pulse IE (pin 83) SAA 4979 controls the data inputs in the second half picture memory. With L level a switch can be made to freeze frame, for example.

Furthermore, the display stage gives a horizontal pulse on pin 54 and a vertical synchronous pulse on pin 55 for the synchronisation of the deflection in TDA9332. At the same time, the vertical pulse VD acts as a reset for the Falconic and the half picture memories, for resetting the address counter on reading from the memory and for writing to the second memory.

4.7 Video/deflection processor TDA 9332/Range Video/RGB path

The last IC for picture signal processing, apart from the RGB output stages, is the TDA 9332. It also controls the deflection stage.
Inputs for analogue R-Y, B-Y and Y signals:

- Two RGB inputs for analogue signals from the CCU and the VGA interface and/or picture in picture generation
- Matrix circuits for RGB generation from the difference signals
- Signal selection for the switching of the required RGB signals
- Y and colour difference matrix for the generation of Y and difference signals from the selected RGB signal
- Hue control for NTSC operation and gamma correction in the Y branch
- Saturation, contrast and brightness setting

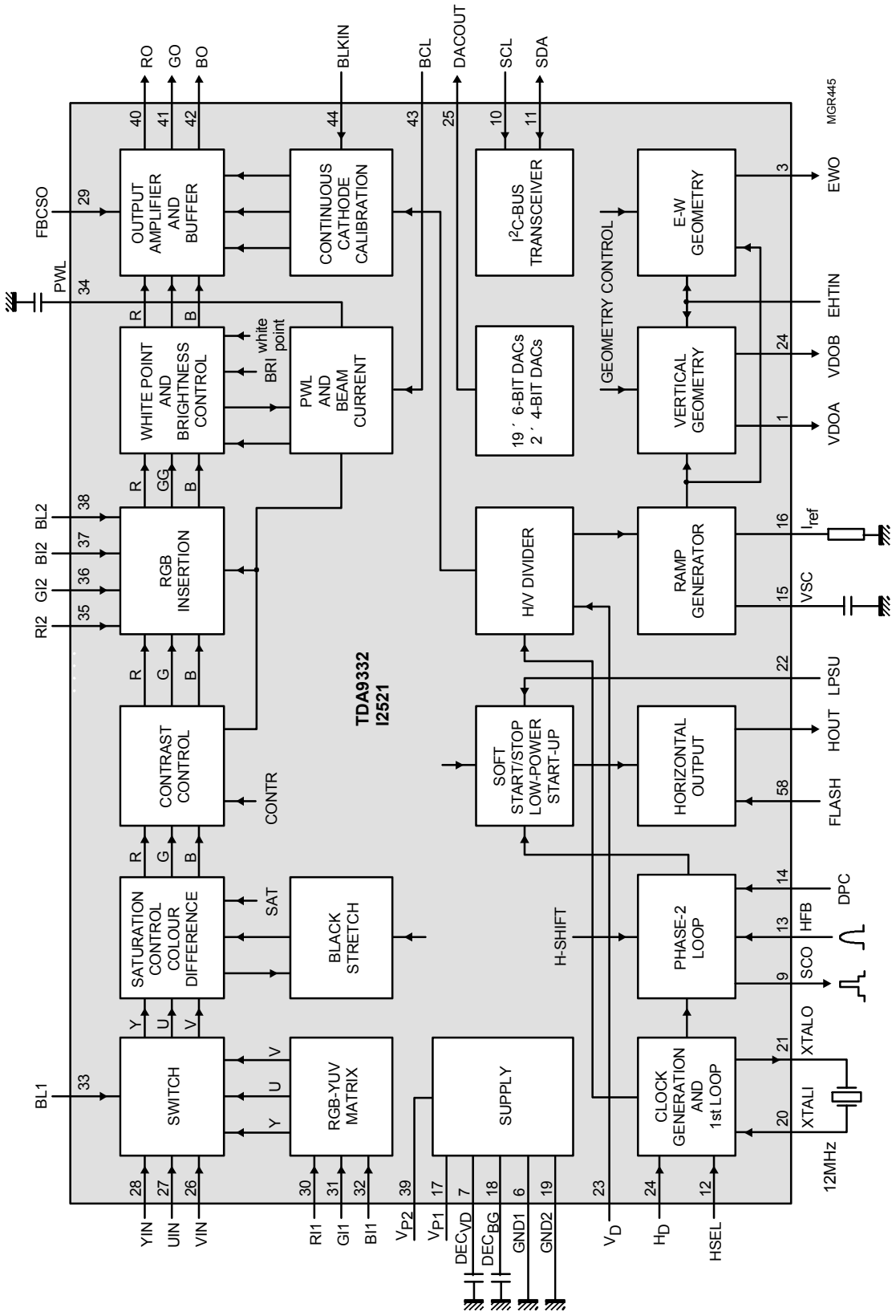
- RGB driver stages
- Beam current limiter circuit
- Automatic cut off control
- I²C bus interface and control register
- DAC for programmable d.c. voltage

– PLL for generation of cycle frequency
– Control block for the synchronisation of the output stages
– DAC for O/W, V control and H output stage
– Beam current dependent correction of the vertical and horizontal amplitude and beam current dependent H phase correction.
– Horizontal start up control
– I²C bus interface

4.7.1 Matrix circuits and signal selection

The R-Y, B-Y and the Y signals are fed to the IC via pins 26, 27 and 28. The green component is recovered and the RGB signals produced using two matrix circuits, one after the other.

These RGB signals are fed to a selection circuit, to which the RGB signals from the CCU via pins 2, 3 and 4 and from the VGA-interface via pins 35, 36 and 137 are also fed. With this circuit the required signal is selected or two signals mixed together.


TDA9332
I2521
OUTPUT AMPLIFIER AND BUFFER
CONTINUOUS CATHODE CALIBRATION
I²C-BUS TRANSCEIVER
E-W GEOMETRY
WHITE POINT AND BRIGHTNESS CONTROL
PWL AND BEAM CURRENT
19 ´ 6-BIT DACs
2 ´ 4-BIT DACs
VERTICAL GEOMETRY
RGB INSERTION
H/V DIVIDER
RAMP GENERATOR
CONTRAST CONTROL
SOFT START/STOP LOW-POWER START-UP
HORIZONTAL OUTPUT
SATURATION CONTROL COLOUR DIFFERENCE
BLACK STRETCH
PHASE-2 LOOP
SWITCH
RGB-YUV MATRIX
SUPPLY
CLOCK GENERATION AND 1st LOOP
RO
GO
BO
BLKIN
BCL
DACOUT
SCL
SDA
FBCSO
PWL
EWO
EHTIN
VDOB
VDOA
GEOMETRY CONTROL
BL2
BI2
GI2
RI2
Iref
VSC
LPSU
HOUT
FLASH
CONTR
SAT
H-SHIFT
DPC
HFB
SCO
XTALO
XTALI
12MHz
BL1
YIN
UIN
VIN
RI1
GI1
BI1
VP2
VP1
DECVD
DECBG
GND1
GND2
VD
HD
HSEL
white point
BRI
MGR445

According to the operating mode selection is either with H level on blank on pins 38 and 33 or controlled from the computer via the I²C bus.

In the following section of the circuit Y and colour difference signals are generated from the RGB signals.

4.7.2 Control stages

In the Y path the first component is a circuit for gamma correction and in the colour difference branch the colour saturation setting stage.

After RGB has been generated again from the difference signals and the Y signal, the setting stages for contrast and brightness are reached.

The control stages for contrast and colour saturation in the other IC's are set to maximum and have no function. There is, in addition, in each channel, a setting stage for the white value, and the black value is set with the amplifier stages that follow.

The white value and the basic setting of the black value are determined in the two corresponding positions of the service mode. In further a operation the black value is determined by the cut off control.

The RGB signals are output at a maximum of 3.5 Vss via pins 40, 41 and 42.
The measured values for cut off and leakage current are fed to the IC on pin 44. With the evaluation circuits for leakage current and cut off, together with the computer, subsequent adjustment is carried out via the output amplifier, in order to keep the picture impression stable independently of aging.

Pin 43 is connected to the base of the diode split transformer. The circuit integrated into the IC thereby receives information about the beam current flowing into the c.r.t.

If the maximum permissible value is exceeded there, the circuit reduces the contrast and the brightness with the corresponding control stages. (see basic board “Beam current limitation“).

4.7.3 I²C bus interface and raster correction

All control processes such as brightness, contrast, etc are controlled via pins 10 and 11 of the I²C bus interface. In addition, a DAC can also be controlled via the I²C bus. For this, TDA 9332 on pin 25 outputs an adjustable voltage. This is fed to the rotation panel on pin 3 of connector W 1021. At this point an additional coil on the tube turns the deflection raster, thus providing compensation of the earth’s magnetic field at the installation site of the device. The value of the raster correction can set in both service mode and in the menu for picture functions.

If the device is turned, the influence of the earth’s magnetic field changes. The planned rotatable rack takes this into account. The rack is controlled from the chassis, with the rotation angle being determined by the TV software. Raster correction can also be determined, in that on rotation the voltage on pin 26 of TDA 9332 is changed.

The influence of the rotation angle on the raster displacement is almost linear. On installation of the device, it is sufficient for correct functioning of the correction to input a value for raster correction into the EAROM for the centre and the two end stops.

4.8 Picture in picture

On the signal board an optional picture in picture circuit is possible. This circuit consists of the video processor

VPC 3233 /I 2151 and the PIP memory I 2161/71 The video processor PIP is the same IC type as the main video processor I 2271. With the VPC 3233 various PIP representations are possible. Our device controls support 3 PIP representations.

Split Screen

The screen is split into two halves. On the left side the half picture is displayed and on the right side the picture of the PIP electronics. Both pictures are the same size and quality. In the horizontal level, sections of a picture on the left and right are naturally cut off. The core area, however, is correctly displayed.

PIP small

The picture in picture, which is reduced to 1/9 of its normal size, can be positioned in any of the four corners.

PIP large

The same is true as for PIP small, only the size is 1/4 of the normal picture.

For 4:3 devices Split Screen is not possible.

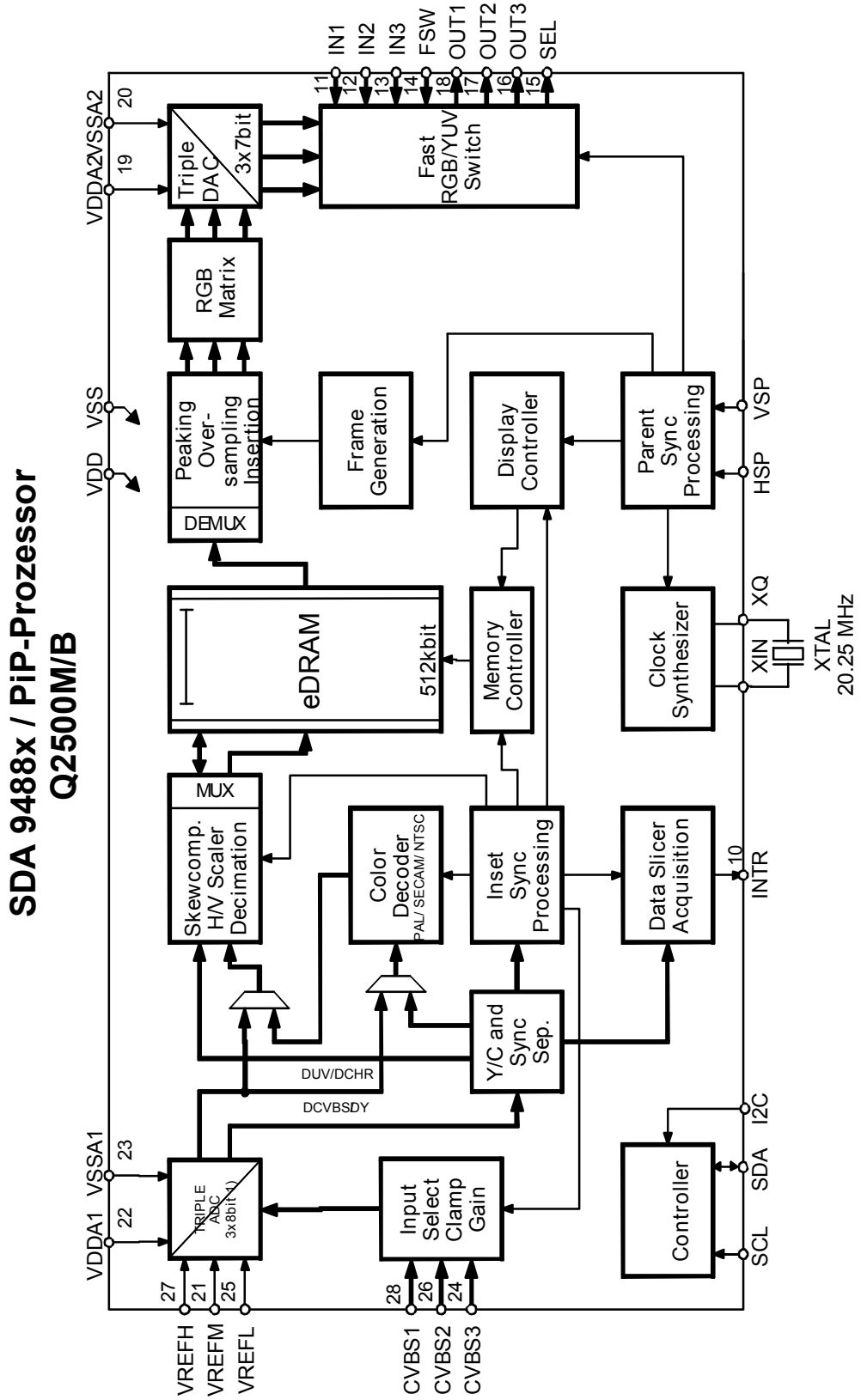
For small and large PIP display the PIP picture must be correspondingly compressed. This occurs at the vertical level by the interpolation of picture lines. For the small setting, 3 lines are compressed and for large setting 2 lines, and for each a new line is calculated by interpolation. In the horizontal level these lines are then compressed accordingly. The writing of the picture in picture data to the PIP memory is controlled completely by the PIP-VPC. Reading from memory is controlled fully from the main VPC.

Writing to and reading from memory is therefore independent. There is no synchronisation between the two VPC's.

The PIP processor processes FBAS as well as Y/C signals. The video transfer applies the FBAS/Y signal to pin 73 and the associated chroma signal to pin 72. All possible signal sources can therefore be displayed as PIP.

If an online module is integrated into the TV set, the picture can also be displayed by the online module as PIP. The Y/C signal from the online module reaches the pin connector W 1531 on the signal board. The TVO/Y signal is applied to pin 74, and the associated chroma signal to pin 71 of I 2151.

For the basic and medium signal board variants a single chip PIP processor SDA 9488 is used.


SDA 9488x / PiP-Prozessor
Q2500M/B
IN1
IN2
IN3
FSW
OUT1
OUT2
OUT3
SEL
11
12
13
14
18
17
16
15
VDDA2
VSSA2
20
19
Triple DAC 3x7bit
Fast RGB/YUV Switch
RGB Matrix
VSS
VDD
Peaking Over-sampling Insertion
DEMUX
Frame Generation
Display Controller
Parent Sync Processing
VSP
HSP
eDRAM
512kbit
Memory Controller
Clock Synthesizer
XQ
XIN
XTAL
20.25 MHz
MUX
Skewcomp. H/V Scaler Decimation
Color Decoder PAL/ SECAM/ NTSC
Inset Sync Processing
Data Slicer Acquisition
10
INTR
Y/C and Sync Sep.
DUV/DCHR
DCVBSDY
VSSA1
VDDA1
23
22
TRIPLE ADC 3x8bit
Input Select Clamp Gain
Controller
I2C
SDA
SCL
27
21
25
28
26
24
VREFH
VREFM
VREFL
CVBS1
CVBS2
CVBS3

With this module the PIP function can be used with our devices. Split screen and Multi PIP are not used.
This processor does not form part of the digital signal processing. As you can see from the circuit diagram, the RGB signals from SDA 9488 pins 15/16 and 17 are fed directly to TDA 9332 (pins 30/31/32).
SDA 9488 receives the FBAS or Y/C signal to be processed on pins 26/28 from the video-conversion IC.
The necessary 100 Hz V/H synchronous signals are fed to pins 4 and 3.
For our medium devices as for our high variant a VGA interface can be retro-fitted. The VGA RGB signals are not, however, fed directly into the TDA 9332, as in the high-end device, but for VGA operation are looped through the SDA 9488 to the TDA 9332.
From the VGA interface the RGB signals are led to pins 11/12 and 13 of SDA 9488.

4.9 Video/deflection controller TDA9332 (deflection area)

The Philips TDA 9332 video/deflection controller can be used in standard TV's as well as in devices with double picture and line frequency.

The video/deflection controller is switched in the Q 2500 chassis in such a way that it can drive the H/V deflection with double the frequency.

4.9.1 Clock generation/Phase 2 loop

All the necessary cycle and synchronous signals necessary for internal signal processing are derived from this block.

The synchronous signals generated by SAA 4979 are fed to pin 24 (H synchronous signal) and to pin 23 (V synchronous signal) of the controller. The cycle frequency for the video/deflection processor is produced with an external 12 MHz quartz on pins 20 and 21. This cycle is synchronised by a PLL that operates with the horizontal synchronous pulse HA.

4.9.2 DAC for OW/V control and H output stage

The DACs for the two vertical -VD± control signals contain all vertical correction information. The VD± control signals are output to pins 1/2 and are fed via R 1032 and R 1033 to pins 2/3 of W 1511. In this way the V output stage on the basic board is controlled by d.c.

The vertical frequency E/W parabola also contains all correction information. The control signal is output by I 2521 on pin 3 and is fed via W 1511 pin 6 to the basic board. In this way the E/W output stage on the basic board is controlled.

The horizontal output is programmed in such a way that on pin 8 a rectangular signal with 13 µs H and 19 µs L level for control of the H-output stage on the basic board is output. The signal reaches Q 2556 and Q 2561 on pin 13 of pin connector W 1511 via two inverter stages and controls H output stage Q 534 on the basic board via H driver stage Q 526.

In the SAT standby, for SAT radio and for overwriting in standby, the c.r.t. must be switched off. For this the horizontal pulse is switched off via transistor Q 2951. The control of Q 2951 is implemented via pin 79 of the SDA 6000 microprocessor. The c.r.t. is switched off here with H level.

4.9.3 Beam current dependent correction the vertical/horizontal amplitude and the H phase

As we know the high voltage at the anode connection of the c.r.t diminishes at high beam currents, owing to the internal resistance of the high voltage generation. The lower high voltage means that the beam of electrons is not so strongly accelerated and can be deflected outwards again by the V/H magnetic deflection fields. The picture becomes larger.

If the beam current decreases (darker picture content) the picture becomes smaller again. Appropriate corrective measures are neces-

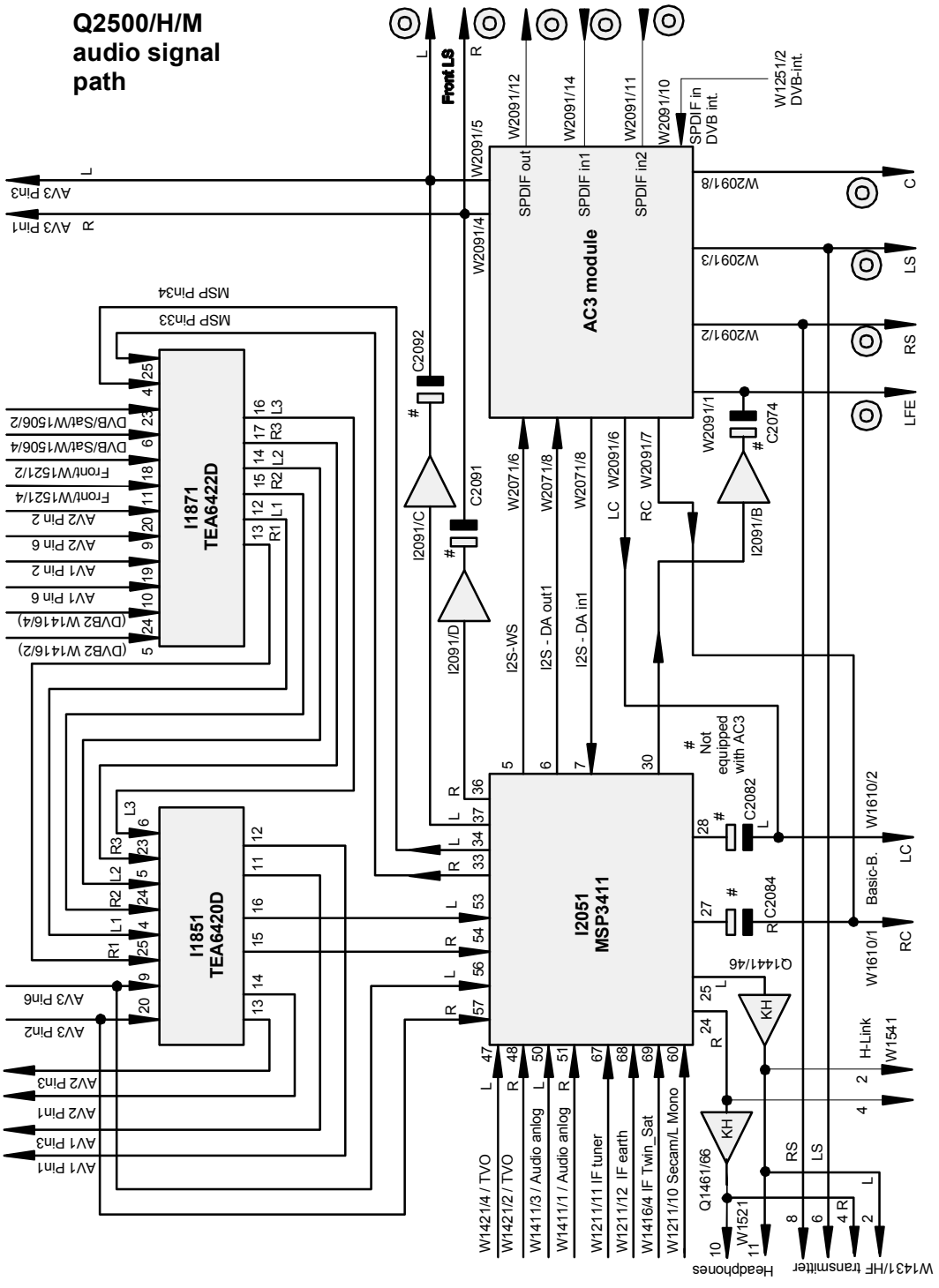
sary to prevent this video pumping or at least to reduce it. To do this beam current dependent correction information is applied to pins 4 and 14 of the deflection controller . The OW and V amplitude are influenced via pin 4 and the H phase via pin 14.

The beam current dependent information taken from the base of the diode split transformer and output by W 1511 via resistances and the two transistors Q 2639/Q 2638 is fed to pin 4 and pin 14 of TDA 9332. Switching via these two transistors ensures that the base voltage is adapted in an optimum way to I2521. pin 4/14 of I 2521 requires a voltage from 1.2 V to 2.8 V. The vertical amplitude compensation is defined firmly in I 2521 and is the same for all types of c.r.t. The horizontal amplitude compensation is influenced via internal registers by I 2521. Various values are held in EAROM for the various c.r.t types.

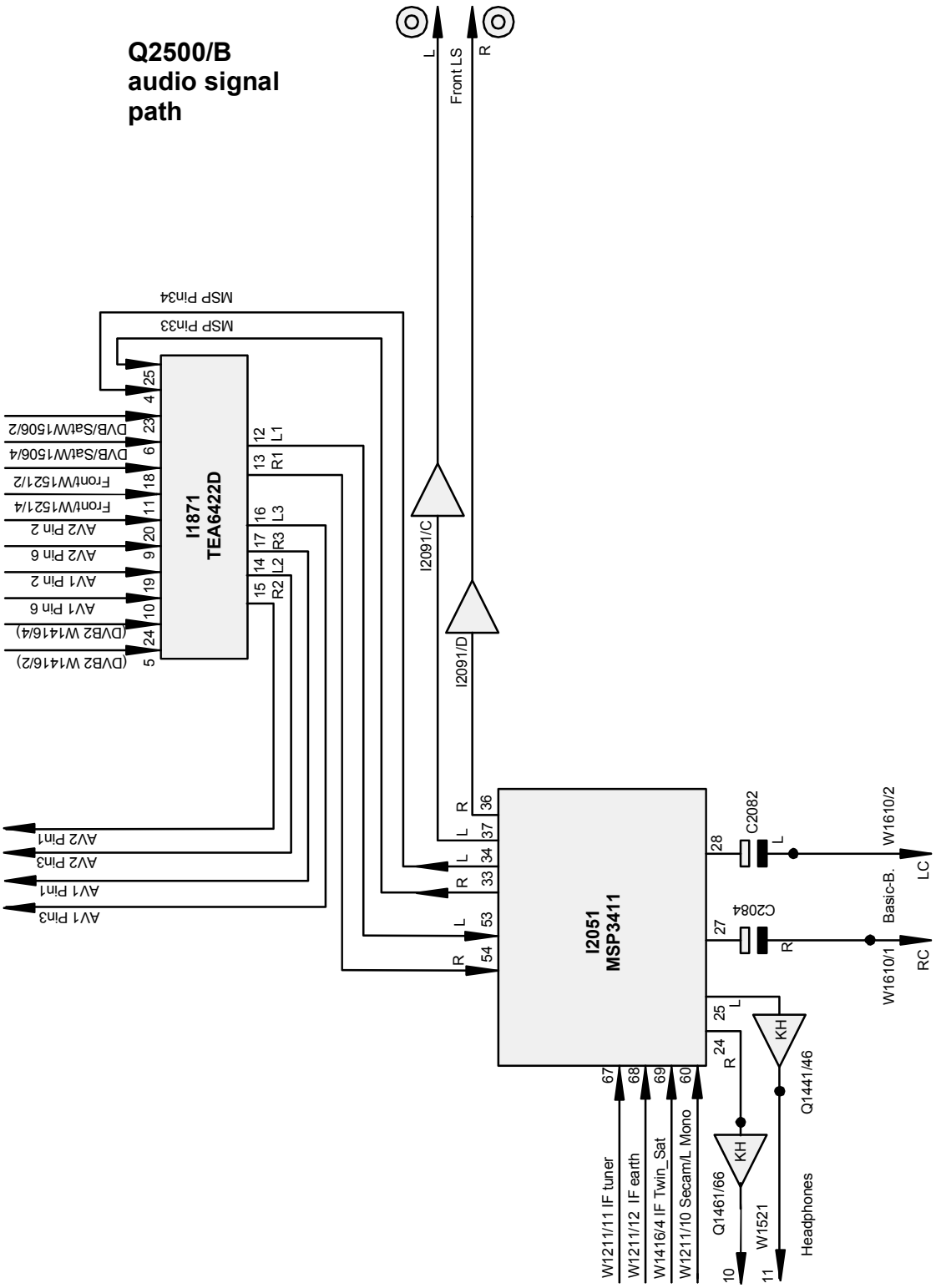
Dependent on the measured values the picture width and, if necessary, the V amplitude are influenced by the E/W output. Delay of the control is about the duration of 10 lines. A lateral glitch at bright picture settings cannot be avoided but can be reduced to some extent.
Due to the varying load on the line output stage, the line flyback pulse is also affected. This means that beam current changes also influence the H phase. The correction information on pin 14 of TDA 9332 opposes this via the internal phase correction.

5 Audio signal processing

5.1 Audio-Signal path Block diagram Q 2500 H/M and B



Q2500/B audio signal path



In the Q 2500 chassis a family of multi-standard sound processors is used, which contain all the modules for digital sound/IF-processing, FM/Nicam signal demodulation, Nicam decoding and audio base band. The multi-standard MSP 3411 sound processor is manufactured in 1.0 µm CMOS technology and incorporated into the Q 2500 chassis in a 80 pin PLCC housing.

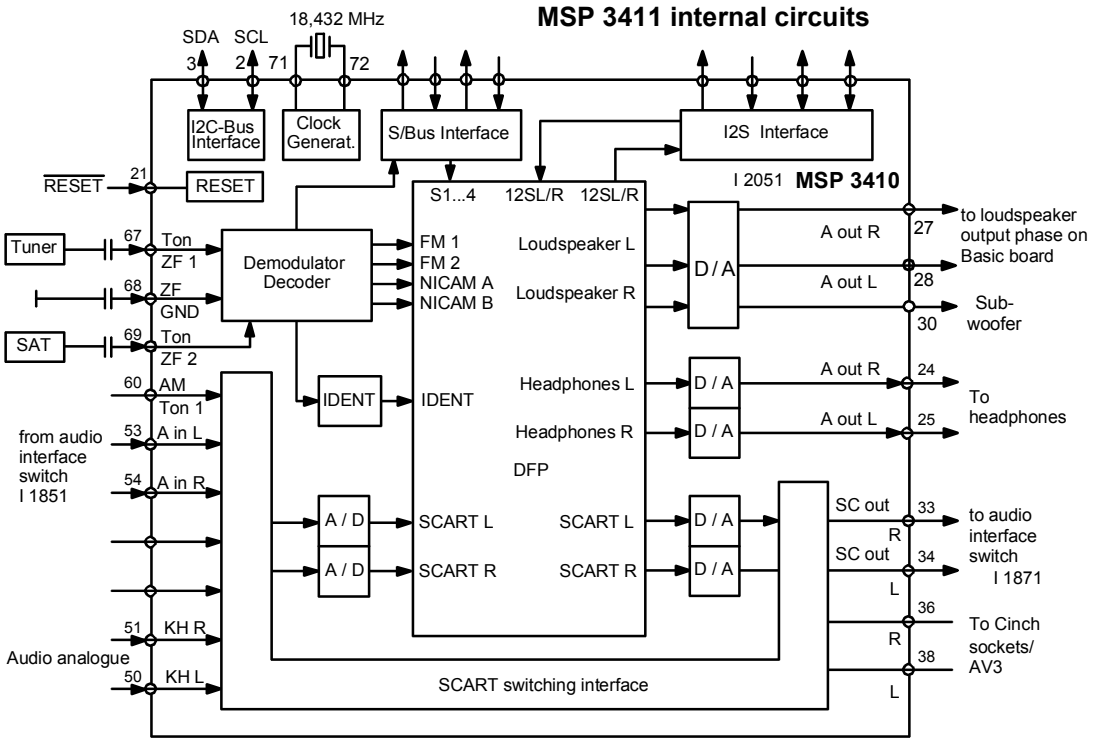
For devices without NICAM an MSP 3400 or 3401 is used, which cannot process these NICAM signals. The MSP 3401 and MSP 3411 also support virtual surround. Otherwise there is no difference between these three types.

The multi-standard sound processor can be roughly divided into a demodulator-decoder-block and into an area that is responsible for the digital audio base band processing - DFP.

The following functions are integrated into the two blocks.

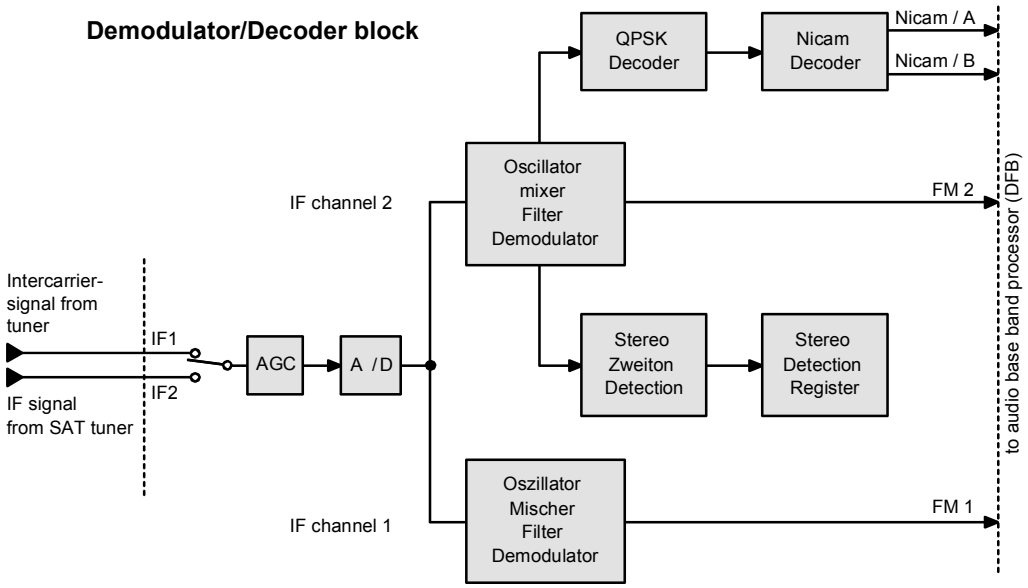
5.2 Demodulator/Decoder-Block

- Two selectable inputs for the sound/IF signal
- Automatic amplification control (AGC) for the selected sound/IF signal
- A/D converter for the sound/IF signal
- Two internal sound/IF channels, e.g. for stereo with sound carrier 5.5 MHz /5.74 MHz
- FM demodulation
- Decoder for Nicam signals



5.2.1 Audio baseband processing

- Flexible selection of the sound source to be processed, e.g. demodulator or Scart socket
- Selectable de-emphasis
- Stereo matrix
- Pre-amplifier for Nicam/FM and Scart signal
- Independent volume adjustment for loudspeaker and headphones
- Adjustment of bass, level, loudness, stereoscopic sound and balance in the loudspeaker branch and virtual surround



5.2.2 Demodulator/decoder block

The sound/IF inter-carrier signal output by the tuner passes via a band-pass consisting of L/C 2032, R/C 2033 and C 2036, to the sound/IF input1, pin 67 of MSP 3411. The band-pass suppresses frequency components below 4.5 MHz and above 10 MHz. In this way sound interference that could be caused by the colour carrier or the neighbouring picture carrier is prevented. If the Twin-SAT unit is used a SAT sound/IF reaches the sound/IF input2 on pin 69 of MSP via pin connector W 1416 /pin 4 and the band-pass, consisting of L/C 2037, R/C 2038 and C 2009.

The analogue sound/IF signal is passed internally from pin 67 (Hyperband tuner) or 69 (SAT unit) to a transfer switch that is able to switch between the two IF inputs of the MSP under software control. The analogue IF signal is then adapted optimally by an automatic amplifier control, which can control input signals from 0.14 to 3 Vss, to the ADC. The ADC changes the sound/IF signal into an 8-bit data stream. The sampling rate is 18.432 MHz.

This is produced by the internal clock generator. The frequency determining 18.432 MHz quartz is connected to pins 71/72 of MSP 3411. This 18.432 MHz clock is also used for all digital processes in the MSP.

The digital sound/IF signal is now processed in a multi-standard sound processor by two independently operating sound/IF channels. This is necessary, for example, in order to process stereo transmissions with carrier fre-

quencies of 5.5 /5.74 MHz or even other sound transmission standards. These two IF channels can be programmed by the operating software to different sound carrier frequencies. For the digitally filtered sound/IF carrier full modulation is carried out in both channels. The digital sound signals are felt on the output of the demodulator/decoder block.

In the second sound/IF channel decoding of the pilot sound carrier takes place with sound transmission by the two carrier frequencies 5.5 /5.74 MHz. In addition to the FM modulated VF signal, the 5.74 MHz carrier is modulated with an AM modulated 54,7 kHz pilot sound carrier. The pilot sound carrier is variously modulated depending on the transmitted VF signals (mono, stereo or two-tone).

Modulation type from pilot sound carrier

Operating type	Natural frequency
Mono	unmodulated
Stereo	117.5 Hz
Two tone	274.1 Hz

Detection of the pilot sound carrier is carried out in the second IF channel, in which the 5.74 MHz sound carrier processing takes place, The result of the continuous pilot sound carrier evaluation is written to the "Stereo Detection Register" of the MSP. This register is read cyclically by the CCU via the I²C bus, and depending on the operating mode set the CCU communicates to the MSP via the I²C bus the type of de-matricising that must be switched on.

5.2.3 Nicam processing

Nicam is a sound transmission system designed for terrestrial transmission. It was developed in the United Kingdom for stereo TV transmission and is now used in a number of other European countries.

The name "Nicam" is an abbreviation and stands for "Near instantaneously compounded audio multiplex".

In this system the digital audio information is modulated by an additional sound carrier.

The signal gets its name QPSK signal from "Quadrature phase shift keying" from the type of modulation, which is quadrature modulation with rotating phase,

Owing to the various television standards two different sound carrier frequencies are used for the Nicam transmission. For PAL-I the sound carrier is 6.552 MHz and for PAL-B/G it is 5.85 MHz.

5.2.4 Audio signals from the interface switching

If audio signals are fed to the Scart sockets, the selected VF signal pair is applied directly to pins 53/54 of the multi-standard sound processor via the audio interface switch (see Audio Signal Path). If the signal board is fitted with 3 AV sockets the audio signal is output by the AV3 socket directly to pins 56/57 of the MSP. The audio signal passes via an internal switch to two ADCs. The audio signal is digitised by the two ADCs for further processing and then led internally to the audio base band processor.

5.2.5 AM audio signals at L standard

If AM signals are processed in the device, the IF preparation and demodulation is carried out in the HF/IF block.
The VF signal comes from pin 23 of the cable tuner to pin 60 of the MSP 3411. Furthermore, the signal path is the same as the signals that come from the interface transfer to pins 53, 54 of the MSP.

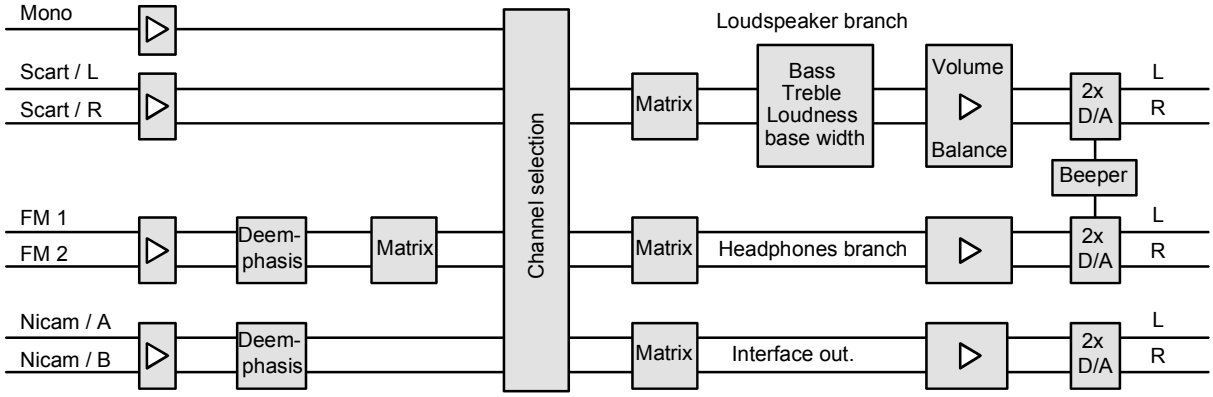
5.2.6 Audio base band processor

In the DFP there is a pre-amplifier for all three digital VF signal pairs; Nicam A/B, FM 1/2 and Scart L/R. The adjustment of the pre-amplifier for each VF input pair is independent and is determined by the software. This means that for further processing nearly the same digital VF level is available.

For the FM 1/2 and Nicam A/B signal pairs the pre-amplifier is followed by the necessary de-emphasis. The FM 1/2 VF signal pair is fed onward to the FM matrix. For an FM stereo transmission the stereo L and R signals are re-constituted from the L+R/2 signal of FM 1 and the R signal of FM 2 in the FM matrix.

The FM matrix is controlled by SDA 6000 via the I²C bus according to the selected operating mode - stereo or mono. In the following channel selection, after the selected operating mode, the selected VF signal is switched to the VF output branches in the MSP, which are controlled independently of one another, for loudspeaker, headphones and interface selection.

Audio Base Processor (DFP)



5.2.7 Loudspeaker branch

After channel selection the two VF channels are led to the digital filter and control stages, which are all controlled from the CCU via the I²C bus. As the processing for both channels is identical, the following description will deal with one channel only.

5.2.8 Loudness

The signal comes from the matrix and is fed initially to a filter with which an 'as heard' loudspeaker control (Loudness) is implemented. Depending on the loudspeaker setting frequencies around 1 kHz are reduced, as for same sound pressure the human ear senses these frequencies as being a lot louder than deeper or higher frequencies. The filter coefficient necessary for the reduction is determined and is applied in varying strengths to the signal, depending on the volume.

5.2.9 Sound setting

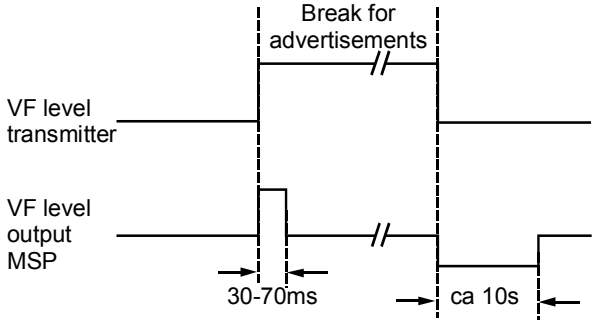
The sound control stage consists of two separate filters for the height and bass settings. The control range for the two filters is ±12 dB.

5.2.10 Loudspeaker control and AVC (Automatic Volume Control)

The signal then passes through the loudspeaker control stage. The control range comprises 64 stages. In MSP 3411 each channel has a second control stage for the balance setting.

In addition, the MSP offers the facility of measuring the level at the input. This is used as the AVC function. This means that it is possible to select different volumes for transmitters during breaks for advertisements or between different transmitters. Therefore, the design does not provide for a programme location related volume correction.

The actual value on the input determined by the MSP is communicated to SDA 6000 via the I^2C bus. In the operating software a precisely defined amplification is assigned via the volume value. If the measured value deviates from the required value, the volume is decreased or increased via the I^2C bus until the required value is reached.



This means that various control constants are used. Loud passages are toned down within 30 to 70 ms. An increase in soft passages on the other hand occurs with a delay of about 10 s, to avoid an unwanted increase in volume during the transmission. In addition, the AVC can be switched off within the sound menu.

5.2.11 DAC

A DAC is controlled with the signal set by the digital controller. The analogue signal is output for the right and left channels on pin 27/28. The signal is then fed via transistors Q 2081 and Q 2083, which are switched as an impedance converter. Via the coupling capacitors C 2082/84 the signal then arrives at W 1610, pins 1 and 2, and from there is fed to the basic board on the two output stages.

5.2.12 Headphone branch

In the headphone branch there is an independent volume setting, that can be changed independently of the loudspeaker volume, also in 64 stages.

The digital/analogue converted audio signals for the headphones are output to pins 24/25.
The W 1494 audio Cinch sockets are supplied with level by pins 36/37 of the MSP. In order to deliver sufficient output level to these Cinch sockets the Q 2500 chassis has in this branch two amplifier stages, consisting of the operational amplifier I 2091C and D. The amplifiers amplify the signal by a factor of 2. For the setting “Sound via HiFi unit“ the output level can be set from 0 Vss to 3.5 Vss.
If “Sound via TV“ is set, then there is a standard level on the Cinch sockets.

5.2.13 Interface branch

The audio level for the interface is set by the operating software and cannot be changed. The digital, analogue-converted VF signals for the interface connection are applied to pins 33/34.

5.2.14 Deadline volume

During operation, a kind of awakening function can be programmed into the Q 2500 chassis as a deadline time. In addition, there is an awakening tone, with an adjustable volume.

Via the I^2C bus it is also possible for MSP 3411 to switch off the sound in the loudspeaker and headphone branch. At the same time an internally generated 1 kHz rectangular signal is applied to these channels. In the headphone branch the level is dependent on the headphone volume. In the loudspeaker branch the level can be set, independently of other volume, in 39 stages in the “Time services“ menu .

5.2.15 Mute circuit

As the only additional switching measure there is an active mute circuit parallel to the output amplifier inputs with transistors Q 1581 and Q 1586. It is controlled by transistors Q 2966 and Q 2961 from the ON/OFF command of the CCU, or via transistor Q 2027 from pin 77 of MSP 3410 .
Noise associated with switching on and off, as well as any crackling when switching over is suppressed.

Mute stages are also incorporated for the headphone branch and the Cinch sockets. If an AC3 module is incorporated it also generates a mute if necessary e.g. if the sound decoder is switched.

On start up the L level of the ON information of the CCU of transistor Q 2961 is blocked. The voltage taken from the conversion transformer and rectified by D 491 is able to charge Elko´s C 2967/68 very quickly via diode D 381. The charge process from C 2963 flows via R 2963 extremely slowly, as D 2964 is now blocked. Not until Elko C 2963 is charged to almost the same potential as C 2967/68 does transistor Q 2966 conduct. A positive voltage is felt on the base of transistors Q 1581/Q 1586 whereby this switches and the VF lines are at earth potential.

Not until C 2963 is charged and Q 2966, Q 1581 and Q 1586 are blocked, can the VF reach the output stage without hindrance.

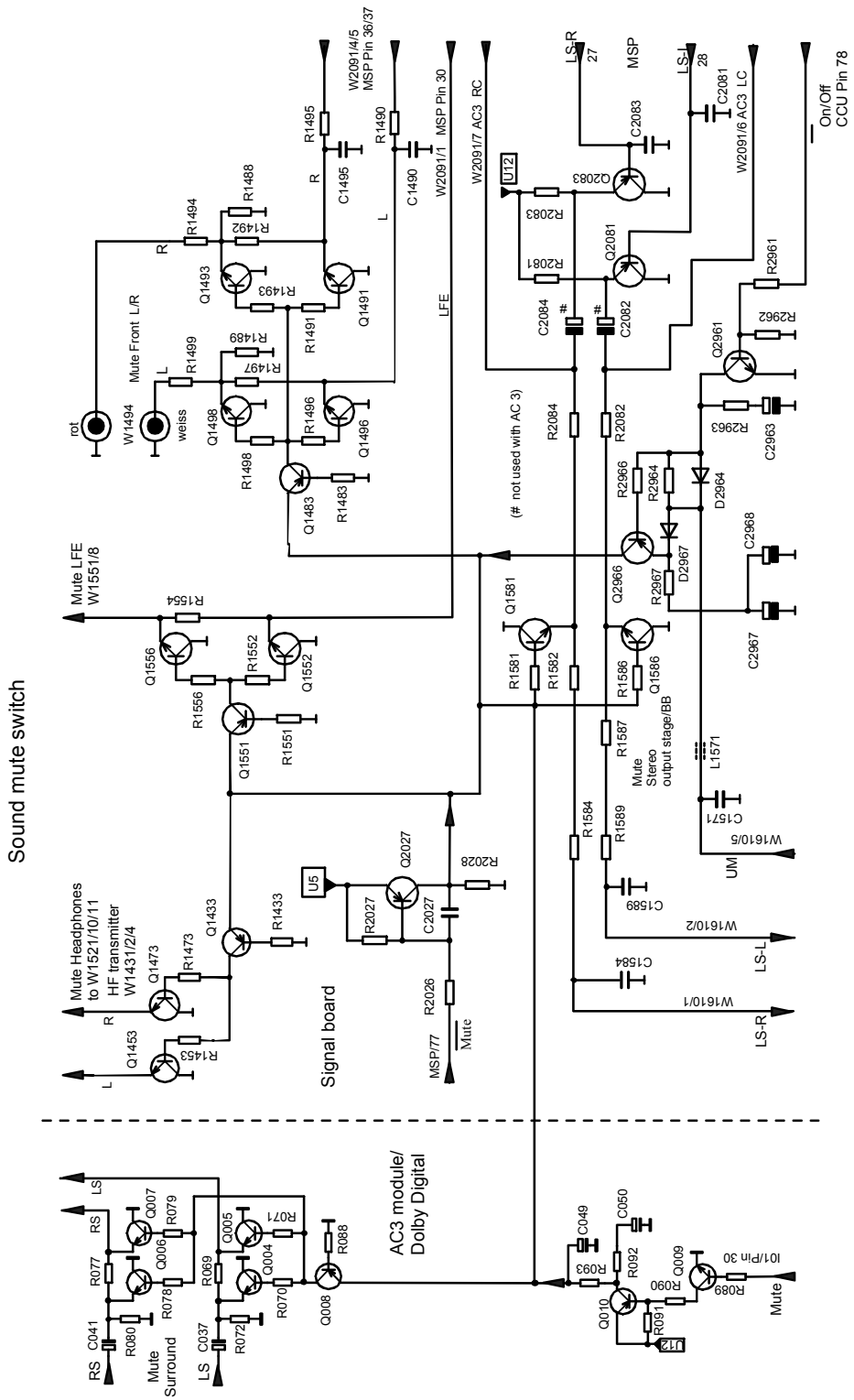
At the point of switching off the voltage from the power supply falls off relatively quickly. Transistor Q 2961 is switched by the H level of the OFF information of the CCU . This means the charge from C 2963 can flow to earth. Q 2966 becomes conductive, whereby the charge from C 2967/68 controls transistors Q 1581 and Q 1586 and the VF lines are at earth potential.

The mute information that is active on start up and shut down activates all the mute levels.

In the initialisation phase pin 77 is set to L level by MSP 3411. With L level transistor Q 2027 switches. Via its emitter-collector path U5 also reaches the mute line and all mute stages are active.
To prevent the VF mute stages themselves producing interference during the switching phase, they are d.c. decoupled and fitted with discharge resistors.

If a Dolby Digital Module is incorporated the LFE channel from the mute function is controlled silently via transistors Q 1551 and Q 1552/56.

The Dolby Digital Module receives the mute function from the signal board on contact connector W 2091 /pin 13.


Sound mute switch
Mute LFE W1551/8
Mute Front L/R
Mute Headphones to W1521/10/11 HF transmitter W1431/2/4
Signal board
AC3 module/ Dolby Digital
Mute Surround
Mute Stereo output stage/BB
W2091/4/5 MSP Pin 36/37
W2091/1 MSP Pin 30
W2091/7 AC3 RC
W2091/6 AC3 LC
LS-R 27
LS-L 28
MSP
On/Off CCU Pin 78
(# not used with AC 3)
LFE
MSP/77
Mute
W1610/5
W1610/2
W1610/1
LS-L
LS-R
101/Pin 30

On the Dolby Digital Module the two surround channels are muted via transistors Q 8/Q 4/5 and Q 6/7. If a data error is detected on the Dolby Digital Module during digital sound signal processing, pin 30 on I 01 outputs H level. Via the two transistors Q 9 and Q 10 the mute function is then activated. For the mute function the Dolby Digital Module represents both input and output.
As you can see from the mute circuit, some sounds have an output line, as, for example, for the LFE channel Q1552/56, two transistors are used. This measure improves the mute behaviour and the error rate of these stages.

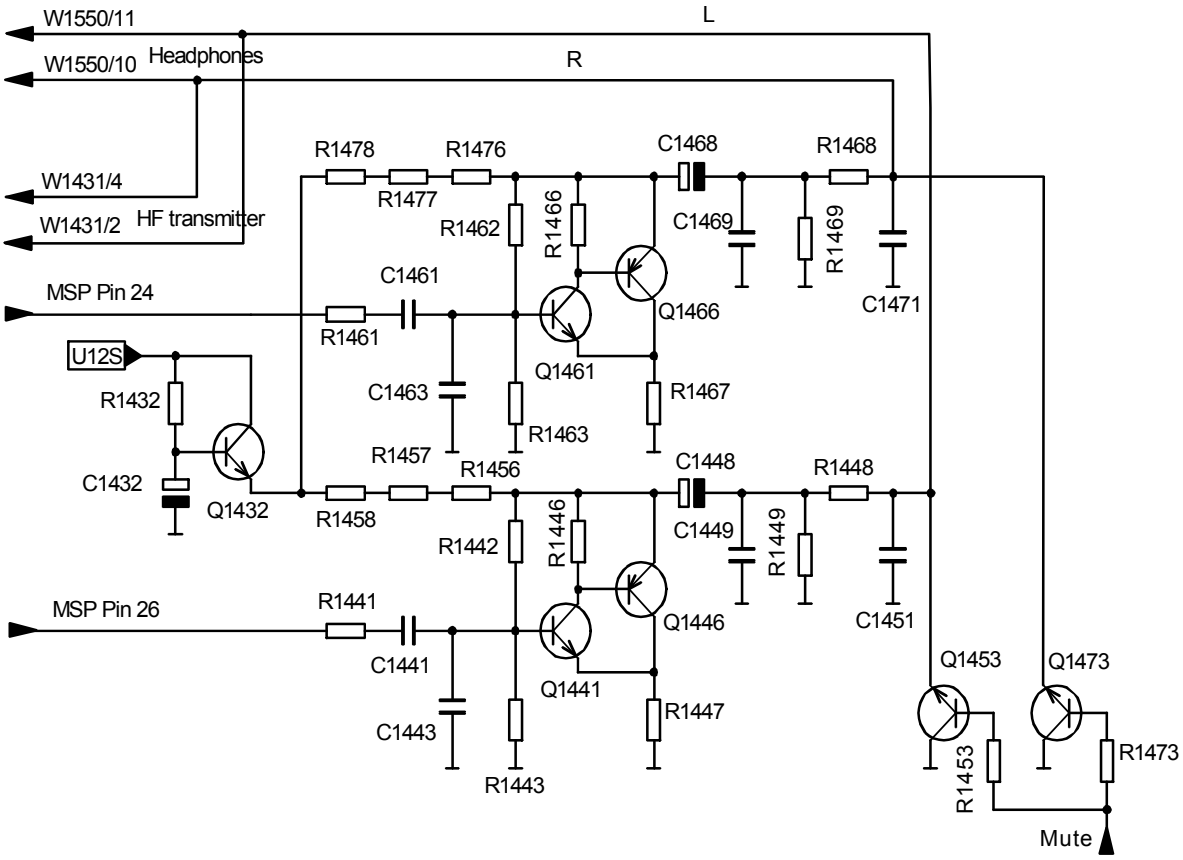
5.2.16 Headphone amplifier

As in previous models the front panel of the device has a connector for headphones. As for the loudspeaker branch the signals are also generated in the MSP 3411. As already described, the loudspeaker control for the headphone control is also implemented in it.

These signals are output in pulse width modulated form on pins 24 and 26 of the MSP and integrated with external RC components into an VF signal at up to 1.2 Vss. They are fed respectively to an amplifier stage, consisting of 2 transistors Q 1441/46 and Q 1461/66. This stage amplifies them to 9 Vss and outputs them via a decoupling through C 1448/68 to the headphones socket and pin 2/4 on pin connector W 1431 for the HF transmitter.

The headphones volume can be controlled in 63 stages and the setting displayed on the screen.

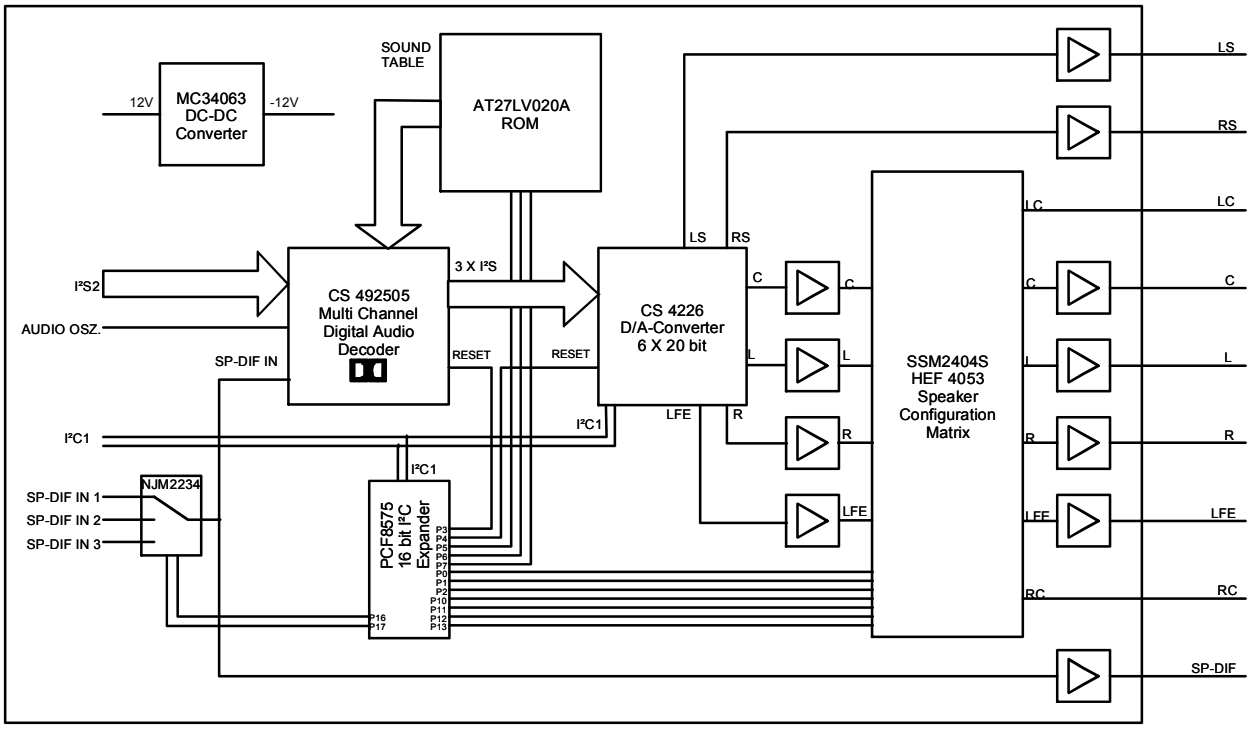
Headphones amplifier



5.3 AC3 module (Dolby Digital)

5.3.1 Block diagram, AC3 module

AC3 modul



5.3.2 AC 3 signal processing

A Dolby Digital Module can also be incorporated into the signal board variants Q 2500/H and Q 2500/M. If a signal board is fitted with the AC 3 module, the essential sound signal processing takes place on the AC 3 module.
The AC 3 module supports:

- Dolby Pro Logic
- Dolby Digital 5.1
- Circle Surround
- PCM Stereo

Dolby Digital 5.1 and Circle Surround can supply up to 6 sound channels.

- 2 channels for Front left and right
- 2 channels for Surround left and right
- 1 Centre channel
- 1 deep sound channel (LFE low frequency effects)

The Dolby Digital 5.1 Decoder is only active, when a correct AC 3 audio digital signal is supplied from a signal source.

The Circle Surround Decoder operates with a normal stereo signal. From this stereo signal the decoder decodes the 6 sound channels. This function has the advantage that for the great majority of stereo transmitters a 5.1 surround signal can already be used.

Dolby Pro Logic supports four sound channels.

2 channels for front left and right

1 centre channel

1 mono surround channel

Dolby Pro Logic also operates with a stereo signal, this must, however, also be coded with the Dolby Pro Logic standard. If this is not the case then no Center/Surround Signal is produced.

NF bandwidth of the sound channels

	Dolby Pro Logic	Dolby Digital 5.1	Circle Surround
2 channels Front L/R	20Hz-20KHz	20Hz-20KHz	20Hz-20KHz
2 channels Surround	no	20Hz-20KHz	20Hz-20KHz
Mono Surround	100-7kHz	no	no
Center	20Hz-7KHz	20Hz-20KHz	20Hz-20KHz
Deepsound-channel LFE	no	20Hz-100Hz	20Hz-100Hz

The AC 3 modules can receive digital audio signals via three paths.

- I^2S bus data supplied from MSP 341x on the signal board.
- SPDIF audio data from the two digital Audio Cinch input sockets.
- SPDIF audio data form the internal DVBi 2 Decoder (deliverable end 2002, not used in all device variants).

The AC 3 module cannot process any analogue sound signals directly. The analogue sound signals from internal – e.g. Sat unit, tuner or DB module – as also from external – e.g. video recorder – sound signal sources, must first be converted into digital sound bus data (I^2S bus). This task is implemented by the Multi Sound Processor MSP 341x, which is incorporated into the signal board.
The digital I^2S bus data is emitted by MSP I 2051 on pins 4/5 and 6 and are fed to the AC 3 module via pins 5/6/7 of contact connector W 2071. All analogue sound output signals to the AV sockets and the headphones amplifier are delivered by the MSP. The AC 3 module has no influence on these output signals. The AC 3 module does not deliver any I^2S bus data back to the MSP. This also means that no sound signals are delivered to the AV sockets and the headphones amplifier, if signals are supplied only via the SPDIF Cinch sockets.

The SPDIF signals (SPDIF **S**ony **P**hilips **D**igital **I**nter**F**ace, level 0.7 Vss-1 Vss to 75 Ohm) are supplied by the Cinch sockets to the contact strip W 2091 pin 14 SPDIF in1 and pin 11 SPDIF in2.
SPDIF data from DVBi 2 module is supplied to W 2091 pin 10.
The SPDIF signals reach the AC 3 module on changeover switch I 18. This is controlled by the I^2C bus expander I 11 via pin 2/4. The SPDIF signal selected for processing is output to pin 7 of I 18. The selected signal is also returned to the SPDIF Cinch outputs via pin 12 of Q 11 and W 301.
I 2 converts the SPDIF signal – input pin 42 – of the I^2S bus data – I 2 pins 1/43/44 - from MSP in the I^2S bus data for the I 1 (DSP - Digital Sound Processor). I 1 processes this audio data according to the prescribed standard. For this the respective software required is loaded from I 5 memory. The memory is organised into 8 blocks, each of 32 kByte. For Circle Surround, Doby Pro Logic and Dolby Digital a 32 kByte block respectively is required. If, for example, Circle Surround is switched to Dolby Surround, the CCU controls Expander I 11 via the I^2C bus in such a way that the address switching lines I 11 pin 9/10/11 of the memory block in I 5 for Dolby Surround can be selected. DSP I 1 receives an interrupt from CCU pin 77 via pin 14 of W 321.

The interrupt causes I 2 to load new software from the memory. Due to the block preselection from the the I2C bus expander, the DSP now loads the software for Dolby Pro Logic.
The DSP processes the I^2S bus data according to the appropriate instructions. The overwhelming number of sound parameters to be set also occur in the DSP.
The DSP feeds the digital sound bus data back to the converter I 2, where the digital/analogue conversion takes place. The 6 sound output channels of I 2 reach W 301 via the operational amplifier and the loudspeaker matrix – consisting of I 6/9/14.

- pin 1 LFE/SUB (deep sound channel)
- pin 2 RS (Surround right)
- pin 3 LS (Surround left)
- pin 4 R (Front right)
- pin 5 L (Front left)
- pin 6 LC (Center left)
- pin 7 RC (Center right)
- pin 8 C (Center channel)

5.3.3 AC 3 IC functions

CS 4925-01 (I 1)
Multi Channel Digital Audio Decoder.

- Processes according to the operating mode, - Circle Surround, Dolby Pro Logic Dolby, Digital 5.1 - digital Sound-bus-data.

- Implements all sound settings, such as height and depth settings.

CS 4226 (I 2)
DAC

- Converts SPDIF signals into I^2S bus data for I 1 .

- Converts the I^2S bus data processed by I 1 into analogue signals for the loudspeaker matrix.

6 Interface switching

Interface switching is via Q 2500 on the signal board. Switching of the various on and off signals is implemented essentially by six ICs; two TEA 6415, two CD 4053 for the video signals, a TEA 6422 and a TEA 6420 for the audio signal switching. Control is directly from I²C bus system 3 via SDA 6000. An exception is CD 4053 I 1631 and I 1771.

I 1631 switches between the RGB lines of the AV3 socket and the RGB signals of the DVB decoder. I 1631 is controlled from a free switch output in MSP, which itself is activated by the CCU via the I2C bus. If the output on pin 78 of the MSP is switched to H level, then L level is felt on pins 9/10/11 of I 1631 via inverter Q 1637. With L level on, its control input I1631 switches to AV3 operation, at H level the RGB signals from the DVB decoder are switched through to the signal processing.

I 1771 is used for chroma signal switching if a Digital Link Plus SVHS video recorder is connected.
During SVHS operation a chroma signal is expected from SVHS Digital Link Plus video recorders on pin 7 of the AV socket. For VHS video recorders it is pin 15.
If the device control detects a SVHS Digital Link Plus VCR, the chroma signal is switched to pin 7 of the AV1 or AV2 socket on overplay and during a DVB recording. I 1771 is switched from two switch outputs on pin 115/116 I 2311. This in turn is controlled by the CCU.

As the two TEA 6415 must be addressed differently for picture signal switching, pin 7 of I 1116 is earthed and I 1181 is at the operating voltage.

The exact signal flow for the video and audio signals can be obtained from the appropriate flow diagrams.