DESCRIPTION

PT6958 is an LED Controller driven on a 1/6 duty factor. Ten segment output lines, five grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to PT6958 via a three-line serial interface. Housed in a 28-pin SOP, PT6958's pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

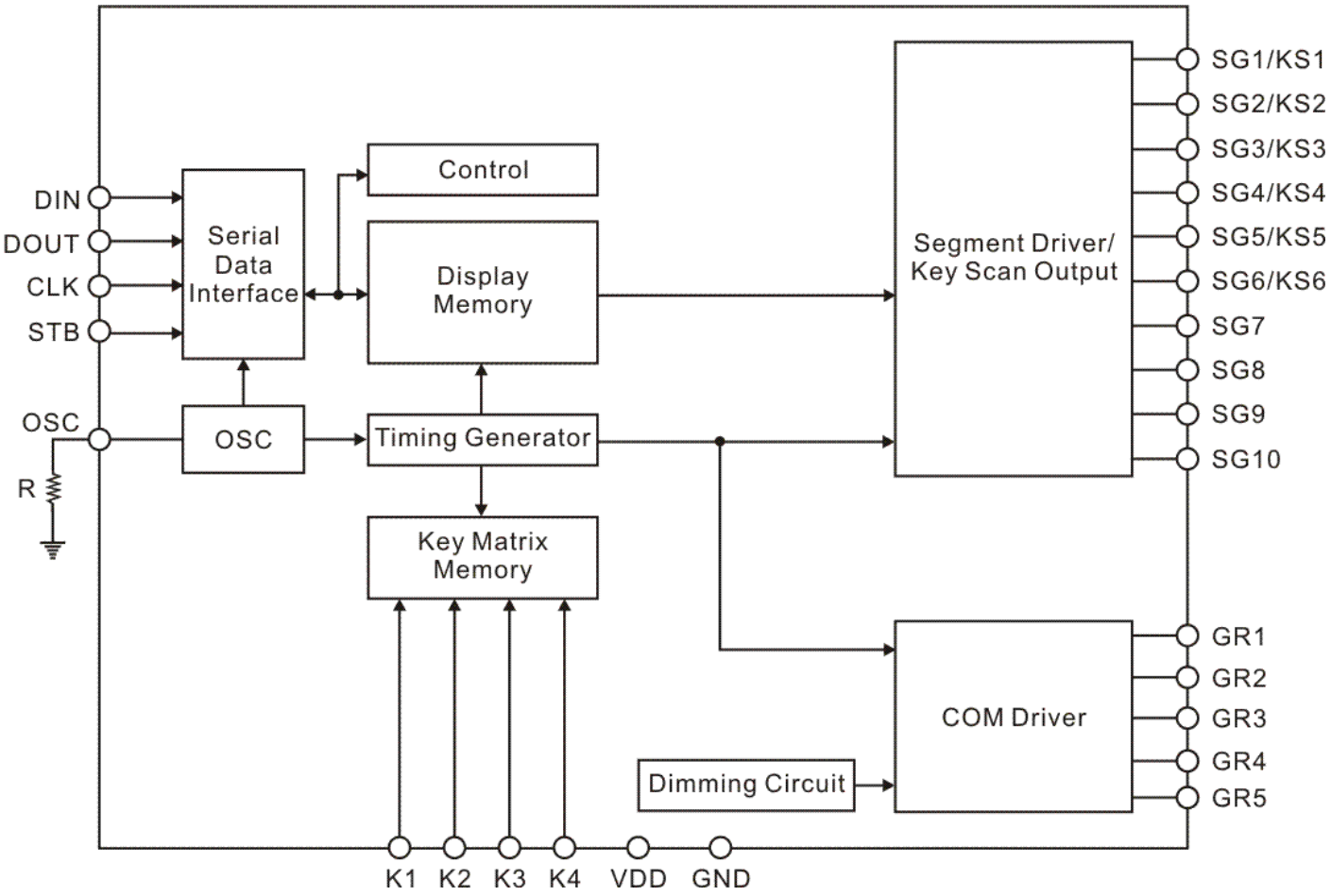
FEATURES

- CMOS Technology
- Low Power Consumption
- Up to 10 Segment Output Drivers
- Up to 5 Grid Output Drivers
- Key Scanning (6 x 4 Matrix)
- 8-Step Dimming Circuitry
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- Available in 28-pin, SOP

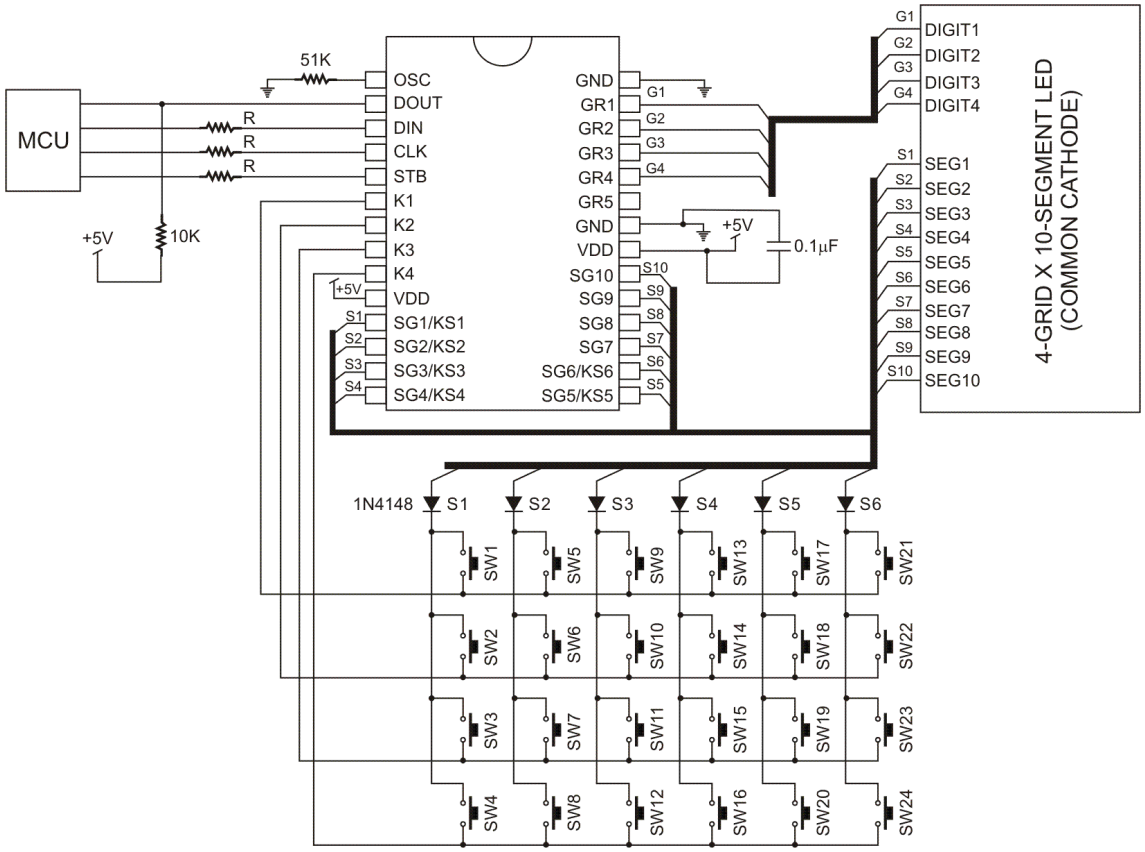
APPLICATION

- Micro-computer Peripheral Device

BLOCK DIAGRAM

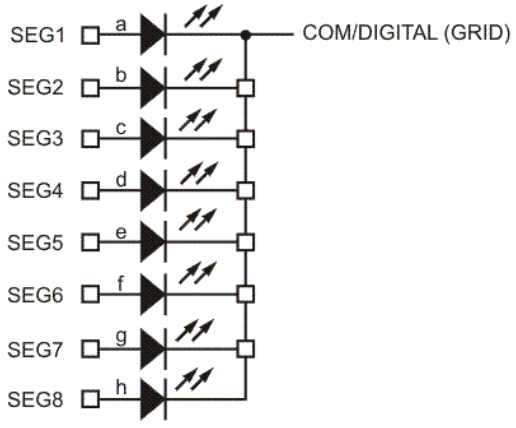


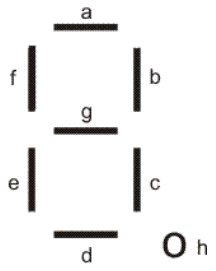
APPLICATION CIRCUIT



Notes:
1. The external capacitor (0.1 μF) that is connected between the GND and the VDD pins must be located as close to the PT6958 chip as possible.
2. The PT6958 power supply is separate from the application system power supply.
3. 10 KΩ ≧ R ≧ 1 KΩ

COMMON CATHODE TYPE LED PANEL

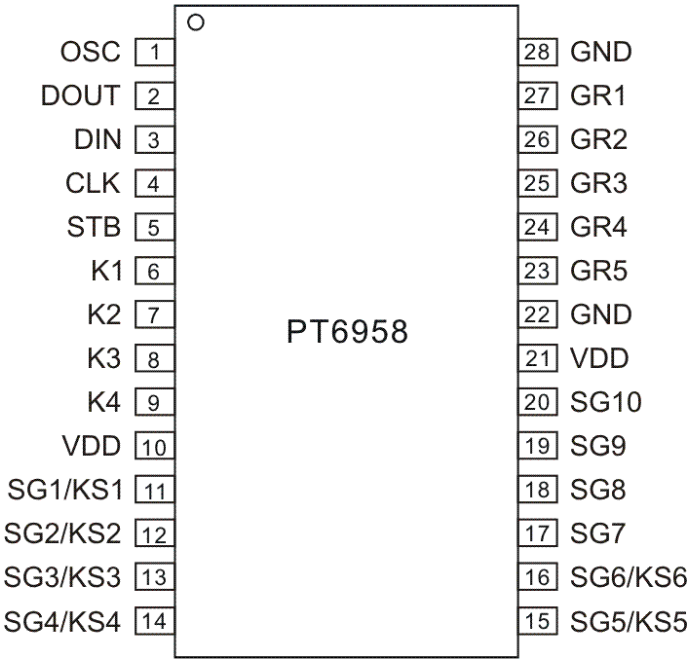




ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6958	28-pin, SOP, 300mil	PT6958

PIN CONFIGURATION



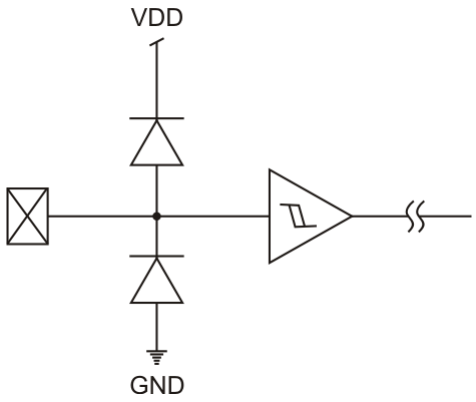
PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency	1
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock.	2
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	3
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge	4
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is “High”, CLK is ignored.	5
K1 ~ K4	I	Key Data Input Pins The data sent to these pins are latched at the end of the display cycle. (Internal Pull-Low Resistor)	6 ~ 9
VDD	-	Power Supply	10, 21
SG1/KS1 ~ SG6/KS6	O	Segment Output Pins (P-Channel, open drain) Also acts as the Key Source	11 ~ 16
SG7 ~ SG10	O	Segment Output Pins (P-Channel, open drain)	17 ~ 20
GND	-	Ground Pin	22, 28
GR5 ~ GR1	O	Grid Output Pins (N-Channel, open drain)	23 ~ 27

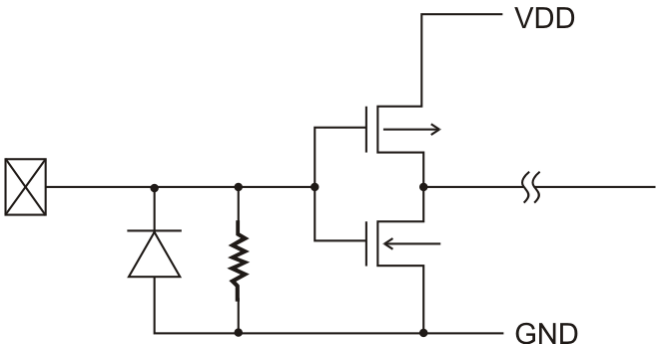
INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below.

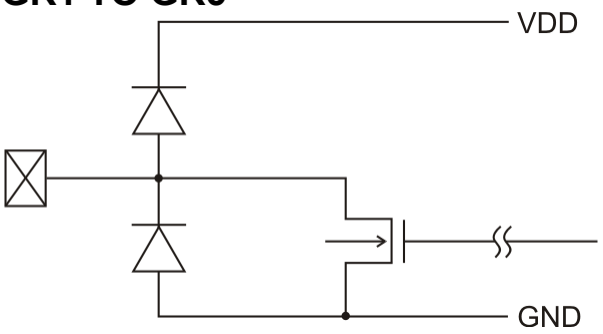
INPUT PINS: CLK, STB, DIN



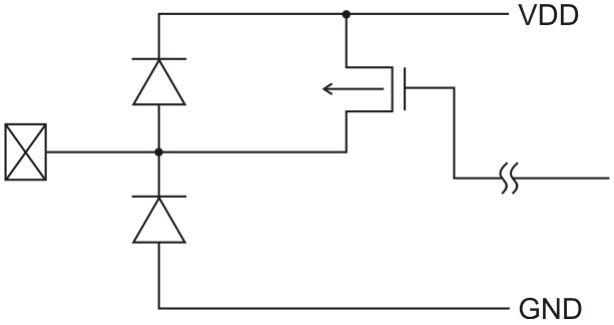
INPUT PINS: K1 TO K4



OUTPUT PINS: DOUT, GR1 TO GR5



OUTPUT PINS: SG1 TO SG10



FUNCTION DESCRIPTION

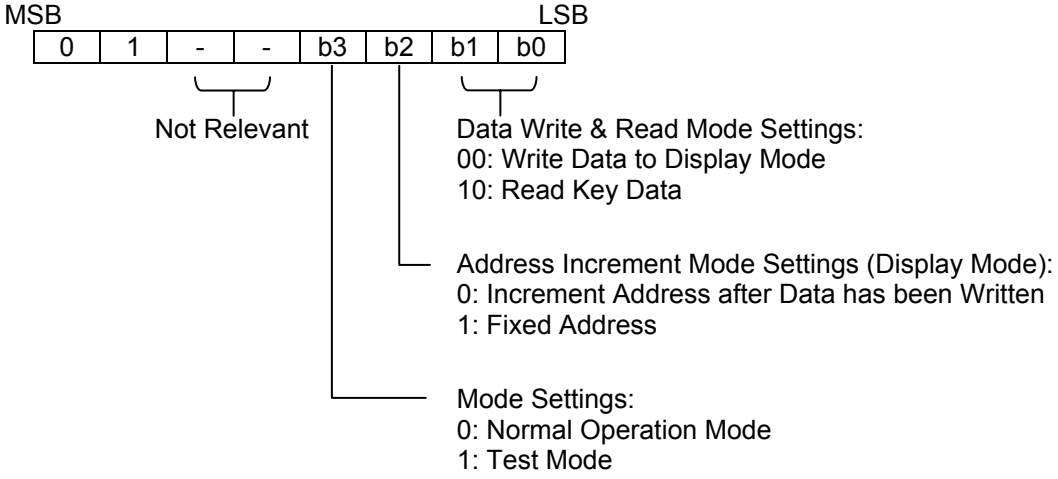
COMMANDS

A command is the first byte (b0 to b7) inputted to PT6958 via the DIN Pin after STB Pin has changed from “HIGH” to “LOW” State. If for some reason the STB Pin is set to “HIGH” while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1: DATA SETTING COMMANDS

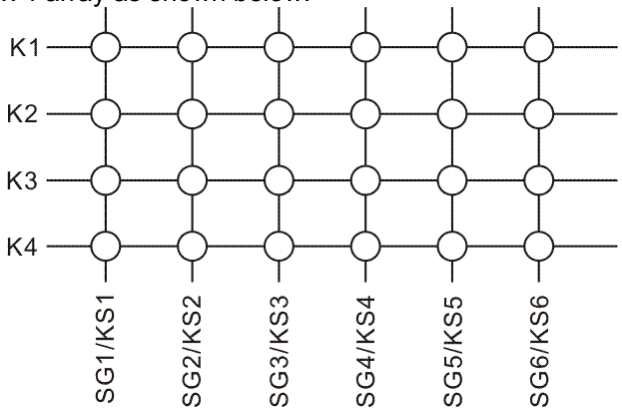
The Data Setting Commands executes the Data Write or Data Read Modes for PT6958. The data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of “1” while bit 8 (b7) is given the value of “0”. Please refer to the diagram below.

When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of “0”.



PT6958 KEY MATRIX & KEY INPUT DATA STORAGE RAM

PT6958 Key Matrix consists of 6 x 4 array as shown below:



Each data entered by each key is stored as follows and read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG6, b7) has been read, the least significant bit of the next data (SG1, b0) is read.

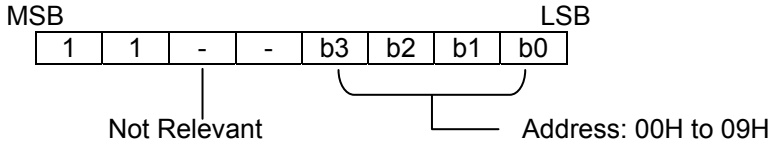
K1……K4	K1……K4
SG1/KS1	SG2/KS2
SG3/KS3	SG4/KS4
SG5/KS5	SG6/KS6
b0……b3	b4……b7

Reading Sequence

COMMAND 2: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of “00H” to 09H”. If the address is set to 0AH or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at “00H”.

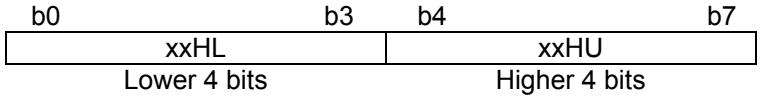
Please refer to the diagram below.



DISPLAY MODE AND RAM ADDRESS

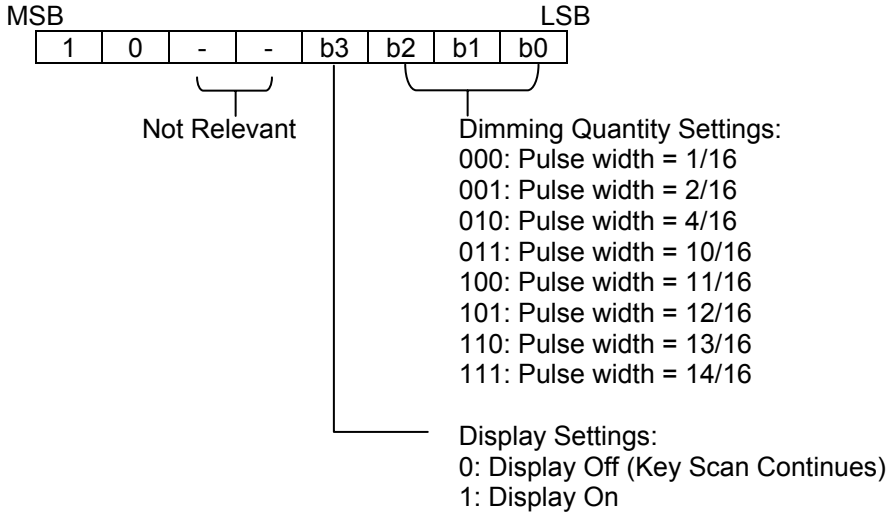
Data transmitted from an external device to PT6958 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of PT6958 are given below in 8 bits unit.

SG1 SG4	SG5 SG8	SG9 SG10	
00HL	00HU	01HL	DIG1
02HL	02HU	03HL	DIG2
04HL	04HU	05HL	DIG3
06HL	06HU	07HL	DIG4
08HL	08HU	09HL	DIG5



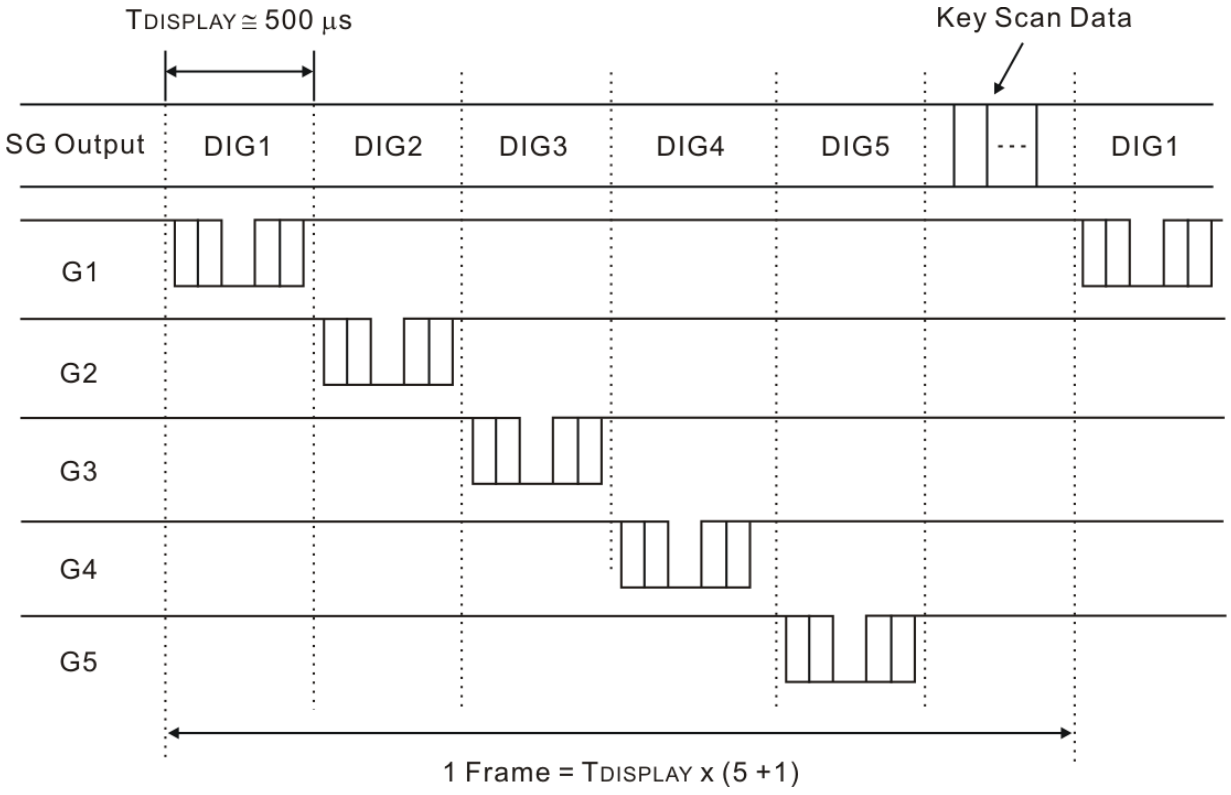
COMMAND 3: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is stopped).



SCANNING AND DISPLAY TIMING

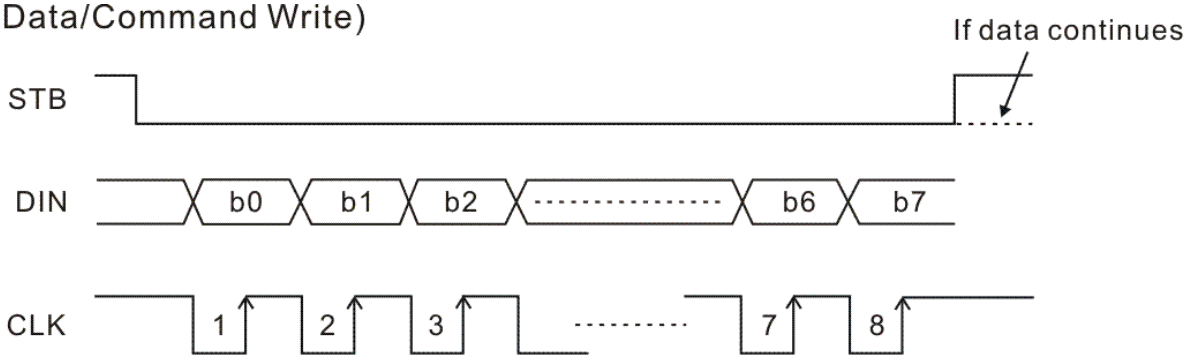
The Key Scanning and Display Timing diagram is given below. One cycle of key scanning consists of 1 frame. The data of the are 6 x 4 matrix is stored in the RAM.



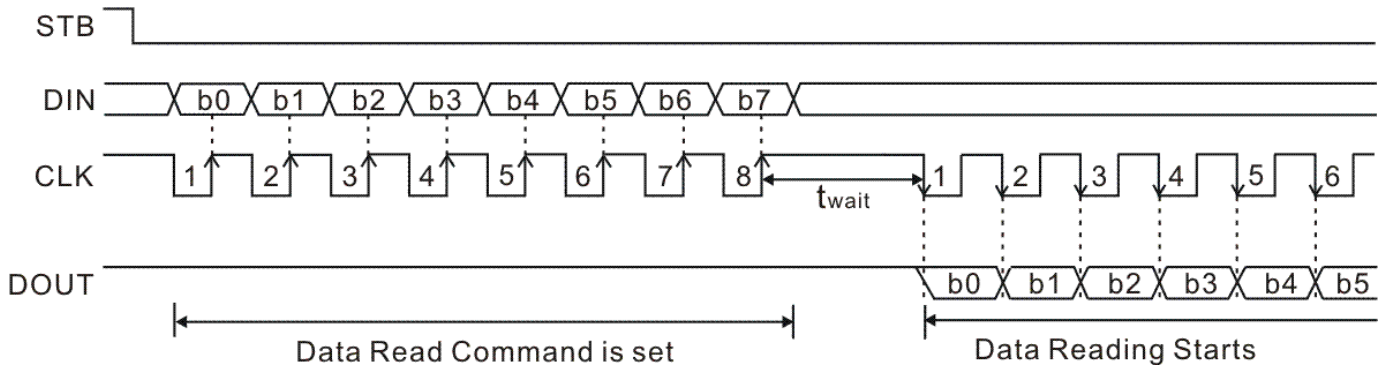
SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6958 serial communication format. The DOUT Pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1 KΩ to 10 KΩ) must be connected to DOUT.

Reception (Data/Command Write)



Transmission (Data Read)

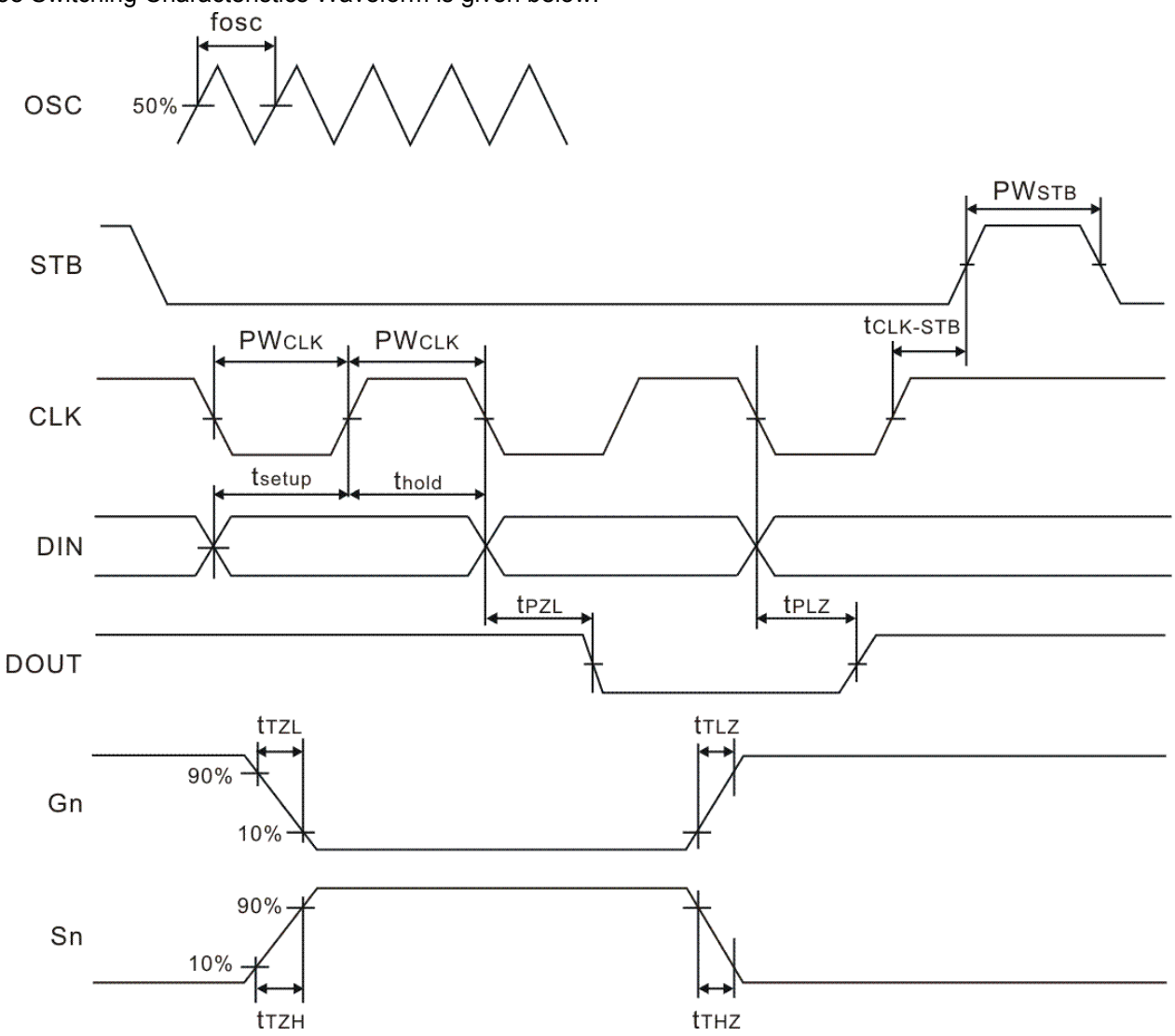


where: twait (waiting time) ≥ 1 μs

It must be noted that when the data is read, the waiting time (t_{wait}) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1 μs.

SWITCHING CHARACTERISTIC WAVEFORM

PT6958 Switching Characteristics Waveform is given below.



where:

fosc = Oscillation Frequency

PW_{STB} (Strobe Pulse Width) ≥ 1 μs

t_{setup} (Data Setup Time) ≥ 100 ns

t_{TZH} (Segment Rise Time) ≤ 1 μs

t_{TZL} (Grid Fall Time) ≤ 2μs(VDD=3.3V)

t_{TZL} (Grid Fall Time) ≤ 1 μs(VDD=5V)

t_{PZL} (Propagation Delay Time) ≤ 200 ns(3.3V)

t_{PZL} (Propagation Delay Time) ≤ 100 ns(5V)

PW_{CLK} (Clock Pulse Width) ≥ 400 ns

$t_{CLK-STB}$ (Clock - Strobe Time) ≥ 1 μs

t_{hold} (Data Hold Time) ≥ 100 ns

t_{THZ} (Segment Fall Time) ≤ 10 μs

t_{TLZ} (Grid Rise Time) ≤ 20 μs(VDD=3.3V)

t_{TLZ} (Grid Rise Time) ≤ 10 μs(VDD=5V)

t_{PLZ} (Propagation Delay Time) ≤ 600 ns(3.3V)

t_{PLZ} (Propagation Delay Time) ≤ 300 ns(5V)

Note:

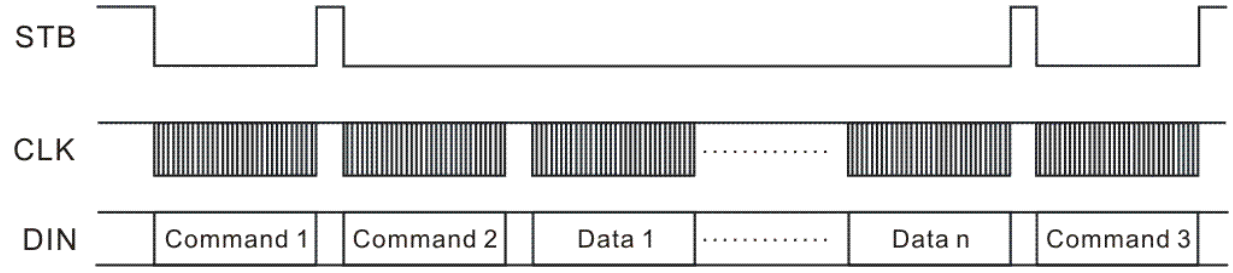
Test Condition Under

t_{THZ}, t_{TZH}: Pull low resistor=10KΩ, Loading capacitor=300pF

t_{TLZ}, t_{TZL}: Pull high resistor=10KΩ, Loading capacitor=300pF

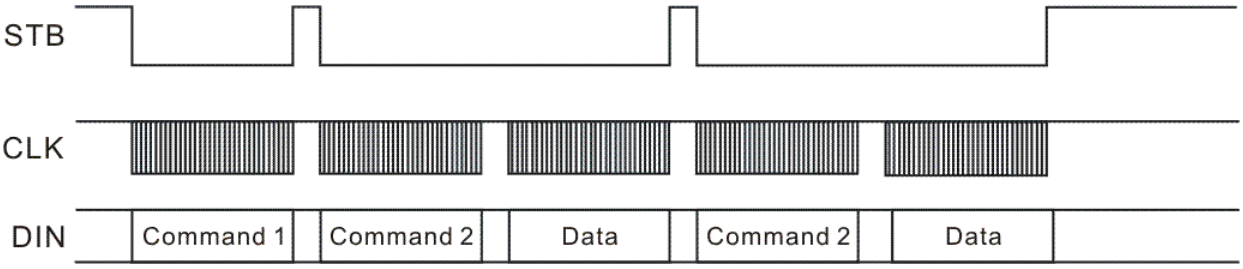
APPLICATIONS

Display memory is updated by incrementing addresses. Please refer to the following diagram.



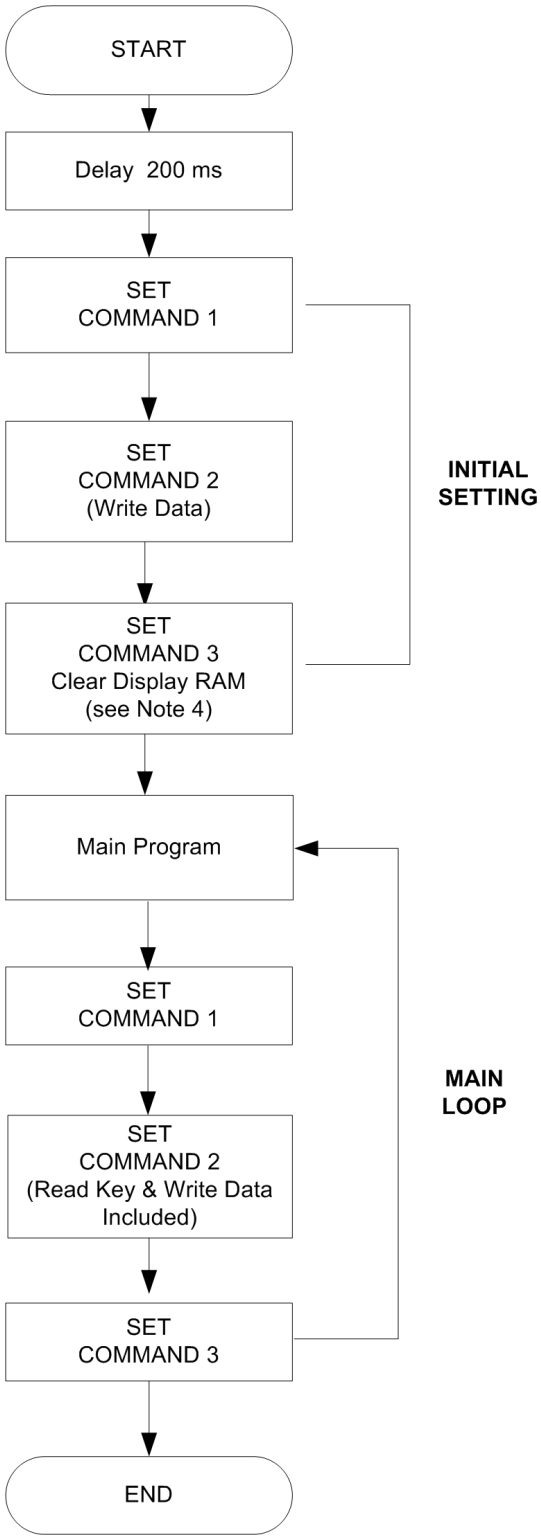
where:
Command 1: Data Setting Command
Command 2: Address Setting Command
Data 1 to n: Transfer Display Data (10 Byte max.)
Command 3: Display Control Command

The following diagram shows the waveforms when updating specific addresses.



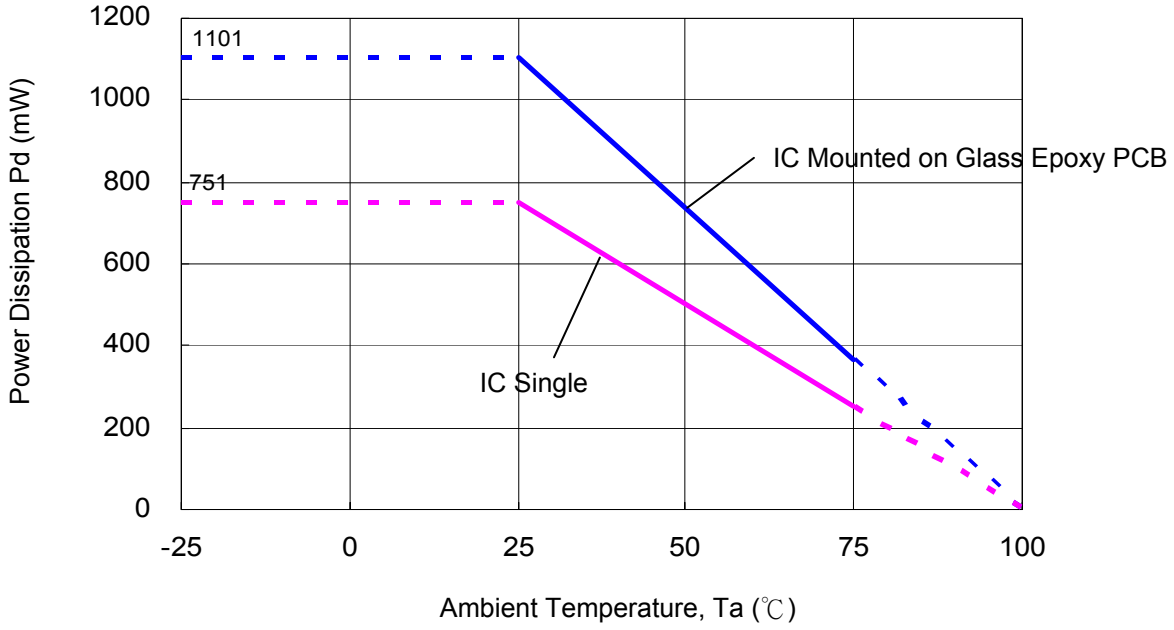
where:
Command 1: Data Setting Command
Command 2: Address Setting Command
Data: Display Data

RECOMMENDED SOFTWARE FLOWCHART



Notes:
1. Command 1: Data Setting Commands.
2. Command 2: Address Setting Commands.
3. Command 3: Display Control Commands.
4. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

SOP 28 (300MIL) THERMAL PERFORMANCE IN STILL AIR
TJ= 100℃



ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta = 25℃, GND = 0 V)

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	-0.3 to +7	V
Logic Input Voltage	V_I	-0.3 to VDD+0.3	V
Driver Output Current	I_{OLGR}	+250	mA
	I_{OHSG}	-50	mA
Operating Temperature	Topr	-40 ~ +85	℃
Storage Temperature	Tstg	-65 ~ +150	℃

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta = -20 ~ +70℃, GND = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply Voltage	V_{DD}	V_{DD}	3.3	5	5.5	V
Dynamic Current (See note)	I_{DDdyn}	V_{DD}	-	-	5	mA
High-Level Input Voltage	V_{IH}	V_{DD}=5V	0.75V_{DD}	-	V_{DD}	V
		V_{DD}=3.3V	0.75V_{DD}	-	V_{DD}	
Low-Level Input Voltage	V_{IL}	V_{DD}=5V	0	-	0.3V_{DD}	V
		V_{DD}=3.3V	0	-	0.2V_{DD}	

Note: Test Condition: Set Display Control Commands = 80H (Display Turn OFF State)

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, V_{DD} = 3.3V, GND = 0 V, Ta = 25℃)

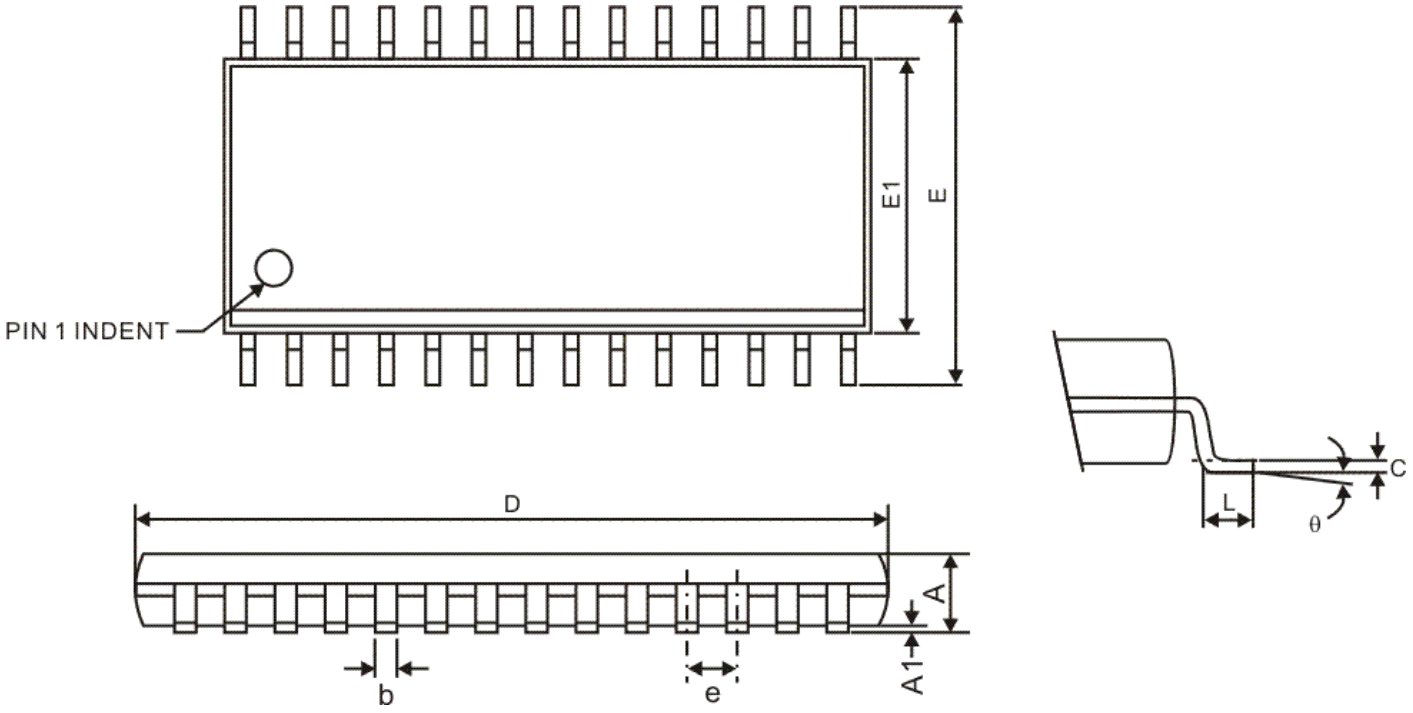
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High-Level Output Current	$I_{OHSG(1)}$	$V_O = V_{DD}$-1 V SG1 to SG10	-8	-10	-	mA
	$I_{OHSG(2)}$	$V_O = V_{DD}$-2 V SG1 to SG10	-16	-20	-	mA
Low-Level Output Current	I_{OLGR}	V_O = 0.3 V GR1 to GR5	65	85	-	mA
Low-Level Output Current	I_{OLDOUT}	VO=0.4V	3	-	-	mA
Segment High-Level Output Current Tolerance	I_{TOLSG}	$V_O = V_{DD}$-1 V SG1 to SG10	-	-	±5	%
High-Level Input Voltage	V_{IH}	-	0.75V_{DD}	-	V_{DD}	V
Low-Level Input Voltage	V_{IL}	-	0	-	0.2V_{DD}	V
Oscillation Frequency	fosc	R =33KΩ	350	500	650	KHz
K1 to K4 Pull Down Resistor	R_{KN}	K1 to K4 V_{DD} = 3.3 V	90	-	180	KΩ

(Unless otherwise stated, VDD =5V, GND=0V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Current	$I_{OHSG(1)}$	VO= VDD -1V SG1 to SG10	-10	-14	-	mA
	$I_{OHSG(2)}$	VO= VDD -2V SG1 to SG10	-20	-25	-	mA
Low-Level Output Current	I_{OLGR}	VO=0.3V GR1 to GR5	100	140	-	mA
Low-Level Output Current	I_{OLDOUT}	VO=0.4V	4	-	-	mA
Segment High-Level Output Current Tolerance	I_{TOLSG}	VO= VDD -1V SG1 to SG10	-	-	±5	%
High-Level Input Voltage	V_{IH}	-	0.75V_{DD}	-	V_{DD}	V
Low-Level Input Voltage	V_{IL}	-	0	-	0.3V_{DD}	V
Oscillation Frequency	fosc	R=51KΩ	350	500	650	KHz
K1 to K3 Pull Down Resistor	R_{KN}	K1 to K4 VDD =5V	40	-	100	KΩ

PACKAGE INFORMATION

28-PIN, SOP, 300MIL



Symbol	Min.	Nom.	Max.
A	-	-	2.65
A1	-	-	0.30
b	0.31	-	0.51
c	0.20	-	0.33
D	17.90 BSC		
E	10.30 BSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.38	-	1.27
θ	0°	-	8°

Note: All controlling dimensions are in millimeters.

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

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