

# M66311P/FP

# 16-Bit LED Driver with Shift Register and Latch

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### **Description**

M66311P/FP is a LED array driver having a 16 bit serial-input and parallel output shiftregister function with direct coupled reset input and output latch function.

This product guarantees the output electric current of 24 mA which is sufficient for anode common LED drive, capable of flowing 16 bits continuously at the same time.

Parallel output is open drain output.

In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

Furthermore, pin lay-out ensures the realization of an easy printed circuit.

#### **Features**

- Anode common LED drive
- High output current all parallel output  $I_{OL} = 24$  mA simultaneous lighting available
- Low power dissipation: 100 µW/package (max)
  - $(V_{CC} = 5 \text{ V}, \text{ Ta} = 25^{\circ}\text{C}, \text{ quiescent state})$
- High noise margin
  - schmitt input circuit provides responsiveness to a long line length.
- Equipped with direct-coupled reset
- Open drain output
  - (except serial data output)
- Wide operating temperature range:  $Ta = -40 \text{ to } +85^{\circ}\text{C}$
- Pin lay-out facilitates printed circuit wiring. (This lay-out facilitates cascade connection and LED connection.)

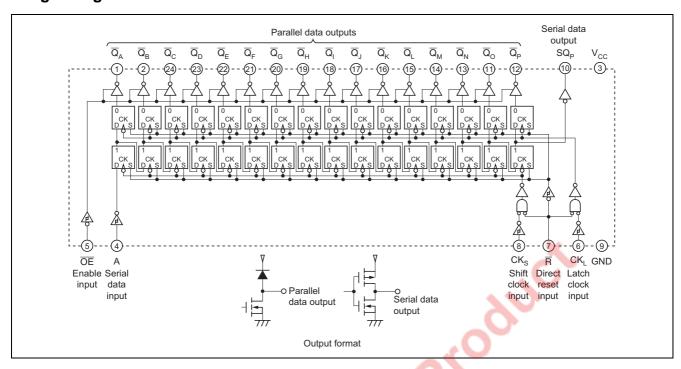
#### **Application**

LED array drive of BUTTON TELEPHONE

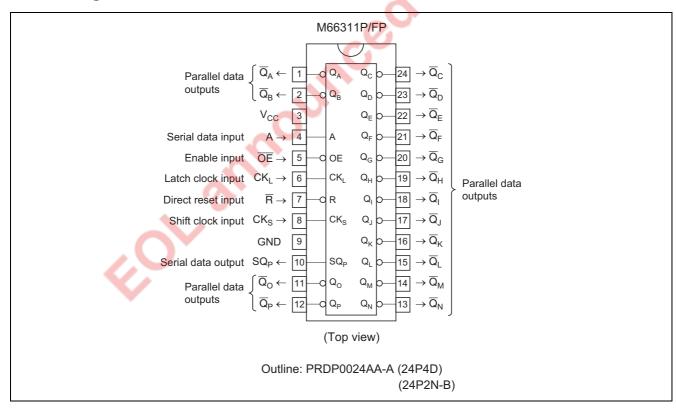
LED array drive of ERASER of a PPC copier

Other various LED modules

# **Logic Diagram**



### **Pin Arrangement**



### **Functional Description**

As M66311P/FP uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shiftregister consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input  $CK_S$  and latch clock input  $CK_L$  are independent from each other, shift and latch operations being made when "L" changes to "H".

Serial data input A is the data input of the first–step shiftregister and the signal of A shifts shifting registers one by one when a pulse is impressed to  $CK_S$ . When A is "H", the signal of "L" shifts.

When the pulse is impressed to  $CK_L$ , the contents of the shifting register at that time are stored in a latching register, and they appear in the outputs from  $\overline{Q}_A$  to  $\overline{Q}_P$ .

Outputs from  $\overline{Q}_A$  to  $\overline{Q}_P$  are open drain outputs.

To extend the number of bits, use the serial data output SQ<sub>P</sub> which shows the output of the shifting register of the 16th bit.

If  $CK_S$  and  $CK_L$  are connected, the state of the shifting register with one clock delay is outputted to  $\overline{Q}_A$  to  $\overline{Q}_P$ .

When reset input  $\overline{R}$  is changed to "L",  $\overline{Q}_A$  to  $\overline{Q}_P$  and  $SQ_P$  are reset. In this case, shifting and latching registers are set.

If "H" is impressed to output enable input OE,  $\overline{Q}_A$  to  $\overline{Q}_P$  reaches the high impedance state, but  $SQ_P$  does not reach the high impedance state. Furthermore, change in OE does not affect shift operation.

#### Function Table (Note)

		Input				Parallel Data Output						Serial Data Output												
Operation	Mode	R	CKs	CKL	Α	ŌĒ	$\overline{Q}_{\overline{A}}$	$\overline{Q}_{\overline{B}}$	$\overline{Q}_{\overline{C}}$	$\overline{Q}_{\overline{D}}$	$\overline{Q}_{\overline{E}}$	$\overline{Q}_{\overline{F}}$	$\overline{Q}_{\overline{G}}$	$\overline{Q}_{\overline{H}}$	$\overline{Q}_{\overline{l}}$	$\overline{Q}_{\overline{J}}$	$\overline{Q}_{\overline{K}}$	$\overline{Q}_{\overline{L}}$	$\overline{Q}_{\overline{M}}$	$\overline{Q}_{\overline{N}}$	$\overline{Q}_{\overline{O}}$	$\overline{Q}_{\overline{P}}$	SQ <sub>P</sub>	Remarks
Reset		L	Х	Х	Х	Х	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	L	-
Shift	Shift t1	Н	1	Х	Н	L	$\overline{Q}_{\overline{A}}^{0}$	$\overline{Q}_{\overline{B}}^0$	$\overline{Q}_{\overline{C}^0}$	$\overline{Q}_{\overline{D}}^0$	$\overline{Q}_{\overline{E}^0}$	$\overline{Q}_{F}^{0}$	$\overline{Q}_{\overline{G}}^{0}$	$\overline{Q}_{\overline{H}^0}$	$\overline{Q}_{\overline{l}}^{0}$	$\overline{Q}_{\overline{J}^0}$	$\overline{Q}_{\overline{K}}^0$	$\overline{Q}_{\overline{L}^0}$	$\overline{Q}_{\overline{M}}^{0}$	$\overline{Q}_{\overline{N}}^{0}$	$\overline{Q}_{\overline{O}}^0$	$\overline{Q}_{\overline{P}}^0$	q <sub>o</sub> <sup>0</sup>	Output
latch	Latch t2	Н	Х	1	Х	L	L	$q_A^0$	q <sub>B</sub> <sup>0</sup>	q <sub>C</sub> <sup>0</sup>	$q_D^0$	q <sub>E</sub> <sup>0</sup>	q <sub>F</sub> <sup>0</sup>	$q_G^0$	q <sub>H</sub> <sup>0</sup>	q <sub>I</sub> <sup>0</sup>	q <sub>J</sub> <sup>0</sup>	q <sub>K</sub> <sup>0</sup>	$q_L^0$	q <sub>M</sub> <sup>0</sup>	q <sub>N</sub> <sup>0</sup>	q <sub>o</sub> <sup>0</sup>	q <sub>o</sub> <sup>0</sup>	lighting "H"
operation	Shift t1	Н	1	Х	L	L	$\overline{Q}_{\overline{A}}^{0}$	$\overline{Q}_{\overline{B}}^0$	$\overline{Q}_{\overline{C}^0}$	$\overline{Q}_{\overline{D}}^0$	$\overline{Q}_{\overline{E}}^{0}$	$\overline{Q}_{F}^{0}$	$\overline{Q}_{\overline{G}^0}$	$\overline{Q}_{\overline{H}^0}$	$\overline{Q}_{\overline{l}}^{0}$	$\overline{Q}_{\overline{J}^0}$	$\overline{Q}_{\overline{K}}^0$	$\overline{Q}_{\overline{L}^0}$	$\overline{Q}_{\overline{M}}^{0}$	$\overline{Q}_{\overline{N}}^{0}$	$\overline{Q}_{\overline{O}}^0$	$\overline{Q}_{\overline{P}}^0$	q <sub>o</sub> <sup>0</sup>	Output
	Latch t2	Н	Х	1	Х	L	Z	q <sub>A</sub> 0	q <sub>B</sub> <sup>0</sup>	q <sub>C</sub> <sup>0</sup>	$q_D^0$	q <sub>E</sub> 0	q <sub>F</sub> 0	$q_G^0$	q <sub>H</sub> <sup>0</sup>	q <sub>I</sub> <sup>0</sup>	q <sub>J</sub> 0	q <sub>K</sub> <sup>0</sup>	$q_L^0$	q <sub>M</sub> <sup>0</sup>	q <sub>N</sub> <sup>0</sup>	q <sub>o</sub> <sup>0</sup>	q <sub>o</sub> 0	lights-out "L"
Output dis	able	Х	Х	Х	Х	Н	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	$q_P$	_

#### Note 1

- 1: Change from low-level to high-level
- Q

  Output state Q before CK<sub>L</sub> changed
- X: Irrelevant
- q0: Contents of shift register before CKs changed
- q: Contents of shift register
- t<sub>1</sub>, t<sub>2</sub>: t<sub>2</sub> is set after t<sub>1</sub> is set
- Z: High impedance

# **Absolute Maximum Ratings**

 $(Ta = -40 \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted})$ 

Item	Symbol	Ratings	Unit	Conditions					
Supply voltage		V <sub>CC</sub>	-0.5 to +7.0	V					
Input voltage			roltage		$-0.5$ to $V_{CC} + 0.5$	V			
Output voltage	t voltage		ut voltage		ut voltage		$-0.5$ to $V_{CC} + 0.5$	V	
Input protection diode current		I <sub>IK</sub>	-20	mA	$V_{I} < 0 V$				
			20		$V_{I} > V_{CC}$				
Output parasitic diode current		lok	-20	mA	V <sub>O</sub> < 0 V				
			20		$V_{O} > V_{CC}$				
Output current per output pin	$\overline{Q}_A$ to $\overline{Q}_P$	lo	50	mA					
	SQ <sub>P</sub>		±25						
Supply/GND current		Icc	-20, +410	mA	V <sub>CC</sub> , GND				
Power dissipation	Power dissipation		500	mW	(Note)				
Storage temperature range		Tstg	-65 to +150	°C					

Note: M66311FP; Ta = -40 to +70°C, Ta = 70 to 85°C are derated at -6 mW/°C.

# **Recommended Operating Conditions**

 $(Ta = -40 \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted})$ 

Item	Symbol	Min	Тур	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5	5.5	V
Input voltage	Vi	0	_	V <sub>cc</sub>	V
Output voltage	Vo	0	_	V <sub>cc</sub>	V
Operating temperature range	Topr	-40		+85	°C

# **Electrical Characteristics**

 $(V_{CC} = 4.5 \text{ to } 5.5 \text{V}, \text{ unless otherwise noted})$ 

	Sy Limits									
	mb	Т	a = 25°	C	Ta = -40	to +85°C				
Item	ol	Min	Тур	Max	Min	Max	Unit	Con	ditions	
Positive-going threshold voltage	V <sub>T+</sub>	0.35×V <sub>CC</sub>	_	0.7×V <sub>CC</sub>	0.35×V <sub>CC</sub>	0.7×V <sub>CC</sub>	V	$V_O = 0.1 \text{ V}, V_{CC}-0.1 \text{ V}$ $ I_O  = 20 \mu\text{A}$		
Negative-going threshold voltage	V <sub>T</sub>	0.2×V <sub>CC</sub>	_	0.55×V <sub>CC</sub>	0.2×V <sub>CC</sub>	0.55×V <sub>CC</sub>	V	$V_0 = 0.1 \text{ V}, V_0$ $ I_0  = 20  \mu\text{A}$	<sub>C</sub> -0.1 V	
Low-level	$V_{OL}$	_	_	0.1	_	0.1	V	$V_I = V_{T_+}, \ V_{T-}$	$I_{OL} = 20 \ \mu A$	
output_voltage		_	_	0.44	_	0.53		$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 24 \text{ mA}$	
$\overline{\mathbf{Q}}_{A}$ to $\overline{\mathbf{Q}}_{P}$		_	_	0.73	_	0.94			I <sub>OL</sub> = 40 mA (Note)	
High-level	V <sub>OH</sub>	V <sub>CC</sub> -0.1	_	_	V <sub>CC</sub> -0.1	_	V	$V_I = V_{T_+}, V_{T}$	I <sub>OH</sub> = -20 μA	
output voltage SQ <sub>P</sub>		3.83	_	_	3.66	_		$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -4 \text{ mA}$	
Low-level	Vol	_	_	0.1	_	0.1	V	$V_I = V_{T_+}, \ V_{T}$	$I_{OL} = 20 \ \mu A$	
output voltage SQ <sub>P</sub>		_	_	0.44	_	0.53	.0	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 4 mA	
High-level input current	Iн	_	_	0.5	_	5.0	μА	$V_{I} = V_{CC}, V_{CC} =$	= 5.5 V	
Low-level input current	I <sub>IL</sub>	_	_	-0.5	_	-5.0	μА	$V_I = GND, V_{CO}$	= 5.5 V	
Maximum	Ιο		_	1.0	- /	10.0	μΑ	$V_I = V_{T+}, \ V_{T-}$	$V_O = V_{CC}$	
output leakage current $\overline{Q}_A$ to $\overline{Q}_P$		_	_	-1.0	70,	<del>/</del> –10.0		V <sub>CC</sub> = 5.5 V	$V_O = GND$	
Quiescent supply current	Icc	_	_	20.0	_	200.0	μА	$V_I = V_{CC}$ , GND	, V <sub>CC</sub> = 5.5 V	

Note: M66311 is used under the condition of an output current I<sub>OL</sub> = 40 mA, the number of simultaneous drive outputs is restricted as shown in the Duty Cycle-I<sub>OL</sub> of Standard characteristics.

# **Switching Characteristics**

 $(V_{CC} = 5 V)$ 

			Ta = 25°C	Ta = -		to +85°C		
Item	Symbol	Min	Тур	Max	Min	Max	Unit	Conditions
Maximum clock frequency	f <sub>max</sub>	5	_	_	4	_	MHz	$C_L = 50 \text{ pF}$
Low-level to high-level and	t <sub>PLH</sub>	_	_	100	_	130	ns	$R_L = 1 \text{ k}\Omega$ (Note 2)
high-level to low-level output propagation time (CK <sub>S</sub> -SQ <sub>P</sub> )	t <sub>PHL</sub>	1	_	100	_	130	ns	(Note 2)
$\begin{array}{l} \mbox{High-level to low-level} \\ \mbox{output propagation time } (\overline{R} - \mbox{$SQ_P$}) \end{array}$	t <sub>PHL</sub>	l		100	_	130	ns	
Low-level to high-level output propagation time ( $\overline{R}$ - $\overline{Q}_A$ to $\overline{Q}_P$ )	t <sub>PLZ</sub>		_	150	_	200	ns	
Low-level to high-level and	t <sub>PZL</sub>	-	_	100	_	130	ns	
high-level to low-level output propagation time $(CK_L-\overline{Q}_A \text{ to } \overline{Q}_P)$	t <sub>PLZ</sub>		_	150	_	200	ns	
Output enable time to low-	t <sub>PZL</sub>	-	_	100	_	130	ns	
level and high-level ( $\overline{OE}$ – $\overline{\mathbb{Q}}_A$ to $\overline{\mathbb{Q}}_P$ )	t <sub>PLZ</sub>	1	_	150	01	200	ns	
Input Capacitance	Cı	_	_	10		10	pF	
Output Capacitance	Co	_	_	15	_	15	pF	$\overline{OE} = V_{CC}$
Power dissipation Capacitance (Note 1)	C <sub>PD</sub>		5	0	_	_	pF	

Note: 1. C<sub>PD</sub> is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)

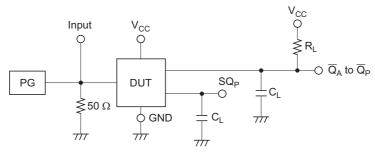
The power dissipated during operation under no-load conditions is calculated using the following formula:  $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_I + I_{CC} \bullet V_{CC}$ 

# **Timing Requirements**

 $(V_{CC} = 5 V)$ 

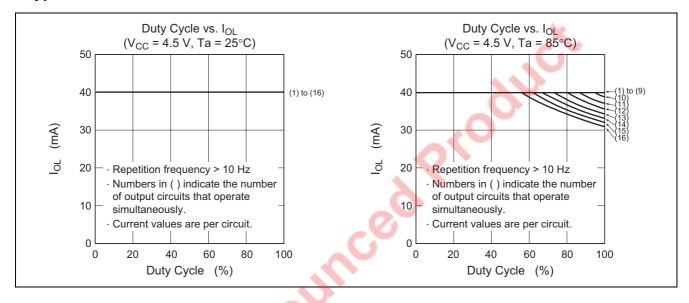
	0		Ta = 25°C		Ta = -40	to +85°C		
Item	Symbol	Min	Тур	Max	Min	Max	Unit	Conditions
CK <sub>S</sub> , CK <sub>L</sub> , R pulse width	t <sub>w</sub>	100	_	_	130	_	ns	(Note 2)
A setup time with respect to CK <sub>S</sub>	t <sub>su</sub>	100	_	_	130	1	ns	
CK <sub>S</sub> setup time with respect to CK <sub>L</sub>	t <sub>su</sub>	100	_	_	130		ns	
A hold time with respect to CK <sub>S</sub>	t <sub>h</sub>	10	_	_	15	_	ns	
R, recovery time with respect to CK <sub>S</sub> , CK <sub>L</sub>	t <sub>rec</sub>	50	_	_	70	_	ns	

Note: 2. Test Circuit

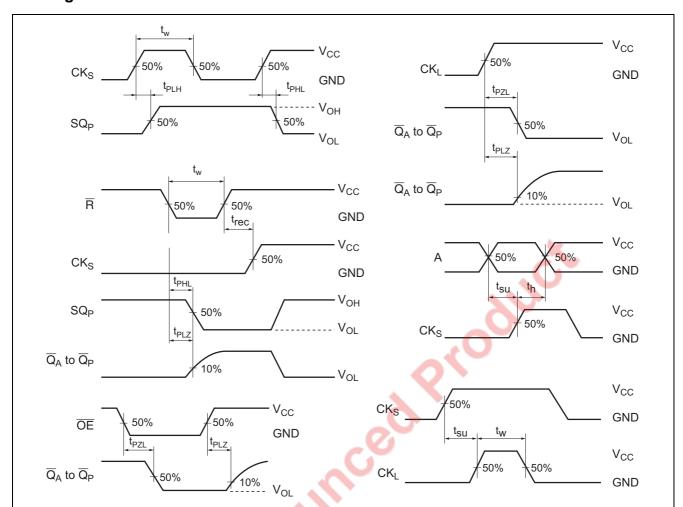


- (1) The pulse generator (PG) has the following characteristics (10% to 90%): tr = 6 ns, tf = 6 ns
- (2) The capacitance C<sub>L</sub> includes stray wiring capacitance and the probe input capacitance.

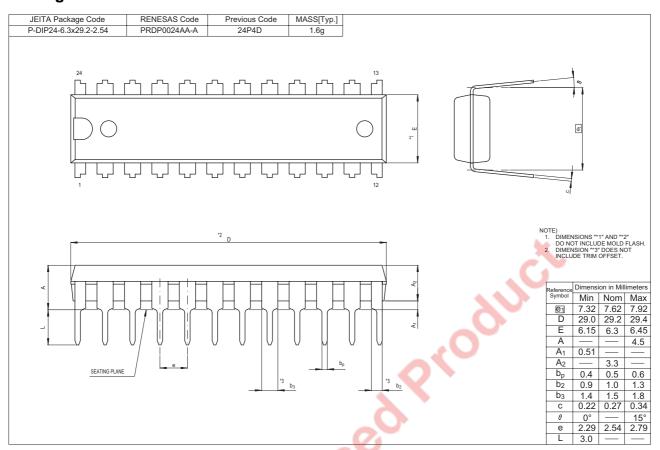
# **Typical Characteristics**



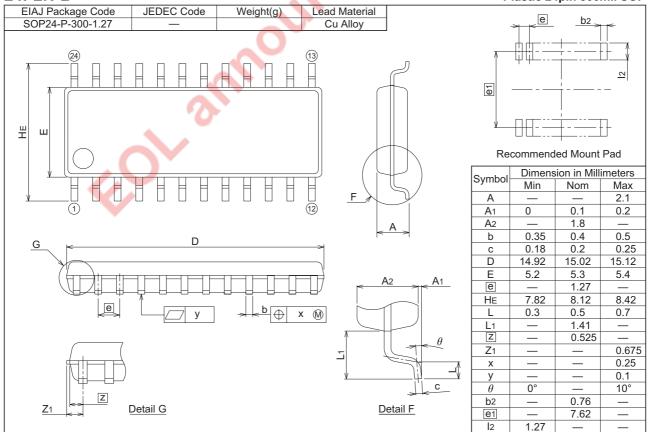
# **Timing Chart**



### **Package Dimensions**







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