Model :755CA0

Mobile AMD Athlon XP with VIA KT400A Chipset

PAGE CONTENT

PCI Resure Allocation

Device	IDSEL	REQ	GNT#	INT
IEEE1394	AD20	REQ#1	GNT#1	INT#D
MINI PCI	AD21	REQ#2	GNT#2	INT#B,C
CB	AD22	REQ#3	GNT#3	INT#B

VT8235 GPIO

GPI0	NC	GPO0	HDDREST#
GPI1	NC	GPO1	SUSA#
GPI2	EXTSMI#	GPO2	SUSB#
GPI3	CARD_RI#	GPO3	SUSST1#
GPI4	NC	GPO4	SUSCLK
GPI5	NC	GPO5	CPUSTP#
GPI6	SCI#	GPO6	PCISTP#
GPI7	NC	GPO7	NC
GPIO8	LCDSEL1#		
GPIO9	LCDSEL0#		
GPIO10	NC		
GPIO11	NC		
GPIO12	NC		
GPIO13	LCDSEL2#		
GPIO14	NC		
GPIO15	NC		
GPI16	NC	GPO16	STRAP
GPI17	NC	GPO17	STRAP
GPI18	NC	GPO18	STRAP
GPI19	NC	GPO19	STRAP
GPIO20	NC		
GPIO21	NC		
GPIO22	NC		
GPIO23	NC		
GPIO24	NC		
GPIO25	NC		
GPIO26	NC		
GPIO27	NC		
GPIO28	NC		
GPIO29	NC		
GPIO30	NC		
GPIO31	NC		

NS87591 GPIO

IOPA0	PME#
IOPA1	BTL_BEEP
IOPA2	CHGLED
IOPA3	PCIRST_MASK#
IOPA4	SUS_LED
IOPA5	LAN_DISABLE
IOPA6	PWR_ON
IOPA7	SUS_ON
IOPB0	KBC_PWRBTN#
IOPB1	PWROK_EC
IOPB2	AMP_MUTE
IOPB3	BAT_SMBCLK
IOPB4	BAT_SMBDAT
IOPB5	KBC_A20G
IOPB6	KBC_RST#
IOPB7	NC
IOPC0	**FAN_INT#**
IOPC1	FAN_SMBCLK
IOPC2	FAN_SMBDATA
IOPC3	NC
IOPC4	NC
IOPC5	SUSC#
IOPC6	FAN_SPD#
IOPC7	SUSA#
IOPD0	MAIL#
IOPD1	AC_IN#
IOPD2	PCIRST#(REV)
IOPD3	SCI#
IOPF0	PS2_MS_CLK
IOPF1	PS2_MS_DATA
IOPF2	PS2_KB_CLK
IOPF3	PS2_KB_DATA
IOPF4	TP_CLK
IOPF5	TP_DATA
IOPF6	PWROK_CPU
IOPF7	E_ID1
IOPH0	XA0
IOPH1	XA1
IOPH2	XA2
IOPH3	XA3
IOPH4	XA4
IOPH5	XA5
IOPH6	XA6
IOPH7	XA7
IOPI0	XD0
IOPI1	XD1
IOPI2	XD2
IOPI3	XD3
IOPI4	XD4
IOPI5	XD5
IOPI6	XD6
IOPI7	XD7
IOPJ0	XMEMR#
IOPJ1	XMEMW#

NS87591 GPIO

IOPD4	PWRON_LED
IOPD5	CAPS#
IOPD6	NUM#
IOPD7	SCROLL#
IOPK0	XA8
IOPK1	XA9
IOPK2	XA10
IOPK3	XA11
IOPK4	XA12
IOPK5	XA13
IOPK6	XA14
IOPK7	XA15
IOPL0	XA16
IOPL1	XA17
IOPL2	XA18
IOPL3	NC
IOPL4	LCD_SW
IOPM0	**ADAP_OFF**
IOPM1	**SUS_SKIP**
IOPM2	CHG_ON
IOPM3	LID#
IOPM4	TP_BTU
IOPM5	TP_BTD
IOPM6	NC
IOPM7	SUSB#
IOPJ2	FLASHEN#
IOPJ3	NC
IOPJ4	NC
IOPJ5	**FSB_EC**
IOPJ6	**NC**
IOPJ7	CORE_ON

NS87591 GPO

IOPC0	NC
DA0	BLDATJ
DA1	SET_I
DA2	**RSMRST**
DA3	FAN_CTRL

NS87591 GPI

IOPE0	V_CPU
IOPE1	GTL+/CPUHOT#
IOPE2	NC
IOPE3	**2FAN_ON**
IOPE4	PWRSW
IOPE5	SEARCH#
IOPE6	+3V_AUX
IOPE7	BROWSER#
AD0	NC
AD1	TEMP
AD2	STOP_CHG#
AD3	I_CPU
AD8	NC
AD9	NC

P/N: 37-UD8000-00B

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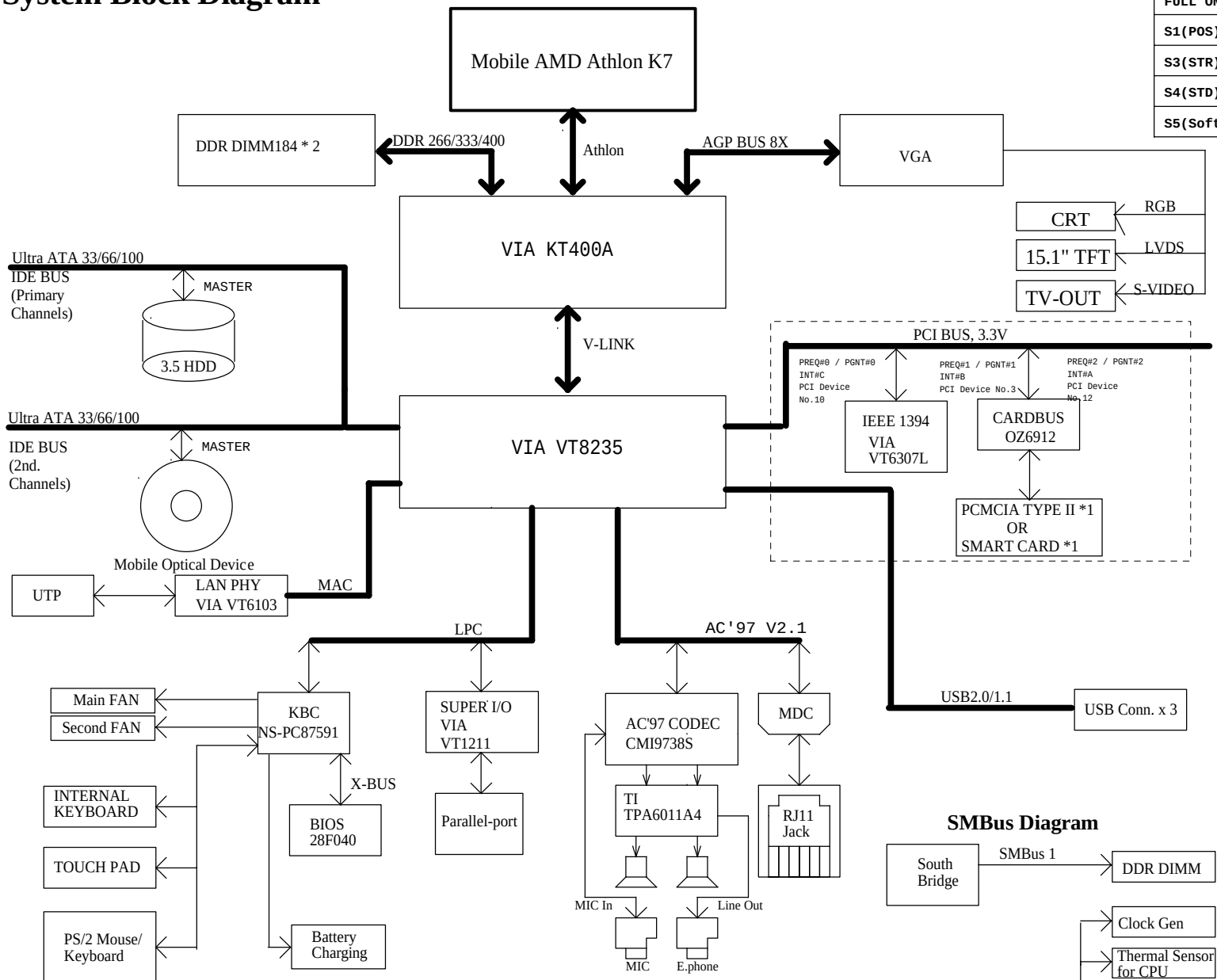
System Block Diagram

P4M Power states						
	SUS_ON	PWR_ON	+*_AUX	+V*	+*SUS	Clocks
FULL ON	HIGH	HIGH	ON	ON	ON	ON
S1(POS)	HIGH	HIGH	ON	ON	ON	LOW
S3(STR)	LOW	HIGH	ON	ON	OFF	LOW
S4(STD)	LOW	LOW	ON	OFF	OFF	OFF
S5(SoftOff)	LOW	LOW	ON	OFF	OFF	OFF



Power Plane

VCC1.5
VCC1.25
VCC2.5
VCC2.5SUS
VCC3
VCC3_SUS
VCC3_AUX
VCC5
VCC5_SUS
VCC5_AUX
VCC12

SMBus Diagram

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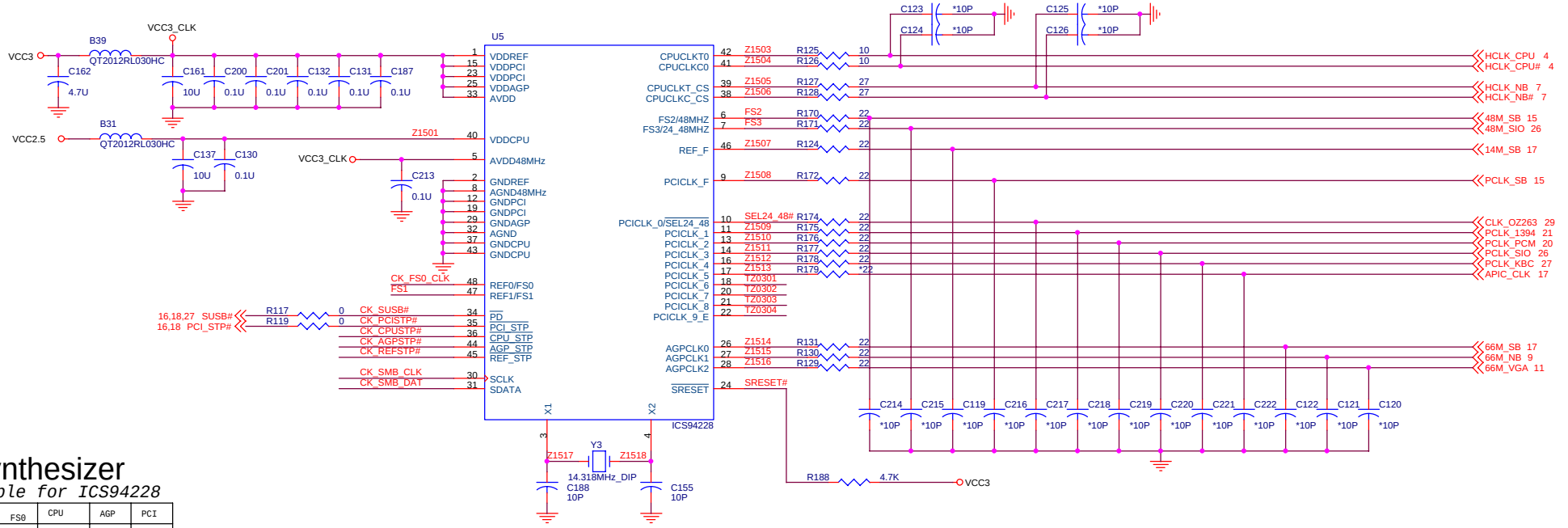
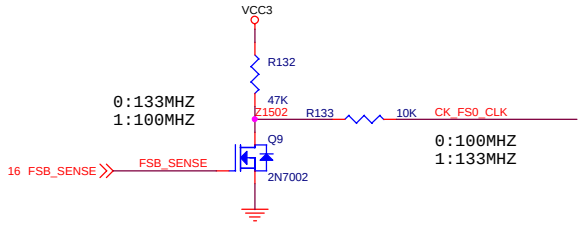
CLock Synthesizer

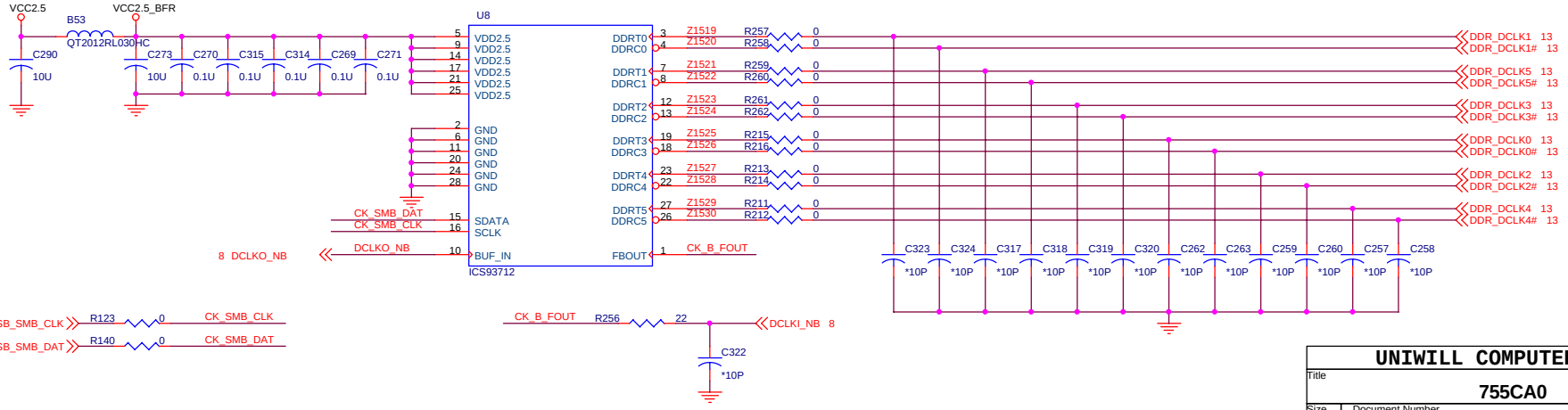
Frequency table for ICS94228

SW1

FS3	FS2	FS1	FS0	CPU	AGP	PCI
1	1	1	1	233.33	77.78	38.88
1	1	1	0	220	73.33	36.67
1	1	0	1	210	70	35
1	1	0	0	200	66.67	33.33
1	0	1	1	190	76	38
1	0	1	0	180	72	36
1	0	0	1	170	68	34
1	0	0	0	150	75	37.5
0	1	1	1	140	70	35
0	1	1	0	120	60	30
0	1	0	1	110	66	33
0	1	0	0	66.67	66.67	33.33
0	0	1	1	200	66.67	33.33
0	0	1	0	166.67	66.67	33.33
0	0	0	1	100	66.67	33.33
0	0	0	0	133.33	66.67	33.33







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UNIWILL COMPUTER CORP.

7 AIN#[2:14]
7 AOUT#[2:14]
7 SDATA#[0:63]
7 DOCLK#[0:3]
7 AIN#[2:14]

U2A

SDATA#0 AA35 SDATA0
SDATA#1 W37 SDATA1
SDATA#2 W35 SDATA2
SDATA#3 Y35 SDATA3
SDATA#4 U35 SDATA4
SDATA#5 U33 SDATA5
SDATA#6 S37 SDATA6
SDATA#7 S33 SDATA7
SDATA#8 AA33 SDATA8
SDATA#9 AE37 SDATA9
SDATA#10 AC33 SDATA10
SDATA#11 AC37 SDATA11
SDATA#12 Y37 SDATA12
SDATA#13 AA37 SDATA13
SDATA#14 AC35 SDATA14
SDATA#15 S35 SDATA15
SDATA#16 Q37 SDATA16
SDATA#17 Q35 SDATA17
SDATA#18 N37 SDATA18
SDATA#19 J33 SDATA19
SDATA#20 G33 SDATA20
SDATA#21 G37 SDATA21
SDATA#22 E37 SDATA22
SDATA#23 G35 SDATA23
SDATA#24 Q33 SDATA24
SDATA#25 N33 SDATA25
SDATA#26 L33 SDATA26
SDATA#27 N35 SDATA27
SDATA#28 L37 SDATA28
SDATA#29 J37 SDATA29
SDATA#30 A37 SDATA30
SDATA#31 E35 SDATA31
SDATA#32 E31 SDATA32
SDATA#33 E29 SDATA33
SDATA#34 A27 SDATA34
SDATA#35 A25 SDATA35
SDATA#36 E21 SDATA36
SDATA#37 C23 SDATA37
SDATA#38 C27 SDATA38
SDATA#39 A23 SDATA39
SDATA#40 A35 SDATA40
SDATA#41 C35 SDATA41
SDATA#42 C33 SDATA42
SDATA#43 C31 SDATA43
SDATA#44 A29 SDATA44
SDATA#45 C29 SDATA45
SDATA#46 E23 SDATA46
SDATA#47 C25 SDATA47
SDATA#48 E17 SDATA48
SDATA#49 E13 SDATA49
SDATA#50 E11 SDATA50
SDATA#51 C15 SDATA51
SDATA#52 E9 SDATA52
SDATA#53 A13 SDATA53
SDATA#54 C9 SDATA54
SDATA#55 A9 SDATA55
SDATA#56 C21 SDATA56
SDATA#57 A21 SDATA57
SDATA#58 E19 SDATA58
SDATA#59 C19 SDATA59
SDATA#60 C17 SDATA60
SDATA#61 A11 SDATA61
SDATA#62 A17 SDATA62
SDATA#63 A15 SDATA63

5 DICLK#0 DICLK#0 W33 SDATAINCLK0
5 DICLK#1 DICLK#1 J35 SDATAINCLK1
5 DICLK#2 DICLK#2 E27 SDATAINCLK2
5 DICLK#3 DICLK#3 E15 SDATAINCLK3

7 DIVAL# DIVAL# AN33 SDATAINVAL

7 DOCLK#0 DOCLK#0 AE35 SDATAOUTCLK0
7 DOCLK#1 DOCLK#1 C37 SDATAOUTCLK1
7 DOCLK#2 DOCLK#2 A33 SDATAOUTCLK2
7 DOCLK#3 DOCLK#3 C11 SDATAOUTCLK3

DOVAL# AL31 SDTATOUTVAL

AIN#0 AJ29 SADDIN0
AIN#1 AL29 SADDIN1
AIN#2 AG33 SADDIN2
AIN#3 AJ37 SADDIN3
AIN#4 AL35 SADDIN4
AIN#5 AE33 SADDIN5
AIN#6 AJ35 SADDIN6
AIN#7 AG37 SADDIN7
AIN#8 AL33 SADDIN8
AIN#9 AN37 SADDIN9
AIN#10 AL37 SADDIN10
AIN#11 AG35 SADDIN11
AIN#12 AN29 SADDIN12
AIN#13 AN35 SADDIN13
AIN#14 AN31 SADDIN14

7 AICLK# AICLK# AJ33 SADDINCLK

7 CFWDRST CFWDRST AJ21 CLKFWDRST
7 CONNECT CONNECT AL23 CONNECT
7 PROCRDY PROCRDY AN23 PROCRDY
FILVAL# AJ31 SFILLVAL

PPGA_462

A20M AE1 ATHLON_A20M# → ATHLON_A20M# 17
FERR AG1 FERR
INIT AJ3 ATHLON_CPUINIT# → ATHLON_CPUINIT# 17
INTR AL1 ATHLON_INTR → ATHLON_INTR 17
IGNNE AJ1 ATHLON_IGNNE# → ATHLON_IGNNE# 17
NMI AN3 ATHLON_NMI → ATHLON_NMI 17
RESET AG3 ATHLON_CPURST# → ATHLON_CPURST# 15
SMI AN5 ATHLON_SMI# → ATHLON_SMI# 17
STPCLK AC1 ATHLON_STPCLK# → ATHLON_STPCLK# 17
NC U37 TZ0402
NC Y33 TZ0403
NC L35 TZ0404
NC E25 TZ0405
NC E33 TZ0406
NC A31 TZ0407
NC C13 TZ0408
NC A19 TZ0409
COREFB- AG13 COREFB-
COREFB+ AG11 COREFB+ → COREFB+ 33

CLKIN AN17 HCLK
CLKIN AL17 HCLK#
RSTCLK AN19
RSTCLK AL19
K7CLKOUT AL21 CLKOUT+
K7CLKOUT AN21 CLKOUT-
PWROK AE3 PWRGOOD → PWRGOOD 6
NC AA5 TZ0410
ANALOG AJ13 TZ0411
VREF_SYS W5 VREF_SYS
ZN AC5 ZN
ZP AE5 ZP
PLLBYPASS AJ25 PLLBP#
PLLBYPASSCLK AN15 PLLCK+
PLLBYPASSCLK AL15 PLLCK-
PLLMON1 AN13 PLLMON1
PLLMON2 AL13 PLLMON2
PLLTEST AC3 PLLTEST#

SCANCLK1 S1 SCANCLK1
SCANCLK2 S5 SCANCLK2
SCANINTEVAL S3 SINTVAL
SCANSHIFTEN Q5 SSHIFTEN

DBRDY AA1 DBRDY
DBREQ AA3 DBREQ#
FLUSH AL3 FLUSH#

TCK Q1 TCK
TDI U1 TDI
TDO U5 TDO
TMS Q3 TMS
TRST U3 TRST#

VID0 L1 CPU_VID0 → CPU_VID0 6
VID1 L3 CPU_VID1 → CPU_VID1 6
VID2 L5 CPU_VID2 → CPU_VID2 6
VID3 L7 CPU_VID3 → CPU_VID3 6
VID4 J7 CPU_VID4 → CPU_VID4 6

FID0 W1 FID0 → FID0 6
FID1 W3 FID1 → FID1 6
FID2 Y1 FID2 → FID2 6
FID3 Y3 FID3 → FID3 6

SVID0 F8 SVID0 → SVID0 6
SVID1 K8 SVID1 → SVID1 6
SVID2 H6 SVID2 → SVID2 6
SVID3 H8 SVID3 → SVID3 6
SVID4 H10 SVID4 → SVID4 6

SADDOUT0 J1 TZ0412
SADDOUT1 J3 TZ0413
SADDOUT2 C7 AOUT#2
SADDOUT3 A7 AOUT#3
SADDOUT4 E5 AOUT#4
SADDOUT5 A5 AOUT#5
SADDOUT6 E7 AOUT#6
SADDOUT7 C1 AOUT#7
SADDOUT8 C5 AOUT#8
SADDOUT9 C3 AOUT#9
SADDOUT10 G1 AOUT#10
SADDOUT11 E1 AOUT#11
SADDOUT12 A3 AOUT#12
SADDOUT13 G5 AOUT#13
SADDOUT14 G3 AOUT#14
SADDOUTCLK E3 AOCLK# → AOCLK# 7

Near socket-A

VCORE
R26 60.4_1
R25 60.4_1
R11 301_1
TP18 HCLK C31 680P HCLK_CPU 3
TP19 HCLK# C30 680P HCLK_CPU# 3

VREF_SYS is set at 50% of VCC_CORE to CPU

VCORE
R91 100_1%
VREF_SYS
C108 0.01U
C109 0.1U
R89 100_1%

Push-pull compensation circuit

VCORE
ZN R68 40.2_1%
ZP R61 40.2_1%

VCORE
CLKOUT- R50 100_1 R59 100_1
CLKOUT+ R60 100_1 R58 100_1

VCORE
PLLCK+ R13 100_1 R28 100_1
PLLCK- R12 100_1 R27 100_1

VCORE
R192 *0
CON28
Z0201 SSHIFTEN SINTVAL SCANCLK2 TZ0401 DBREQ# ATHLON_CPURST#
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
TCK TMS SCANCLK1 TDI TRST# TDO DBRDY PLLTEST#
*HDT CON_OP(BOT)

Near socket-A

VCORE
COREFB+ R10 10
COREFB- R14 10

VCORE
ATHLON_A20M# R64 820
ATHLON_CPURST# R21 820
ATHLON_IGNNE# R24 820
ATHLON_CPUINIT# R18 820
ATHLON_INTR R23 820
ATHLON_NMI R20 820
ATHLON_SMI# R17 820
ATHLON_STPCLK# R49 820

VCORE
FLUSH# R19 820
TRST# R186 820
TDI R182 820
TCK R84 820
TMS R478 820
PLLBP# R53 820
PLLMON1 R16 56
PLLMON2 R15 56
DBREQ# R56 820
PLLTEST# R48 820
AIN#0 R62 820
AIN#1 R63 820

DOVAL# R52 820
FILVAL# R51 820
SCANCLK2 R183 1.5K
SSHIFTEN R477 1.5K
SINTVAL R187 1.5K
SCANCLK1 R191 1.5K

VCORE
R22 75
FERR
VCC3
R6 510
ATHLON_FERR# → ATHLON_FERR# 17
Q5 2N3904

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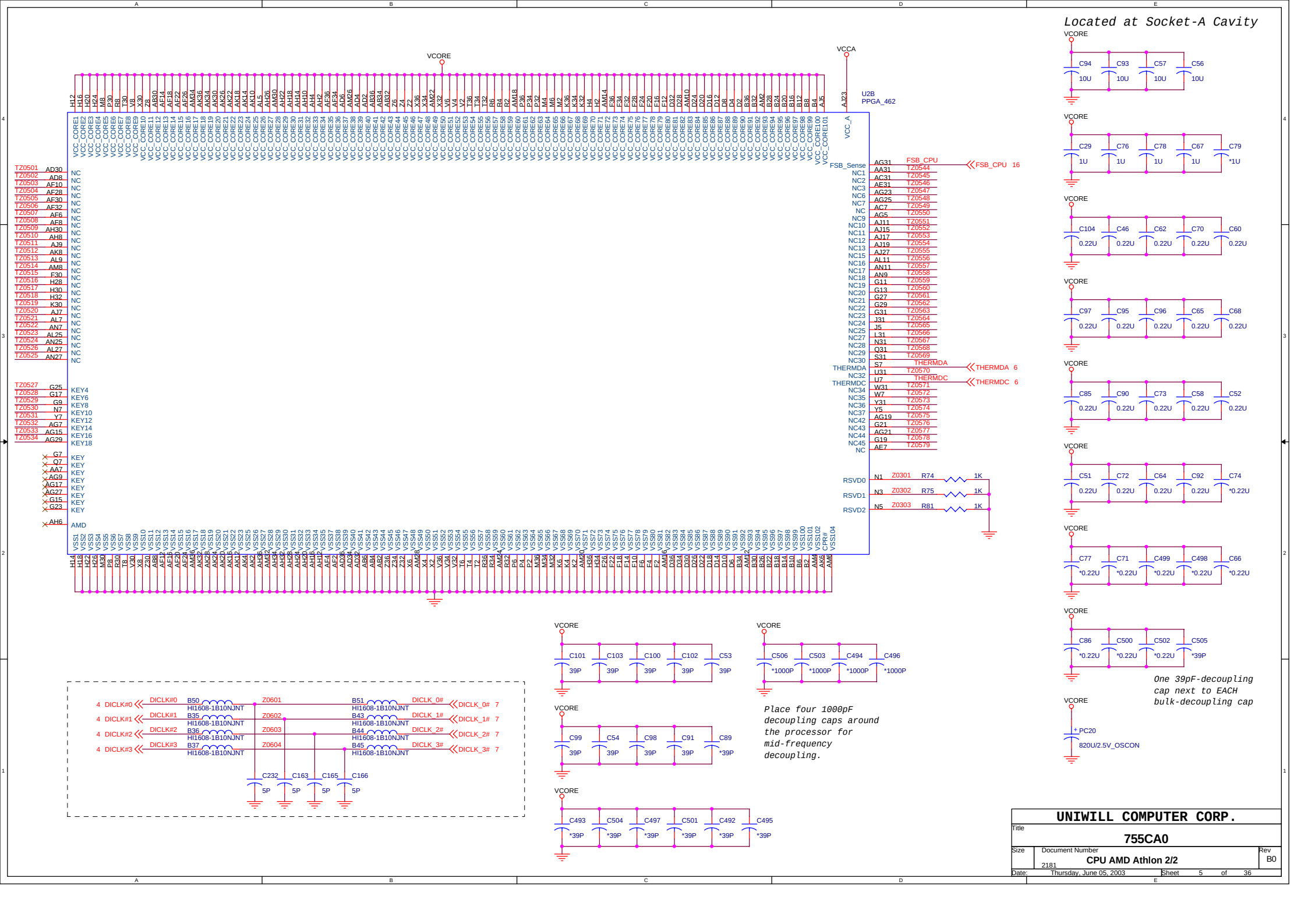

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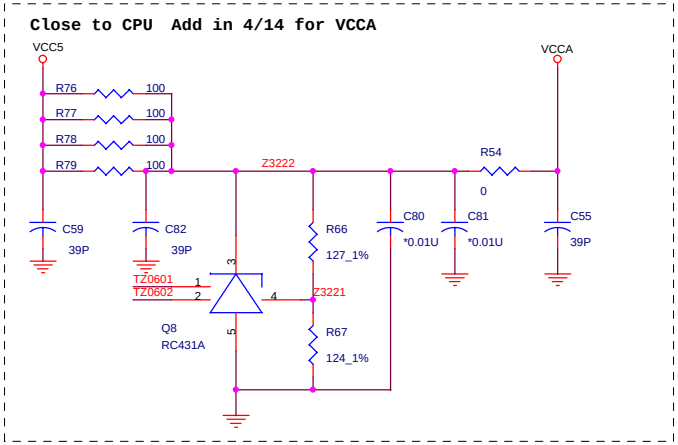
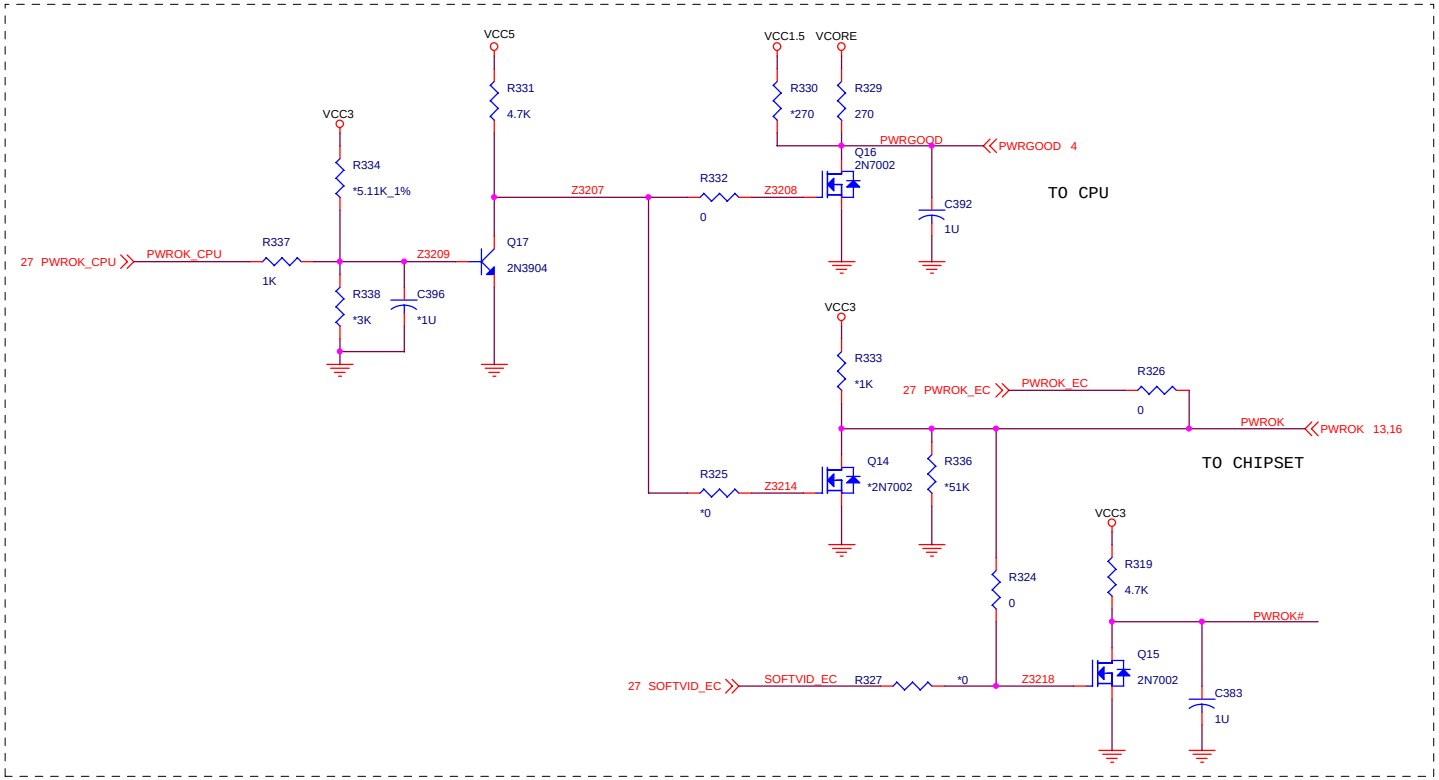
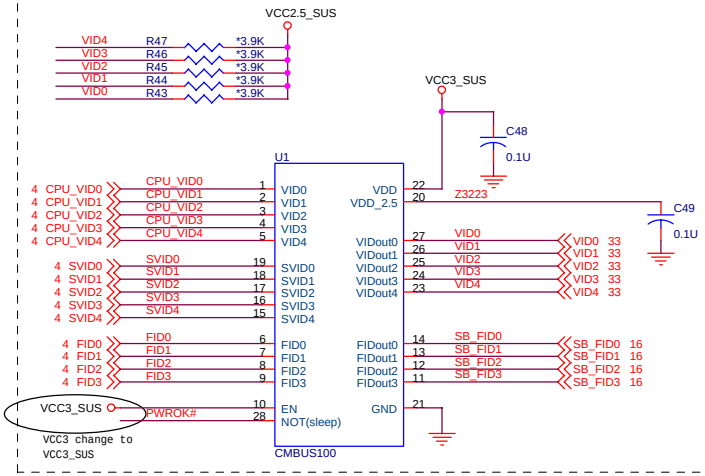
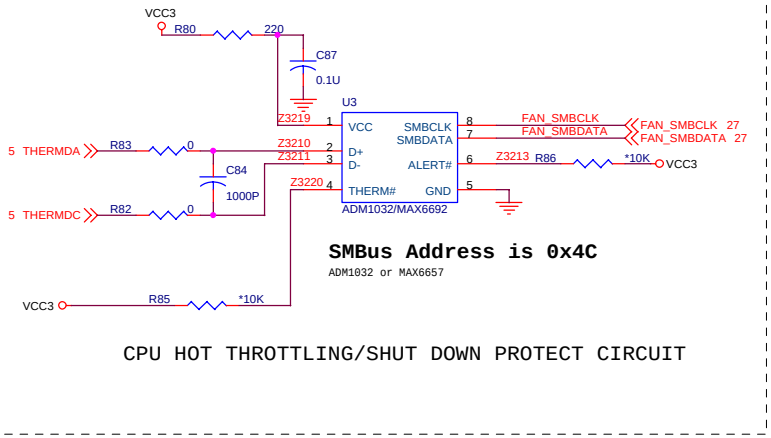






	VID4	VID3	VID2	VID1	VID0
1.75V	0	0	1	0	1
1.70V	0	0	1	1	0
1.65V	0	0	1	1	1
1.60V	0	1	0	0	0
1.55V	0	1	0	0	1
1.50V	0	1	0	1	0
1.45V	0	1	0	1	1
1.40V	0	1	1	0	0
1.35V	0	1	1	0	1

Model	133	Voltage	100	Voltage
2000+	12.5	1667MHZ	1.65V	1250	1.4V
2200+	13.5	1800MHZ	1.65V	1350	1.4V
2400+	15	2000MHZ	1.65V	1500	1.4V
2600+	16	2133MHZ	1.65V	1600	1.4V



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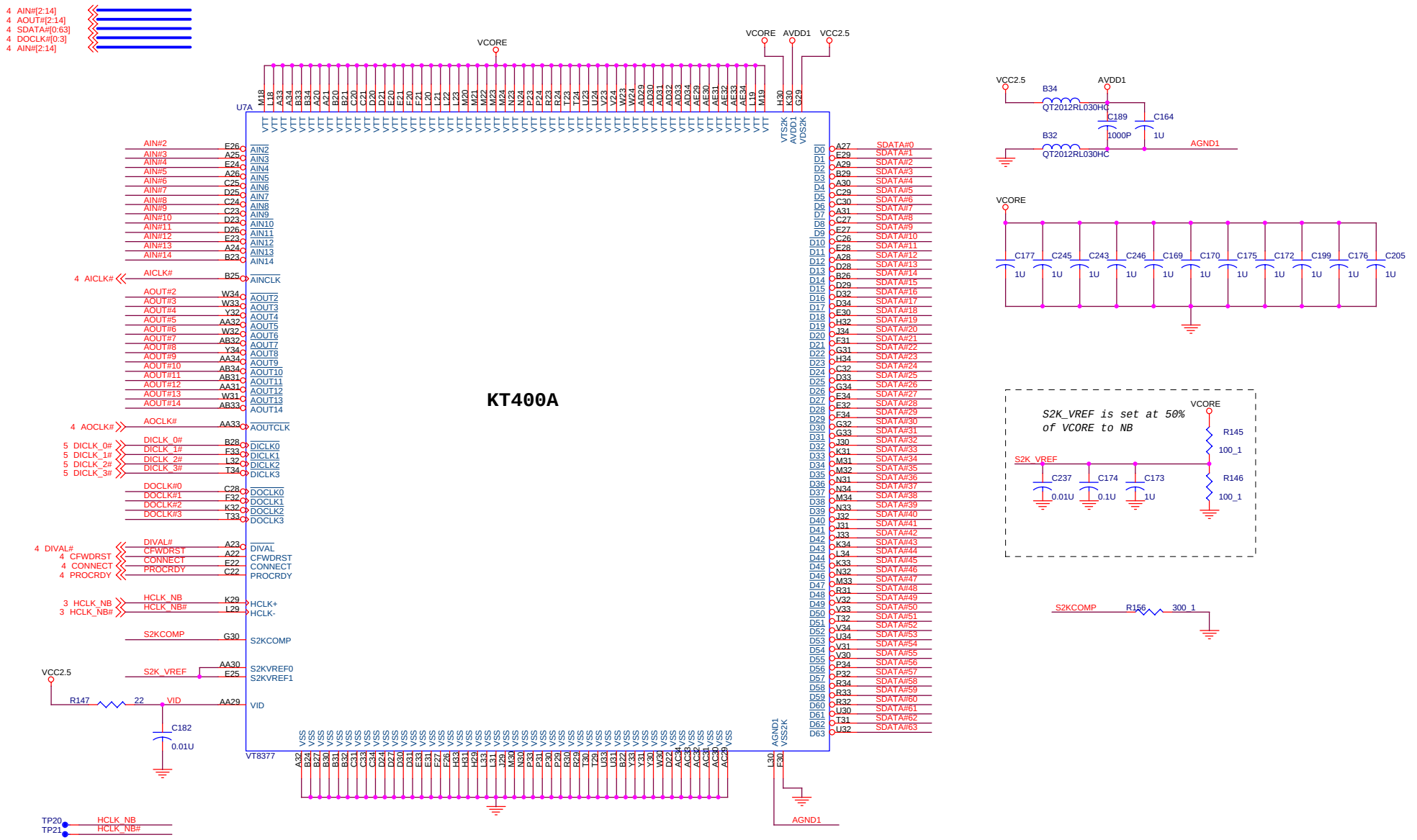

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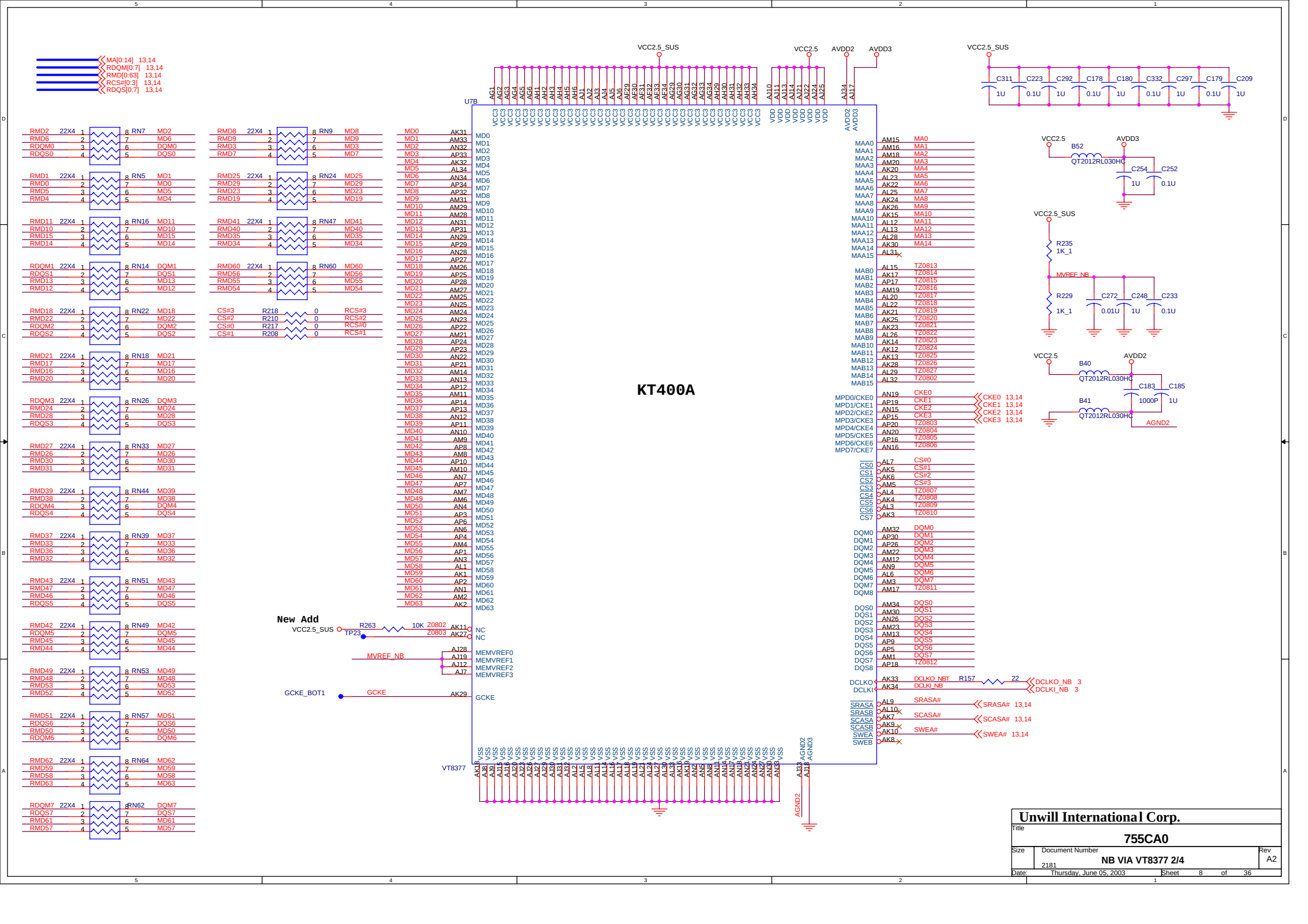

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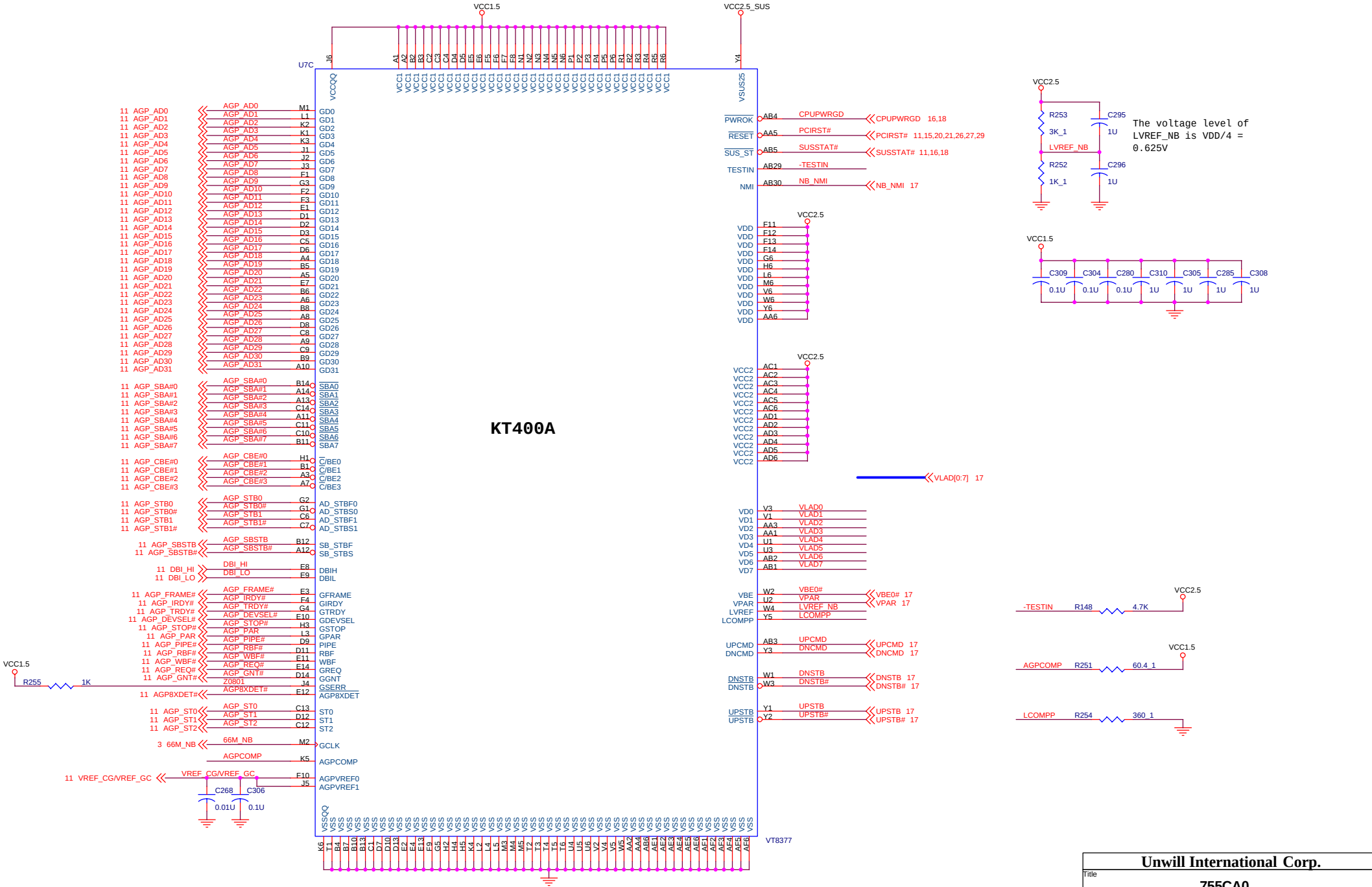

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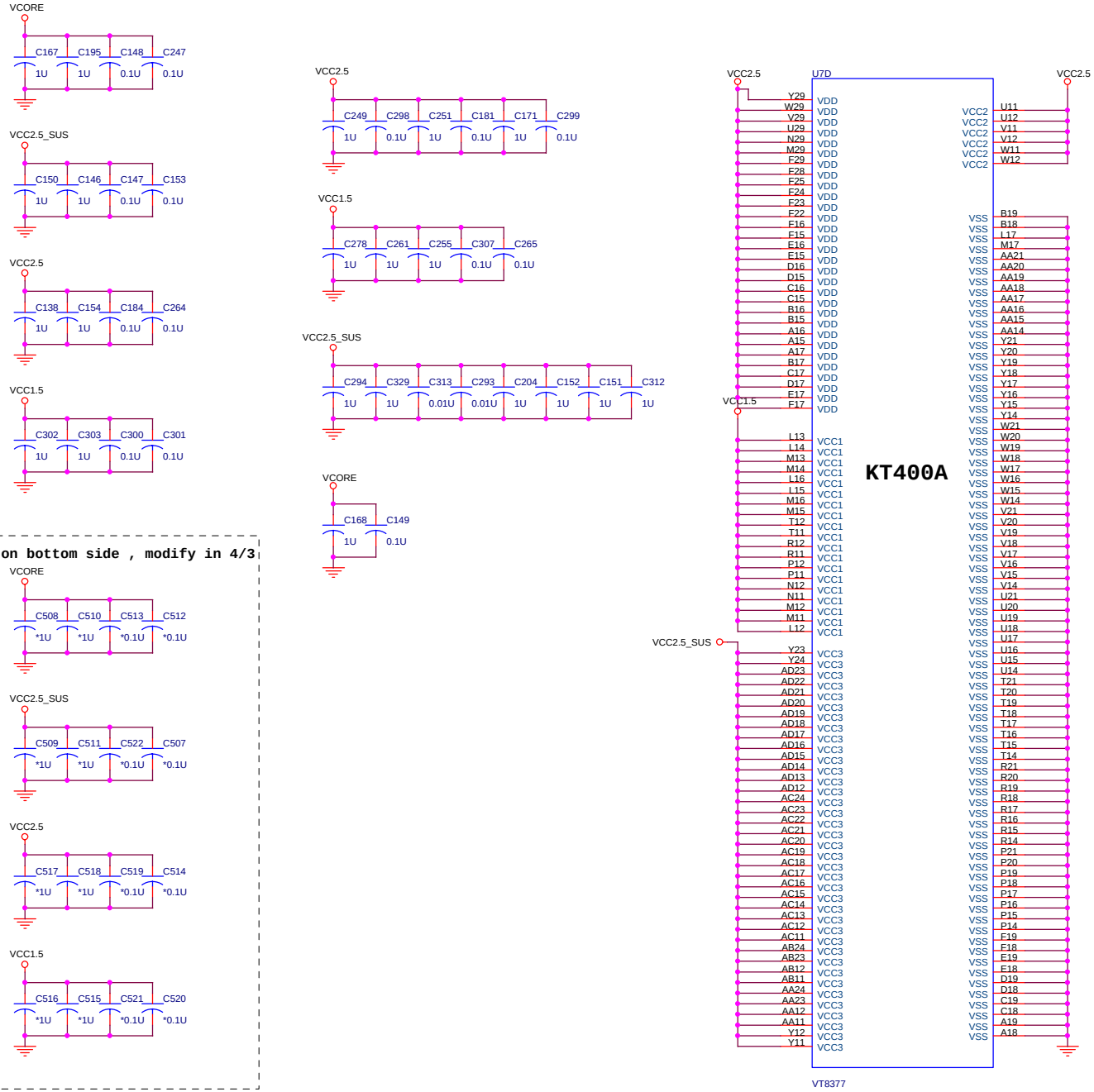

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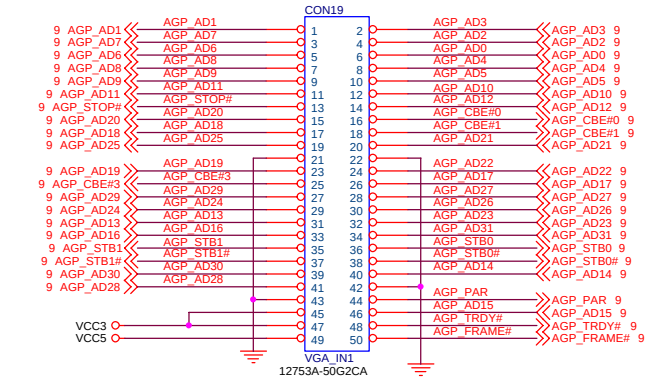

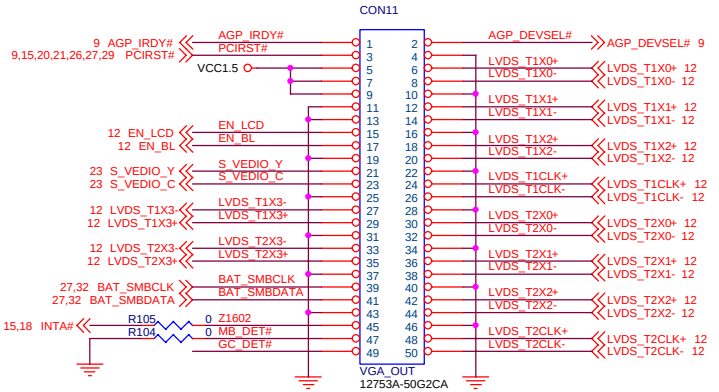

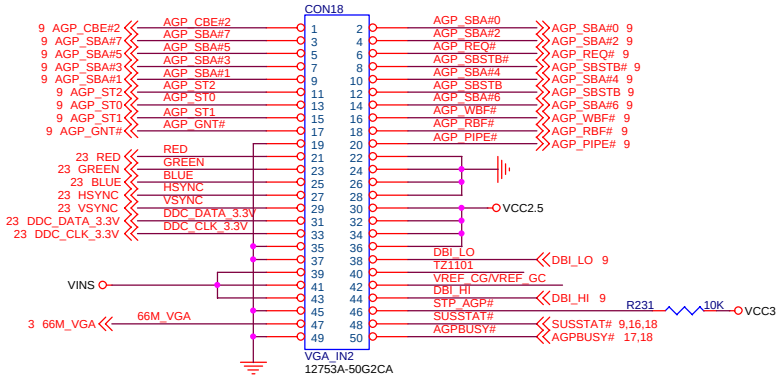

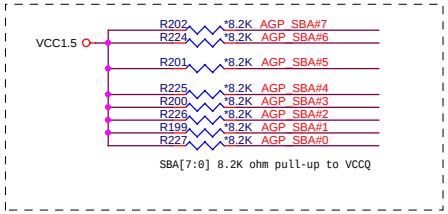

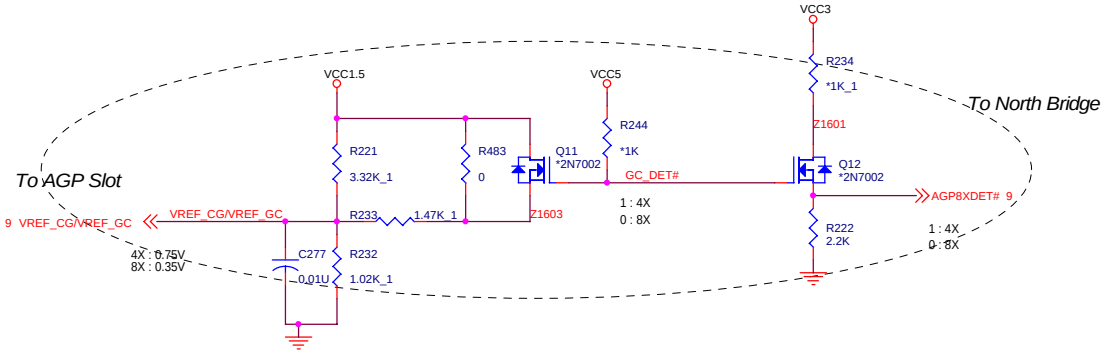

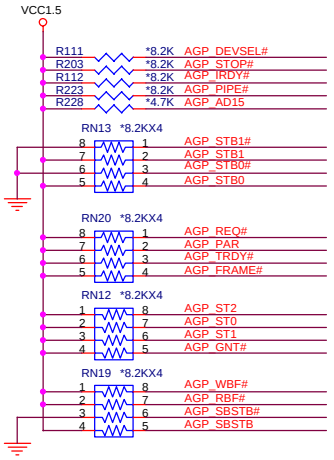

Pull High/Down Requirement for VT8377 Series

Unwill International Corp.		
Title: **755CA0**		
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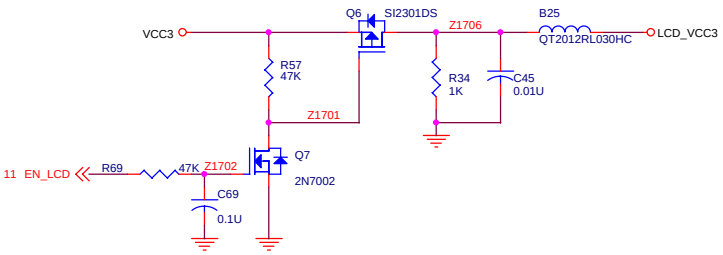
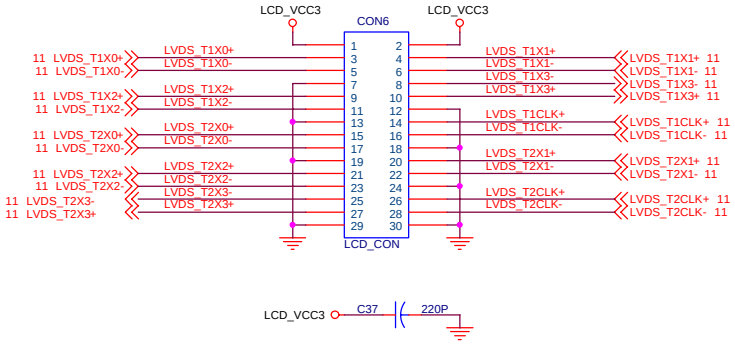
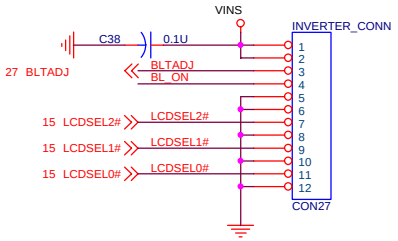
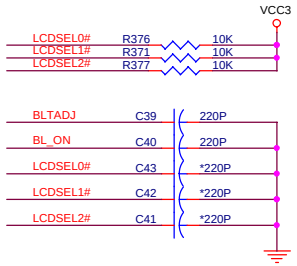
LVDS I/F

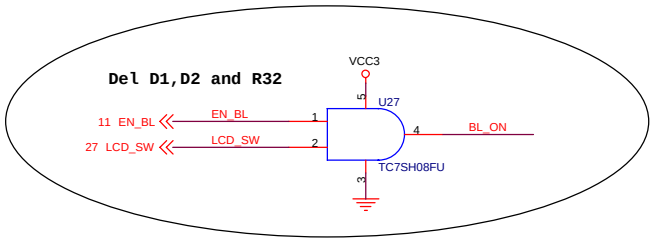




Back Light I/F & MIC







LCD TYPE	18Bit XGA	18Bit SXGA	18Bit SXGA+	Reserve	24Bit XGA	24Bit SXGA	24Bit SXGA+	Reserve
LCDSEL2	1	1	1		0	0	0	
LCDSEL1	1	1	0		1	1	0	
LCDSEL0	1	0	0		1	0	0	

Unwill International Corp.		
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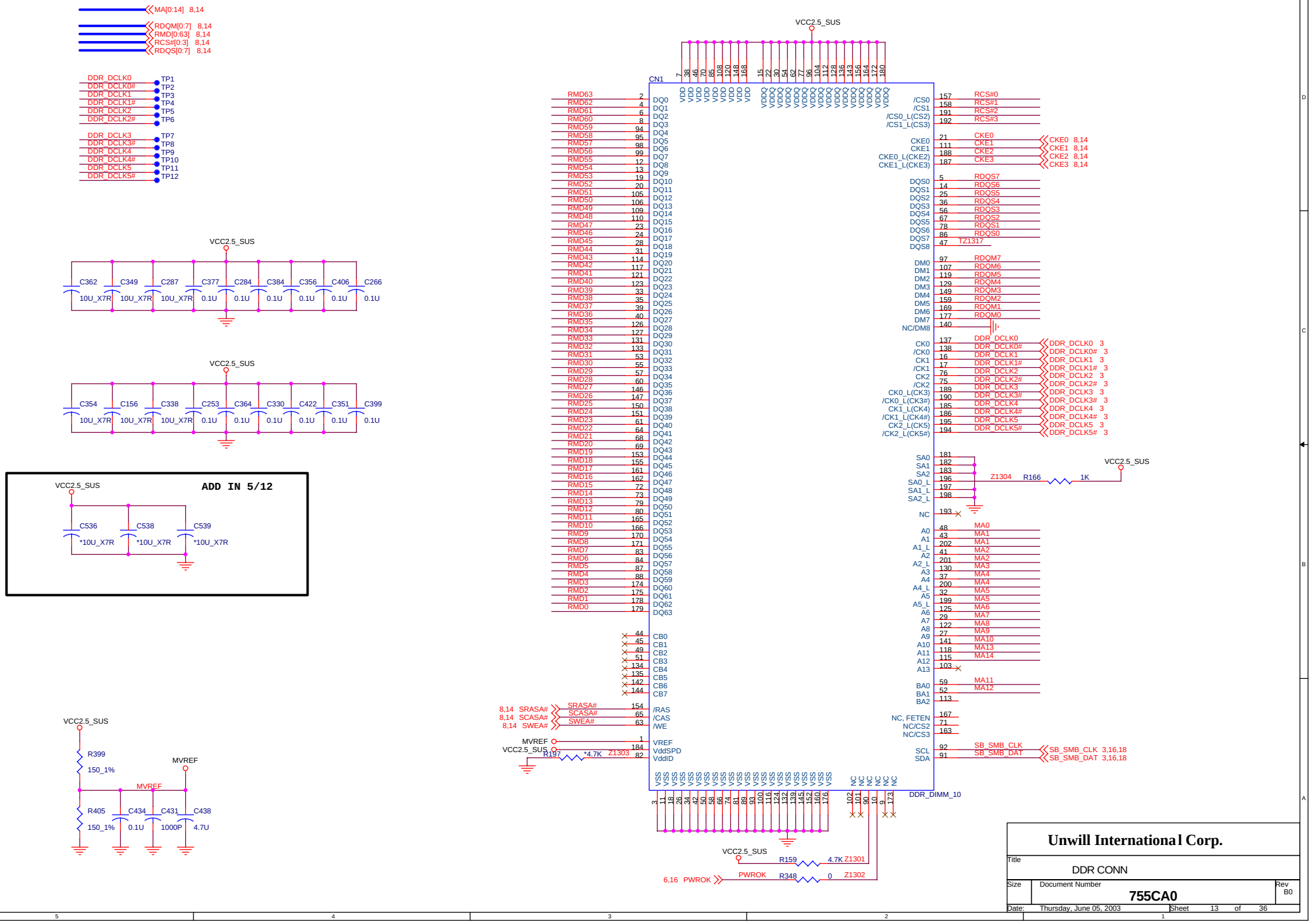
MA[0:14] 8,14
RDQM[0:7] 8,14
RMD[0:63] 8,14
RCS#[0:3] 8,14
RDQS[0:7] 8,14
DDR_DCLK0
DDR_DCLK0#
DDR_DCLK1
DDR_DCLK1#
DDR_DCLK2
DDR_DCLK2#
DDR_DCLK3
DDR_DCLK3#
DDR_DCLK4
DDR_DCLK4#
DDR_DCLK5
DDR_DCLK5#
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
VCC2.5_SUS
C362 C349 C287 C377 C284 C384 C356 C406 C266
10U_X7R 10U_X7R 10U_X7R 0.1U 0.1U 0.1U 0.1U 0.1U 0.1U
C354 C156 C338 C253 C364 C330 C422 C351 C399
10U_X7R 10U_X7R 10U_X7R 0.1U 0.1U 0.1U 0.1U 0.1U 0.1U
ADD IN 5/12
C536 C538 C539
*10U_X7R *10U_X7R *10U_X7R
R399
150_1%
MVREF
R405
C434
C431
C438
150_1%
0.1U
1000P
4.7U
CN1
DDR_DIMM_10
RMD63 RMD62 RMD61 RMD60 RMD59 RMD58 RMD57 RMD56 RMD55 RMD54 RMD53 RMD52 RMD51 RMD50 RMD49 RMD48 RMD47 RMD46 RMD45 RMD44 RMD43 RMD42 RMD41 RMD40 RMD39 RMD38 RMD37 RMD36 RMD35 RMD34 RMD33 RMD32 RMD31 RMD30 RMD29 RMD28 RMD27 RMD26 RMD25 RMD24 RMD23 RMD22 RMD21 RMD20 RMD19 RMD18 RMD17 RMD16 RMD15 RMD14 RMD13 RMD12 RMD11 RMD10 RMD9 RMD8 RMD7 RMD6 RMD5 RMD4 RMD3 RMD2 RMD1 RMD0
CB0 CB1 CB2 CB3 CB4 CB5 CB6 CB7
SRASA# SCASA# SWEA#
/RAS /CAS /WE
MVREF
VddSPD
VddID
R197 *4.7K Z1303
/CS0 /CS1 /CS0_L(CS2) /CS1_L(CS3)
RCS#0 RCS#1 RCS#2 RCS#3
CKE0 CKE1 CKE0_L(CKE2) CKE1_L(CKE3)
CKE0 CKE1 CKE2 CKE3
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7 DQS8
RDQS7 RDQS6 RDQS5 RDQS4 RDQS3 RDQS2 RDQS1 RDQS0
TZ1317
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7 NC/DM8
RDQM7 RDQM6 RDQM5 RDQM4 RDQM3 RDQM2 RDQM1 RDQM0
CK0 /CK0 CK1 /CK1 CK2 /CK2 CK0_L(CK3) /CK0_L(CK3#) CK1_L(CK4) /CK1_L(CK4#) CK2_L(CK5) /CK2_L(CK5#)
DDR_DCLK0 DDR_DCLK0# DDR_DCLK1 DDR_DCLK1# DDR_DCLK2 DDR_DCLK2# DDR_DCLK3 DDR_DCLK3# DDR_DCLK4 DDR_DCLK4# DDR_DCLK5 DDR_DCLK5#
SA0 SA1 SA2 SA0_L SA1_L SA2_L NC
Z1304 R166 1K
MA0 MA1 MA1 MA2 MA2 MA3 MA4 MA4 MA5 MA5 MA6 MA7 MA8 MA9 MA10 MA13 MA14
A0 A1 A1_L A2 A2_L A3 A4 A4_L A5 A5_L A6 A7 A8 A9 A10 A11 A12 A13
BA0 BA1 BA2
MA11 MA12
NC, FETEN NC/CS2 NC/CS3
SCL SDA
SB_SMB_CLK SB_SMB_DAT
R159 4.7K Z1301
PWROK R348 0 Z1302
6,16 PWROK
Unwill International Corp.
Title
DDR CONN
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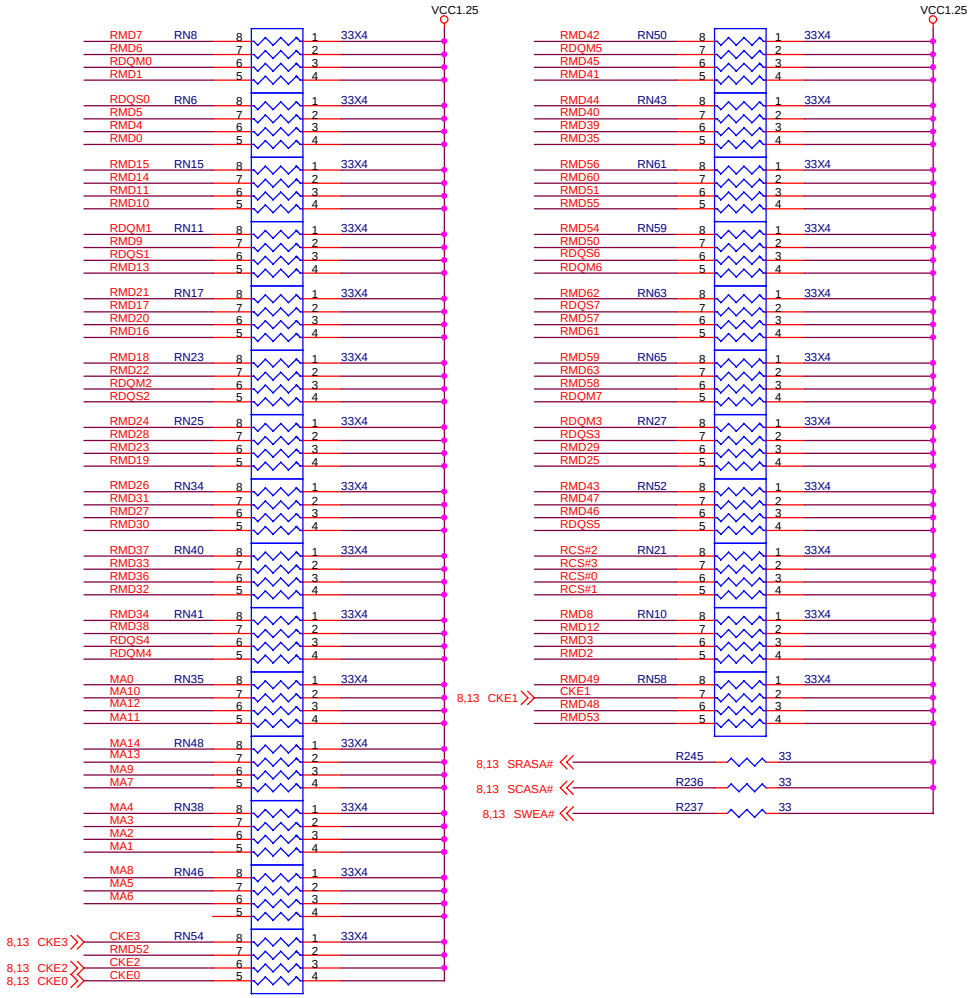
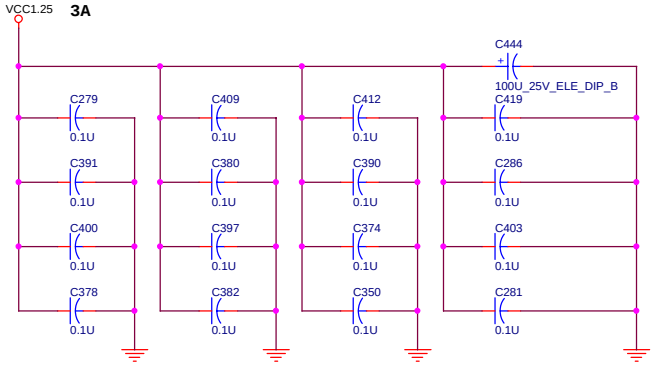
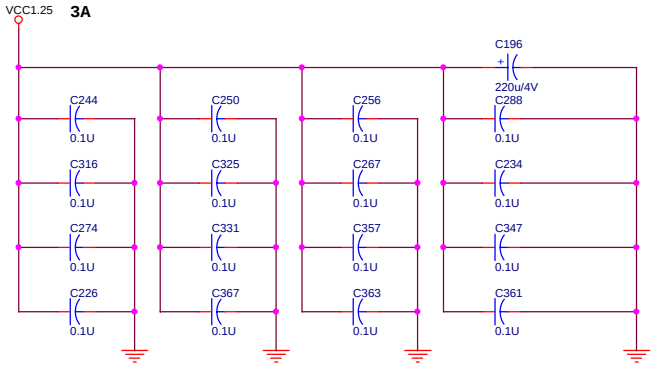
RMD[0:63] 8,13
RDQM[0:7] 8,13
RDQS[0:7] 8,13
MA[0:14] 8,13

RCS#[0:3] 8,13







Unwill International Corp.

Title: DDR PULL UP		
Size	Document Number: **755CA0**	Rev: B0
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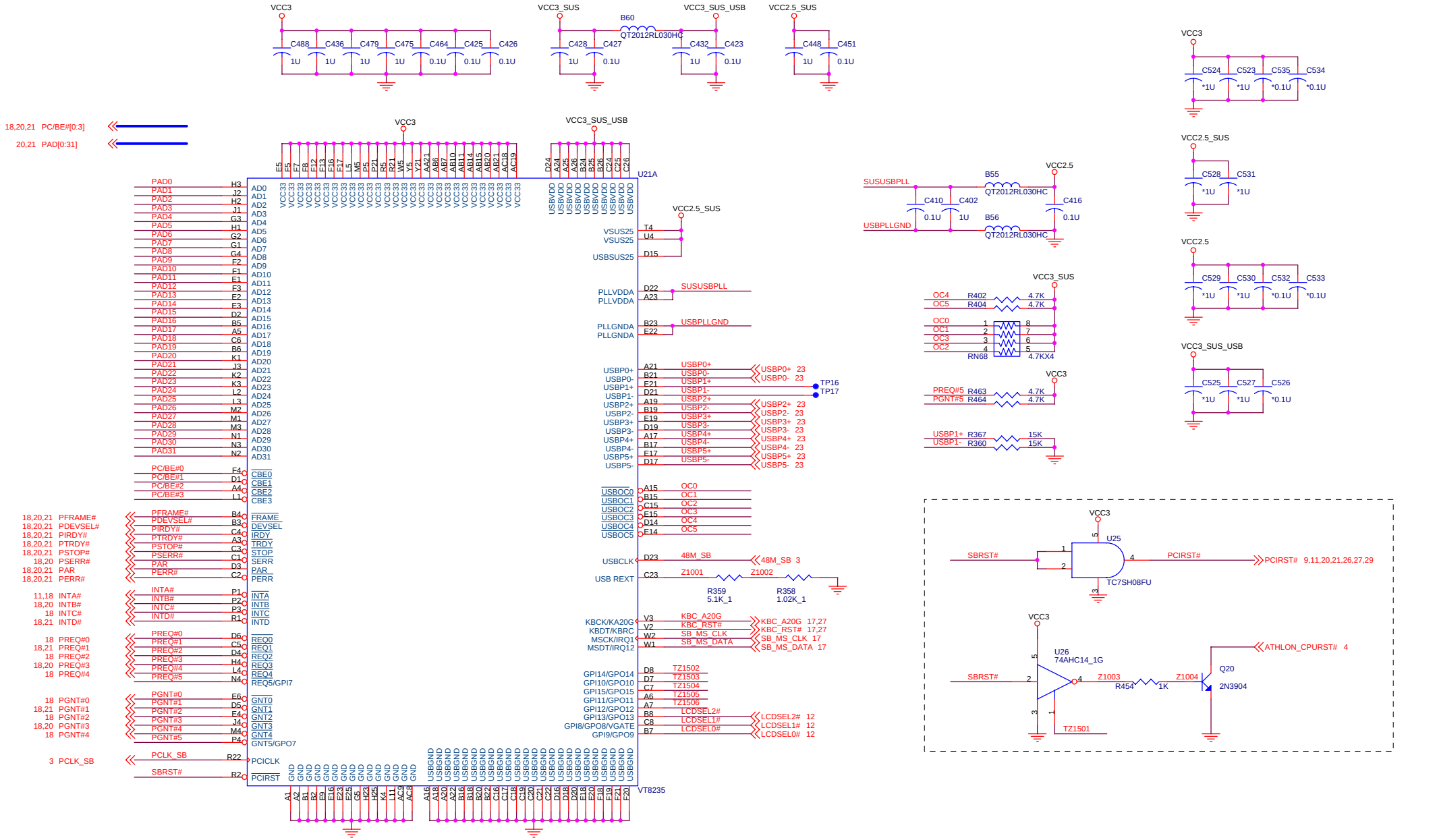

Unwill International Corp.		
Title: 755CA0		
Size	Document Number: SB VIA VT8235 1/3	Rev: B0
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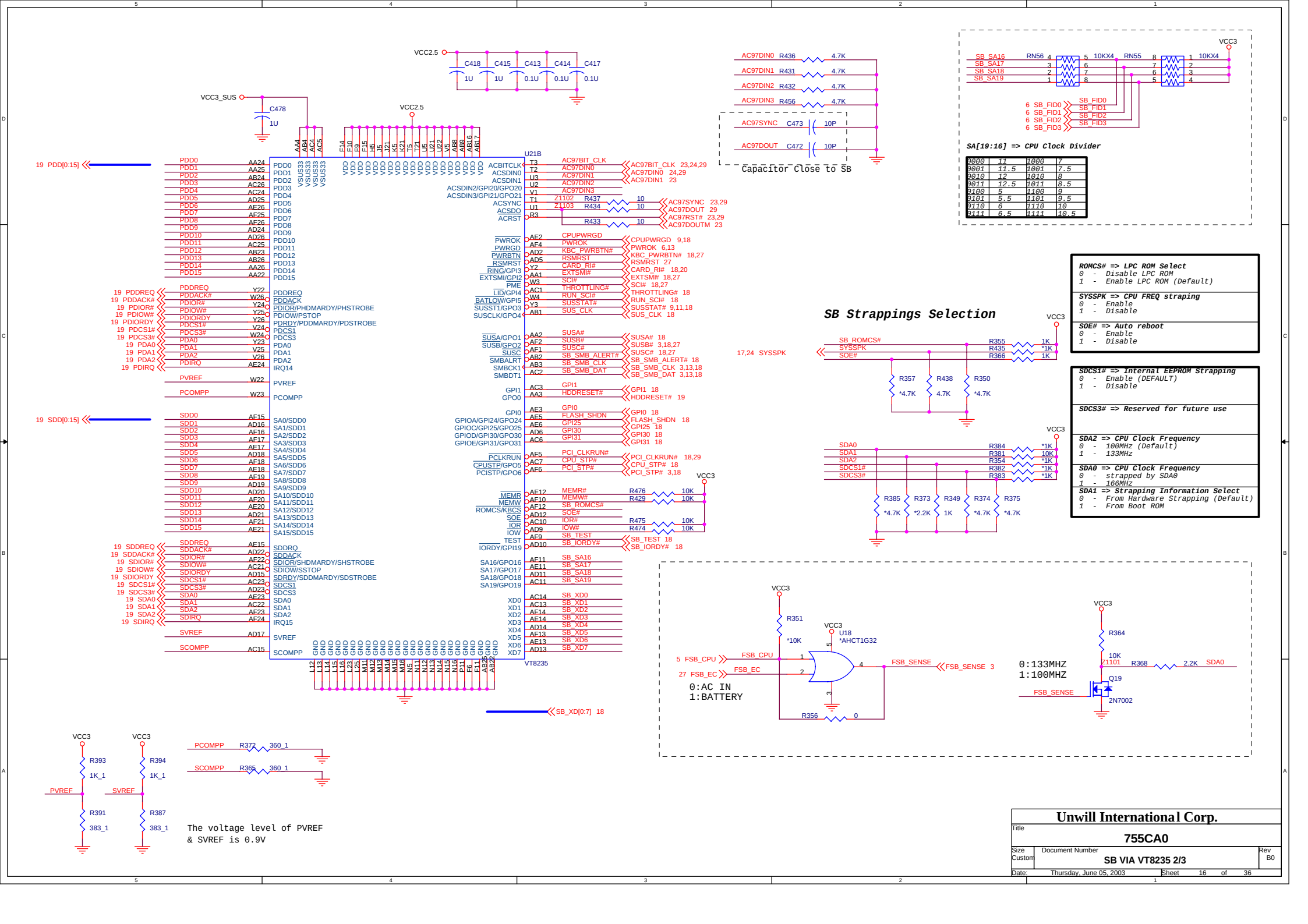

Unwill International Corp.		
Title: 755CA0		
Size: Custom	Document Number: SB VIA VT8235 2/3	Rev: B0
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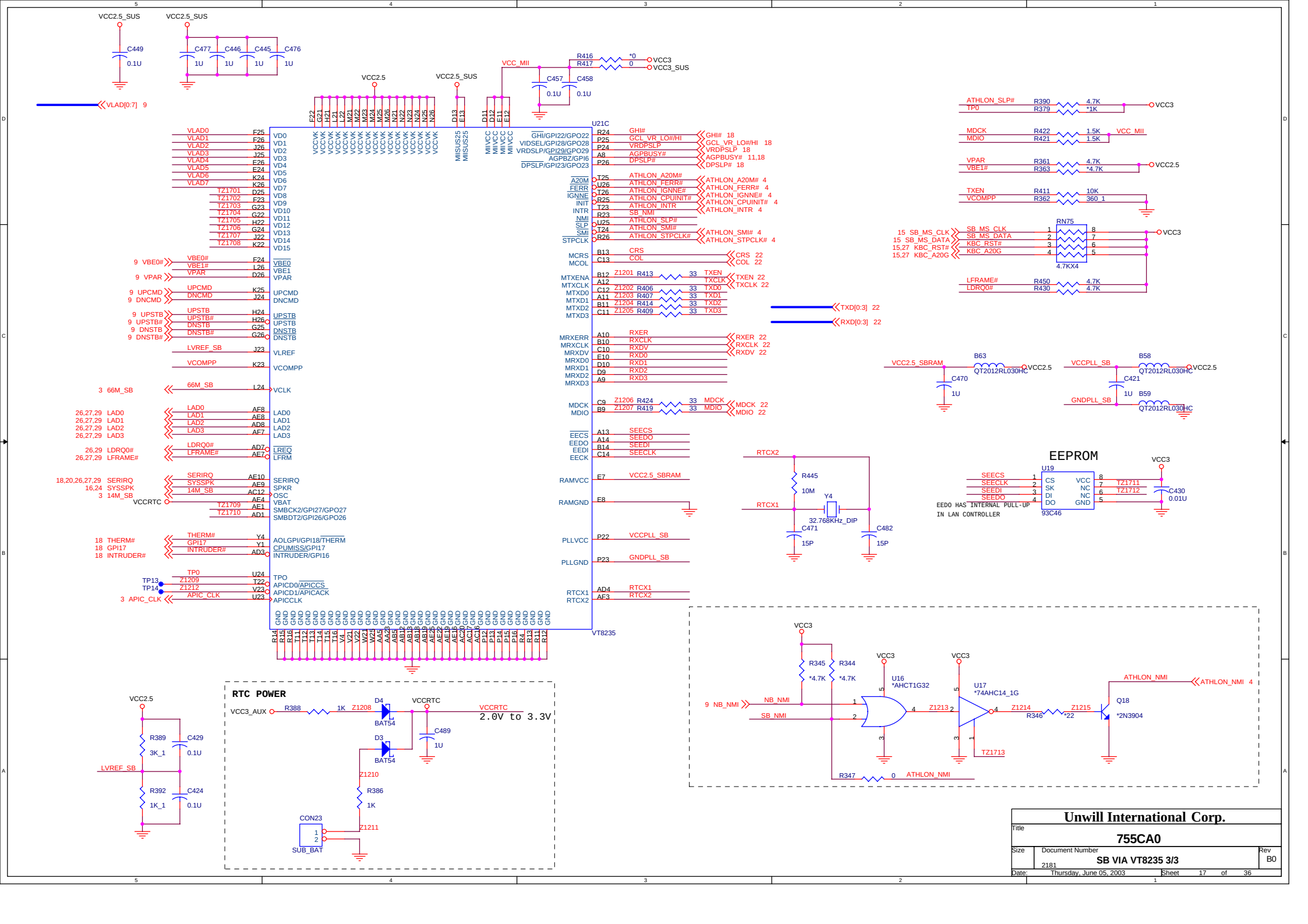
VCC2.5_SUS
C449
0.1U
C477
C446
C445
C476
1U
VLAD[0:7] 9
VCC2.5
VCC2.5_SUS
VCC_MII
R416
R417
*0
0
VCC3
VCC3_SUS
C457
C458
U21C
VT8235
VLAD0
VLAD1
VLAD2
VLAD3
VLAD4
VLAD5
VLAD6
VLAD7
VBE0#
VBE1#
VPAR
UPCMD
DNCMD
UPSTB
UPSTB#
DNSTB
DNSTB#
LVREF_SB
VCOMPP
66M_SB
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LFRAME#
SERIRQ
SYSSPK
14M_SB
VCCRTC
THERM#
GPI17
INTRUDER#
TP0
Z1209
Z1212
APIC_CLK
TXEN
TXCLK
TXD0
TXD1
TXD2
TXD3
RXER
RXCLK
RXDV
RXD0
RXD1
RXD2
RXD3
MDCK
MDIO
SEECS
SEEDO
SEEDI
SEECLK
RAMVCC
RAMGND
PLLVCC
PLLGND
RTCX1
RTCX2
VCCPLL_SB
GNDPLL_SB
TXD[0:3] 22
RXD[0:3] 22
ATHLON_SLP#
MDCK
MDIO
VPAR
VBE1#
TXEN
VCOMPP
LFRAME#
LDRQ0#
R390
R379
R422
R421
R361
R363
R411
R362
R450
R430
4.7K
*1K
1.5K
10K
360_1
RN75
4.7KX4
SB_MS_CLK
SB_MS_DATA
KBC_RST#
KBC_A20G
B63
B58
B59
C470
C421
C430
0.01U
QT2012RL030HC
VCC2.5_SBRAM
VCCPLL_SB
GNDPLL_SB
EEPROM
U19
93C46
EEDO HAS INTERNAL PULL-UP
IN LAN CONTROLLER
RTCX2
RTCX1
R445
10M
Y4
32.768KHz_DIP
C471
C482
15P
RTC POWER
VCC3_AUX
R388
1K
D4
D3
BAT54
C489
1U
VCCRTC
2.0V to 3.3V
Z1208
Z1210
Z1211
R386
CON23
SUB_BAT
R389
3K_1
C429
R392
1K_1
C424
0.1U
U16
*AHCT1G32
U17
*74AHC14_1G
R345
R344
*4.7K
NB_NMI
SB_NMI
R347
ATHLON_NMI
Z1213
Z1214
Z1215
R346
*22
Q18
*2N3904
TZ1713
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Title
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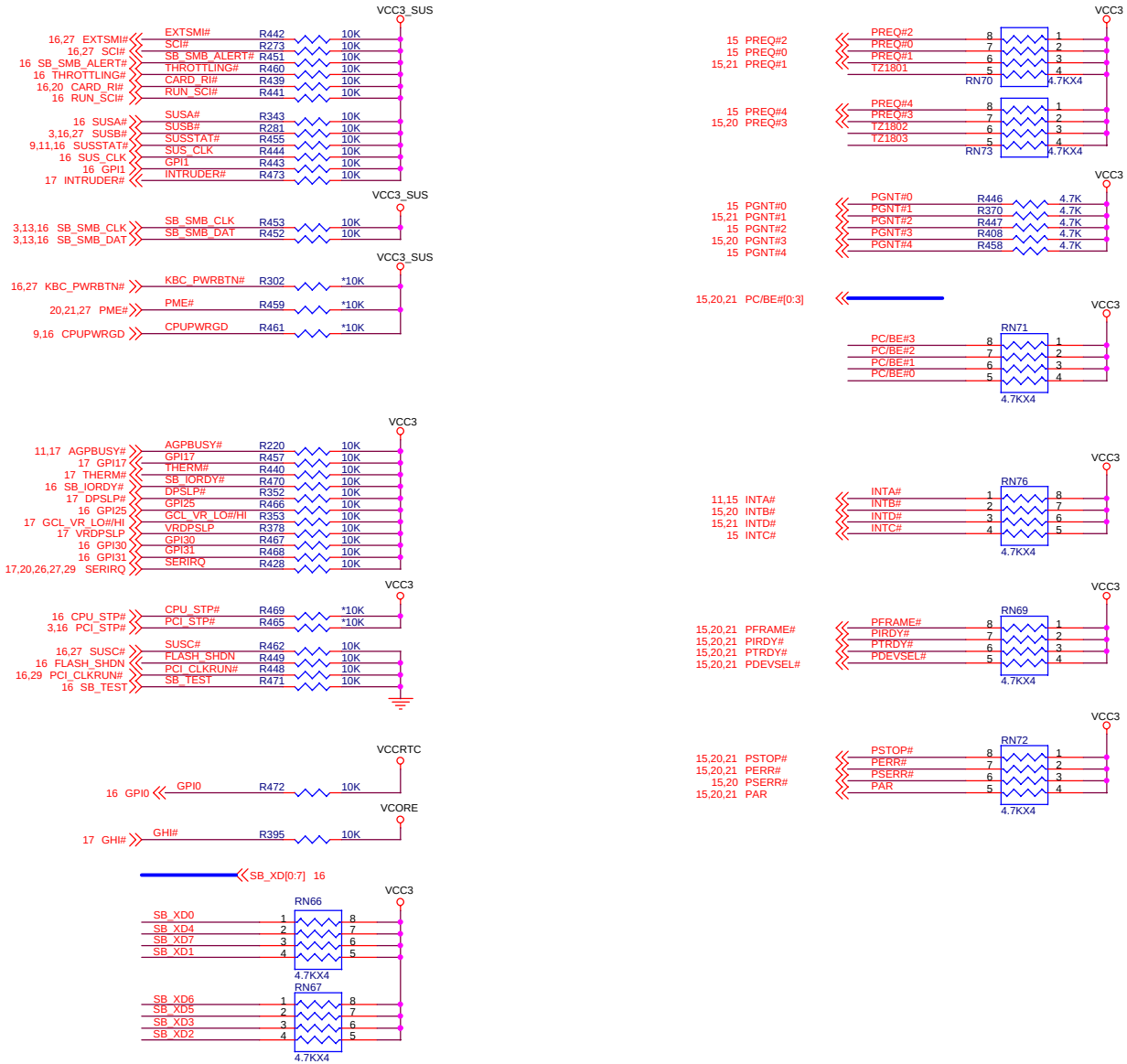

Unwill International Corp.		
Title: 755CA0		
Size	Document Number: 2181 SYSTEM PULL UP / DOWN	Rev: B0
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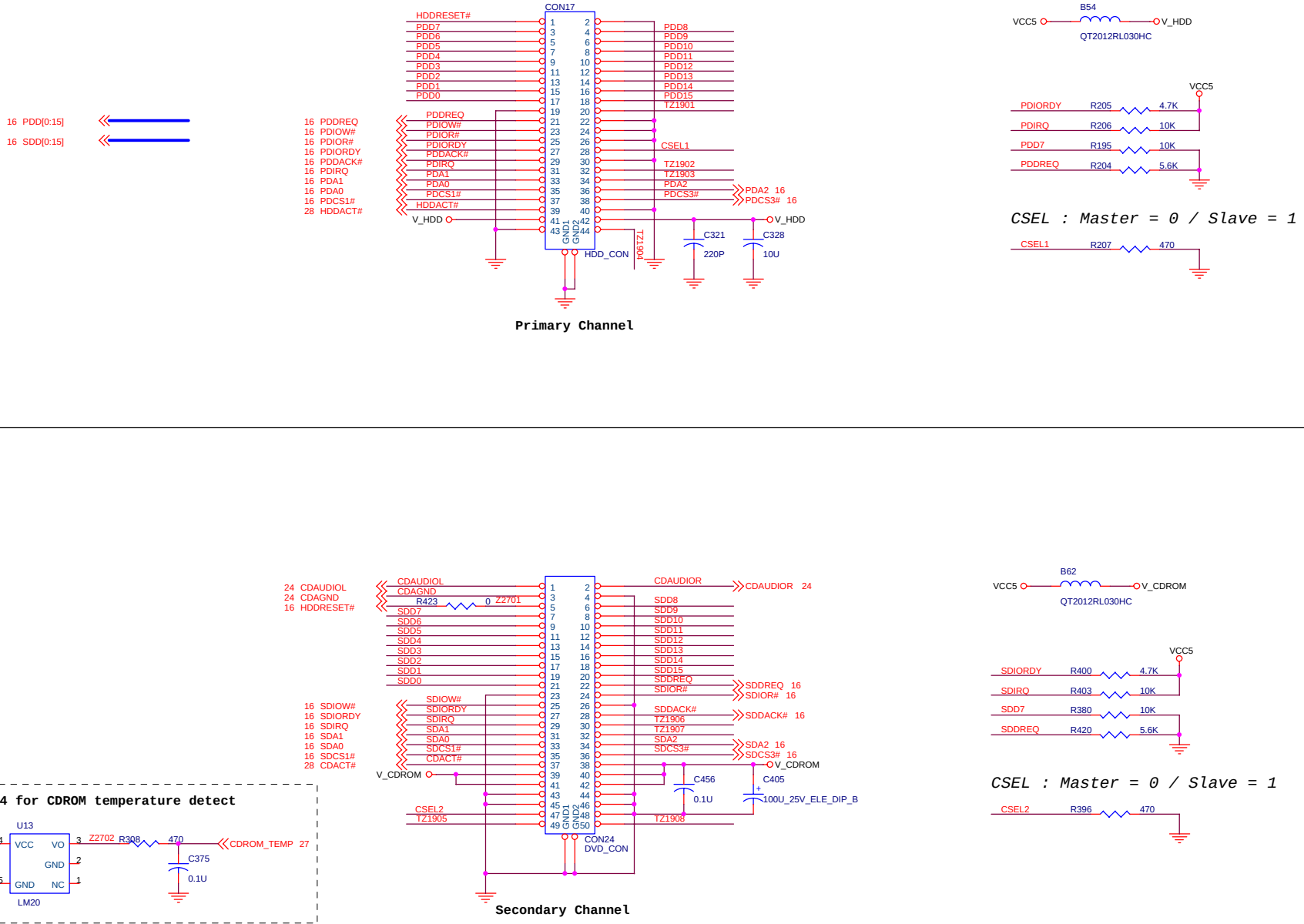

Uniwill International Corp.		
Title	755CA0	
Size	Document Number: 2181 HDD & CDROM	Rev: B0
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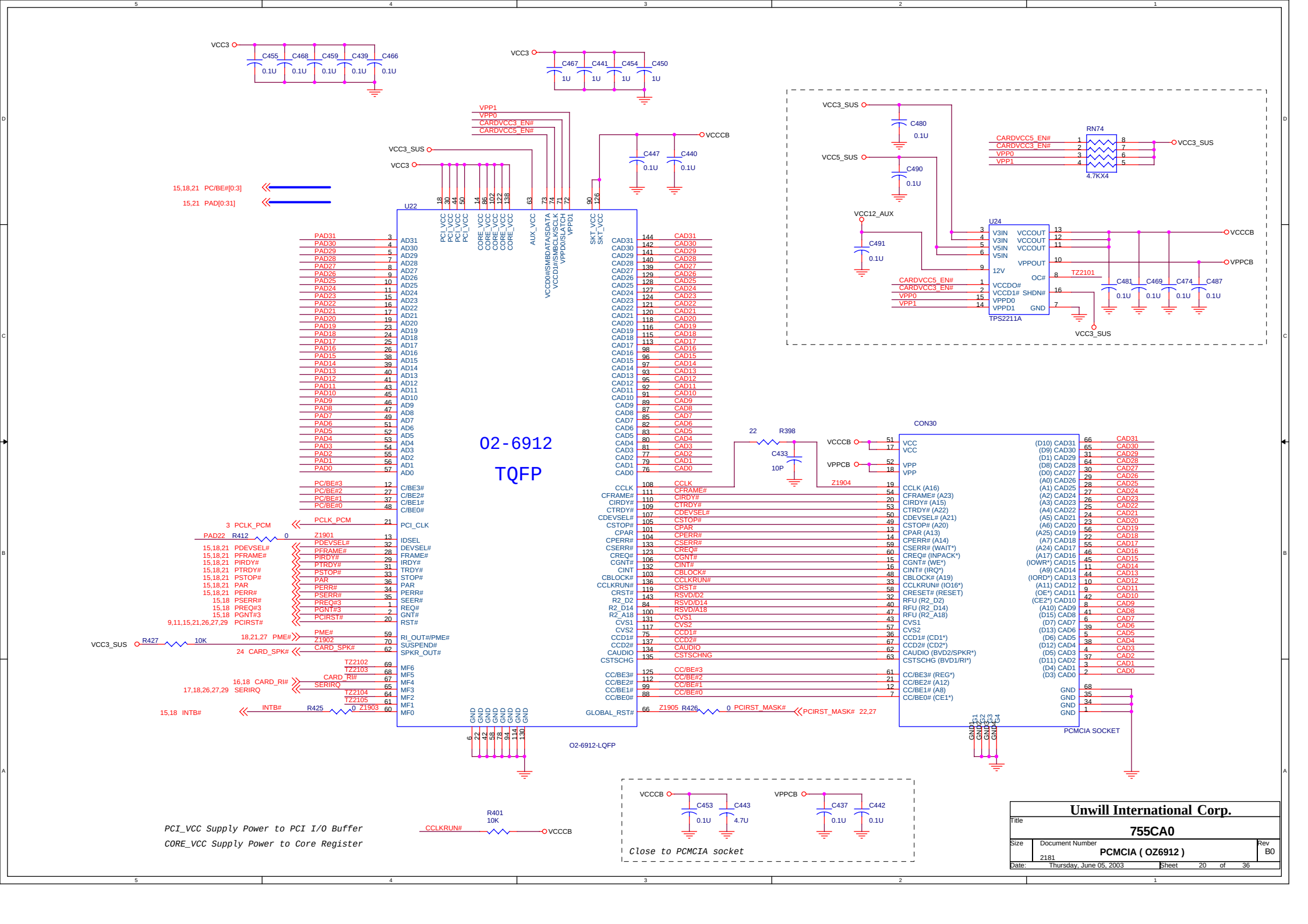

Unwill International Corp.		
Title	755CA0	
Size	Document Number: PCMCIA (OZ6912) 2181	Rev: B0
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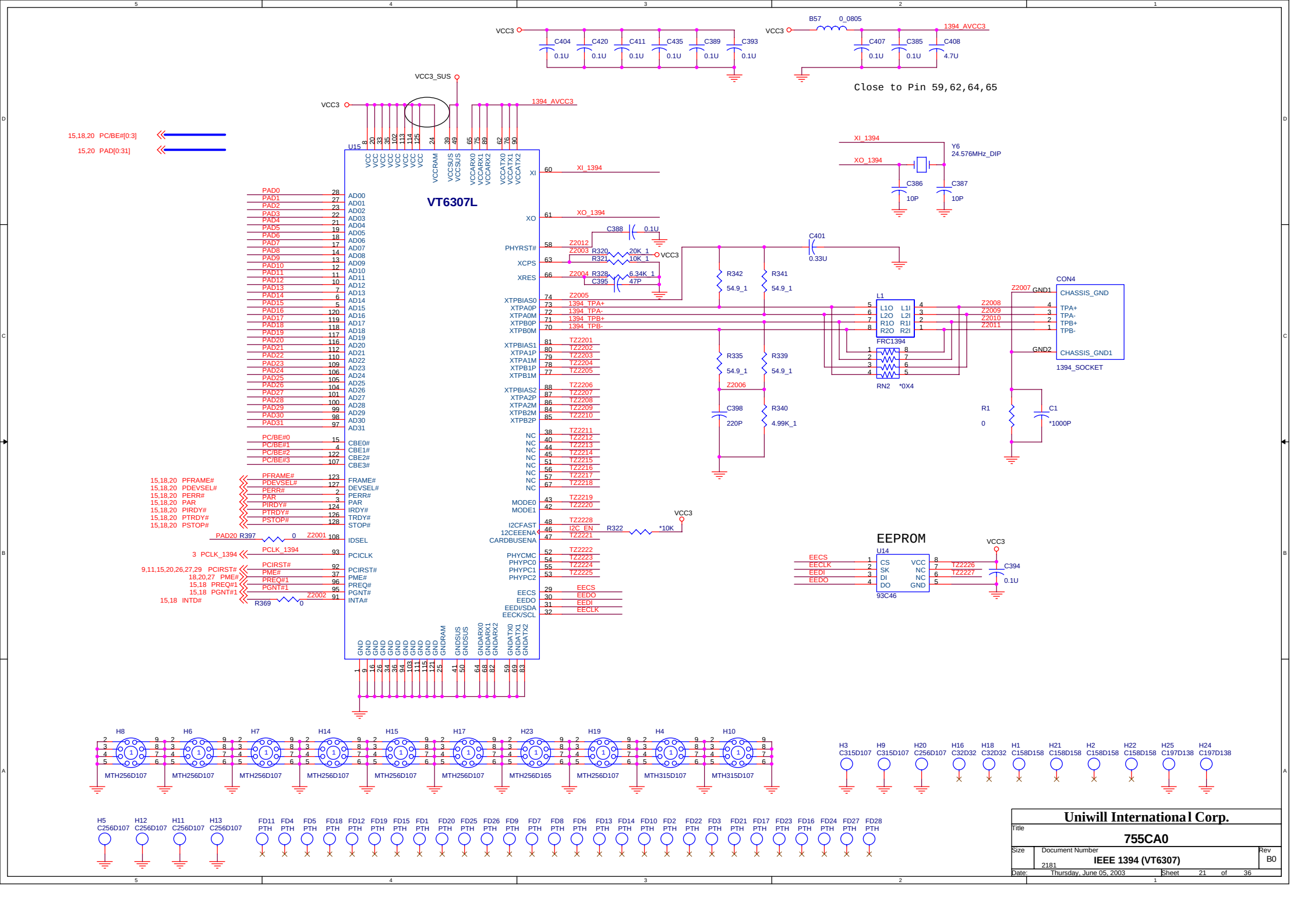
VT6307L
U15
VCC3
VCC3_SUS
1394_AVCC3
B57 0_0805
C404 C420 C411 C435 C389 C393 0.1U
C407 C385 C408 0.1U 0.1U 4.7U
Close to Pin 59,62,64,65
15,18,20 PC/BE#[0:3]
15,20 PAD[0:31]
XI_1394
XO_1394
Y6 24.576MHz_DIP
C386 10P
C387 10P
C388 0.1U
C401 0.33U
PHYRST#
XCPS
XRES
R320 20K_1
R321 10K_1
R328 6.34K_1
C395 47P
R342 54.9_1
R341 54.9_1
R335 54.9_1
R339 54.9_1
C398 220P
R340 4.99K_1
L1
FRC1394
RN2 *0X4
CON4
1394_SOCKET
CHASSIS_GND
CHASSIS_GND1
GND1
GND2
TPA+
TPA-
TPB+
TPB-
R1 0
C1 *1000P
R322 *10K
EEPROM
U14
93C46
EECS
EECLK
EEDI
EEDO
C394 0.1U
PCLK_1394
PCIRST#
PME#
PREQ#1
PGNT#1
INTD#
R369 0
R397 0
MTH256D107
MTH315D107
MTH256D165
C315D107
C256D107
C32D32
C158D158
C197D138
C197D138
PTH
Uniwill International Corp.
Title
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Size
Document Number
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2181
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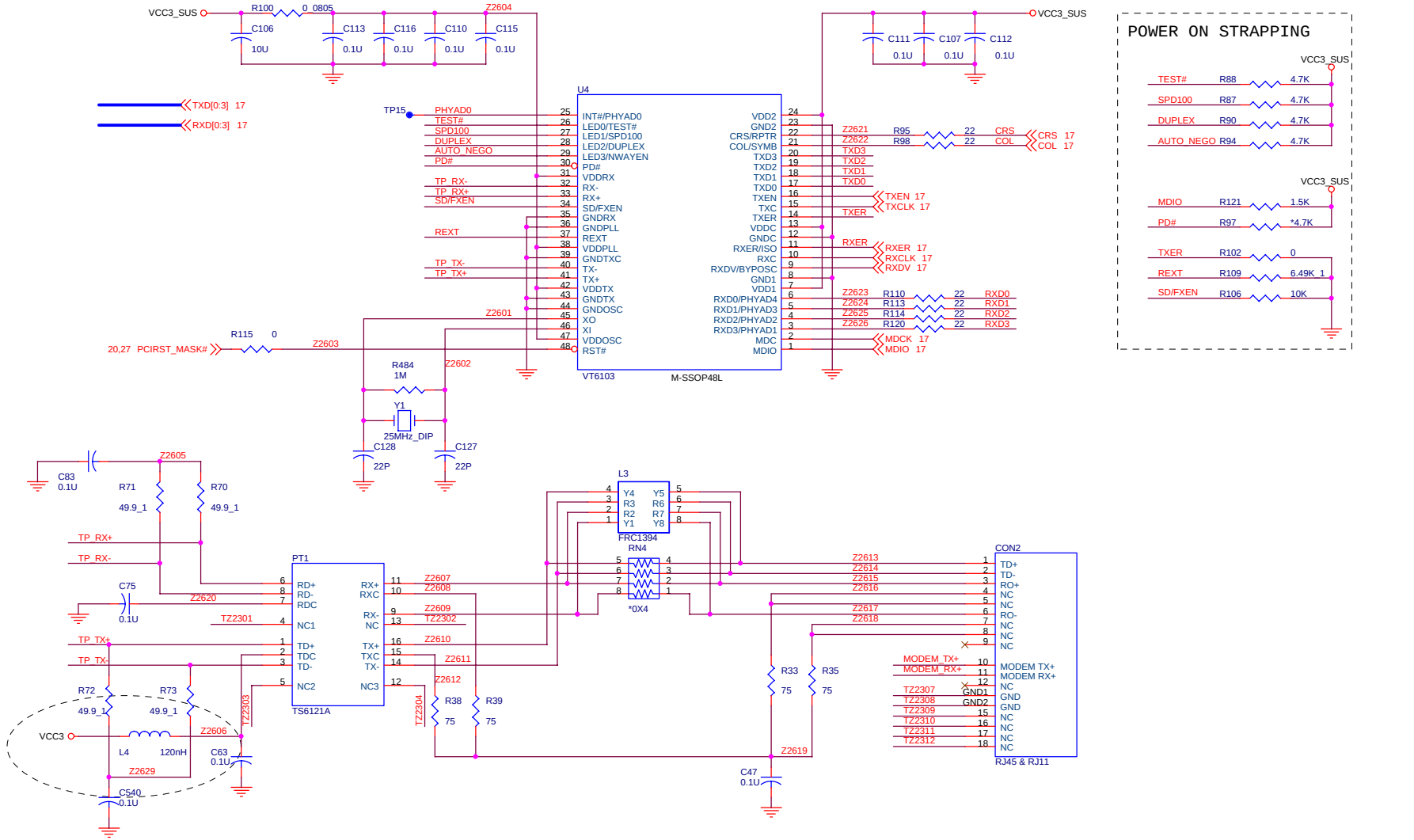
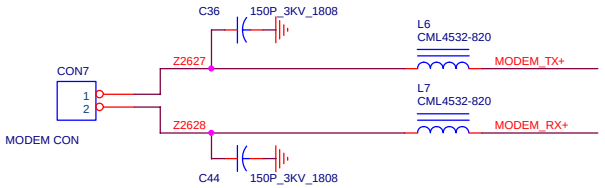


MODEM



2.5mm should avoid away from other trace, components!

Uniwill International Corp.		
Title: 755CA0		
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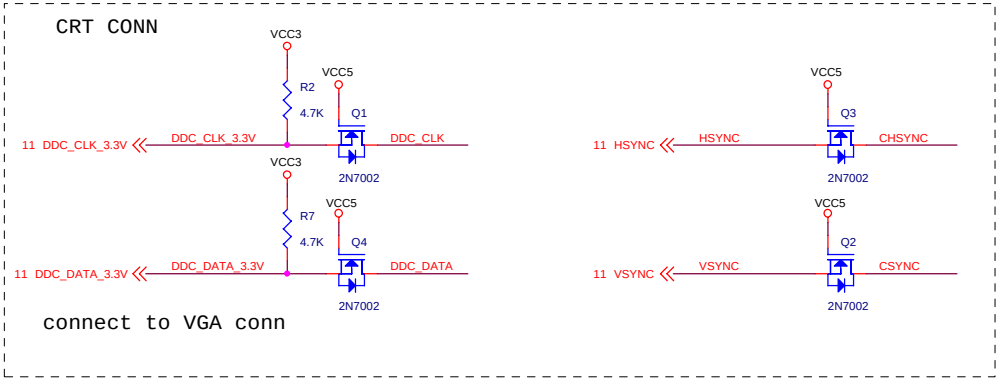
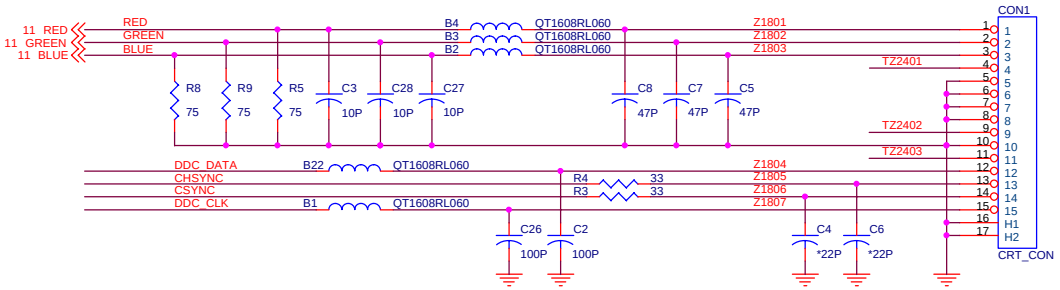
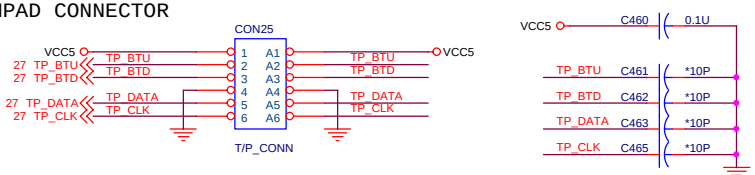
CRT CONN

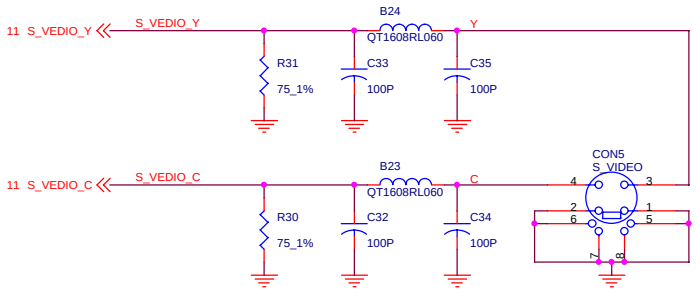




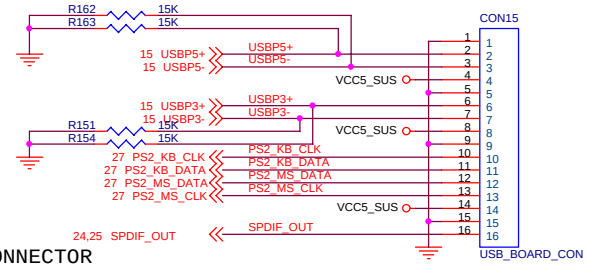
TOCHPAD CONNECTOR



S-VIDEO

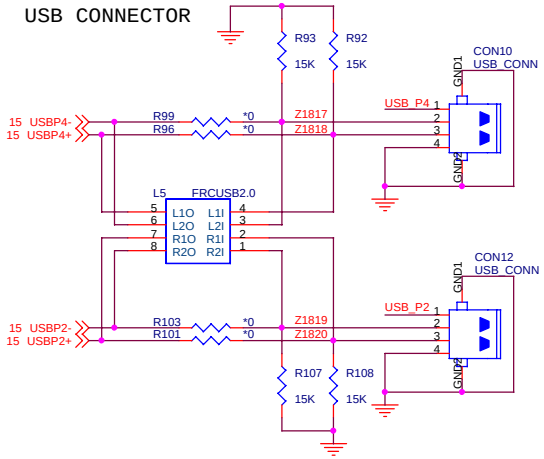


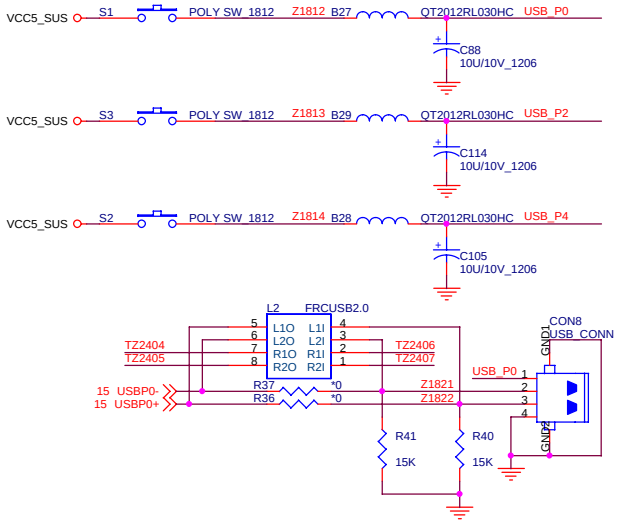
CARD READER CONNECTOR



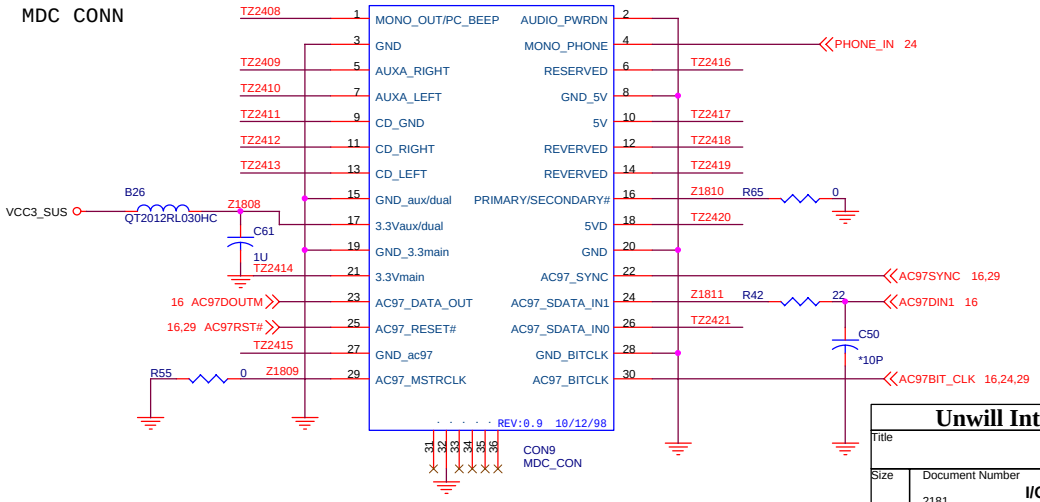
Del all in 3/4

USB CONNECTOR





MDC CONN



Unwill International Corp.		
Title: 755CA0		
Size	Document Number: 2181 I/O CONNECTORS	Rev: B0
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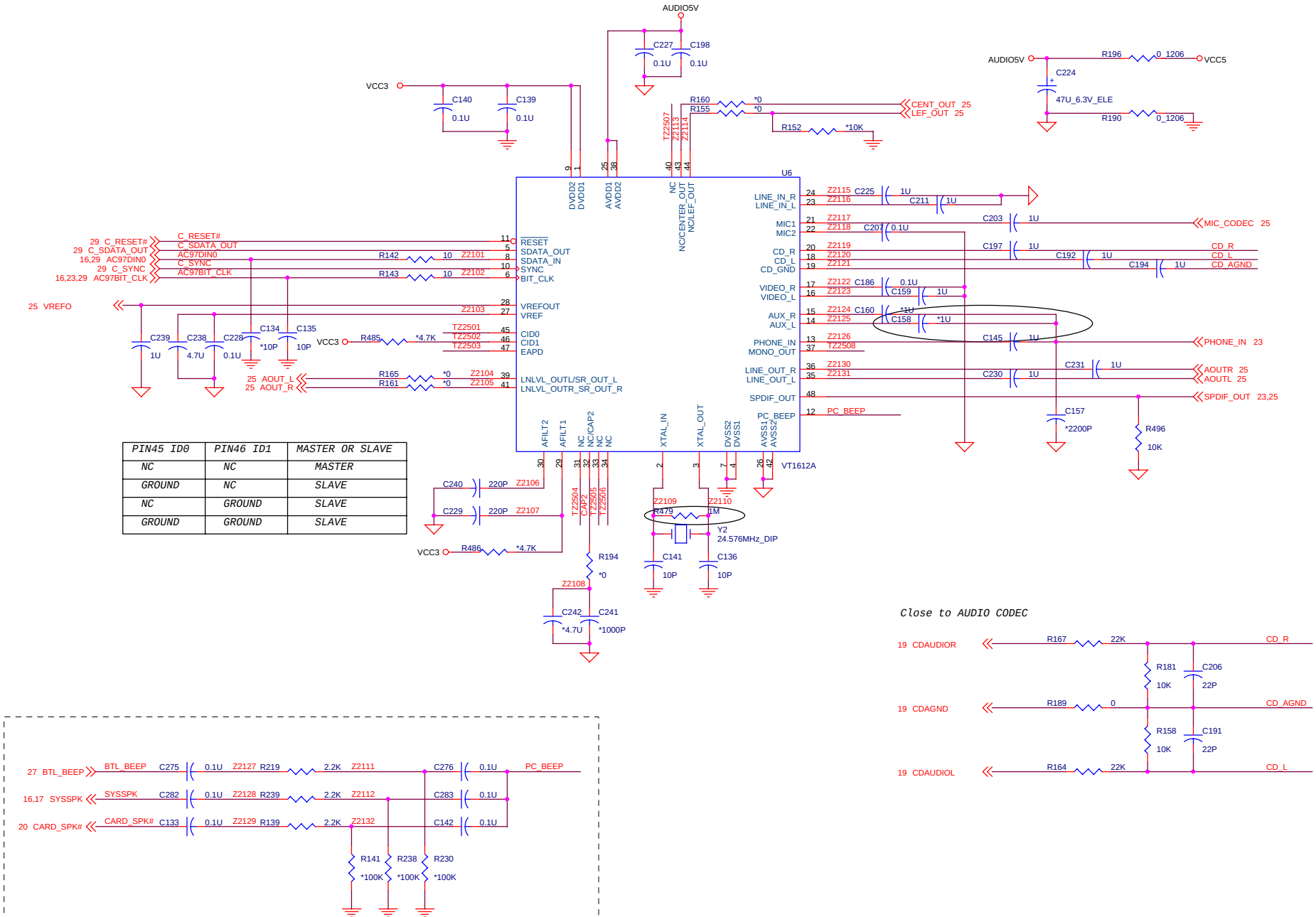

PIN45 ID0	PIN46 ID1	MASTER OR SLAVE
NC	NC	MASTER
GROUND	NC	SLAVE
NC	GROUND	SLAVE
GROUND	GROUND	SLAVE

Uniwill International Corp.		
Title: 755CA0		
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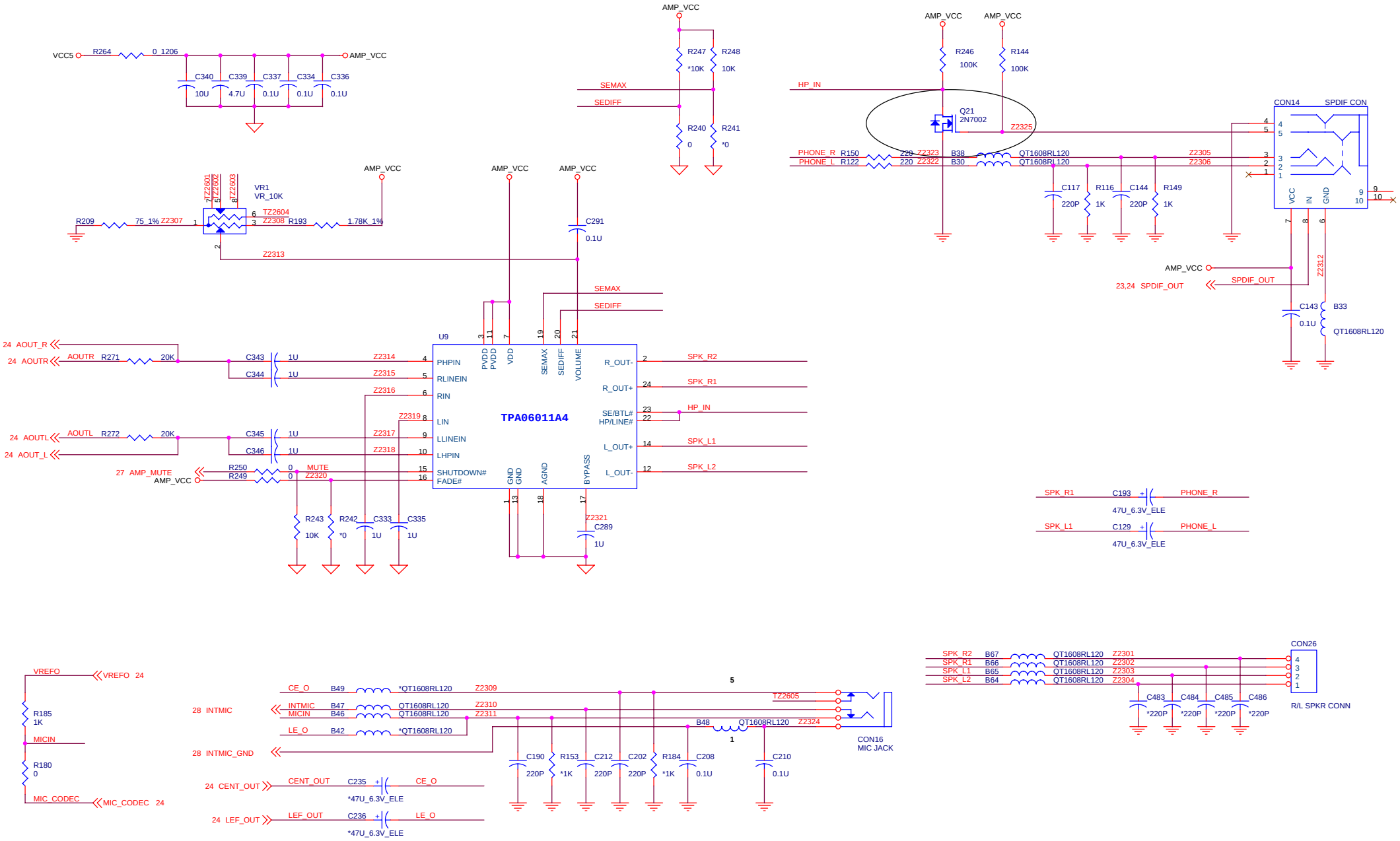

Uniwill International Corp.		
Title: **755CA0**		
Size	Document Number: **AMPLIFIER (LM4835)** 2181	Rev: B0
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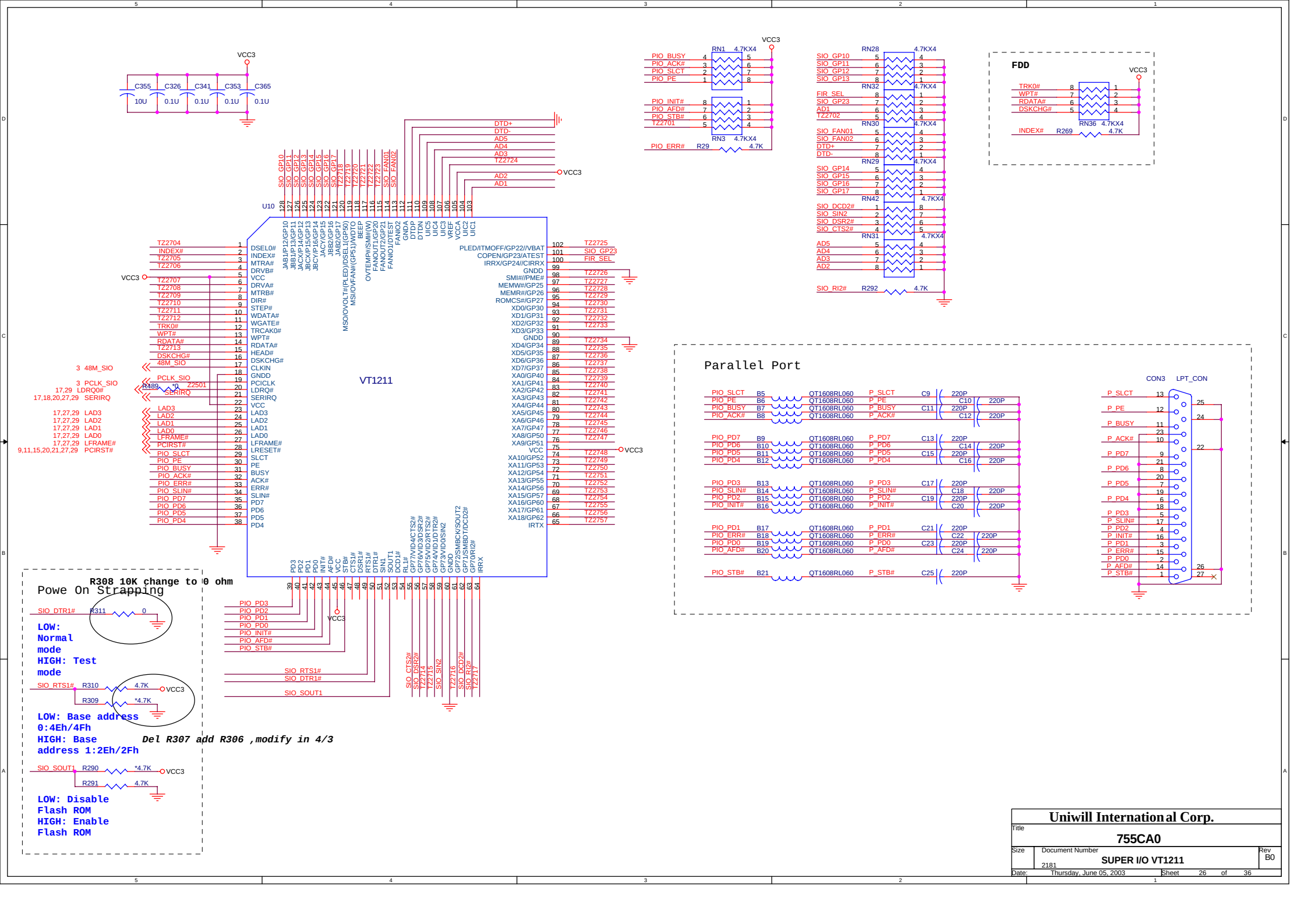
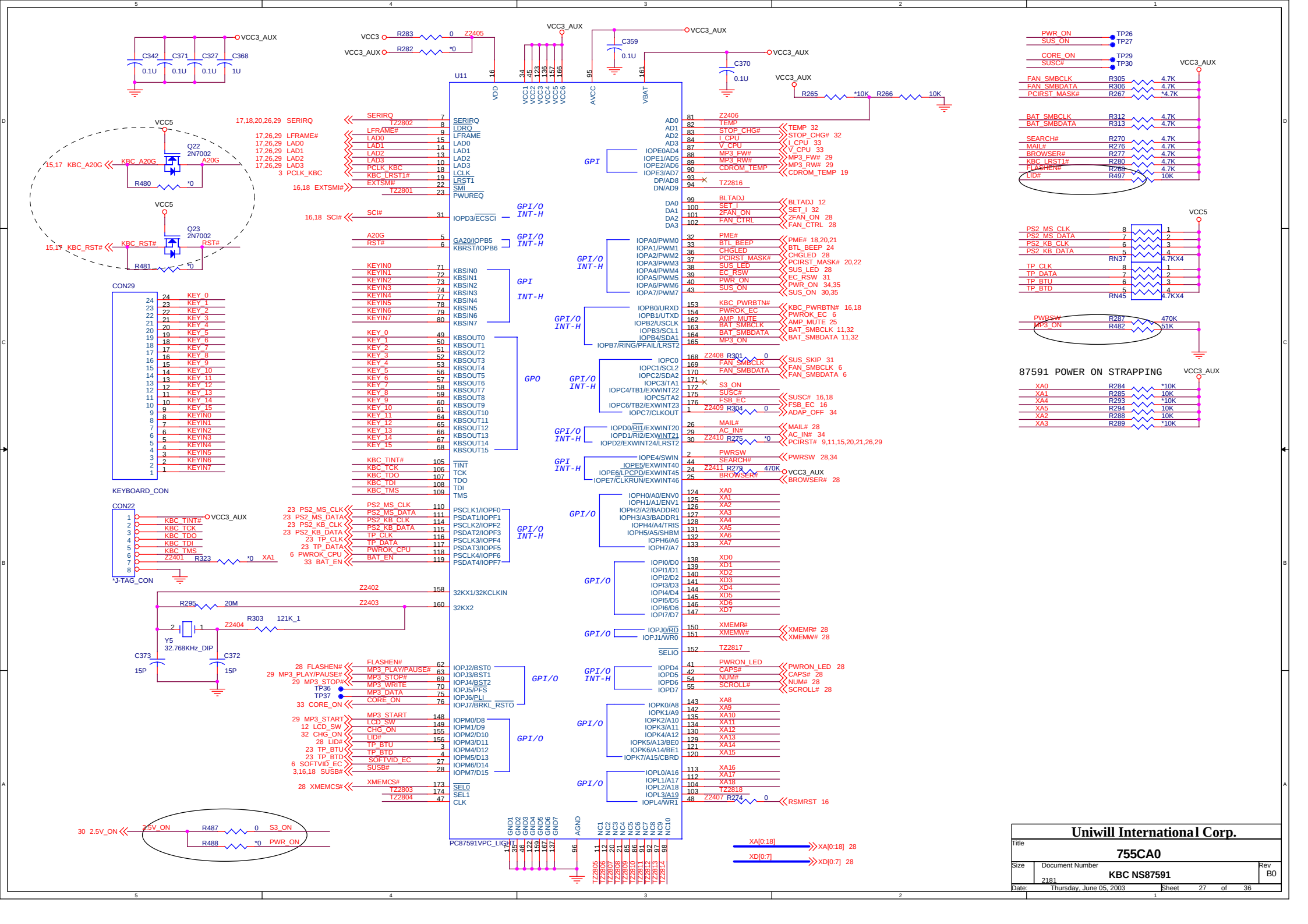
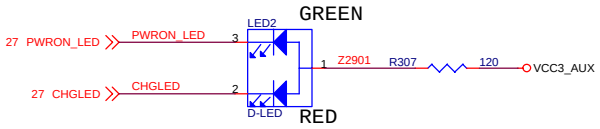
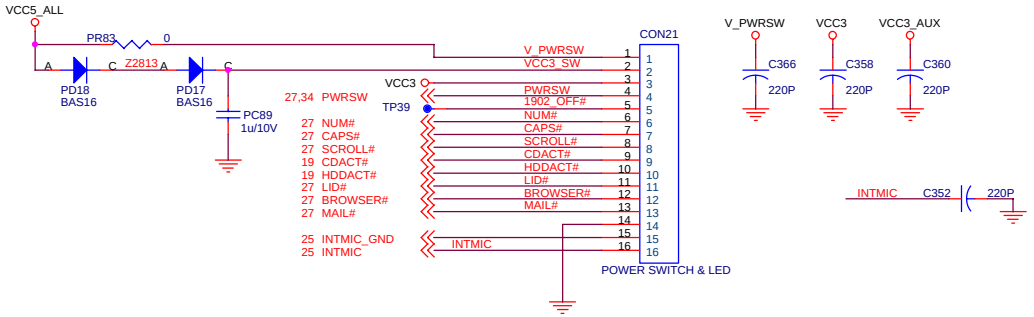
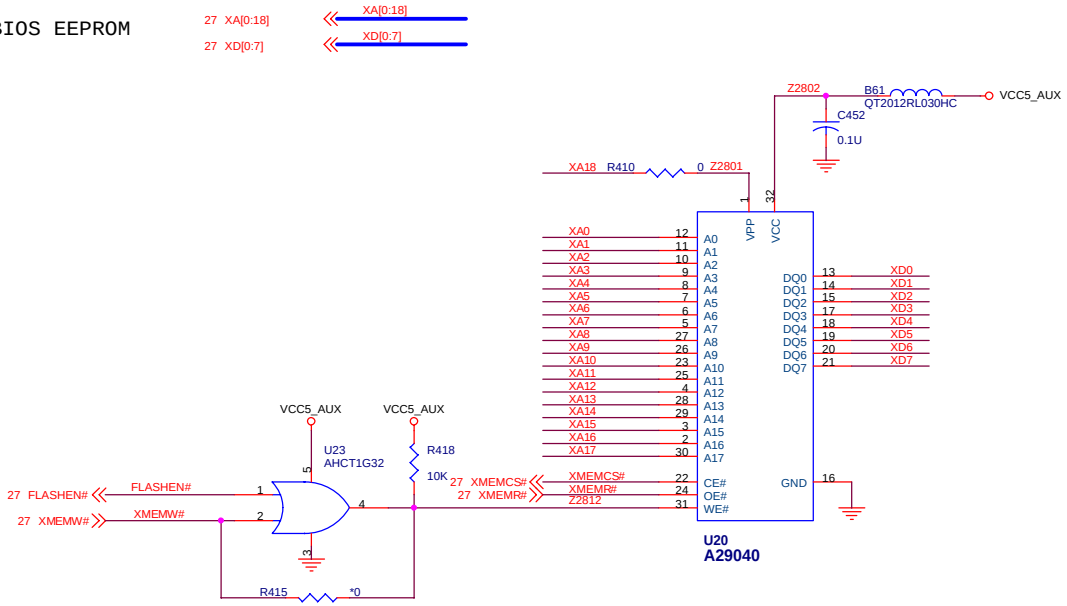

VCC3
C355 10U
C326 0.1U
C341 0.1U
C353 0.1U
C365 0.1U
U10
VT1211
DTD+
DTD-
AD5
AD4
AD3
TZ2724
AD2
AD1
DSEL0#
INDEX#
MTRA#
DRVB#
VCC
DRVA#
MTRB#
DIR#
STEP#
WDATA#
WGATE#
TRCAK0#
WPT#
RDATA#
HEAD#
DSKCHG#
CLKIN
GNDD
PCICLK
LDRQ#
SERIRQ
VCC
LAD3
LAD2
LAD1
LAD0
LFRAME#
LRESET#
SLCT
PE
BUSY
ACK#
ERR#
SLIN#
PD7
PD6
PD5
PD4
PLED/ITMOFF/GP22//VBAT
COPEN/GP23/ATEST
IRRX/GP24//CIRRX
GNDD
SMI#//PME#
MEMW#/GP25
MEMR#/GP26
ROMCS#/GP27
XD0/GP30
XD1/GP31
XD2/GP32
XD3/GP33
GNDD
XD4/GP34
XD5/GP35
XD6/GP36
XD7/GP37
XA0/GP40
XA1/GP41
XA2/GP42
XA3/GP43
XA4/GP44
XA5/GP45
XA6/GP46
XA7/GP47
XA8/GP50
XA9/GP51
VCC
XA10/GP52
XA11/GP53
XA12/GP54
XA13/GP55
XA14/GP56
XA15/GP57
XA16/GP60
XA17/GP61
XA18/GP62
IRTX
RN1 4.7KX4
PIO_BUSY
PIO_ACK#
PIO_SLCT
PIO_PE
PIO_INIT#
PIO_AFD#
PIO_STB#
TZ2701
RN3 4.7KX4
PIO_ERR# R29 4.7K
RN28 4.7KX4
SIO_GP10
SIO_GP11
SIO_GP12
SIO_GP13
RN32 4.7KX4
FIR_SEL
SIO_GP23
AD1
TZ2702
RN30 4.7KX4
SIO_FAN01
SIO_FAN02
DTD+
DTD-
RN29 4.7KX4
SIO_GP14
SIO_GP15
SIO_GP16
SIO_GP17
RN42 4.7KX4
SIO_DCD2#
SIO_SIN2
SIO_DSR2#
SIO_CTS2#
RN31 4.7KX4
AD5
AD4
AD3
AD2
SIO_RI2# R292 4.7K
FDD
TRK0#
WPT#
RDATA#
DSKCHG#
RN36 4.7KX4
INDEX# R269 4.7K
Parallel Port
CON3 LPT_CON
PIO_SLCT B5 QT1608RL060 P_SLCT C9 220P C10 220P
PIO_PE B6 QT1608RL060 P_PE
PIO_BUSY B7 QT1608RL060 P_BUSY C11 220P C12 220P
PIO_ACK# B8 QT1608RL060 P_ACK#
PIO_PD7 B9 QT1608RL060 P_PD7 C13 220P C14 220P
PIO_PD6 B10 QT1608RL060 P_PD6
PIO_PD5 B11 QT1608RL060 P_PD5 C15 220P C16 220P
PIO_PD4 B12 QT1608RL060 P_PD4
PIO_PD3 B13 QT1608RL060 P_PD3 C17 220P C18 220P
PIO_SLIN# B14 QT1608RL060 P_SLIN#
PIO_PD2 B15 QT1608RL060 P_PD2 C19 220P C20 220P
PIO_INIT# B16 QT1608RL060 P_INIT#
PIO_PD1 B17 QT1608RL060 P_PD1 C21 220P C22 220P
PIO_ERR# B18 QT1608RL060 P_ERR#
PIO_PD0 B19 QT1608RL060 P_PD0 C23 220P C24 220P
PIO_AFD# B20 QT1608RL060 P_AFD#
PIO_STB# B21 QT1608RL060 P_STB# C25 220P
P_SLCT
P_PE
P_BUSY
P_ACK#
P_PD7
P_PD6
P_PD5
P_PD4
P_PD3
P_SLIN#
P_PD2
P_INIT#
P_PD1
P_ERR#
P_PD0
P_AFD#
P_STB#
R308 10K change to 0 ohm
Powe On Strapping
SIO_DTR1# R311 0
LOW: Normal mode
HIGH: Test mode
SIO_RTS1# R310 4.7K
R309 *4.7K
LOW: Base address 0:4Eh/4Fh
HIGH: Base address 1:2Eh/2Fh
Del R307 add R306 ,modify in 4/3
SIO_SOUT1 R290 *4.7K
R291 4.7K
LOW: Disable Flash ROM
HIGH: Enable Flash ROM
R489 *0 Z2501
48M_SIO
PCLK_SIO
SERIRQ
LDRQ0#
3 48M_SIO
3 PCLK_SIO
17,29 LDRQ0#
17,18,20,27,29 SERIRQ
17,27,29 LAD3
17,27,29 LAD2
17,27,29 LAD1
17,27,29 LAD0
17,27,29 LFRAME#
9,11,15,20,21,27,29 PCIRST#
PIO_PD3
PIO_PD2
PIO_PD1
PIO_PD0
PIO_INIT#
PIO_AFD#
PIO_STB#
SIO_RTS1#
SIO_DTR1#
SIO_SOUT1
SIO_CTS2#
SIO_DSR2#
SIO_SIN2
SIO_DCD2#
SIO_RI2#
Uniwill International Corp.
Title
755CA0
Size
Document Number
2181
SUPER I/O VT1211
Rev
B0
Date: Thursday, June 05, 2003
Sheet 26 of 36


U11
PC87591VPC_LIGHT
VCC3_AUX
VCC3
C342
C371
C327
C368
0.1U
1U
R283
R282
C359
C370
R265
*10K
R266
10K
Q22
2N7002
Q23
2N7002
R480
R481
CON29
KEYBOARD_CON
CON22
*J-TAG_CON
Y5
32.768KHz_DIP
C373
C372
15P
R295
20M
R303
121K_1
R487
R488
2.5V_ON
S3_ON
PWR_ON
SERIRQ
LFRAME#
LAD0
LAD1
LAD2
LAD3
PCLK_KBC
KBC_LRST1#
EXTSMI#
SCI#
A20G
RST#
KEYIN0
KEYIN1
KEYIN2
KEYIN3
KEYIN4
KEYIN5
KEYIN6
KEYIN7
KSBSIN0
KSBSIN1
KSBSIN2
KSBSIN3
KSBSIN4
KSBSIN5
KSBSIN6
KSBSIN7
KSBSOUT0
KSBSOUT1
KSBSOUT2
KSBSOUT3
KSBSOUT4
KSBSOUT5
KSBSOUT6
KSBSOUT7
KSBSOUT8
KSBSOUT9
KSBSOUT10
KSBSOUT11
KSBSOUT12
KSBSOUT13
KSBSOUT14
KSBSOUT15
KBC_TINT#
KBC_TCK
KBC_TDO
KBC_TDI
KBC_TMS
PS2_MS_CLK
PS2_MS_DATA
PS2_KB_CLK
PS2_KB_DATA
TP_CLK
TP_DATA
PWROK_CPU
BAT_EN
32KX1/32KCLKIN
32KX2
FLASHEN#
MP3_PLAY/PAUSE#
MP3_STOP#
MP3_WRITE
MP3_DATA
CORE_ON
MP3_START
LCD_SW
CHG_ON
LID#
TP_BTU
TP_BTD
SOFTVID_EC
SUSB#
XMEMCS#
GPI
GPO
GPI/O
INT-H
Z2406
TEMP
STOP_CHG#
I_CPU
V_CPU
MP3_FW#
MP3_RW#
CDROM_TEMP
BLTADJ
SET_I
2FAN_ON
FAN_CTRL
PME#
BTL_BEEP
CHGLED
PCIRST_MASK#
SUS_LED
EC_RSW
PWR_ON
SUS_ON
KBC_PWRBTN#
PWROK_EC
AMP_MUTE
BAT_SMBCLK
BAT_SMBDATA
MP3_ON
FAN_SMBCLK
FAN_SMBDATA
S3_ON
SUSC#
FSB_EC
ADAP_OFF
MAIL#
AC_IN#
PCIRST#
PWRSW
SEARCH#
BROWSER#
XA0
XA1
XA2
XA3
XA4
XA5
XA6
XA7
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
XMEMR#
XMEMW#
SELIO
TZ2817
PWRON_LED
CAPS#
NUM#
SCROLL#
XA8
XA9
XA10
XA11
XA12
XA13
XA14
XA15
XA16
XA17
XA18
TZ2818
RSMRST
TZ2816
TZ2802
TZ2801
TZ2803
TZ2804
Z2402
Z2403
Z2404
Z2401
Z2405
Z2408
Z2409
Z2410
Z2411
Z2407
R301
R304
R275
R279
R274
R323
PWR_ON
SUS_ON
CORE_ON
SUSC#
TP26
TP27
TP29
TP30
FAN_SMBCLK
FAN_SMBDATA
PCIRST_MASK#
BAT_SMBCLK
BAT_SMBDATA
SEARCH#
MAIL#
BROWSER#
KBC_LRST1#
FLASHEN#
LID#
R305
R306
R267
R312
R313
R270
R276
R277
R280
R268
R497
4.7K
*4.7K
10K
PS2_MS_CLK
PS2_MS_DATA
PS2_KB_CLK
PS2_KB_DATA
TP_CLK
TP_DATA
TP_BTU
TP_BTD
RN37
RN45
4.7KX4
PWRSW
MP3_ON
R287
R482
470K
51K
87591 POWER ON STRAPPING
XA0
XA1
XA4
XA5
XA2
XA3
R284
R285
R293
R294
R288
R289
*10K
10K
XA[0:18]
XD[0:7]
Uniwill International Corp.
755CA0
KBC NS87591
B0
2181
Thursday, June 05, 2003
27
36

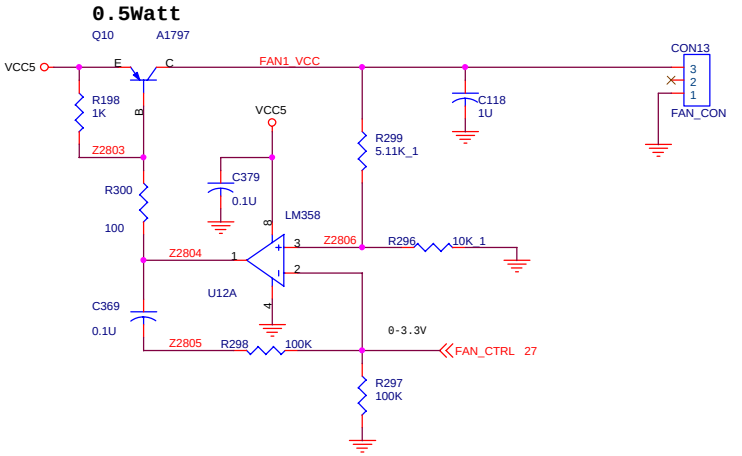


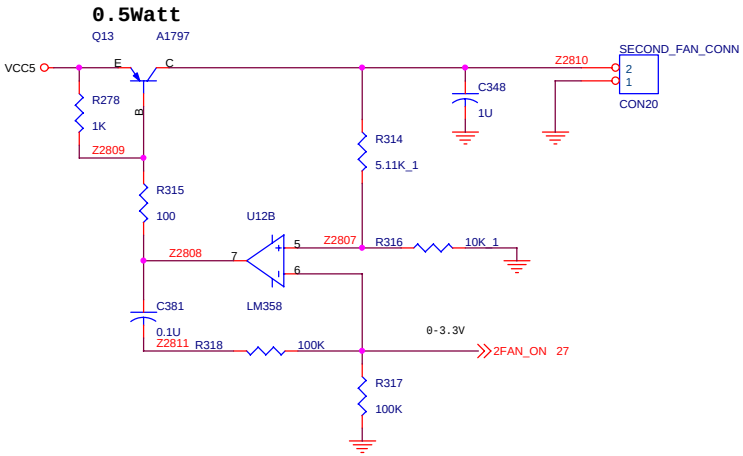


BIOS EEPROM

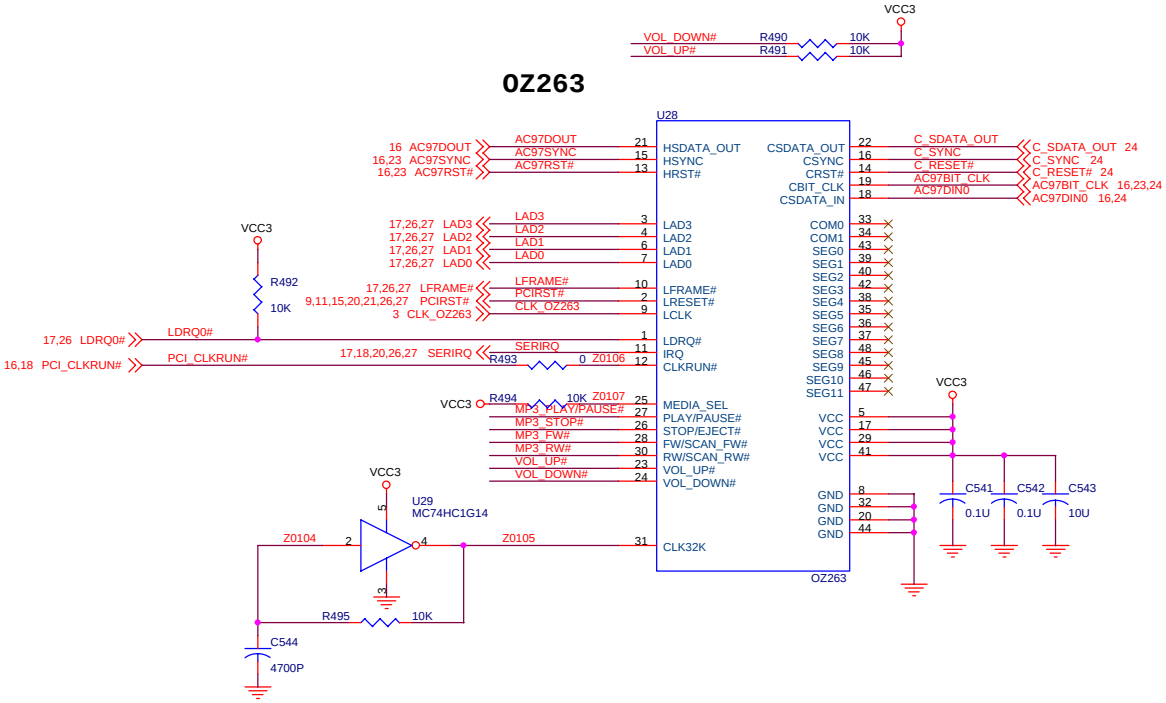


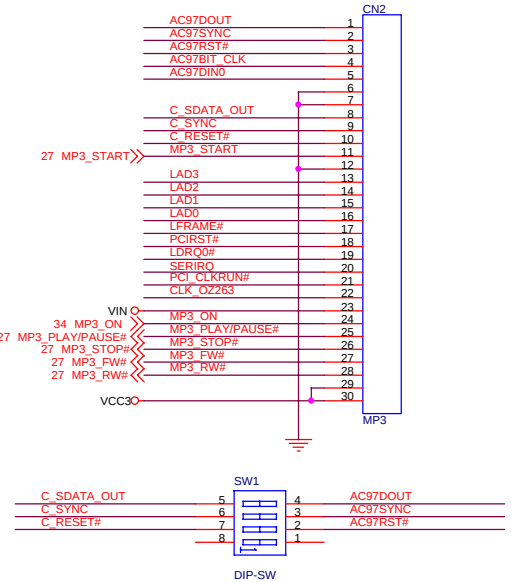
FAN CONTROL CIRCUIT





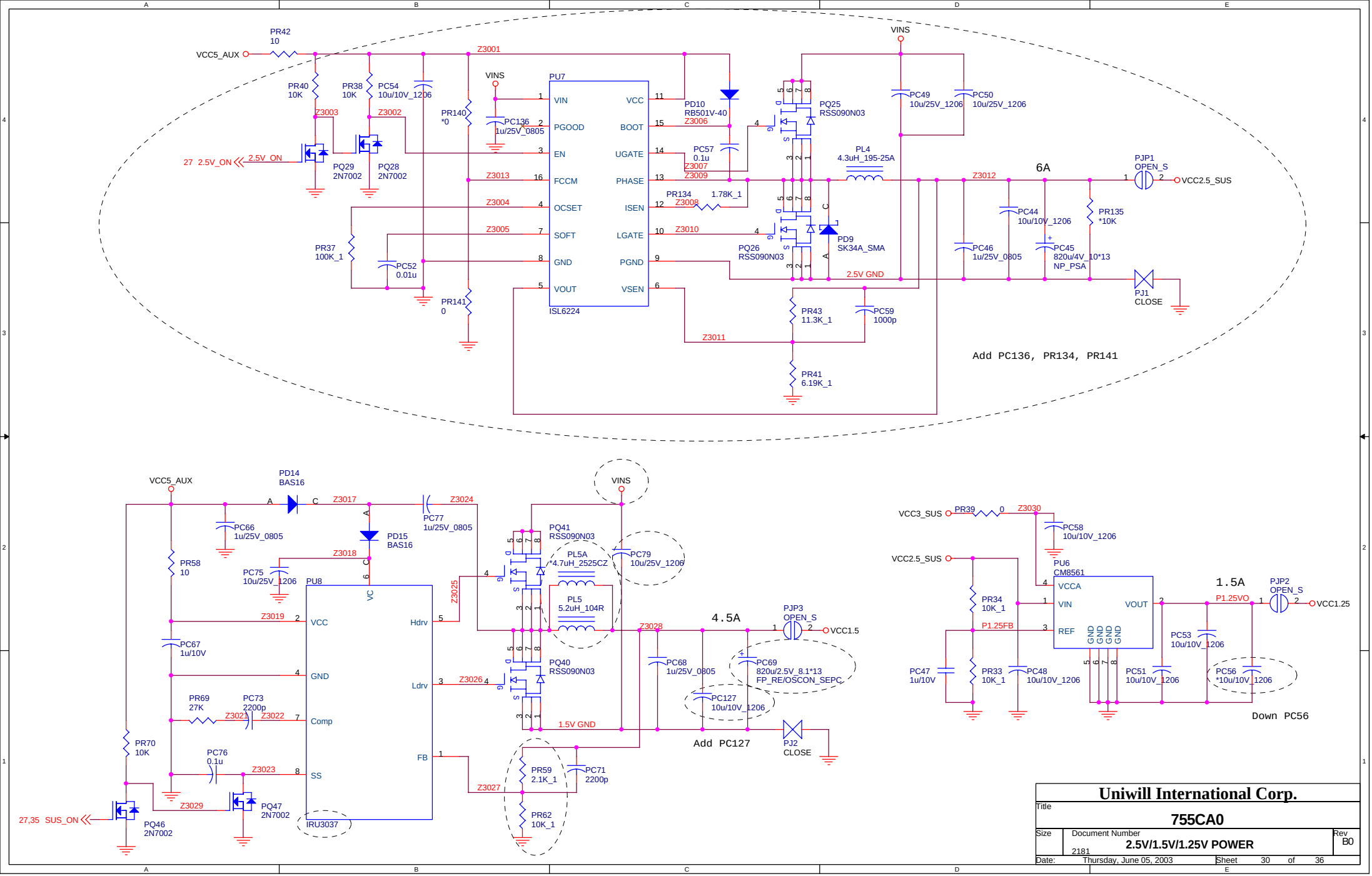
Uniwill International Corp.		
Title: **755CA0**		
Size	Document Number: **FAN & SHDN DETECT** 2181	Rev: B0
Date: Thursday, June 05, 2003	Sheet 28 of 36	



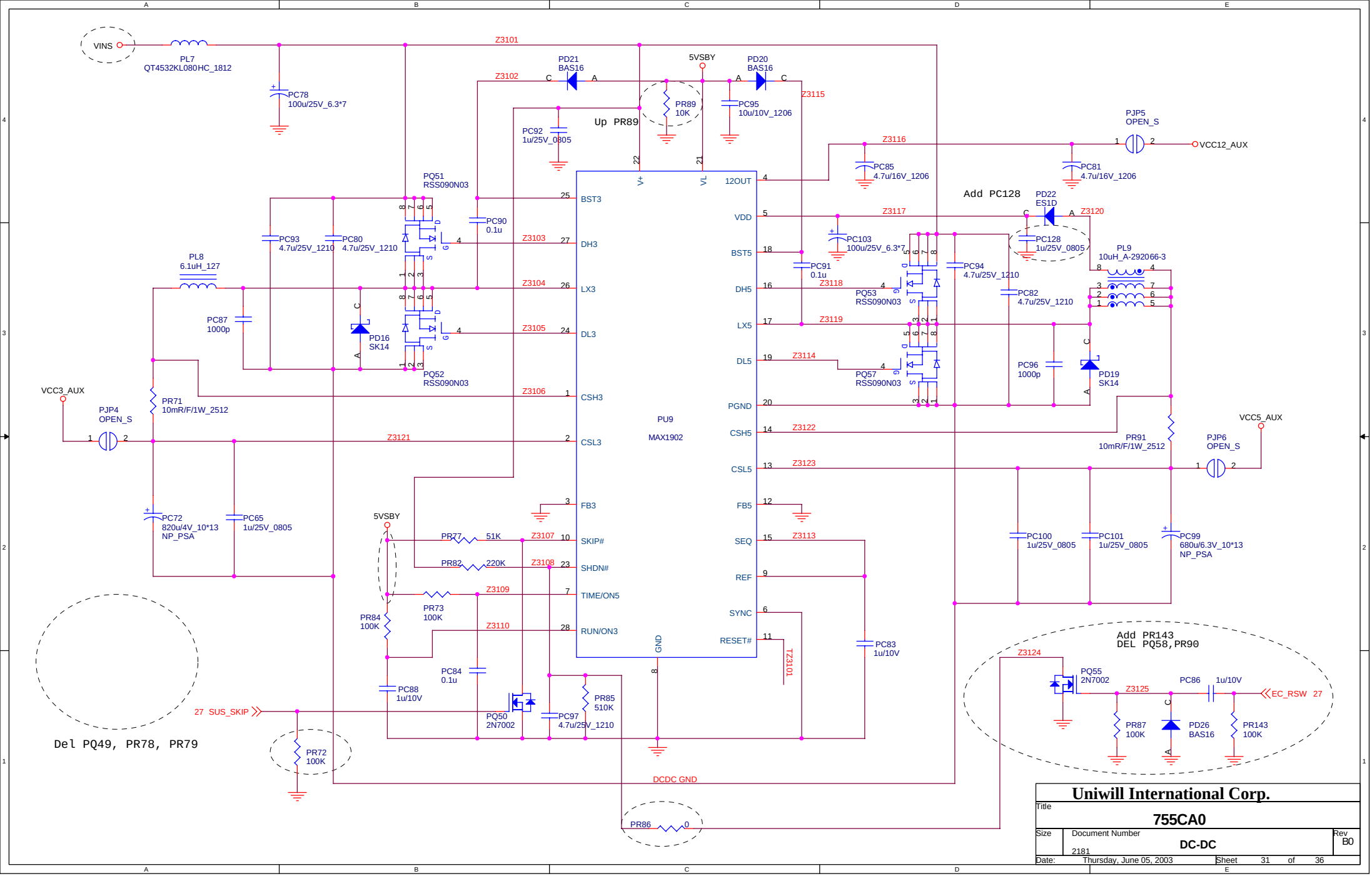


SW1	1	2	3
Without MP3	ON	ON	ON
With MP3	OFF	OFF	OFF

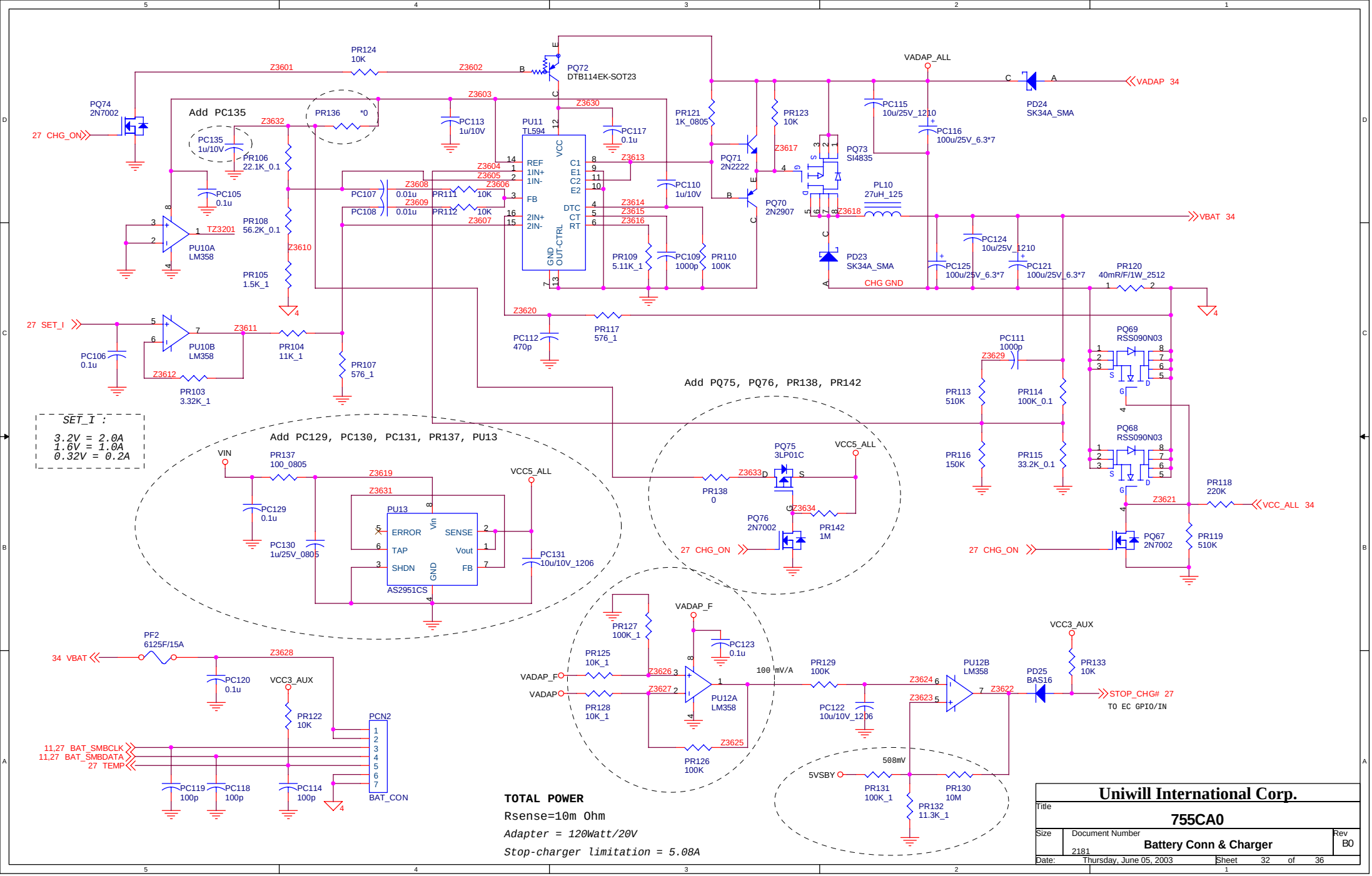
Title	MP3		
Size	Document Number 755CA0		Rev B0
Date: Thursday, June 05, 2003	Sheet 29 of 36		

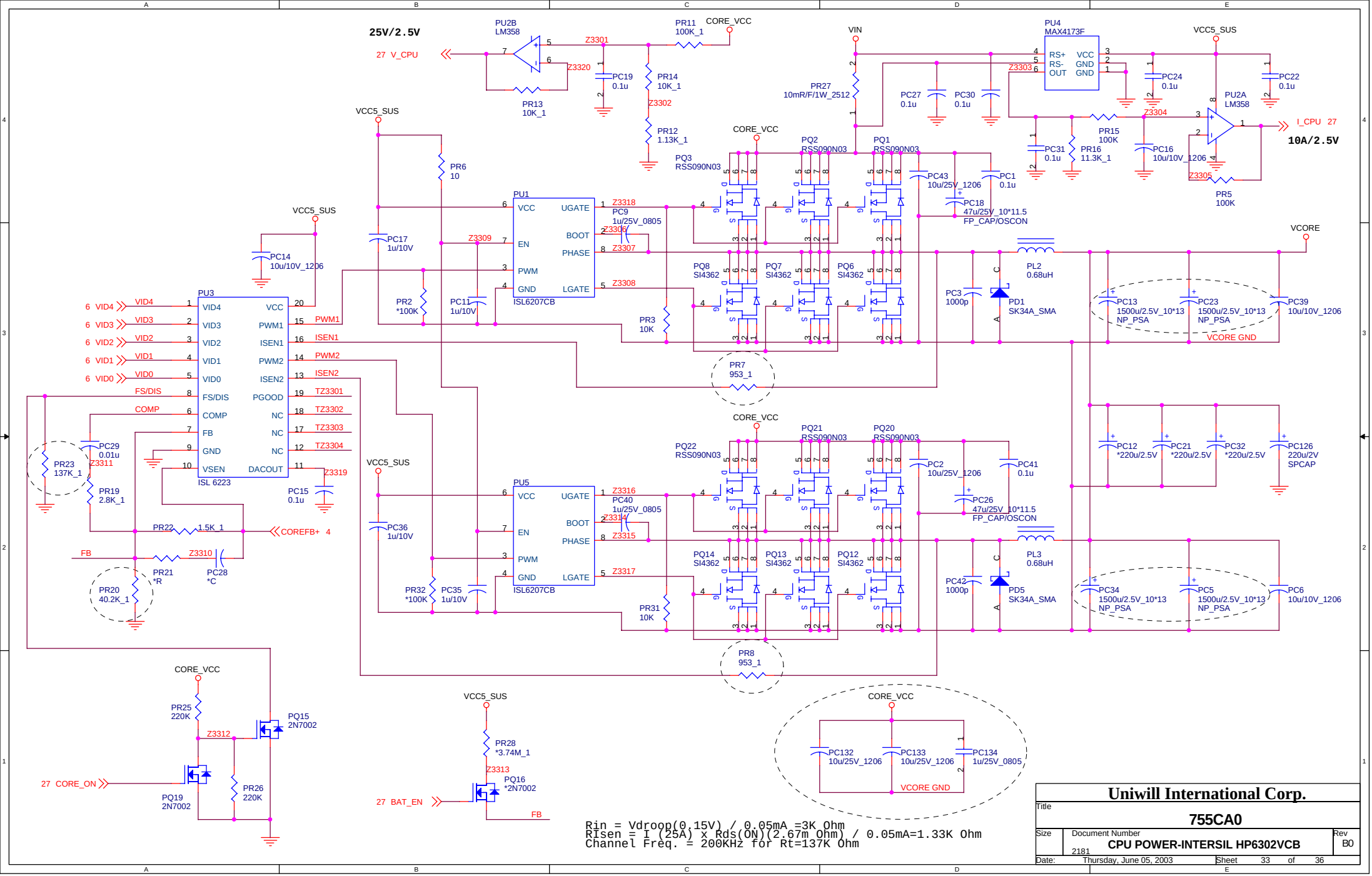


Uniwill International Corp.		
Title	**755CA0**	
Size	Document Number: 2181 — **2.5V/1.5V/1.25V POWER**	Rev: B0
Date: Thursday, June 05, 2003	Sheet 30 of 36	



Uniwill International Corp.		
Title	755CA0	
Size	Document Number: 2181 — DC-DC	Rev: B0
Date: Thursday, June 05, 2003	Sheet 31 of 36	


Add PC135
Add PC129, PC130, PC131, PR137, PU13
Add PQ75, PQ76, PR138, PR142
SET_I :
3.2V = 2.0A
1.6V = 1.0A
0.32V = 0.2A
TOTAL POWER
Rsense=10m Ohm
Adapter = 120Watt/20V
Stop-charger limitation = 5.08A
Uniwill International Corp.
755CA0
Battery Conn & Charger
2181
B0
Thursday, June 05, 2003
Sheet 32 of 36


25V/2.5V
27 V_CPU
PU2B
LM358
PR11
100K_1
CORE_VCC
Z3301
Z3320
PC19
0.1u
PR14
10K_1
Z3302
PR13
10K_1
PR12
1.13K_1
VIN
PU4
MAX4173F
RS+
RS-
OUT
VCC
GND
GND
Z3303
PR27
10mR/F/1W_2512
PC27
0.1u
PC30
0.1u
VCC5_SUS
PC24
0.1u
PC22
0.1u
PU2A
LM358
Z3304
PR15
100K
PC31
0.1u
PR16
11.3K_1
PC16
10u/10V_1206
Z3305
PR5
100K
I_CPU 27
10A/2.5V
VCC5_SUS
PR6
10
CORE_VCC
PQ2
RSS090N03
PQ1
RSS090N03
PQ3
RSS090N03
PC43
10u/25V_1206
PC1
0.1u
PC18
47u/25V_10*11.5
FP_CAP/OSCON
VCC5_SUS
PC14
10u/10V_1206
PU1
VCC
UGATE
BOOT
PHASE
EN
PWM
GND
LGATE
ISL6207CB
Z3318
PC9
1u/25V_0805
Z3306
Z3307
Z3308
Z3309
PC17
1u/10V
PR2
*100K
PC11
1u/10V
PR3
10K
PQ8
SI4362
PQ7
SI4362
PQ6
SI4362
PL2
0.68uH
PC3
1000p
PD1
SK34A_SMA
VCORE
PC13
1500u/2.5V_10*13
NP_PSA
PC23
1500u/2.5V_10*13
NP_PSA
PC39
10u/10V_1206
VCORE GND
PR7
953_1
PU3
VID4
VID3
VID2
VID1
VID0
FS/DIS
COMP
FB
GND
VSEN
VCC
PWM1
ISEN1
PWM2
ISEN2
PGOOD
NC
NC
NC
DACOUT
ISL 6223
TZ3301
TZ3302
TZ3303
TZ3304
Z3319
PC15
0.1u
PC29
0.01u
Z3311
PR23
137K_1
PR19
2.8K_1
PR22
1.5K_1
COREFB+ 4
FB
Z3310
PR21
*R
PC28
*C
PR20
40.2K_1
CORE_VCC
PQ22
RSS090N03
PQ21
RSS090N03
PQ20
RSS090N03
PC2
10u/25V_1206
PC41
0.1u
PC26
47u/25V_10*11.5
FP_CAP/OSCON
PC12
*220u/2.5V
PC21
*220u/2.5V
PC32
*220u/2.5V
PC126
220u/2V
SPCAP
VCC5_SUS
PC36
1u/10V
PU5
VCC
UGATE
BOOT
PHASE
EN
PWM
GND
LGATE
ISL6207CB
Z3316
PC40
1u/25V_0805
Z3314
Z3315
Z3317
PR32
*100K
PC35
1u/10V
PR31
10K
PQ14
SI4362
PQ13
SI4362
PQ12
SI4362
PL3
0.68uH
PC42
1000p
PD5
SK34A_SMA
PC34
1500u/2.5V_10*13
NP_PSA
PC5
1500u/2.5V_10*13
NP_PSA
PC6
10u/10V_1206
PR8
953_1
CORE_VCC
PR25
220K
Z3312
PQ15
2N7002
27 CORE_ON
PQ19
2N7002
PR26
220K
VCC5_SUS
PR28
*3.74M_1
Z3313
PQ16
*2N7002
27 BAT_EN
FB
CORE_VCC
PC132
10u/25V_1206
PC133
10u/25V_1206
PC134
1u/25V_0805
VCORE GND
Rin = Vdroop(0.15V) / 0.05mA =3K Ohm
RIsen = I (25A) x Rds(ON)(2.67m Ohm) / 0.05mA=1.33K Ohm
Channel Freq. = 200KHz for Rt=137K Ohm
Uniwill International Corp.
Title
755CA0
Size
Document Number
2181
CPU POWER-INTERSIL HP6302VCB
Rev
B0
Date: Thursday, June 05, 2003
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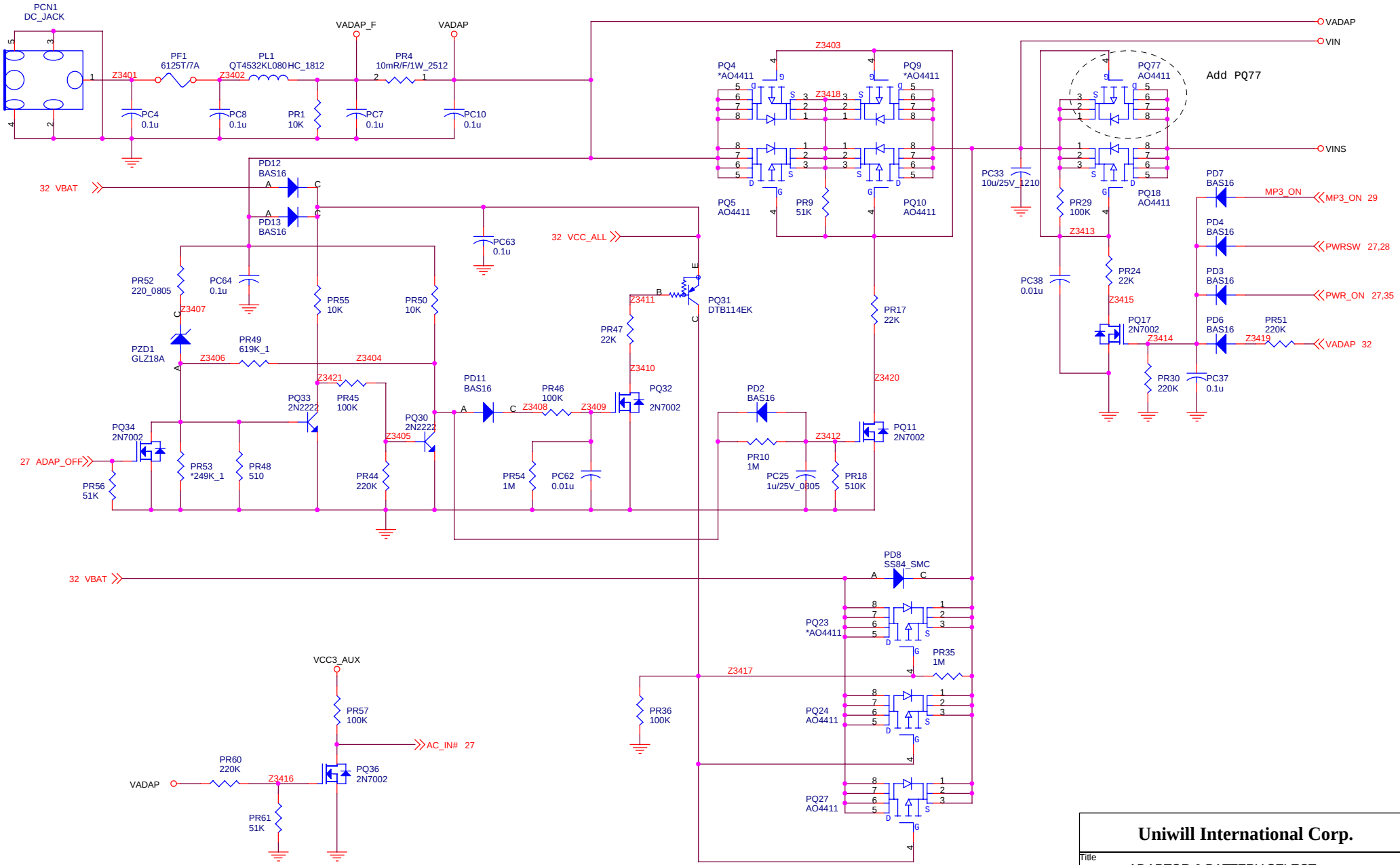
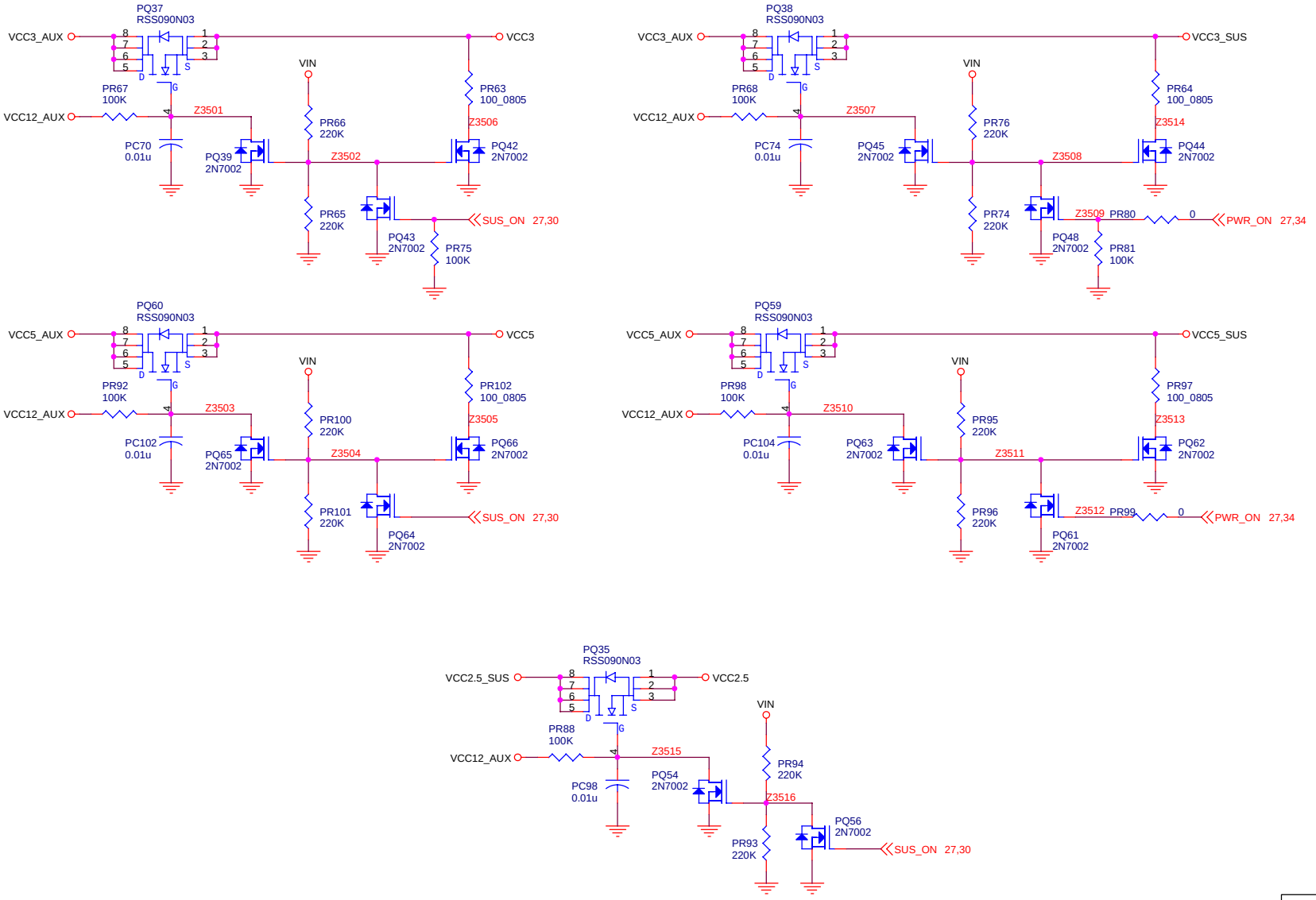

PCN1
DC_JACK
PF1
6125T/7A
PL1
QT4532KL080HC_1812
PR4
10mR/F/1W_2512
VADAP_F
VADAP
Z3401
Z3402
PC4
0.1u
PC8
0.1u
PR1
10K
PC7
0.1u
PC10
0.1u
Z3403
PQ4
*AO4411
PQ9
*AO4411
Z3418
PQ5
AO4411
PR9
51K
PQ10
AO4411
PQ77
AO4411
Add PQ77
VADAP
VIN
VINS
PC33
10u/25V_1210
PR29
100K
PQ18
AO4411
Z3413
PC38
0.01u
PR24
22K
Z3415
PQ17
2N7002
Z3414
PR30
220K
PC37
0.1u
PD7
BAS16
MP3_ON
MP3_ON 29
PD4
BAS16
PWRSW 27,28
PD3
BAS16
PWR_ON 27,35
PD6
BAS16
PR51
220K
Z3419
VADAP 32
32 VBAT
PD12
BAS16
PD13
BAS16
PC63
0.1u
32 VCC_ALL
PR52
220_0805
PC64
0.1u
Z3407
PZD1
GLZ18A
PR55
10K
PR50
10K
PR49
619K_1
Z3406
Z3404
Z3421
PQ33
2N2222
PR45
100K
PQ30
2N2222
Z3405
PD11
BAS16
PR46
100K
Z3408
Z3409
PQ32
2N7002
Z3411
PQ31
DTB114EK
PR47
22K
Z3410
PR17
22K
Z3420
PD2
BAS16
Z3412
PQ11
2N7002
PR10
1M
PC25
1u/25V_0805
PR18
510K
PQ34
2N7002
27 ADAP_OFF
PR56
51K
PR53
*249K_1
PR48
510
PR44
220K
PR54
1M
PC62
0.01u
32 VBAT
PD8
SS84_SMC
PQ23
*AO4411
PR35
1M
Z3417
PR36
100K
PQ24
AO4411
PQ27
AO4411
VCC3_AUX
PR57
100K
AC_IN# 27
PR60
220K
Z3416
PQ36
2N7002
VADAP
PR61
51K
Uniwill International Corp.
Title
ADAPTOR & BATTERY SELECT
Size
Document Number
755CA0
Rev
B0
Date: Thursday, June 05, 2003
Sheet 34 of 36



Uniwill International Corp.

Title	DC-DC Connector & VCC_MOSFET	
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A0 to A1 change lists

1.Page6: del R111
2.Page8: U7 AK11 add R494 , pull-up to 2.5V_SUS (fix cann't boot)
3.Page10: Add CAP(page10) on U7 bottom side
4.Page11: CON11 pin39,41 change net
5.Page15: Add CAP(page15) on U22 bottom side
6.Page17: del R362 , connect ATHLON_STPCLK# to U22 pin R26
7.Page23: del RV1
8.Page25: C155,C158 connect to PHONE_IN (fix no MODEM dial phone)
9.Page26: AMP_VDD connect to AMP_VCC
10.Page26:C166 + connect to SPK_R1 , C126 + connect to SPK_L1
11.Page28: add R495,R496 to U10 pin81 for M/B control
Page28: del R249 (cancel the function)
Page28: SOFTVID_EC change to U10 pin90 from pin27
Page28: SUS_SKIP and R292 change to U10 pin168 from pin149
Page28: FSB_EC change to U10 pin176 from pin70
Page28: ADAP_OFF and R291 change to U10 pin1
Page28: RSMRST and R258 change to U10 pin48 from pin63
Page28: Del S3_ON on U10 pin75
Page28: Del R297 and R272

A1 to A2 change lists

1.Page13: Change DDR DIMM to 184PIN
2.Page14: Change 33 ohm 8P4R pull-high to 0603 size

A2 to B0 change lists

1.Page 6: U1 pin10 change to net:VCC3_SUS
2.Page11: Add R483 for AGP 4X,8X test
3.Page12: Add U27 , Del D1,D2 and R32 to fix backlight problem
4.Page13: Add C536,C538 and C539 10U_X7R for 2.5V
5.Page21: Change U15 pin24 to VCC3 to fix VCC3 and VCC3_SUS shortage
6.Page22: Add shunt resistor R484 on Y1
7.Page25: Add Q21 to fix no internal SPK sound while external SPK not plug in
8.Page27: Add Q22,Q23,R480,R481 to fix reverse current
9.Page27: Add R482 to fix auto boot
10.Page27: Add R487,R488 for S3 support

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