What's New in Altium Designer 6.3

Summary

Continuing to improve productivity, the release of Altium Designer 6.3 brings a new PCB graphics engine, offering substantial drawing speed improvements. Numerous other new and enhanced features help make Altium Designer an even more productive development environment.

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Altium Designer 6.3 delivers an extensive range of new features and productivity enhancements designed to help users produce better designs faster. These latest improvements include major advancements in Altium Designer's board layout capabilities and FPGA design capacity, plus expanded support for working with and importing data from external systems. With this new release, Altium Designer again pushes the boundaries of electronic product design to help engineers produce more innovative products within shorter timeframes.

The new enhancements included in the Altium Designer 6.3 release combine to provide broad improvements across most major areas, from fundamental board layout facilities through to interfacing to external systems.

The physical design platform has undergone a core performance enhancement through Altium Designer's new Hardware Accelerated Graphics Engine which offers a speed improvement of up to 20 times, for fast, smooth panning and redraws. Also included are significant productivity enhancements such as a powerful new polygon (copper pour) manager, improved Smart Drag support for multi-track routing and the ability to create PCB slots and square holes.

Altium Designer 6.3 includes significant improvements to import support for OrCAD® and PADS® and P-CAD® designs, further easing the translation process from other systems. The release also offers new project managements benefits such as version-controlled database libraries and new IPC compliant board level libraries.

Increased programmable device support and processor coverage has also been added to this release. Altium Designer now offers full toolchain support for Altera® Nios® II embedded processors plus support for all currently available ARM®-7 based Sharp BlueStreak® processors, support for popular soft cores such as the BT656 Video Capture core and the I2S Audio Streaming core.

These are just some of the new enhancements delivered by this significant new release of Altium Designer. To learn more about the new capabilities and productivity benefits offered in Altium Designer 6.3, read on!

New – Hardware accelerated graphics engine

Altium Designer's PCB editor has a new Hardware Accelerated Graphics Engine. This engine provides a substantial increase in drawing speed over the current GDI-based graphics engine, providing smooth, real-time graphics within the PCB editor. The redraw speed is effectively instant, even on the largest PCBs.

The new graphics engine is built around the Shader Model 3.0 technology supported by Microsoft DirectX 9.0c. Shader Modeling is a technique where the code for rendering the objects displayed by an application is executed on the Graphics card Processor Unit (GPU), instead of on the main CPU.

Traditionally the graphics card is treated as a dumb pixel painter, where the application code first renders the image as a bitmap in memory and then passes all of the pixel data from the main CPU to the GPU.

Using Shader modeling technology the rendering code is executed on the GPU, the application code issues instructions to the GPU to render a particular type of object, supplying a minimal set of data such as object locations, color, lighting, and so on.

In the case of Altium Designer's PCB editor, this means that rather than passing a large number of pixels that when rendered paint a track object on the screen, the GPU is programmed to know how to draw a track – Altium Designer simply passes location coordinates, width and color information.

The new Hardware Accelerated Graphics Engine will:

- Provide drawing speed improvements in the order of 20 times over GDI.
- Remove the impact of polygons on drawing speed.
- Provide smooth panning and scrolling, at all zoom levels.
- Maintain drawing and panning performance for the largest of boards.
- Be thoroughly tested and benchmarked on a wide variety of graphics cards.
- Work in harmony with the existing graphics engine, allowing the user to switch between them as needed.

Note that the new graphics engine requires a graphics card that supports DirectX® 9.0c and Shader Model 3.0.

Use the following links to learn more about Shader technology:
http://en.wikipedia.org/wiki/Shader
http://www.microsoft.com/whdc/winhec/partners/shadermodel30_NVIDIA.mspx

New – Copper pour (polygon) management system

A standard design technique on today's dense, high-speed boards is to use all spare board space as reference planes, filling them with regions of solid copper. These regions of copper, known as copper pours, are created by placing polygons. It is not uncommon for a multi-layer board design to include 50 or more polygons.

The new **Polygon Manager** provides a powerful control center for reviewing and managing all of the polygons on a board. The Polygon Manager is launched from the **Tools » Polygon Pours** submenu.

The Polygon Manager not only provides a high-level view of all polygons on the entire board, with it you can:

- Name and rename each polygon.
- Set the pour order of polygons.
- Perform actions on selected polygons, such as *repour* or *shelve* (hide from display and DRC).
- Add and scope design rules for selected polygons.

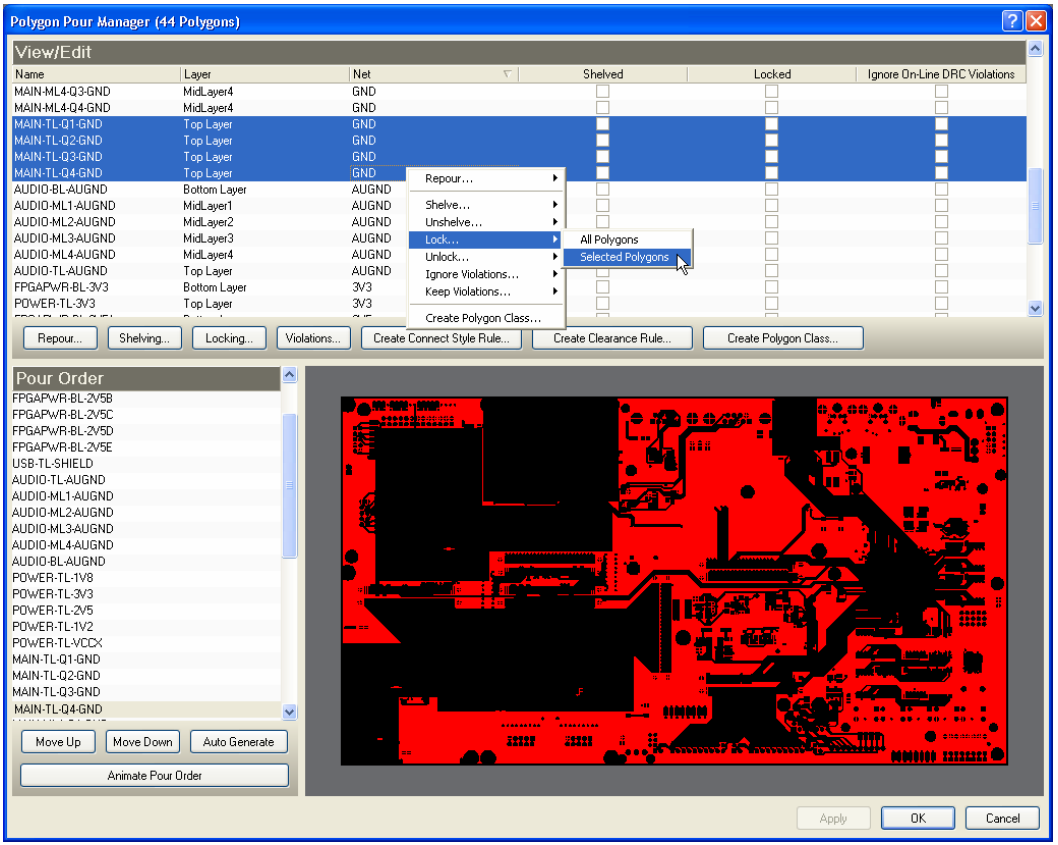


Figure 1. Polygon manager allows you to review and manage all polygons on the board.

Improved – Polygon connectivity and speed

Appreciating the importance of working with polygons in the board design process, Altium Designer 6.3 delivers enhancements to polygon connectivity and polygon pouring speeds.

It offers:

- Full support for connectivity between polygons and vias. Vias can be directly connected or thermally connected to polygons. Opening an older format file will warn of potential connection changes.
- Polygon pouring speed has been substantially improved.
- Polygon graphics performance has been improved. This benefit is delivered in both the existing and new graphics engine.

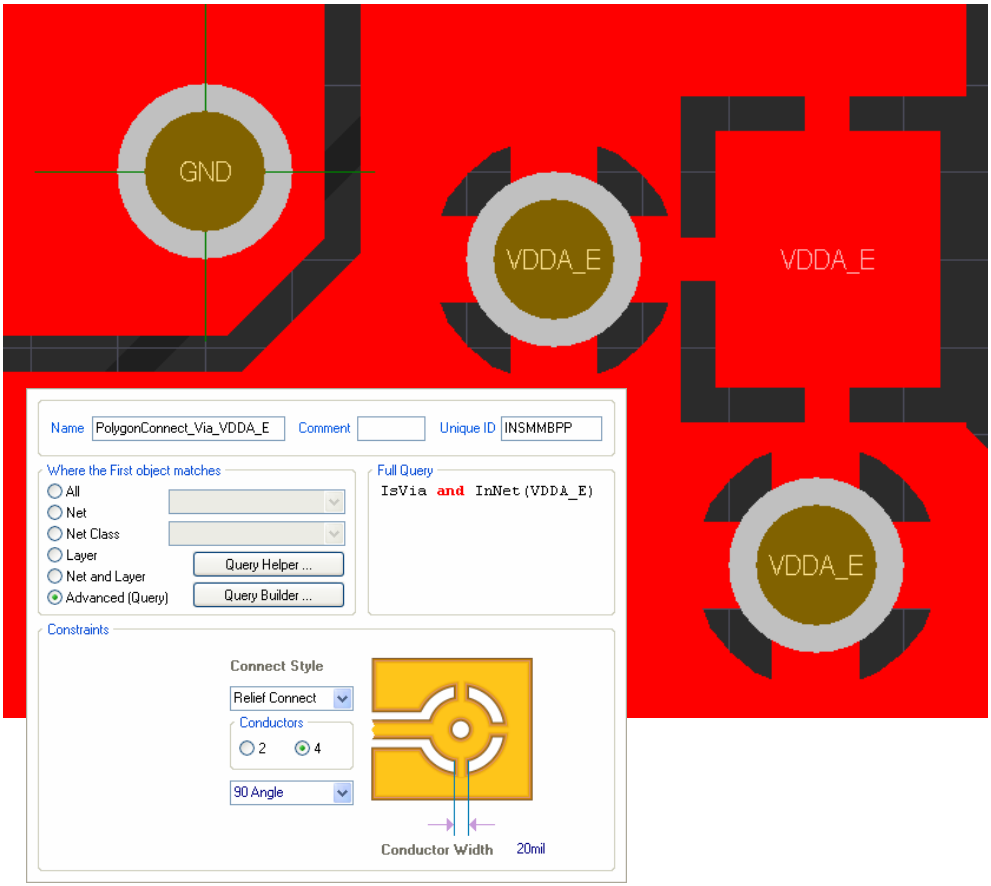


Figure 2. Control the via-to-polygon connection using Design Rules. Here the GND via is directly connected, while the VDDA_E net vias are thermally connected.

New – Place and gather multiple traces

Altium Designer 6.0 saw the addition of Smart Dragging – a powerful feature for easily moving existing track segments while maintaining the correct angles to connected segments. Smart Drag also incorporated a simple yet elegant feature for extending an unconnected track end – dragging on the end vertex adds a new segment, correctly angled away from the existing segment.

This Smart Drag capability has been substantially improved in Altium Designer 6.3 by the addition of support for multiple tracks. This allows a group of tracks to be selected and then extended as a single entity. You can use successive drags to continue to add new segments.

Taking the Smart Drag concept a step closer to becoming a bus routing tool is the new **Place » Multiple Traces** command. Using this command you can start with an unrouted component and effectively *pull* the routing out of the selected component pads. The multiple traces are then automatically gathered together, as shown in Figure 3. Simply move the cursor around as you place the multiple traces to explore various gather options. These multi-trace capabilities from pads or track ends represents the first stage in the development of a Bus Routing strategy.

Keep the following tips in mind when working with the **Multiple Traces** command:

- Rather than selecting component pads one by one, hold the **Ctrl** key as you click and drag a rectangle to select. Holding Ctrl limits the selection to the pad objects only, rather than selecting the parent component. This also works with the **Select Touching Line** and **Select Touching Rectangle** commands.
- Press the **Tab** key to open the *Bus Routing* dialog, where you set the **Bus Spacing** (track center to track center separation).
- Alternatively, use the **,** (comma) and **.** (full stop) shortcuts to interactively decrement and increment the bus spacing, in steps of the current snap grid.
- Press the **** (Backslash) to change the end alignment (once the first set of segments has been placed).
- Press the ~ (Tilda) key for a list of interactive shortcuts.

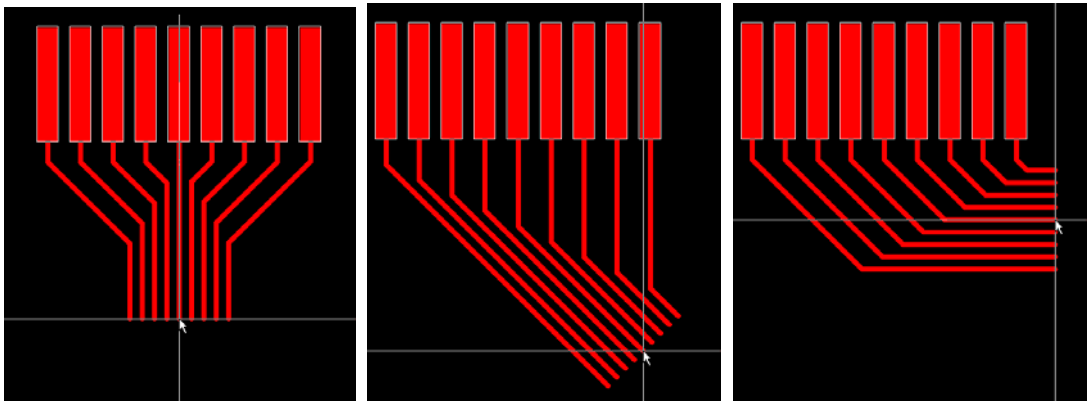


*Figure 3. Use the **Place » Multiple Traces** command to start from selected pads in an unrouted component. Move the cursor to explore gathering options.*

New – Slotted and square holes in PCB pads

Altium Designer 6.3 supports slotted and square holes in PCB pads. Slotted and square holes are defined in the redesigned PCB **Pad** dialog, giving you immediate visual feedback on the design of the pad.

Support for slotted/square holes includes:

- Round ended (NC routed) slotted holes.
- Square (punched) holes.
- Plated or un-plated slotted and square holes
- Separate drill files (NC Drill Excellon format 2) are generated for each hole kind (round, square, slot), as well as for plated and non-plated (up to 6 different drill files).
- Full support for power plane connections and clearances.
- Updated PCB Pad dialog, giving instant visual feedback on the pad design.

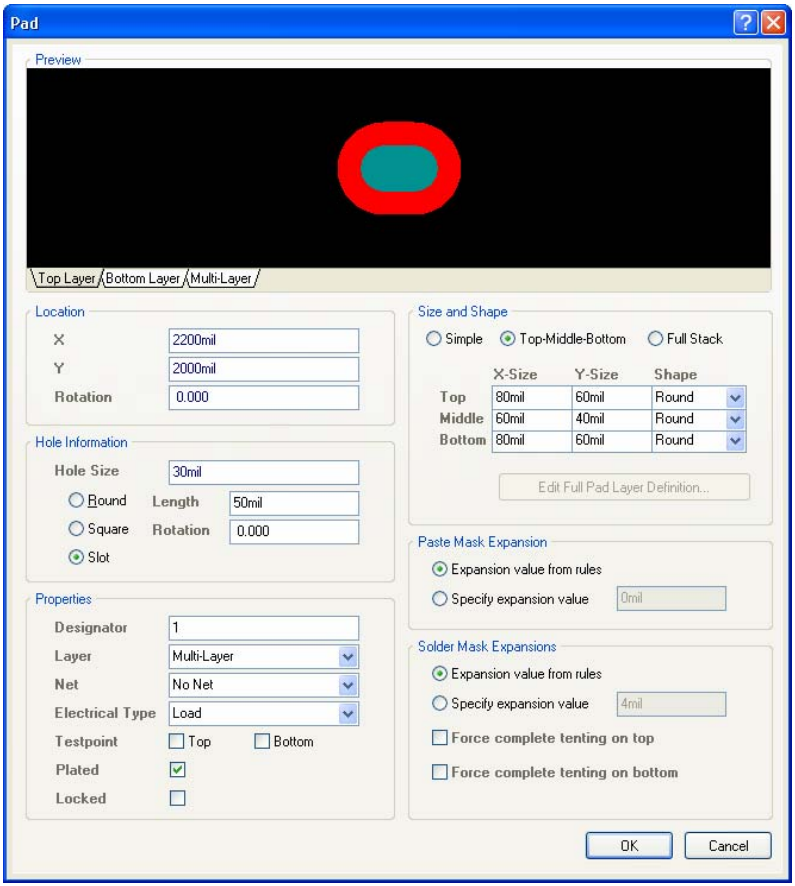


Figure 4. Create slotted or square holes in your PCB.

New – Version-controlled libraries

Version control systems provide an ideal method for managing and controlling access to electronic documents. Altium Designer 6.3 brings library management and version control together with the new version-controlled database libraries. Version-controlled database libraries are an extension of Altium Designer's database libraries, a type of library where components are placed directly from a company database.

The new version-controlled database libraries offer:

- Ease of use; all Altium Designer library components are placed directly from the **Libraries** panel – component data is read directly from the company database, with the referenced symbol and footprint being placed from the version control repository (Subversion).
- When you click to place a component from the **Libraries** panel, the component status is checked and if the symbol or footprint are not the latest then they are automatically updated from the repository.
- A new Library type, *.SVNDBLib has been added. The SVNDBLib library file is added to the **Libraries** panel and components placed directly from there (the same as the standard database libraries, *.DBLib).
- A new Wizard has been added to help restructure libraries for version control, converting multi-component libraries into single model (symbol, footprint, 3d model) files, ready for adding to the Subversion repository. Storing each model in its own file is more appropriate for version-controlled sources.
- Altium Designer models that are stored in the repository can be edited directly from Altium Designer and the updated model checked back into the repository.
- A detailed physical difference check can be performed between revisions of a model, directly from within Altium Designer.

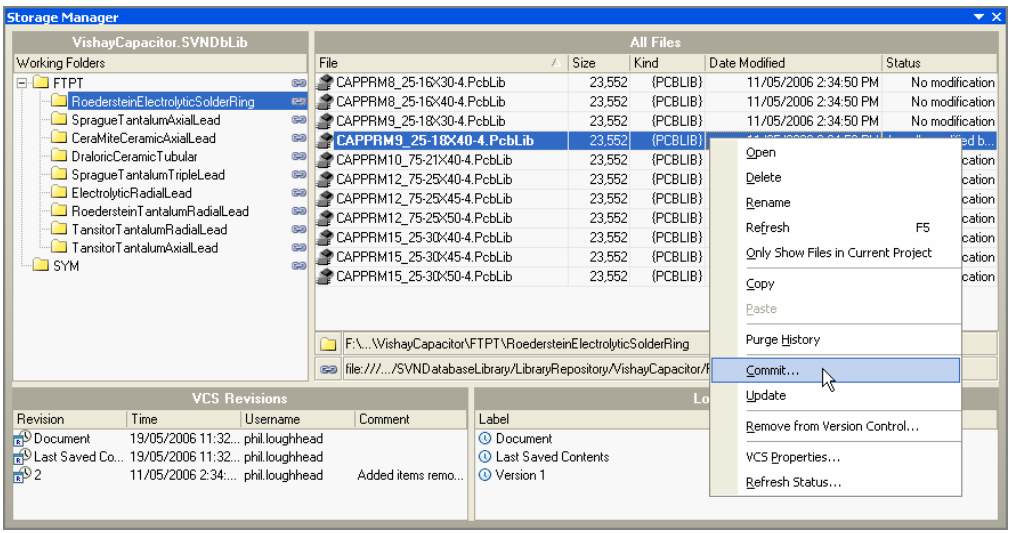


Figure 5. Use the Storage Manager to manage version-controlled models.

Adding model files to the SVN repository and managing the structure of files and folders in the repository is performed in an SVN client, such as TortoiseSVN.

For more information on working with Version-Controlled Database Libraries, refer to the application note included with the software, *Working with Version-Controlled Database Libraries*.

New – Create offline library from database library

Altium Designer's Database Libraries are an ideal choice if you want your Altium Designer components to be tightly coupled to your company database. There will be situations where direct database access is not desirable though, for example when the design needs to leave your company site, or you have contract designers and you prefer they work from secure integrated libraries. With Altium Designer 6.3's new **Offline Integrated Library Maker** wizard you can achieve this.

Use the new **Offline Integrated Library Maker** to compile an integrated library directly from a database library, or a Subversion-based database library. The wizard will build Altium Designer schematic and PCB libraries, create a new library package and compile the portable integrated library – creating an integrated library for each table in the database.

Select the **Tools » Offline Integrated Library Maker** from the DBLib or SVNDBLib menus to run the wizard.

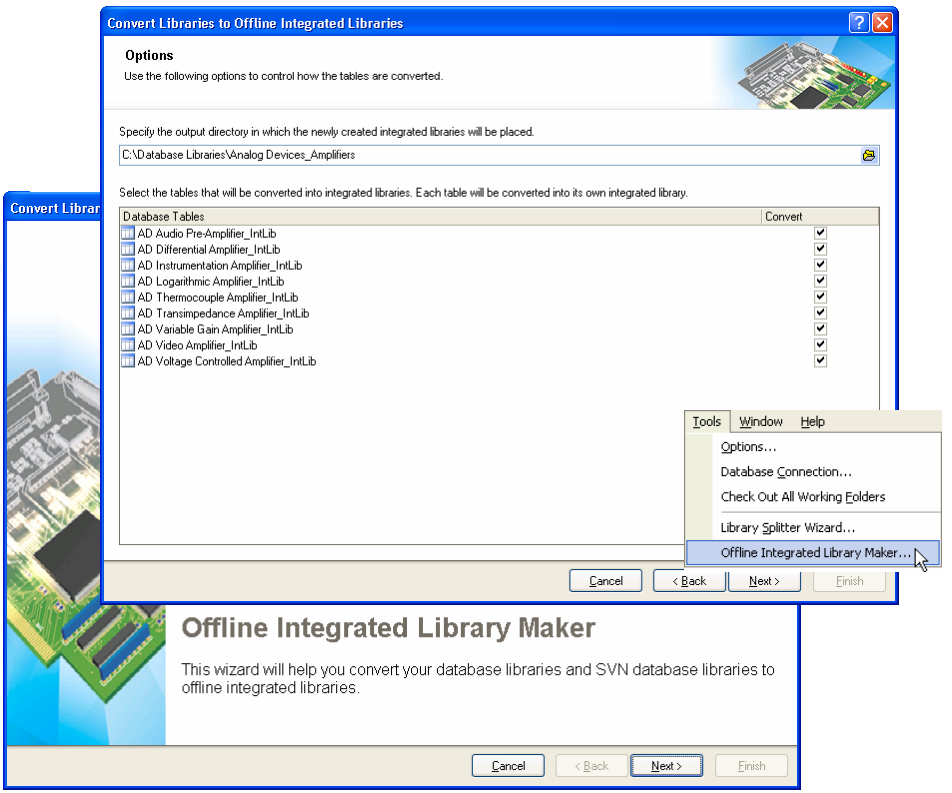


Figure 6. Create a portable offline library from your company database library.

New – IPC compliant board-level libraries

Altium's Library Development Center is in the process of developing IPC-7350 series footprint libraries (current surface mount footprints are created to IPC-SM-782).

- These footprints will be supplied in both PCB footprint library format (*.PcbLib) and also used across the manufacturer-based integrated libraries (*.IntLib) included with Altium Designer, where appropriate. Check the \Altium Designer 6\Library\Pcb\IPC-7530 Series folder to see which footprints are currently available.
- As specified by IPC-7351 and where applicable, each component will have three footprint variants denoted *Nominal*, *Least* and *Maximum*. Footprints are named with the appropriate letter at the end of the name. The default for each component is the Nominal (_N) footprint, this can be changed to the Least (_L) or Maximum (_M) in the Component Properties dialog in the schematic editor.
- As specified in IPC-7351, each footprint includes an Assembly layer (Mechanical13) and Courtyard layer (Mechanical15).

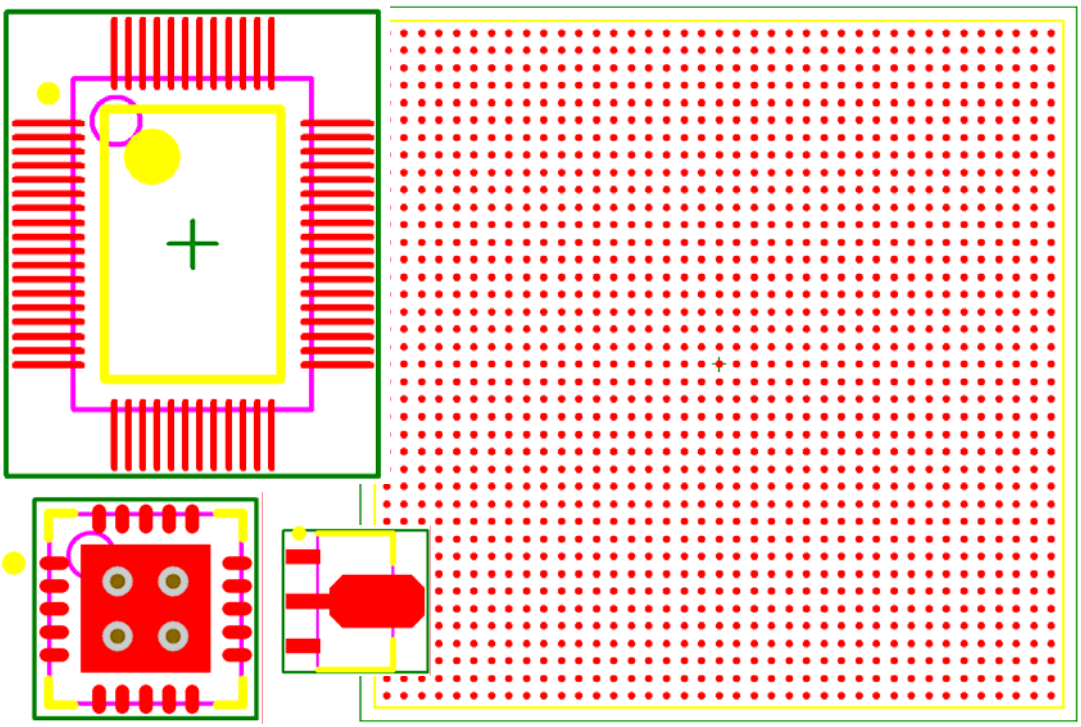


Figure 7. The new IPC-7350 series footprints come in 3 variants (Nominal, Least and Maximum), and include assembly and courtyard details.

New – IPC Footprint Wizard

The new IPC Footprint Wizard creates IPC-compliant component footprints. Rather than working from footprint dimensions, the IPC Footprint Wizard uses dimensional information from the component itself, in accordance with the algorithms released by the IPC.

In accordance with the IPC standard it also supports three footprint variants, tailored to suit the board density. With its initial release the wizard supports BGA, QFP and SOIC footprints. Support for other package kinds will be added in future Altium Designer updates.

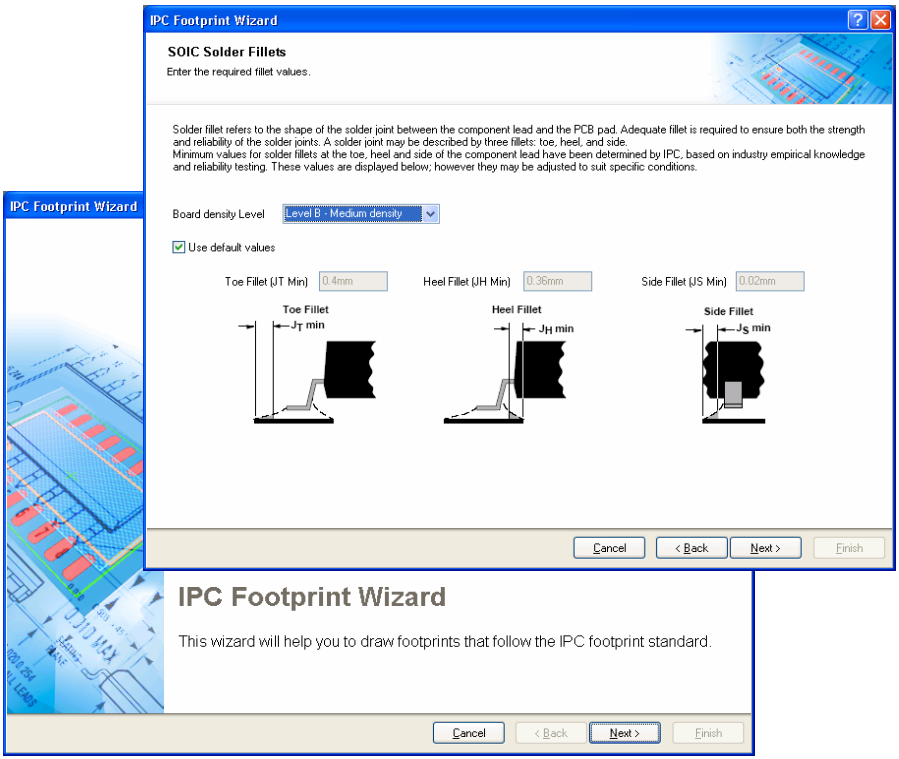
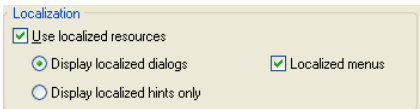


Figure 8. Quickly create IPC-compliant component footprints from the component dimensions in the new IPC Footprint Wizard.

New – Traditional Chinese localization support

Altium Designer has in-built support for detecting and working in the language locale of the Windows installation. Supported languages include French, German, Japanese and Simplified Chinese – all of these have been extensively reviewed and updated.



New to Altium Designer 6.3 is language localization support for Traditional Chinese, allowing the dialogs, menus and hints to be presented in that language. Set the **Localization** options in the *Preferences* dialog.

New – PADS® library importer

A new importer has been added to the **Import Wizard** for importing PADS® footprint (Pattern) libraries. ASCII library files up to PADS PowerPCB® version 2005 (SP0) can be imported.

Improved – OrCAD® importer

The OrCAD® importer now fully supports importing OrCAD® design components that include simulation data. Importing of both simulation-ready schematics and schematic libraries is supported.

New – PADS®/OrCAD® importer

Designers moving from legacy systems, such as an OrCAD® schematic + PADS® PCB editor combination can now easily transfer their valuable libraries and design files into Altium Designer.

The new importer, accessed via the **Import Wizard**, imports the OrCAD® schematic symbols and PADS® footprints (Patterns), adding them to a new Altium Designer Library Package ready for compiling into an Altium Designer integrated library. The importer also supports importing OrCAD® schematics and PADS® PCB documents in a single operation to create an Altium Designer PCB project.

This importer provides a straight-forward and robust methodology for managing the transfer of legacy designs into Altium Designer.

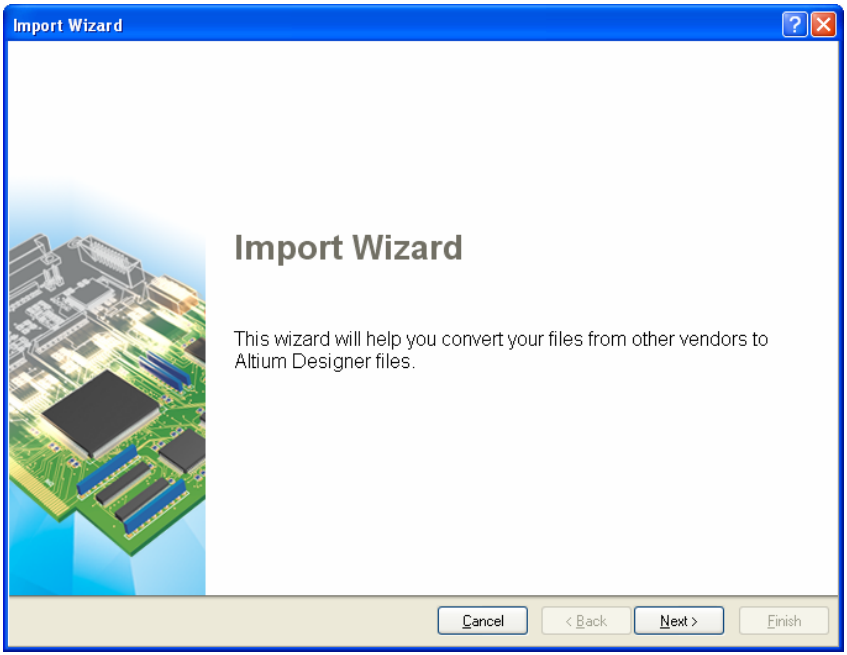


Figure 9. The Import Wizard can import design and library files for various design tools.

New – Slice PCB tracks

A tool that helps strengthen Altium Designer's general editing capabilities is the new Track Slicer. The Track Slicer provides an easy mechanism for cutting one or more track segments into two. Use the Track Slicer to slice one or more tracks on the current layer, or all layers.

To use the Track Slicer:

- Choose **Slice Track** from the **Edit** submenu (press **E** to display), then move the mouse over existing tracks for a visual indication of which tracks are to be cut.
- Press the **Spacebar** to lock the Slicer to vertical/horizontal/45 degrees.
- Press the **,** (comma) **.** (full stop) **/** (slash) or **M** keys to select the segments on the left side, right side, both sides, or to not select any segments.
- Press the **Tab** key to configure the Slicer.
- Press the **Tilda** key (**~**) for a full list of interactive shortcuts.

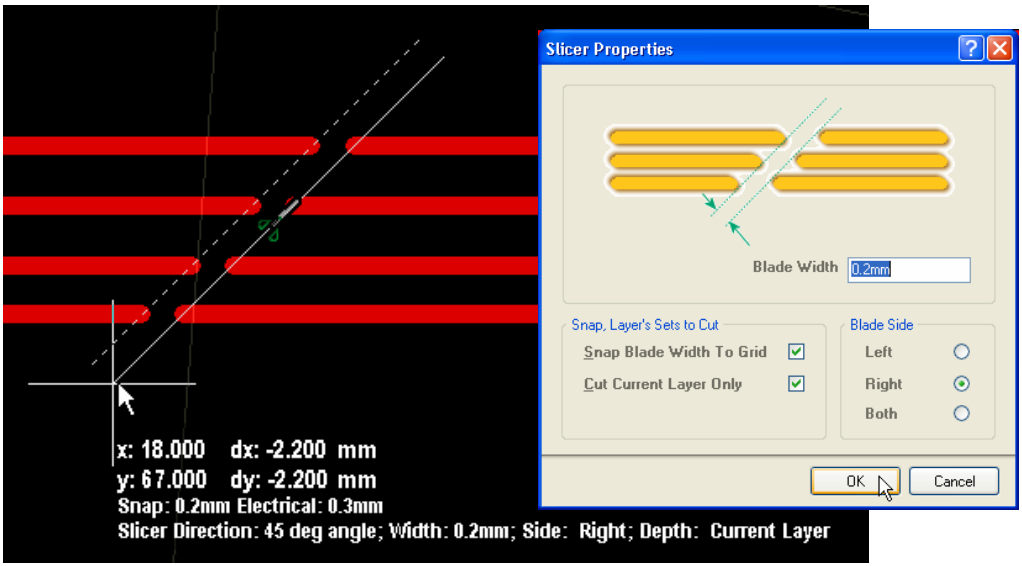


*Figure 10. Use the Track Slicer to break track segments into two, press **Tilda** (~) to see the full range of options.*

New – Subnet jumpers feature

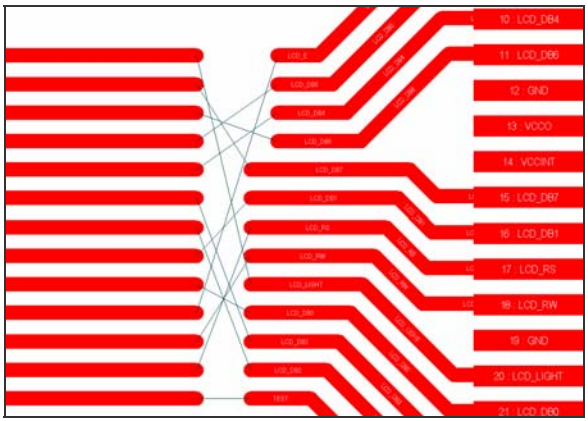
One of the great strengths of an FPGA-based design is that the routing challenge can be moved from the PCB to inside the FPGA, potentially resulting in fewer routing layers and a simpler, cheaper and more reliable PCB. For this to be a reality the design system must support both PCB-driven and FPGA-driven pin swaps, with full synchronization between the PCB and FPGA designs – Altium Designer provides this high-level of support.

The best way to exploit this advantage is to route the board in an iterative process – escape routing out of the FPGA, then routing incoming signal buses toward the FPGA. Once the incoming and outgoing routes are near each other it is a straightforward process of performing interactive or automatic pin swaps on the FPGA escape routing to *de-tangle* the connection lines, ready to complete the routing.

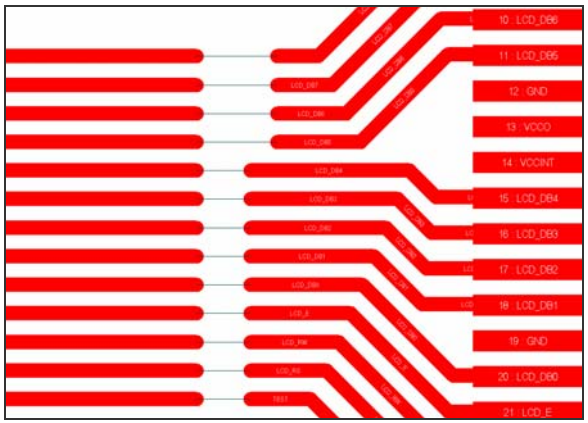
With the new subnet jumper feature you no longer need to manually complete the short routing segments. Selecting **Add Subnet Jumpers** from the **Autoroute** menu will detect any direct (horizontal, vertical, diagonal) connection line shorter than the specified distance, then automatically add a track segment of the correct width to complete the route.

And, since the reality is that design does not happen in a simple, linear fashion, you have full support to remove the subnet jumpers when you need to re-adjust the FPGA pinouts and perform further pin swaps, to again *de-tangle* the connection lines.

Use the **Remove Subnet Jumpers** command to remove the jumpers, and **Add Subnet Jumpers** to recreate them.



Route from both sides to create the cleanest routing.



Use the pin swapping features to de-tangle the connection lines.

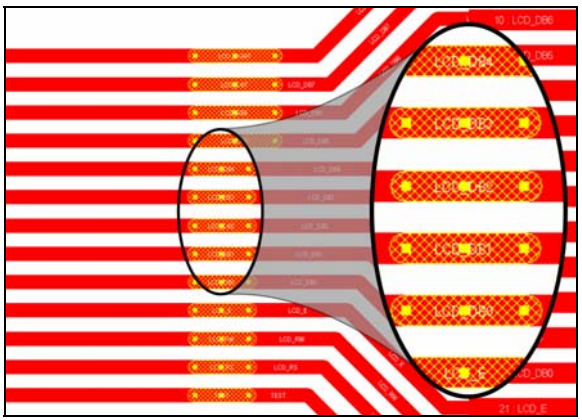


Figure 11. Run the Subnet jumper command to automatically add short jumpers that complete the routing.

New – PCB selection tools

Selection is a core function in the designer's editing toolset, being used constantly during the design process. New selection tools in the PCB editor greatly simplify the process of building up a selection set. The new selection features can be accessed from the **Selection** submenu (press **S** to display) and include:

- **Select Touching Rectangle** – any object touched by the selection rectangle will be selected.
- **Select Touching Line** – any object touched by the selection line will be selected.
- Hold the Shift key after choosing the command to add to an existing selection set.

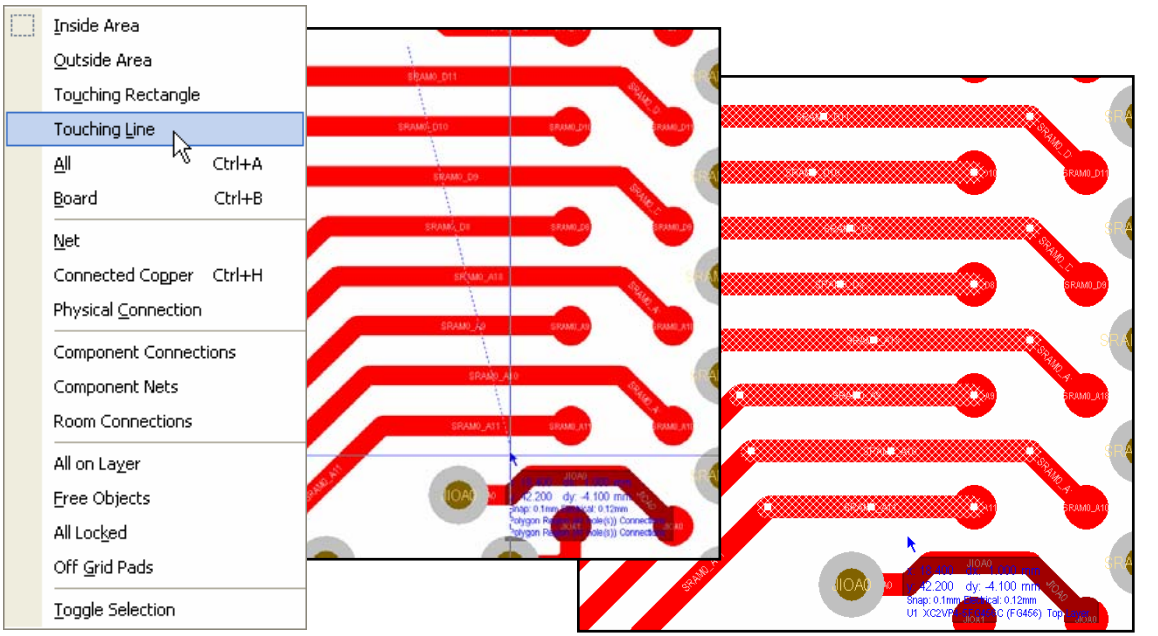


Figure 12. Press S to access the new Select Touching Line and Touching Rectangle commands.

New – STEP (3D File Format) export

STEP, the **ST**andard for the **E**xchange of **P**roduct model data is becoming a preferred standard for ECAD to MCAD data exchange. Altium Designer 6.3 includes a new STEP export capability, generating a 3D STEP format file ready for import into your preferred mechanical CAD system.

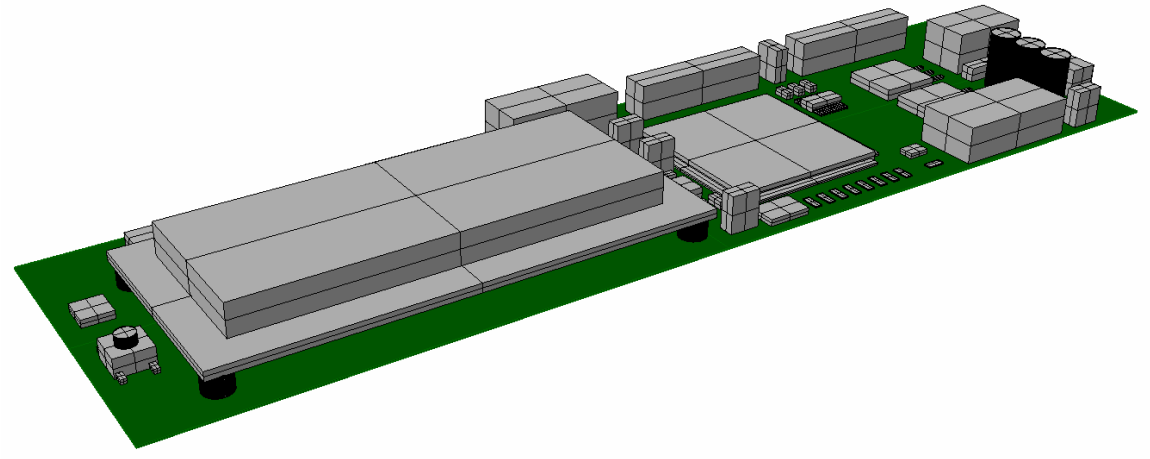


Figure 13. Export the board in the STEP format, and import to your preferred mechanical CAD tool.

New – Signal Integrity examples

New examples demonstrating the use and power of Altium Designer's Signal Integrity analysis capabilities have been added. They include examples of Altium Designer's support for:

- Signal Integrity analysis of a design using differential pairs.
- Signal Integrity analysis of a design with a *programmed* FPGA – correct pin models are automatically applied to the FPGA to support the chosen I/O type, I/O standard, slew rate and drive strength.

Improved – Differential pair interactive router

Today differential pairs is the preferred method of managing the integrity of high-speed signals. Interactive differential pair routing has been improved in Altium Designer 6.3 by the addition of:

- Improved gathering of signals in the pair – pad exits automatically center with a short straight+diagonal route, control the behavior by positioning the cursor.
- Detailed Heads Up information, including current delta (difference in routed pair length) and applicable Delta in design rules.

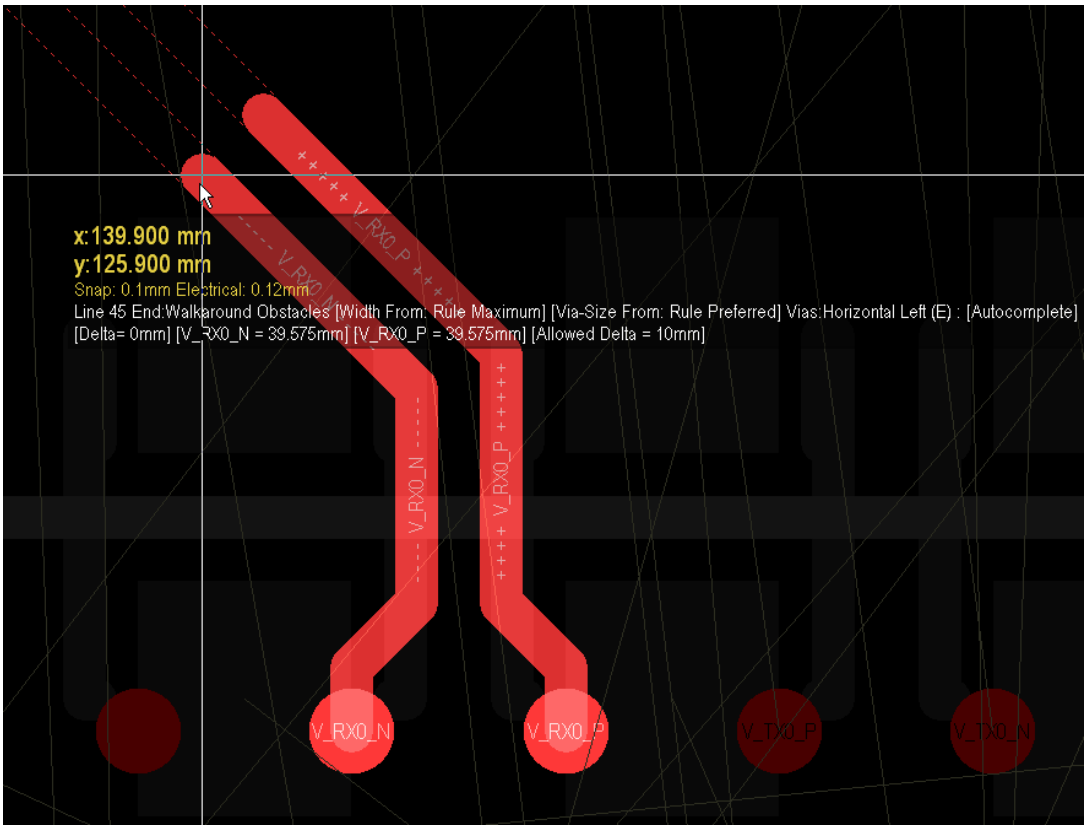
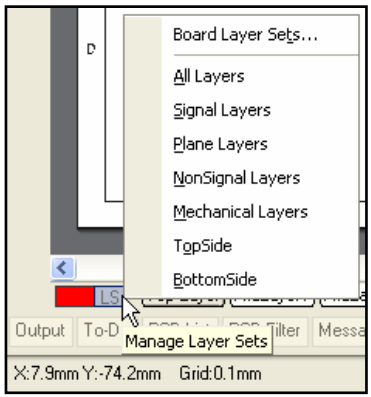


Figure 14. Improvements to the differential pair interactive router give neater and more efficient differential pair routing.

New – PCB Layer Sets

A typical board design could include 8 signal layers, 4 plane layers and 10 mechanical layers, as well as the top and bottom silkscreen and ancillary layers, such as solder and paste masks. Layer sets are an ideal way of managing the display of this large number of layers.



PCB layer sets can be defined in the **Layer Sets Manager** dialog (**Design » Manage Layer Sets** menu). Any number of layer sets can be defined, and each can include any of the layers available in the board design.

To toggle the workspace to display a different set of layers, use the **Layer Set** control at the bottom left of the workspace. The popup menu will automatically present your current list of Layer Sets. Include the & character in the Layer Set Name to define the following character as an accelerator key.

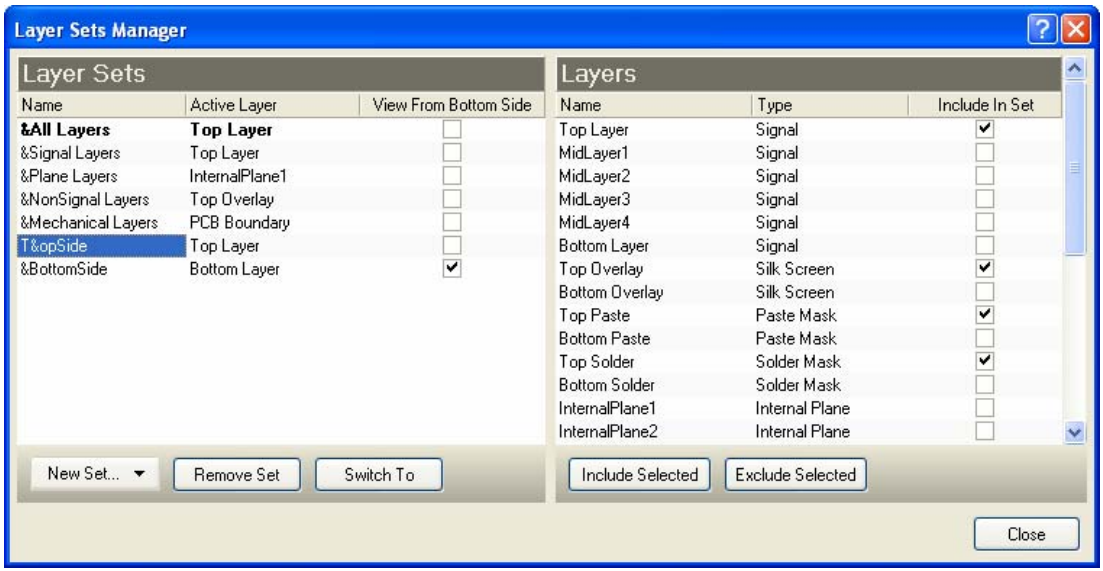


Figure 15. Define Layer sets in your board, and use them to quickly switch between different sets of displayed layers.

New – PCB file versioning

To support the introduction of new features, such as slotted holes in PCB pads, the PCB file format has changed. As part of this release an intelligent file versioning system has been introduced, where, going forward, all future releases will be able to intelligently handle PCB files that have a newer format than the format created by that release.

This release also supports more detailed warnings about potential design changes caused by file format or feature enhancements, such as the via-to-polygon connection warning that occur when an older version file is opened in Altium Designer 6.3.

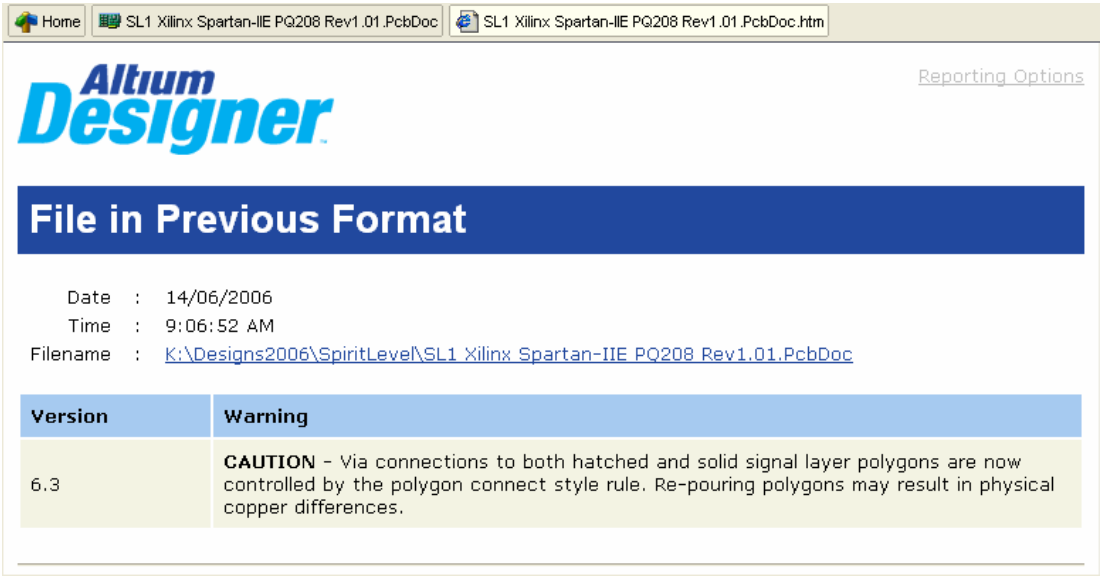


Figure 16. Details of file version support is automatically reported when an older format file is opened.

New – Managing uninstall information

Altium Designer updates are performed via the internet, using a patching technology that applies updates to the Altium Designer installation files. To ensure that you can uninstall any of the updates that you have applied, backup copies of all modified files are stored on your hard drive.

These backup files can be removed if required, open the License Management page (**DXP » Licensing**), expand the applied update and click the *Remove Uninstall Info* hyperlink. Note that update information is removed separately for each update, allowing you to manage which updates are still uninstallable and which are not. This process is not reversible, once you have removed the uninstall information you will no longer be able to uninstall that update.

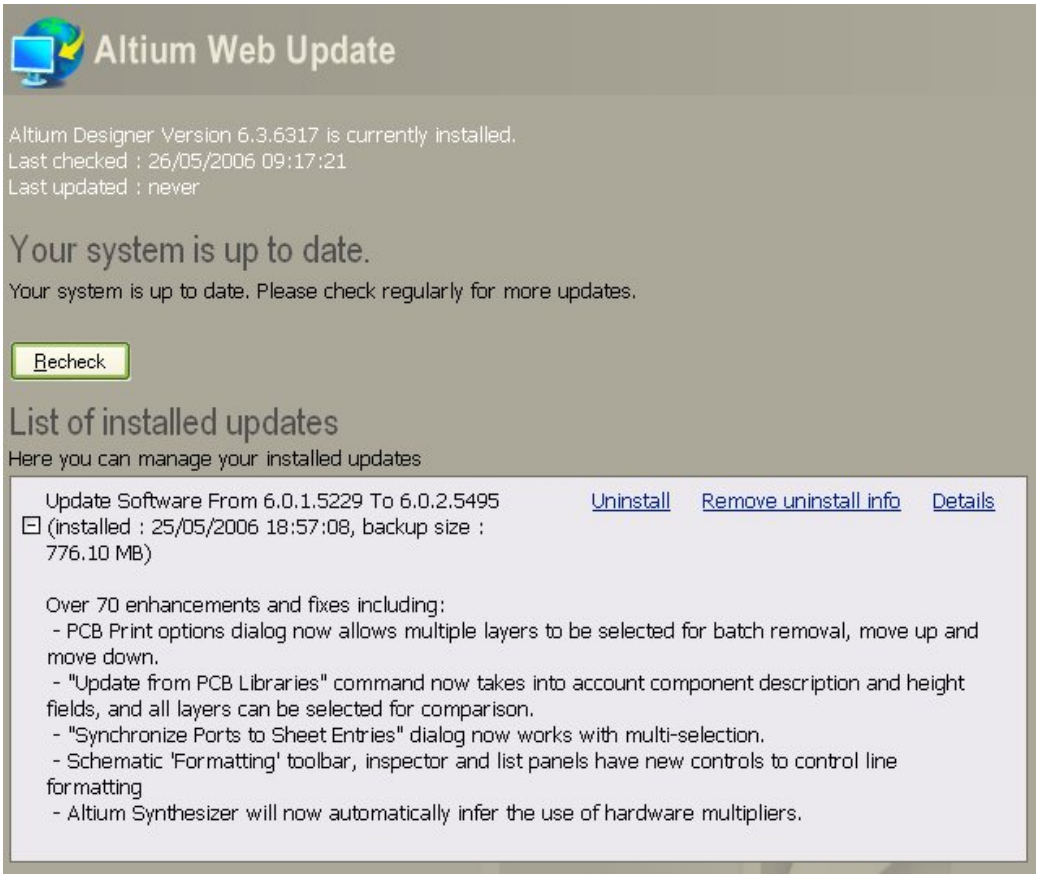


Figure 17. Use the Remove Uninstall Info feature to remove the backup files from your hard drive.

New – Altera® Nios® II support

If the Altera® Nios® is your embedded processor of choice, then you will be pleased to hear that Altium Designer 6.3 brings full embedded tool chain support for the latest range of Nios II embedded processors.

Working in Altium Designer's professional coding environment, your code is compiled by the TASKING Viper compiler, producing highly optimized application code that is substantially more compact than that produced by the GNU compiler. Debug your code running on the target Altera FPGA directly from within Altium Designer – on an Altium NanoBoard, a third-party FPGA development board, or directly on your product board.

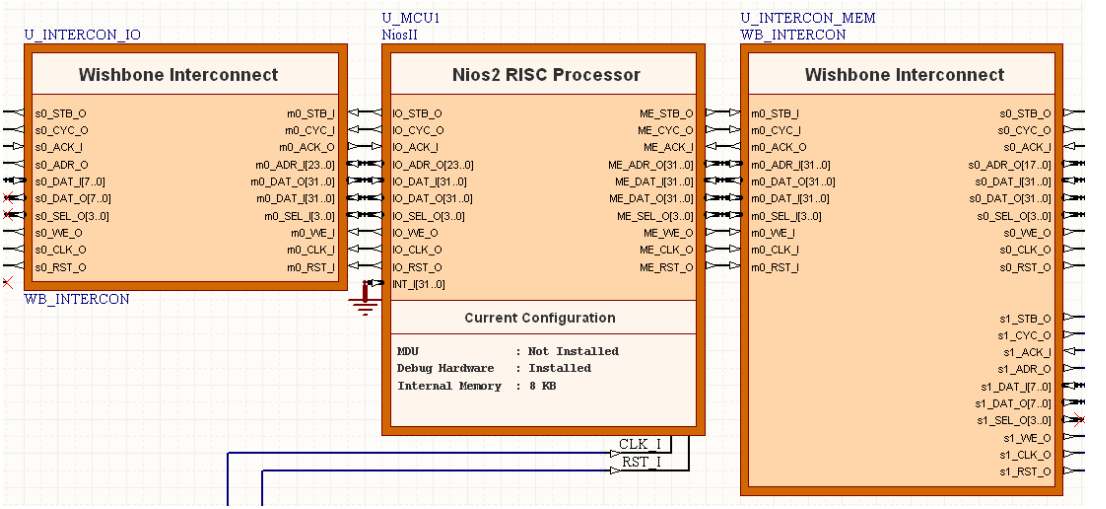
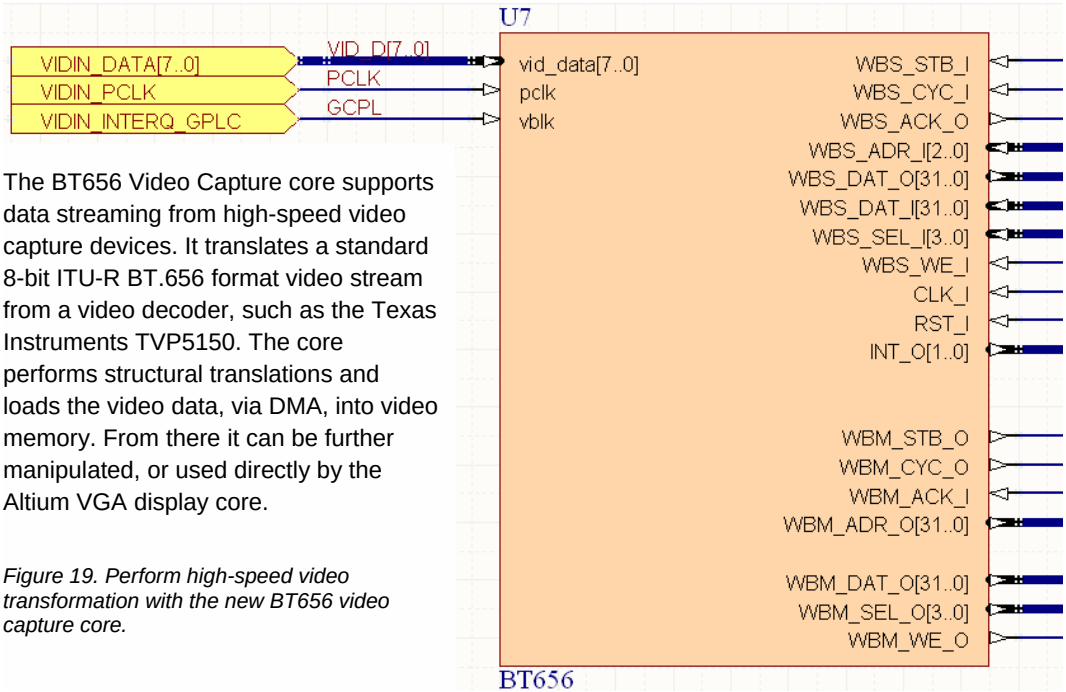


Figure 18. Full embedded toolchain support for the latest Altera Nios II processor.

New – BT656 Video capture core



The BT656 Video Capture core supports data streaming from high-speed video capture devices. It translates a standard 8-bit ITU-R BT.656 format video stream from a video decoder, such as the Texas Instruments TVP5150. The core performs structural translations and loads the video data, via DMA, into video memory. From there it can be further manipulated, or used directly by the Altium VGA display core.

Figure 19. Perform high-speed video transformation with the new BT656 video capture core.

New – I2S Audio streaming core

I2S is a popular serial bus designed for digital audio. The new I2S core provides a convenient wishbone compliant interface for streaming data to or from a high-speed audio codec. The core performs the serial to parallel conversion required to directly interface high-speed serial audio to a microprocessor.

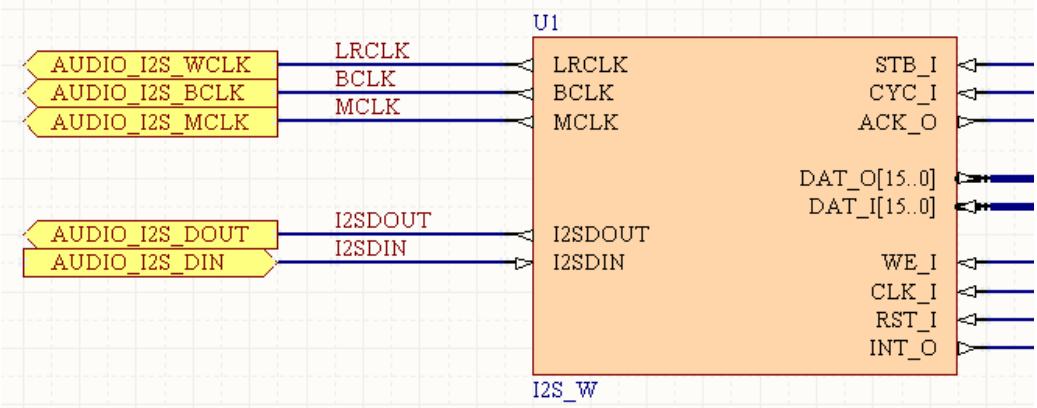


Figure 20. Stream high-speed serial audio data into your FPGA design with the new I2S core.

Improved – SDRAM support

Using SDRAM memory in Altium Designer 6.3 is now as easy as using SRAM or Block RAM memory. The memory controller core has been updated to allow support for SDRAM devices. This support is configurable to support the wide variety of these devices available.

Improved – ProASIC3® support

Support for the Actel® ProASIC3® range of devices has been enhanced. You can now use the Altium Designer TSK3000 32-bit RISC processor in your ProASIC3-based design. The ProASIC3's on-chip PLL is also supported.

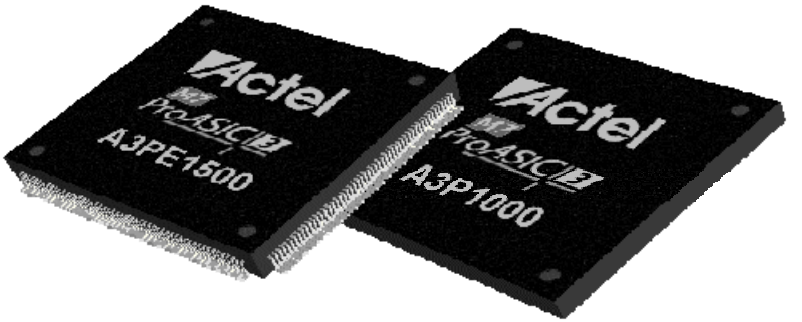


Figure 21. Use the TSK3000 RISC processor in your ProASIC-based FPGA design.

New – Lattice XP® support

Support for the Lattice XP® range of devices has been added. You can now use the Altium Designer environment to work with these powerful and flexible Lattice devices.

Figure 22. Altium Designer now supports the Lattice XP series of FPGAs.

Improved – ARM®-based Sharp BlueStreak® support

Altium Designer's support for the Sharp BlueStreak® processors has been extended to include all the available ARM®-7 based Sharp devices. The supported devices include:

- Sharp LH754xx series (ARM7TDMI)
- Sharp LH795xx series (ARM720T)

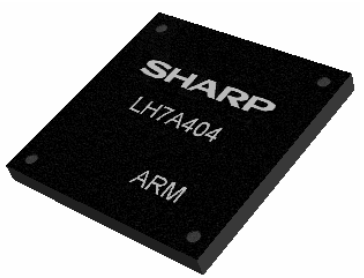


Figure 23. Full toolchain and device support for the Sharp BlueStreak.

Improved – Embedded system editing performance

Altium Designer has improved responsiveness when large embedded projects and project files are opened. Enhancements focus on the following areas:

- Opening large source documents
- Loading libraries
- Switching documents
- Projects that are linked to a VCS
- Panel responsiveness.

```
        break;
    case 2: /* want to calibrate wind direction */
        if (menu_update)
        {
            lcd_clear_screen();
            puts_lcd("Cal: direction");
            lcd_gotoxy( 0, 1 );
            puts_lcd("Ok     next  Esc");
            menu_update = 0;
        }
        switch (key)
        {
            case 0x01: /* OK */
                menu_state = 4;
                menu_update = 1;
                break;
            case 0x03: /* next */
                menu_state = 1;
                menu_update = 1;
                break;
            case 0x04: /* Esc */
                menu_state = -1;
                break;
            default:
                break;
        }
        break;
    case 3: /* calibrate temperature */
        cal_temp();
        menu_state = 0;
        menu_update = 1;
        break;
    case 4: /* calibrate direction */
        cal_dir();
        menu_state = 0;
        menu_update = 1;
        break;
```

Figure 24. Embedded system development has been enhanced by improved system responsiveness.

New – Device-Software-Framework (DSF)

A new Device Software Framework (DFS) for embedded projects has been added in Altium Designer 6.3. The DSF has been designed to simplify embedded application development.

The DSF delivers:

- A Low Level Peripheral Interface (LLPI) layer, with tight integration between the FPGA peripherals and their driver code.
- A Processor Abstraction Layer (PAL) greatly simplifies the portability of your embedded application across all target processors, both embedded and discrete 32-bit, supported by Altium Designer.
- While the DSF 'abstracts away' most of the physical layer from the embedded application development process, you continue to have direct access to the processor's interrupt system.

All of the sample embedded projects included with Altium Designer have been upgraded to use the new DSF as part of the Altium Designer 6.3 release.

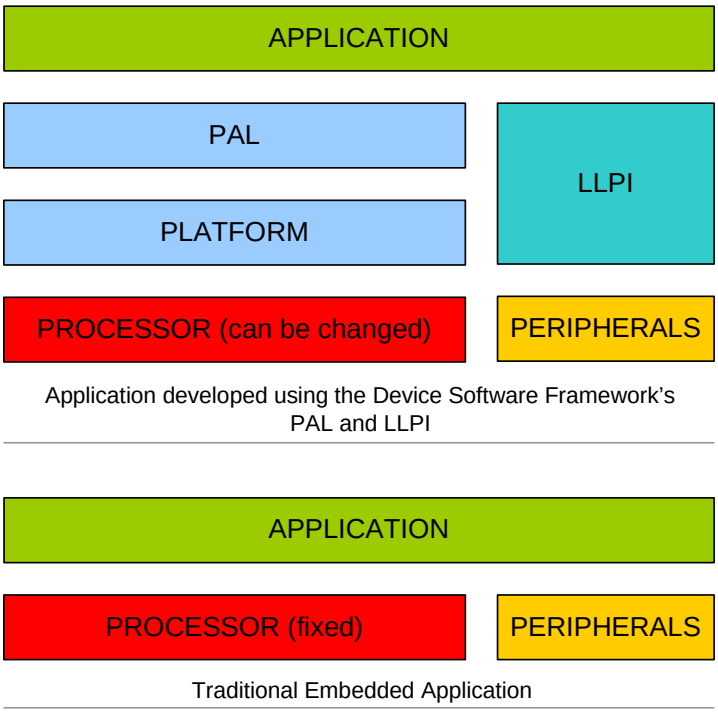


Figure 25. The DSF allows the embedded application to be portable between processors, instead of being tightly coupled to the hardware, as it is in the traditional approach.

New – Logging in license server

Altium Designer can be licensed as a standalone product, or to use a network license. Network licenses are managed by the Altium Designer License Server, which has been upgraded to support tracking license usage by user name, and machine name.

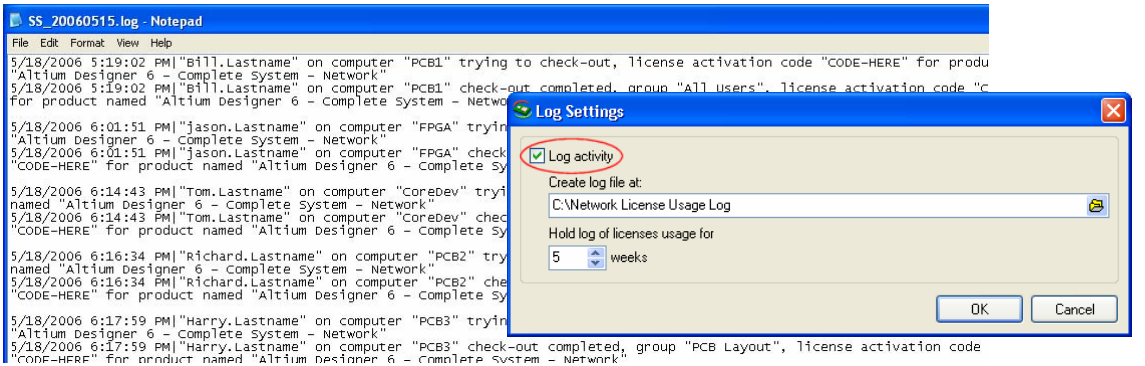
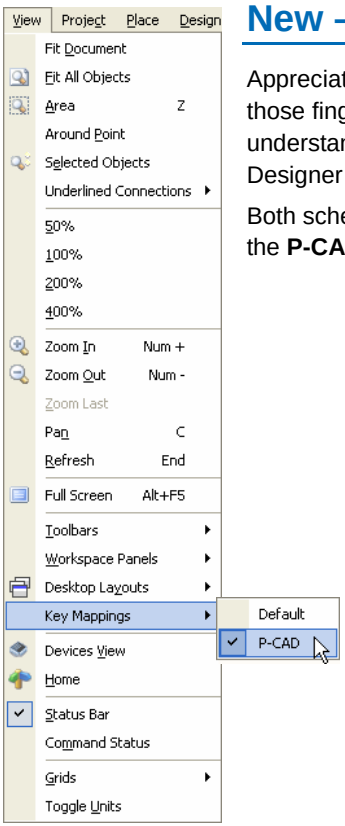


Figure 26. Track network license usage with the new license logging feature.



New – P-CAD hotkey support

Appreciating that learning a new design environment is as much about retraining those fingers that press shortcuts faster than you can recall them, as it is about understanding the conceptual differences between design environments, Altium Designer 6.3 includes support for P-CAD shortcut keys.

Both schematic editor and PCB editor, P-CAD shortcuts are supported – select the **P-CAD Key Mappings** from the **View** menu to enable them.

New – Project packager

An Altium Designer project can include many files, including source files, libraries, reports, documentation, data sheets, project PDFs, manufacturing files, and more. The new Wizard-based Project Packager greatly simplifies the task of managing this large fileset. Guided by you in the easy-to-use Wizard, the Project Packager gathers and packages the project into a portable ZIP file.

The Project Packager supports:

- Any situation where your project must be moved. For example, moving a project from one site to another, or backing up your project for secure storage.
- Packaging a complete Altium Designer project tree – ideal for linked PCB + FPGA + embedded projects.
- Packaging a complete Altium Designer workspace – ideal for designers that include all the board designs destined for a company product in a single workspace.
- Managing how directory paths are handled during packaging.
- Managing how files outside the project folder are handled during packaging.
- Including/excluding generated files, such as reports, in the project package.
- Including/excluding history files (files created by Altium Designer's built in file history/restore system).

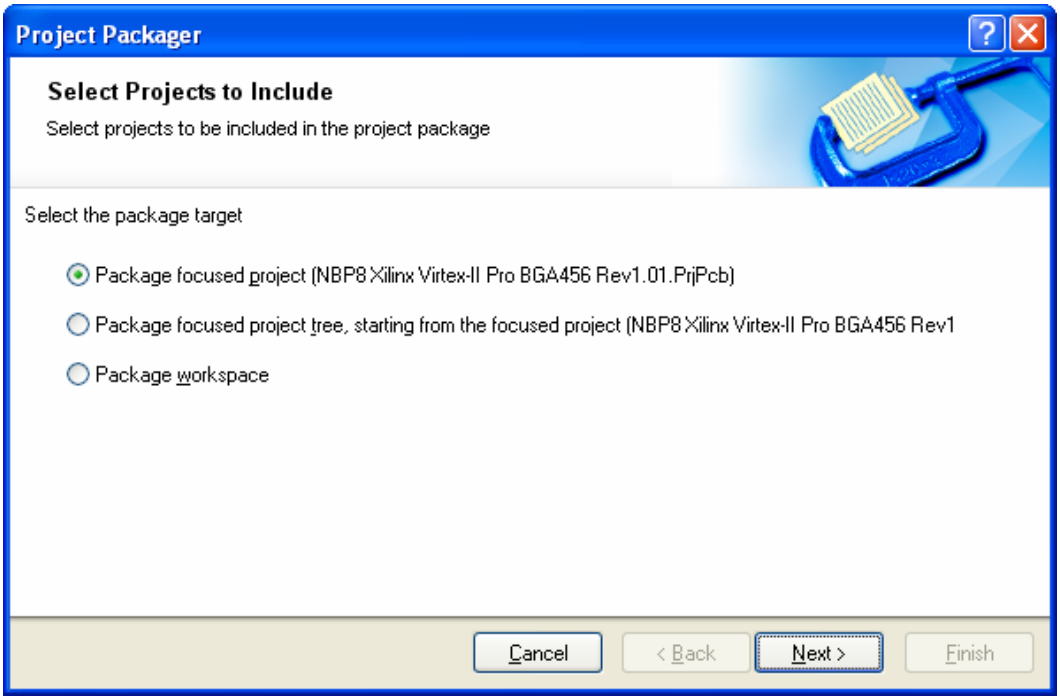


Figure 27. Use the Project Packager to pack the project or the workspace, ready to be moved.

Revision History

Date	Version No.	Revision
20-Jun-2006	1.0	Altium Designer 6.3 release