What's New in Altium Designer 6.7

Summary

Altium Designer 6.7 continues to improve your productivity delivering features for high-speed design such as Interactive Length Tuning and PCB Layer Tabs. New library tools and a variety of new capabilities strengthen Altium Designer as a unified electronic product development solution.

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You need full control over all aspects of your design in an intuitive and productive environment. Altium Designer 6.7 brings some noteworthy enhancements to the PCB and FPGA design process. A number of other areas of the software have been streamlined for substantial productivity improvements in areas once considered time-consuming.

Physical platform design has been improved further to support the complex multi-layer board densities and high-speed signaling found in today's designs. A greater level of control over the routing process is accomplished with Interactive Length Tuning. Making sense of a visually-crowded workspace is made even easier with PCB Layer Tabs and a new Hole Size Editor. Delivering output for designs that contain embedded board arrays is improved with redesigned and updated output dialogs for Gerber and ODB++.

You need to be able to fully exploit the potential offered by today's large-capacity programmable devices. Embedded tools support for FPGA development is expanded to allow you to take advantage of core technology from your favorite third party vendors with the new FPGA Third Party Core Import Wizard.

You need better ways to manage the design process. It's significantly easier with this release to do design debugging in large complex pieces of code with new Text Editor Options and Grid Paste Tools.

These are just a few of the new features in the release of Altium Designer 6.7. Read on to learn more about what's the new and improved electronic product development technology.

Seeing is believing – watch demos of Altium Designer 6.7

Altium's DEMOcenter gives you the opportunity to walk through the extensive design capabilities of Altium Designer featured as individual demos, each only taking a couple of minutes, making this a quick and easy way for you to browse the areas of most importance to you.

If you'd like to learn more about updates in Altium Designer 6.7, as well as watch short videos about some of the exciting new features, then visit the **What's New in Altium Designer 6.7** page on the website and enjoy the action. Click the link below to read more and watch the videos.

www.altium.com/Evaluate/DEMOcenter/WhatsnewinAltiumDesigner

New – Hole Size Editor

An additional **Hole Size Editor** mode has been added to the **PCB** panel, providing a greater level of visibility and management of drill sizes on your boards. Various criteria can be defined to allow you to zero-in on and display only holes of interest. Some of these criteria allow you to consider only:

- Holes associated with pads and/or vias.
- Plated and/or non-plated holes.
- Holes associated with pads/vias that are part of a component and/or free.
- All hole types, or only round, square or slotted holes.
- Selected and/or unselected holes.
- Only the layer-pairs of interest.

Once the criteria defined, the panel lists all unique hole definitions and subsequently the pads and/or vias associated with each. Click on a **Unique Hole** entry to view the instances of that hole in the design in accordance with your defined highlighting options (Zoom, Mask, and Select) for the panel.

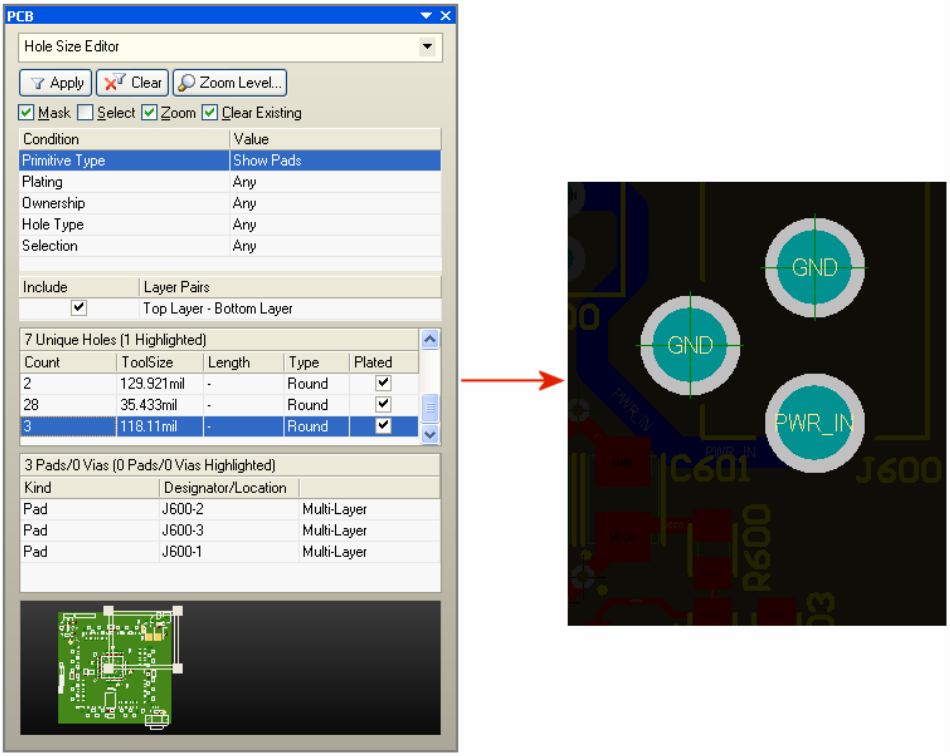


Figure 1. Locate and edit holes of interest quickly and efficiently in dense boards from within the PCB panel.

Editing of a hole entry can then be carried out directly in the panel. Simply click in the relevant field to edit the hole's Size (ToolSize), Length, Type and whether it is to be plated or not.

Pad or via properties can be accessed directly – double-click on an entry to access the associated properties dialog.

Improved – PCB Layer Tabs

Moving around a large or complex design can often mean lots of layer switching. You'll appreciate the fact that the **PCB Layer** tabs are improved to help you better manage, navigate and inspect layers in your design.

Enhancements include:

- Color-coded **Layer** tabs allow easier identification of layers and their content.
- Current layer drawn name can be intuitively bolded for quicker identification.
- Shortened layer names on tabs can give you more control over managing your space with less scrolling and searching for hidden layer tabs.
- Commonly-used commands for layer-related dialogs available through right-click menu.
- Layer visibility adjusted through right-click menu commands **Show Layers** and **Hide Layers**.
- Conveniently accessed using the same interface as net highlighting.

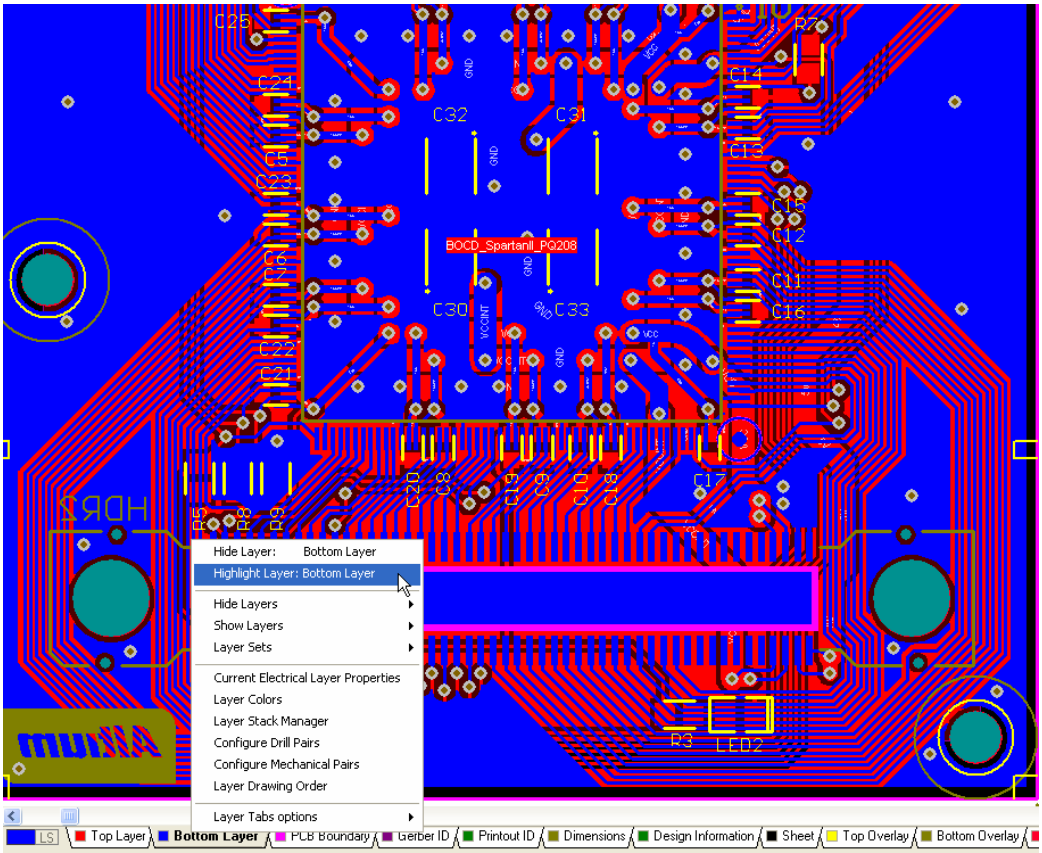


*Figure 2. Layers can be highlighted through right-click menu commands as shown here, or through shortcut keys on the layer tabs (**Ctrl+Click** highlights layer content, **Ctrl+Shift+Click** increments highlighting, and **Ctrl+Alt+Mouse** hovers highlight layer).*

New – Interactive Length Tuning

Matching route lengths is a standard technique for maintaining data integrity in a high-speed digital system, and an essential ingredient of differential pair routing. **Interactive Length Tuning** allows a dynamic means of optimizing and controlling nets lengths by allowing variable amplitude patterns to be inserted according to the available space, rules, and obstacles in your design. Launched from the **Tools** menu, it can be based on design rules, properties of the net, or values you enter into a dialog.

Once you have launched the command, click on the routed net and move the mouse along the net to add tuning segments. The Interactive Length Tuning cursor guides you during the tuning process. The yellow cursor bars indicate the possible minimum and maximum lengths. The green bar indicates the target length, as determined from the applicable Matched Length and Max Length design rules, or the settings in the *Interactive Length Tuning* dialog. The sliding indicator shows how close you are to achieving a match.

Highlights of the **Interactive Length Tuning** tool include:

- Target Length can be directed either according to rules in your design, a design net, or manually.
- Three tuning styles available –Mitered with Lines, Mitered with Arcs, and Rounded.
- Option to precisely clip tuning patterns to **Target Length** when Mitered with Lines and Mitered with Arcs styles are used.
- Consistent interface with other Altium Designer Interactive Routing tools ensures intuitive and quick control using familiar keyboard shortcuts.

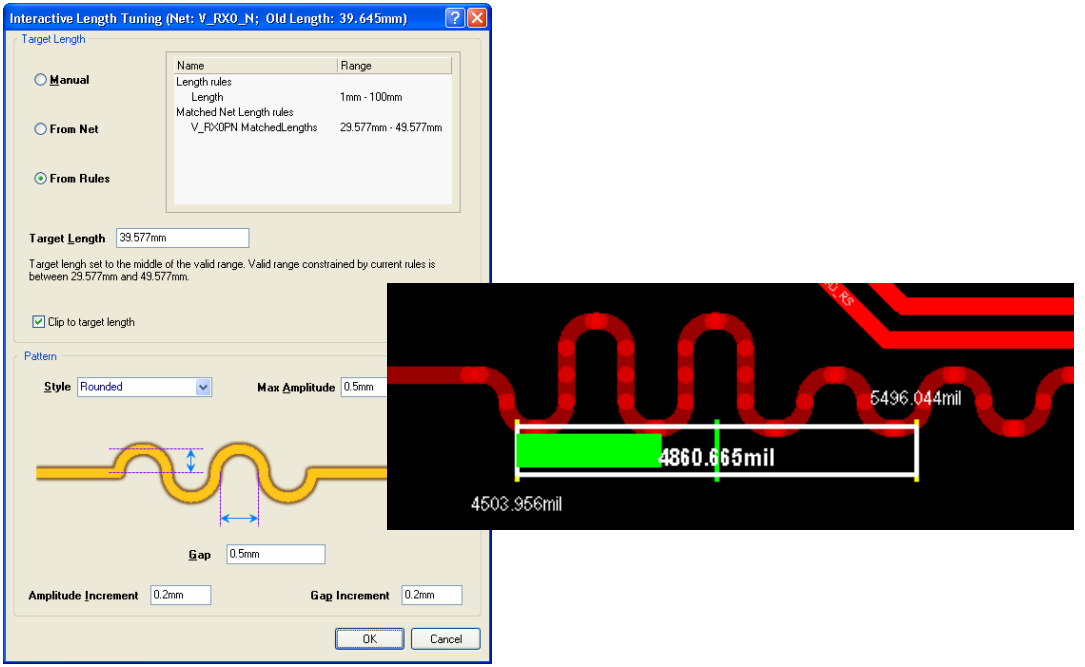


*Figure 3. Current length as well as valid length range is displayed dynamically using the gauge bar. Hitting the **Tab** key (or press **Shift+F1** for shortcut keys) while you are routing will bring up the new Interactive Length Tuning dialog where you can make changes as needed.*

Improved – Polygon Placement and Editing

Placement of polygon outlines now follows a similar behavior that you are accustomed to in interactive routing – being more intuitive and allowing greater control and flexibility. Additionally, editing of placed polygons supports the sliding of edges (including arcs).

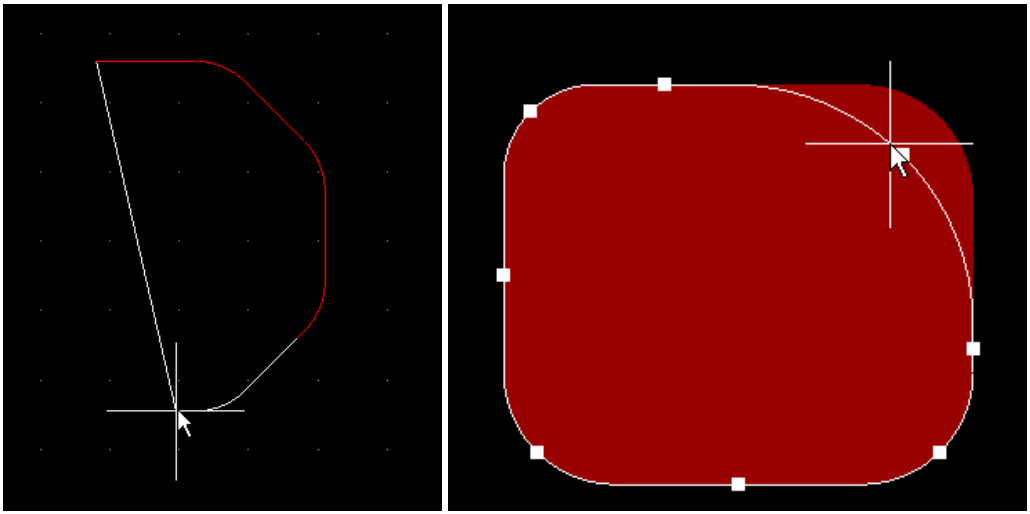
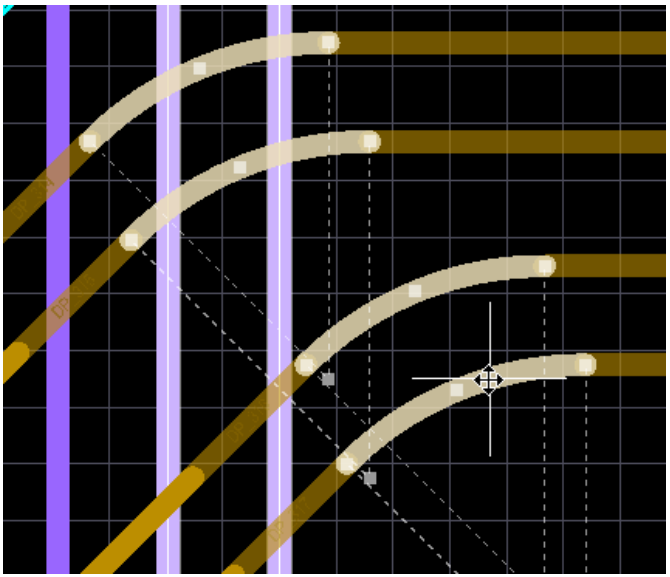


*Figure 4. Greater control when placing and editing polygons: note that the Sliding of polygon edges can only be performed when in Move Polygon Vertices mode (**Edit » Move » Polygon Vertices**).*

Improved – Smart Drag now supports arcs



The Smart Drag functionality has been extended to support arcs, allowing for quick and efficient manipulation of arc-mitered corners.

*Figure 5. Simply click to select the routing segment(s) you wish to drag – the cursor will change to a quad arrow – and then click and drag to slide to the new location. Alternatively, use the **Ctrl+click & drag** shortcut to drag without having to select first.*

New and Improved – Embedded Board Array

The *Gerber* and *ODB++ Setup* dialogs have been redesigned and updated making it easier to create and deliver output for designs that contain embedded board arrays. Added intelligence identifies any layer stackup violations before you output, and gives you an option to either continue with output or review a new **Stackup Compatibility** report.

With your embedded board array project open in the PCB Editor, select **File » Fabrication Outputs**. Select the output format you require and your design is analyzed automatically for layer stackup violations.

Enhancements in the *Gerber* and *ODB++ Setup* dialogs include:

- Ability to preview Gerber files extensions for each layer and ODB++ directory structure.
- Embedded boards that are flipped will display their layer stacks as flipped.
- Mid signal layers and internal planes that are different can still appear on the same mid layer panel.
- Mid signal layers and internal planes can be flipped against each other.

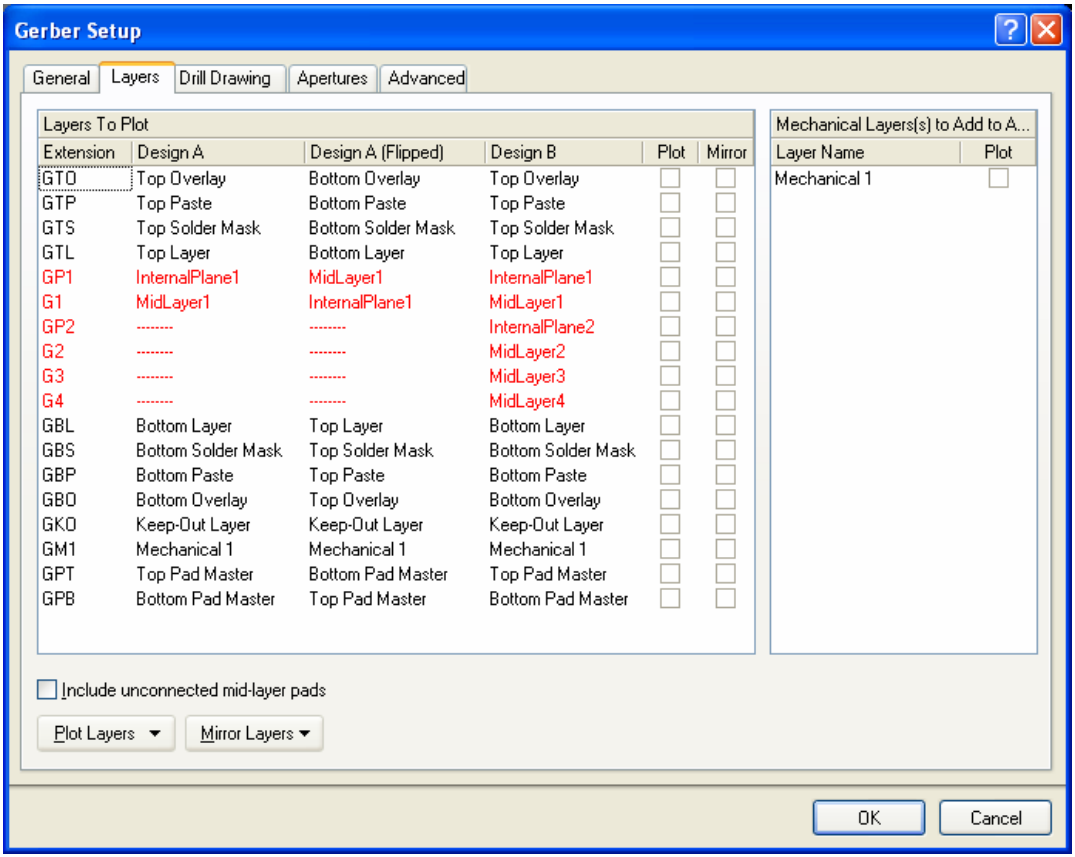


*Figure 6.The new **Gerber** and **ODB++ Setup** dialogs display layer stackups for embedded board arrays. Notice here that any compatibility violations display in red.*

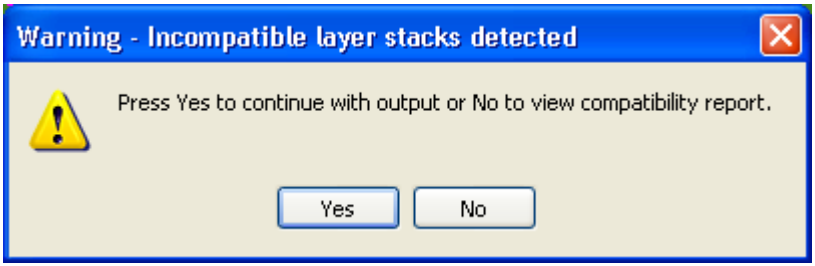


Figure 7. When generating output, a warning dialog alerts you if the layer stacks are incompatible. You then have the option of deciding to go forward with output or resolving the violation.

The new **Stackup Compatibility** report features:

- Immediate feedback on the layer stackup of any embedded board arrays in the current **Fabrication** panel.
- Hyperlinks for the **Layer Stack Manager** allow access for resolving violations quickly.
- Report can be viewed either at the time of output generation or run from the **Reports** menu in the PCB Editor.

Altium Designer

customize

Stackup Compatibility

Date : 1/03/2007
Time : 9:01:01 AM
Elapsed Time : 00:00:00
Filename E:\Completed Panel\Panel.PcbDoc

ERROR : 6 incompatible layer(s) found in the embedded boards placed in the current PCB panel document.

Layer Stack Compatibility Table

Design B	Design A (Flipped)	Test Coupon	Design A	Panel
Top Layer (Signal)	BottomLayer (Signal)	Top Layer (Signal)	TopLayer (Signal)	Top Layer (Signal)
InternalPlane1 (Plane)	MidLayer1 (Signal)	Internal Plane 1 (Plane)	InternalPlane1 (Plane)	--------
InternalPlane2 (Plane)	InternalPlane1 (Plane)	Mid-Layer 1 (Signal)	MidLayer1 (Signal)	--------
MidLayer1 (Signal)	--------	--------	--------	--------
MidLayer2 (Signal)	--------	--------	--------	--------
MidLayer3 (Signal)	--------	--------	--------	--------
MidLayer4 (Signal)	--------	--------	--------	--------
Bottom Layer (Signal)	TopLayer (Signal)	Bottom Layer (Signal)	BottomLayer (Signal)	Bottom Layer (Signal)
Open Layer Stack Manager	Open Layer Stack Manager	Open Layer Stack Manager	Open Layer Stack Manager	Open Layer Stack Manager

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*Figure 8. The **Stackup Compatibility** report shows incompatible layers in red and the total count of violations at the top of the report.*

New – FPGA Third Party Core Import Wizard

Embedded tools support for FPGA development is expanded to allow you to take advantage of core technology from your favorite third party vendors – providing increased linking of vendor-specific FPGA cores with the designs that incorporate them.

Available through the **Tools** menu when a schematic document in an FPGA project is active, the new wizard automates importing third party IP cores from FPGA vendor tools such as Xilinx, Altera, Actel, and Lattice.

Some features of the **FPGA Third Party Core Import Wizard** include:

- Schematic components and their corresponding libraries are automatically created with the correct parameters (ChildModel parameters) ready to use.
- Sheet symbols are created for HDL formats such as Altera's Megafunction Core Wizard.
- Binary file formats, such as NGC, are supported.
- Ability to declare and instantiate a core in a VHDL or Verilog file is supported.
- Non-design files such as memory initialization can be associated as part of the core.

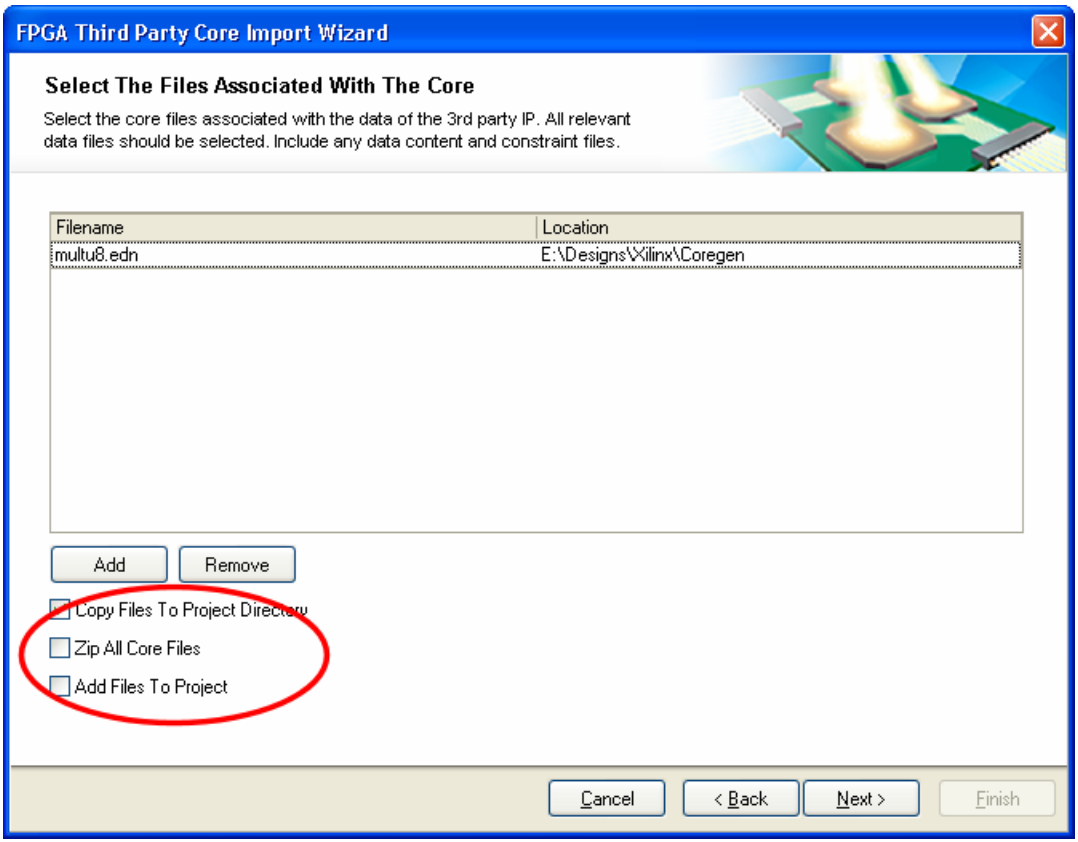


Figure 9. Multiple IP files are supported. For better management, there are options for copying to a project directory or zipping up core files together.

New – IPC Footprints Batch Generator

Available through the **Tools** menu when a PCB library is the active document, the **IPC Footprint Batch Generator** makes it possible to quickly generate multiple footprints as well as multiple density levels for a single component from a package input file that contains datasheet package information.

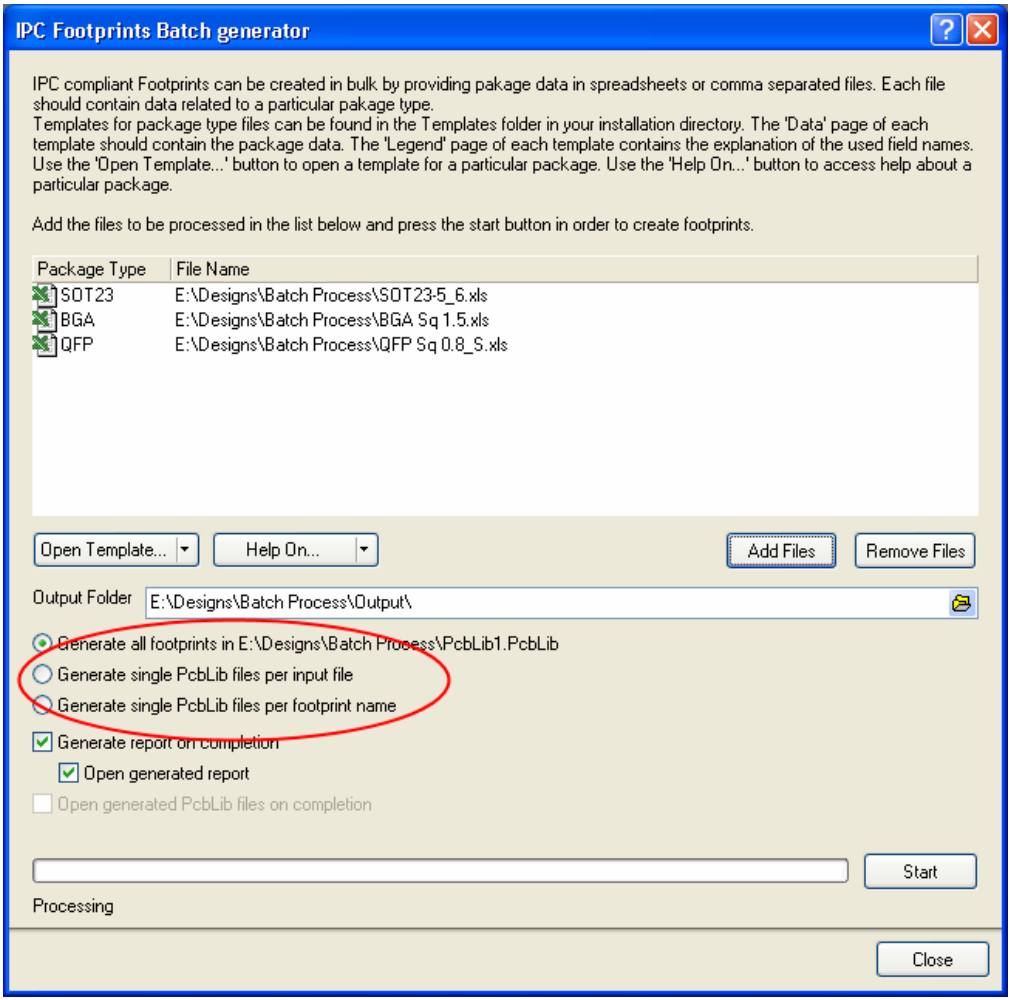


*Figure 10. The IPC Footprint Batch Generator has options that either create all the footprints into the current open **.PcbLib**, or generate a single **.PcbLib** file based on either an input file or footprint name.*

Support for the **IPC Footprints Generator** includes:

- Package type blank template files can be opened within the dialog and are provided in the `\Templates` folder of the installation directory. Help for any of the package type templates is also available.
- Package input files need only to contain the information for one or more footprints of a single package type, and can be either an Excel or comma-delimited file format.

Improved – IPC Footprints Wizard

As a complimentary tool to the **IPC Footprints Batch Generator**, the **IPC Footprints Wizard** has been updated to keep up with evolving technology. Available through the **Tools** menu when a PCB library is the active document, the **IPC Footprint Wizard** creates IPC-compliant component footprints.

Rather than working from footprint dimensions, the **IPC Footprint Wizard** uses dimensional information from the component itself in accordance with the standards released by the IPC.

For Altium Designer 6.7, it has been enhanced by the addition of support for the following additional package types:

- CFP (Ceramic Dual Flat Pack)
- DPAK (Transistor Outline)
- Laminate CSP (QFN with 2 rows of pads)
- LCC (Leadless Chip Carrier)
- LLP (QFN with power bars)
- MOLDED (2-pin components, includes capacitor, diode, inductor)
- MELF (2-pin components, includes diode and resistor)
- PQFP (Plastic Quad Flat Pack, includes PQFP Exposed Pad)
- SOIC (Small Outline Integrated Package – Gullwing Leads, includes SOIC Exposed Pad)
- SOP (Small Outline Package – Gullwing Leads, includes SOP Exposed Pad)
- SOT89 (Small Outline Transistor)
- WIRE WOUND (Precision wire-wound inductor, 2-pins)

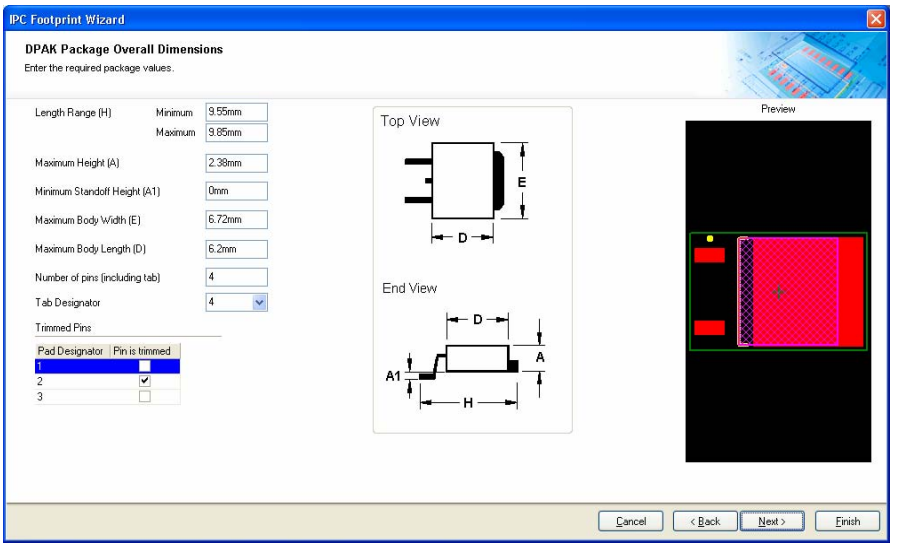


Figure 11. One of the new supported packages in the IPC footprint Wizard is the DPAK (Transistor Outline).

The **IPC Footprints Wizard** and **IPC Footprints Generator** are complimentary tools – the wizard is best for a single footprint whereas the batch generator is best for creating multiple footprints at a time.

New – Text Editor Options

Design debugging support extends back to the design documents. Appreciating how difficult it can be to work with and keep track of changes you have made in complex pieces of code, Altium Designer 6.7 delivers two new complimentary options in the Text Editor.

Previously, your Undo data was lost after the saving of a text file. You'll appreciate that now any Undo/Redo data are kept after saving, allowing you to revert all changes you may have made. Found in **Preferences » Text Editors » General**, this option is enabled (ON) by default.

Text lines that are modified or added are now automatically highlighted with color markers in the gutter. Unsaved changes are indicated with red markers while saved changes are indicated with green markers – allowing you to quickly identify how much of your work is committed. Found in **Preferences » Text Editors » Display**, this option is enabled (ON) by default.

Figure 12. Color-coded markers in the Text Editor give you immediate visual feedback showing you which change you have saved.

Improved – P-CAD Binary Translation

Translating complete binary P-CAD designs, including schematics, PCB layout, and library files can all be directly imported by Altium Designer's **Import Wizard** without converting to ASCII first – thus avoiding the need for having P-CAD installed.

The **Import Wizard** (**File » Import Wizard**) removes much of the headache normally found with design translation by analyzing your files and offering many defaults and suggested settings for project structure, layer mapping, PCB pattern (footprint) naming, and more. Complete flexibility is found in all pages of the wizard, giving you as little or as much control as you would like over the translation settings before committing to the actual translation process.

For more detailed information on directly importing your designs using the **Import Wizard**, refer to the documentation *AP0130 Moving to Altium Designer from P-CAD.*

Improved – PADS® Importer

The PADS Importer – accessed through the Import Wizard (**File » Import Wizard**) – has been enhanced to now handle the import of PADS Logic files (`*.txt`). Such files will be converted into Altium Designer Schematic documents (`*.SchDoc`) – one schematic document per sheet defined within the Logic file – and added to a PCB project (`*.PrjPcb`).

The following versions of PADS Logic files are supported: V5.0, V5.2, V2005.0, and V2005.2.

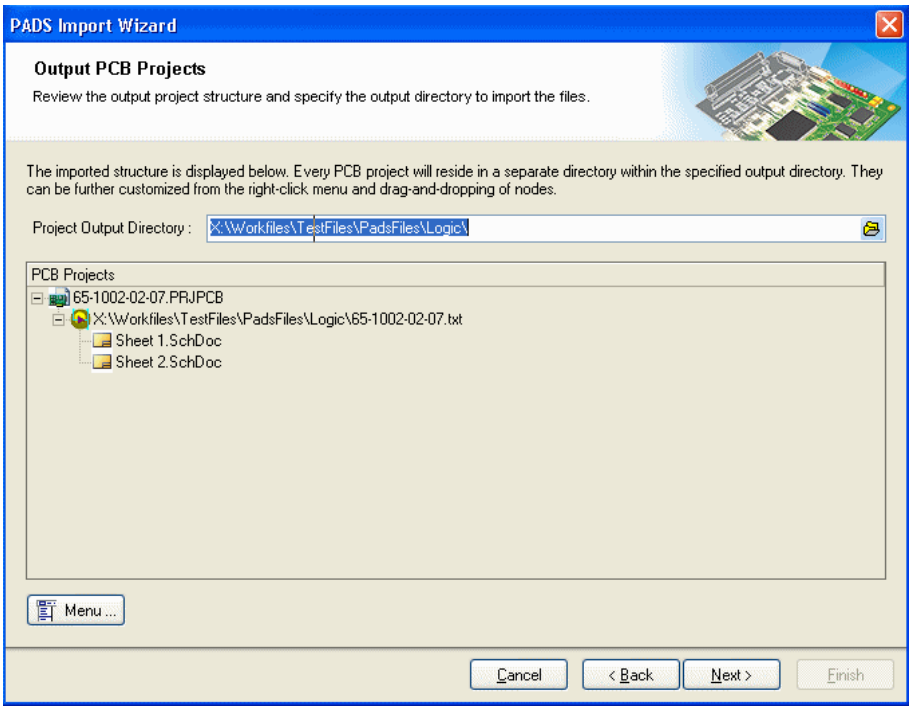


Figure 13. Import structure for PADS Logic file on import.

The PADS Importer will now handle the following PADS PCB and Schematic ASCII libraries:

- PADS PCB Decal library (`*.d`)
- PADS Schematic Part Type library (`*.p`)
- PADS Schematic CAE Decal library (`*.c`)

The PCB Decal libraries will be used to create Altium Designer PCB footprint libraries (`*.PcbLib`). The Part Type and CAE Decal libraries will be used to create an Altium Designer Schematic Library (`*.SchLib`).

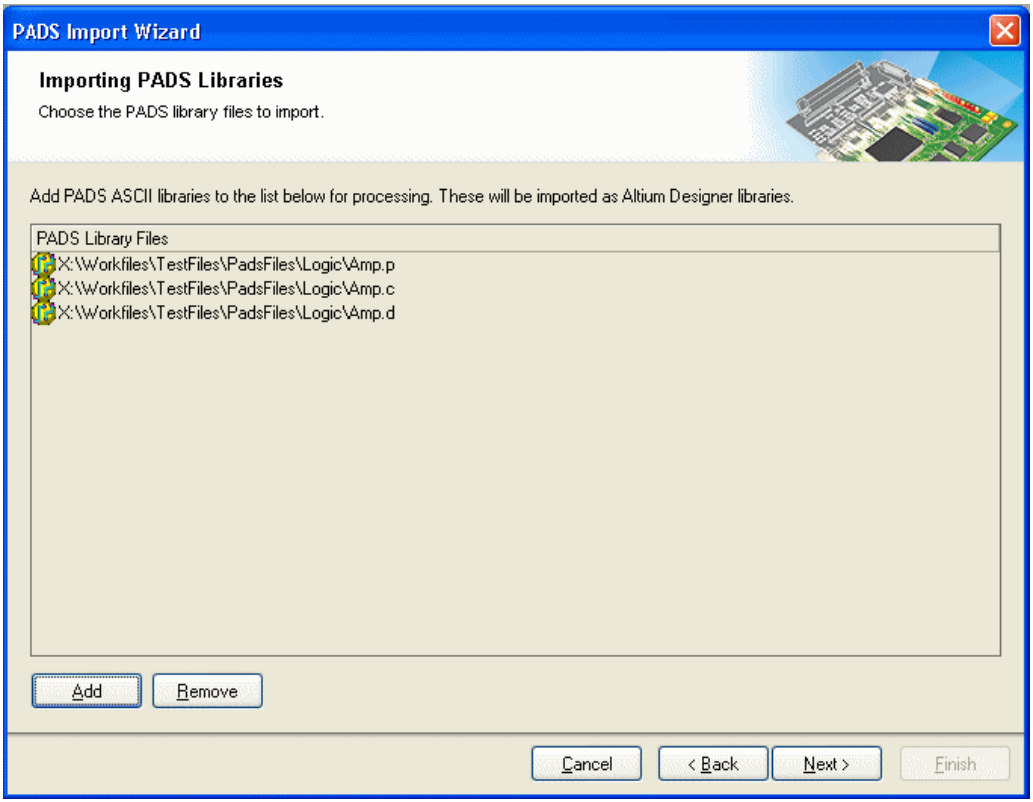


Figure 14. Importing PADS ASCII libraries.

Note that Part Type and CAE Decal libraries must be imported together, otherwise an Altium Designer Schematic library cannot be created. It is recommended that all library types be included in the import, as this allows for the creation of complete libraries for Altium Designer.

New – Smart Grid Tools

Creating and manipulating large amounts of data for library documents for today's complex designs can be a tedious and time-consuming process. Available as right-click options from the **List** panel of the Schematic and PCB editors (and corresponding library editors), two new **Smart Grid** commands streamline this process – saving you valuable time when importing and creating new object data from an external spreadsheet or table. **Smart Grid Insert** creates objects from pasted data, and **Smart Grid Paste** alters the value of existing objects.

Note that a **List** panel must be in Edit mode in order to access and use these tools.

Smart Grid Insert

After copying data from a spreadsheet or table that you wish to use, Smart Grid Insert will create new objects into a column with the header of 'Object Kind' (but they can be mapped to any column). Right-click in the List Panel and choose **Smart Grid Insert** and the *Smart Grid Insert* dialog appears:

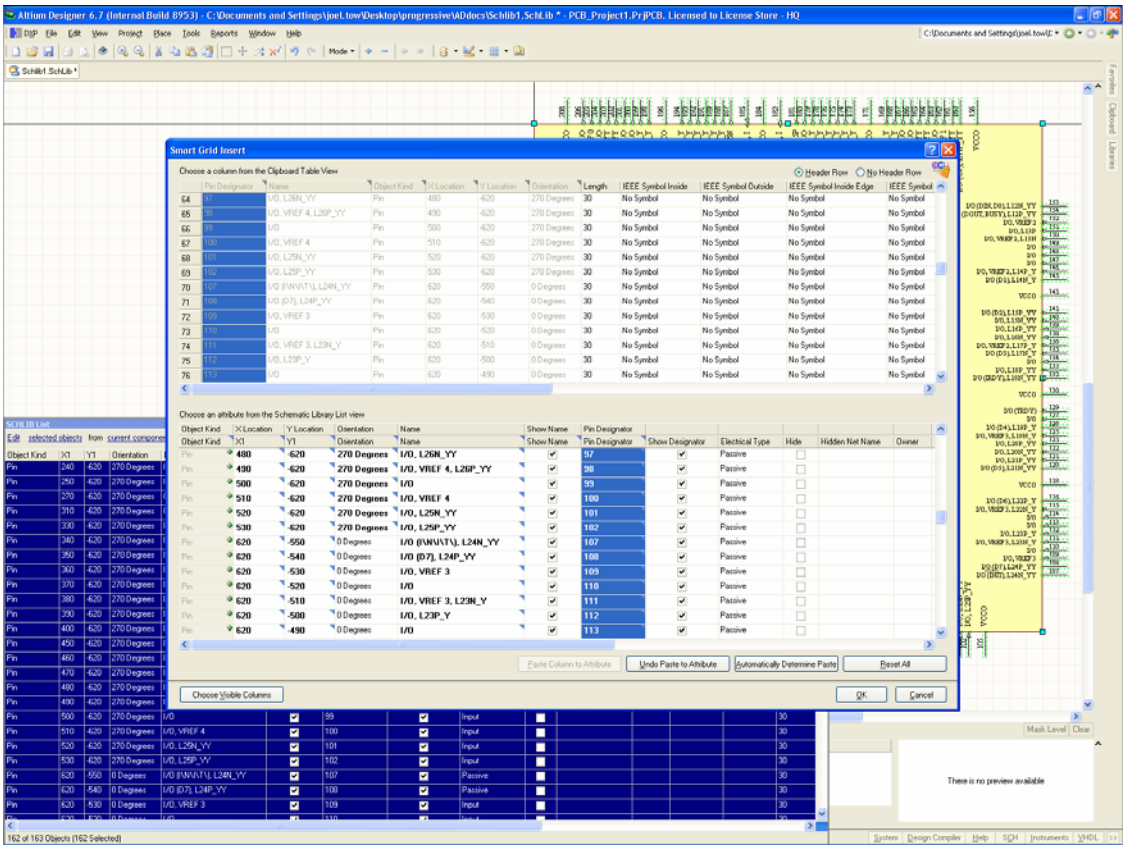


Figure 15. The top half of a Smart Grid dialog represents copied table data while the lower half shows the contents of the List panel. Newly-created objected, as shown here, can be seen flagged in the lower half of the dialog.

You can then match the copied data to the attributes in the dialog using the Smart Grid Paste tool. Clicking OK closes the dialog, creating the objects with their matching data.

Smart Grid Paste

After copying data from the spreadsheet or table that you wish to use, and then selecting the appropriate objects in the List panel, choose **Smart Grid Paste** from the pop-up menu and the *Smart Grid Paste* dialog can be accessed.

Additional support of Smart Grid Paste includes:

- **Paste Column to Attribute** buttons allow you to paste column data into the attribute for corresponding objects. The List View updates to show any changes in bold text with a blue flag.
- Original values can be easily restored using the **Undo Paste to Attribute** button.
- Copied data intelligently matched to attributes in the list using the **Automatically Determine Paste** button. **Reset All** button will cancels all previous actions.
- Any attributes that are not currently visible in the List view can be made visible through the **Choose Visible Columns** button.

For more detailed information, refer to the documentation available for each List-based panel, in the *TR0104 Altium Designer Panels Reference*. Access to specific panel information can be made by pressing **F1** over a panel, and following the relevant link available in the **Knowledge Center** panel.

New – Smart Component Identification

Having portability of designs and libraries has become a common work requirement – it's more the norm that libraries are in separate locations from the design itself or there may be alternate sets of libraries used for a single design. Sometimes the designer may just wish to take his work home where he's using a local copy of the company library. Because such a flexible way to reference source libraries is needed, it's critical to be able to control the source of the components and identify that they are the right ones.

The reason for this is that when you place a component from a library you need to remember which library (or table in the case of a DBLib) that component came from. Knowing where a component came from then becomes very valuable as a record for design management. If you have ever tried updating components and didn't have the original libraries and had to work within a restrictive design environment, then you'll appreciate how frustrating this problem can quickly become! A solution that thus provides both definable levels of control that can suit any work environment's configuration and help maintain the integrity of the design components is needed.

Altium Designer 6.7 introduces a smarter and more flexible approach for managing your component-to-library relationships. **Smart Component Identification** offers both the flexibility and control to be able to easily switch between locations of reference libraries, and identify and validate that you are using the correct components from the design.

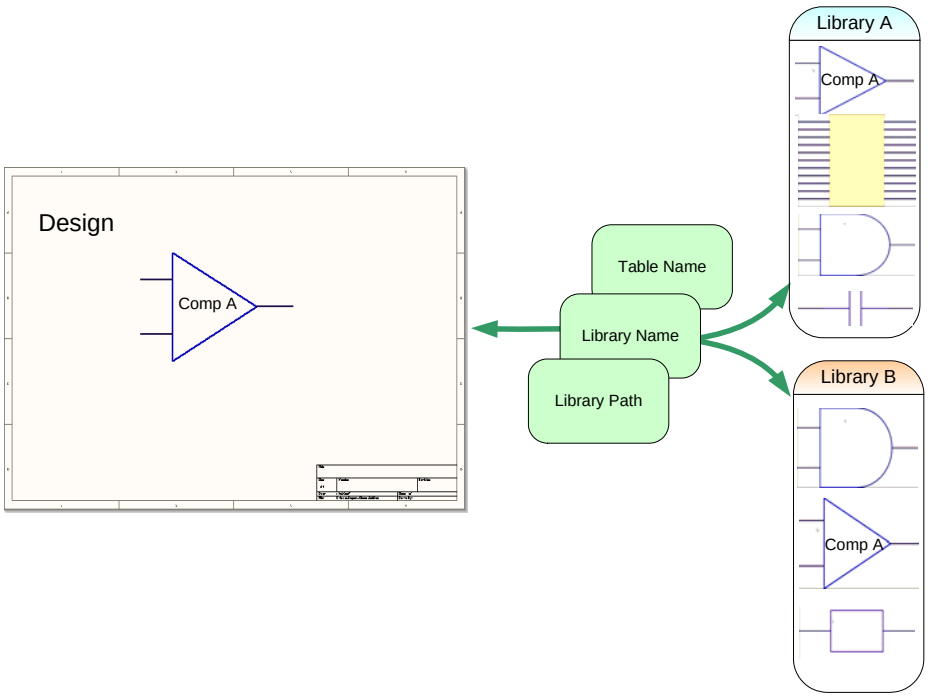


Figure 16. Here we see that Component A is the same component referenced in both Library A and Library B. You can change the Library Path, Library Name for a component, or Table Name for a DBLib to switch between the source components.

Levels of identification

Smart Component Identification is a composite of three new levels of library features that accomplish this purpose: relative path installation for libraries, changing the library name at component level, and changing table names from a DBLib.

Relative path installation for libraries

Any libraries added to the Installed Libraries list can now be installed relative to a nominated path. Available in the **Installed** tab of the *Available Libraries* dialog, this makes it easy to switch between different sets of libraries and control the source of components in your design. Changing the entry for the path will automatically reload those existing libraries in the list that are found at the new location.

Library activation and deactivation

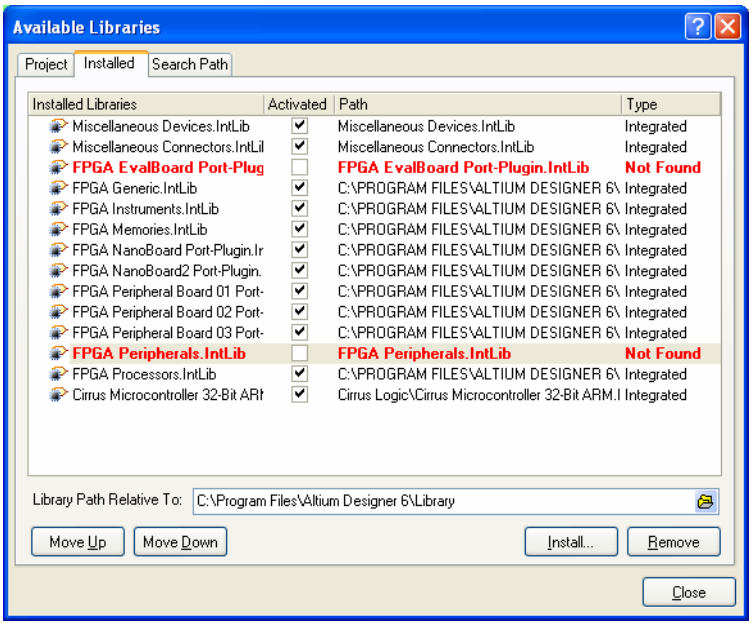


Figure 17. Libraries in the list that are not found at the new location appear highlighted in red.

Each library currently added to the Installed Libraries list (accessed on the **Installed** tab of the *Available Libraries* dialog) can also be 'Activated' or 'Deactivated'. This allows you to visually identify quickly which sets of libraries you are using with your design. Simply toggle the associated **Activated** option accordingly (as shown in Figure 17).

A Deactivated library is treated as though it had been uninstalled, but remains in the list so that it may quickly be activated, based on your design requirements. A library that is not found along the specified relative path cannot be activated.

Changing the library name at component level

The next level down for identifying your components is being able to change the library name for a component itself. Done within the **Component Properties** dialog there are three levels of component identifications:

- **Design Item ID –** the first library component found, within the current set of activated libraries and whose component name matches that of the design component on the sheet, will be used.
- **Use Library Name –** the first library component found, within an activated library whose name matches that of the specified library name, and whose component name matches that of the design component on the sheet, will be used.

- **Use Database Table Name –** the first library component found, within an activated library whose name matches that of the specified library name, within a table within that library whose name matches the specified table name, and whose component name matches that of the design component on the sheet, will be used.

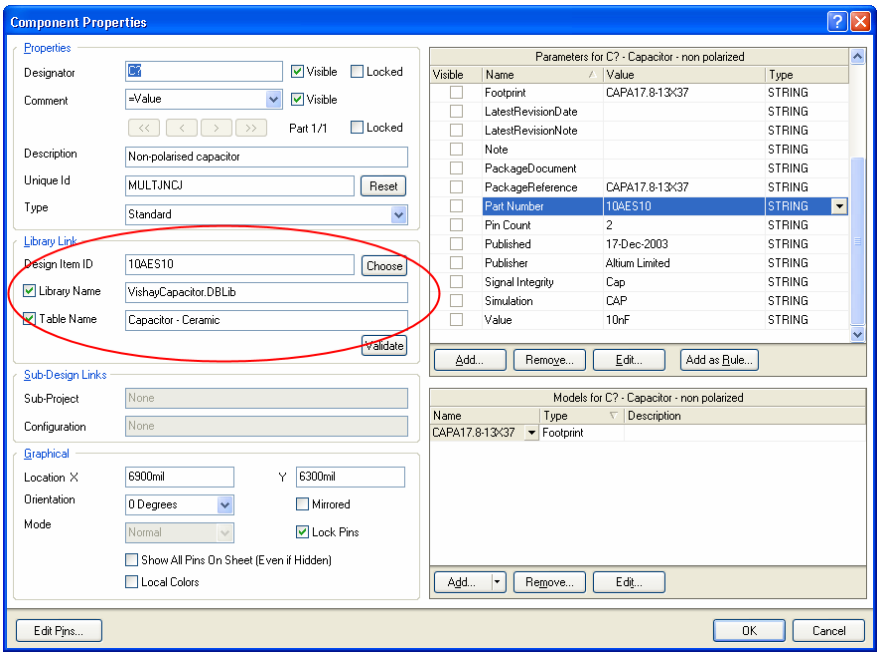


*Figure 18. Controlling the different levels of component identification through the **Component Properties** dialog.*

Component name (Design Item ID), Use Library Name and Use Database Table Name can all be specified in the Library Link region of the properties dialog for any placed component. The use of Library Name and Table Name can then be selectively enabled/disabled using available options.

Changing Table Names from a DBLib

For design components that were originally placed from integrated libraries, you can now change the base reference library to that of a newly converted DBLib or SVNDBLib simply by selecting all components in the design and:

- Disabling the **Use Library Name** option (you would need to ensure that the new DBLib/SVNDBLib has been added to the Installed Libraries list and made active, and that the previous integrated libraries are removed or deactivated.
- Leaving the **Use Library Name** option enabled, but entering the name of the DBLib/SVNDBLib instead. The Table Name could be specified if all selected components belong to that same table, or could be left blank/disabled, meaning the first match found in any table in the database would be used in each case.

To verify that the correct library is indeed being used as reference for a design component, simply click on the **Validate** button – found in the Library Link region of the *Component Properties* dialog. A dialog will appear displaying the path and library in which the first match for the design component has been found.

New – Commit Whole Project

Modified project documents under version control can now be committed in a batch fashion saving you time. **Commit Whole Project** is available from the right-click menu in both the **Projects** panel and the **Storage Manager** panel. Further options are defined in the *Check-In to Version Control* dialog.

For Subversion users, performing this commit will be atomic, resulting in a single revision. For the other VCS systems that do not support atomic check-in, the files will be committed as a batch but may result in different revision numbers for each of the files.

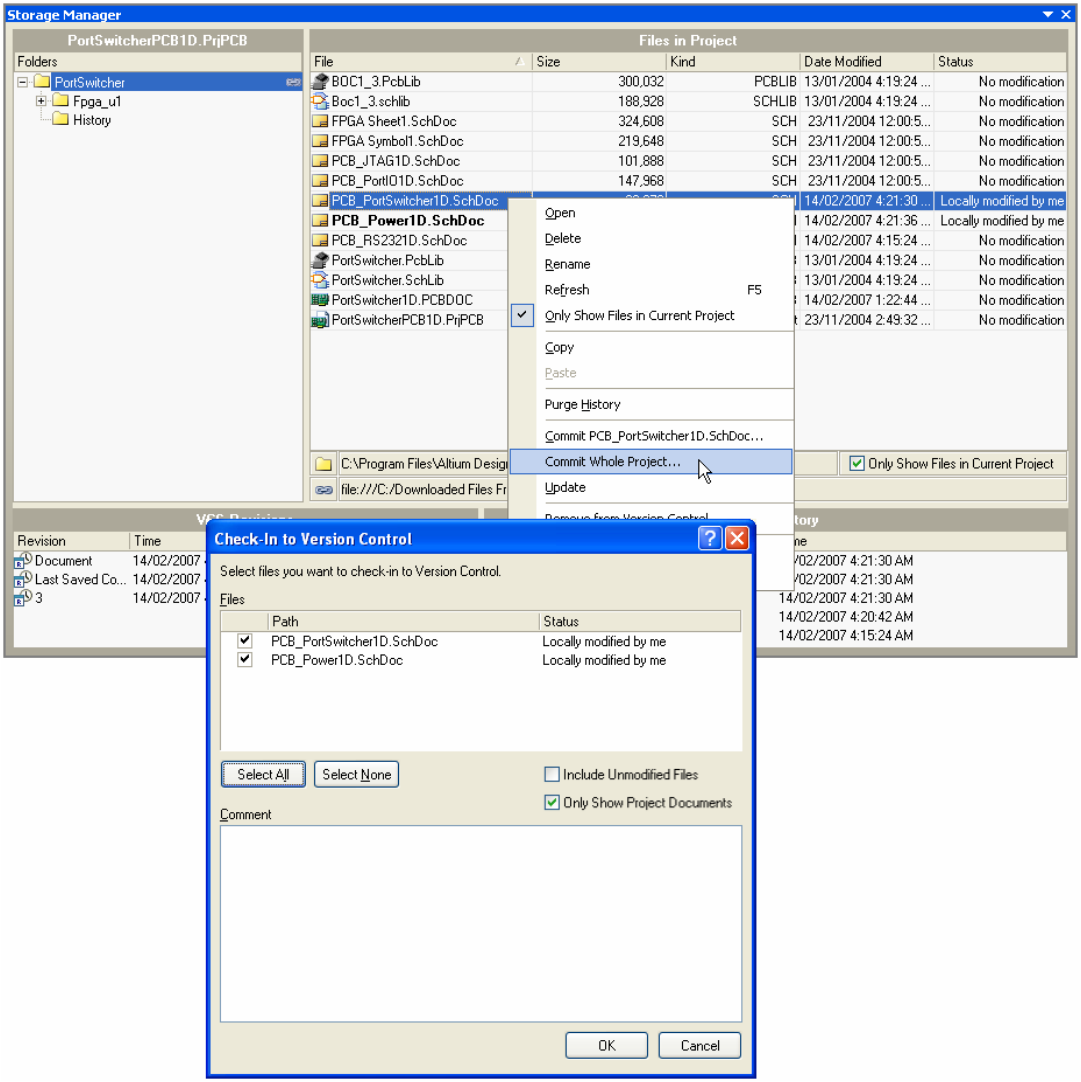


*Figure 19. Committing multiple modified files in a batch-style check-in using the **Commit Whole Project** command.*

When committing your files, the *Check-In to Version Control* dialog can be configured to show not just the project documents, but documents in other folders as well. This is particularly useful for checking-in generated files that are not part of the project. In this mode, the list of files will be expanded to include:

- All files that are in a sub-folder of the project
- If there are project documents that are not in a sub-folder of the project, then all files in the same folder as those project documents will be added as well.

New – Version Control Support for MatrixOne® PLM System

Support has been added for using Enovia's MatrixOne Product Lifecycle Management solution (PLM) as a Version Control System from Altium Designer.

Choose MatrixOne as your version control provider on the **Version Control – General** page of the *Preferences* dialog.

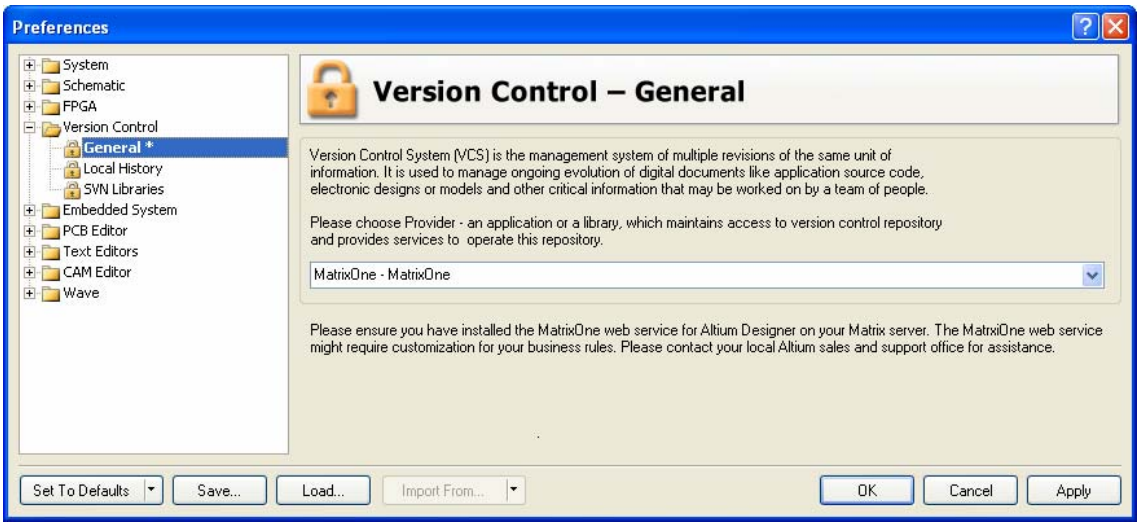
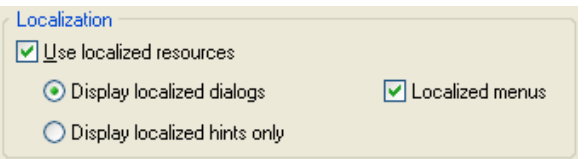


Figure 20. Setting the version control Provider to be MatrixOne.

New - Korean Language Support

Altium Designer has in-built support for detecting and working in the language locale of the Windows installation. Supported languages include French, German, Japanese, Simplified Chinese and Traditional Chinese.



New to Altium Designer 6.7 is language localization support for Korean, allowing the dialogs, menus and hints to be presented in that language. Set the localization options on the **System – General** page of the *Preferences* dialog (**DXP » Preferences**).

Improved – Third Party FPGA Vendor Options

More options have been added in most of the **Third Party Vendor Tools Options** pages. It is now possible to use **Show** and **Hide Advanced Options**, and either specify those options that you would like to use in the various sub-stages of the main Build stage, or those associated with the process flow for a particular physical device.

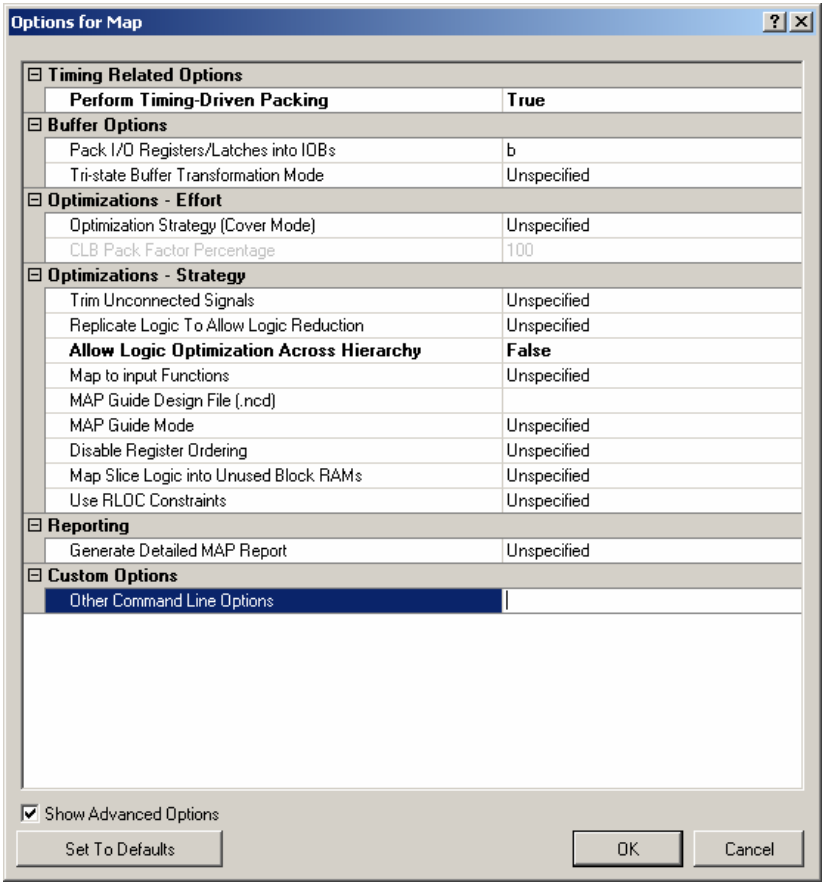


Figure 21. Advanced and custom build stage options give you full control over every build stage. The ability to insert custom command lines is also available.

New – Microsoft Windows Vista® supported

Considering your systems' readiness for Windows Vista? Altium Designer has been tested and is compatible with the latest version of Windows Vista. You can deploy Altium Designer across your organization knowing that you not only get the most productive design system available, but also the security and confidence of knowing that Altium is committed , at every level, to ensuring your complete success.

Revision History

Date	Version No.	Revision
15-Mar-2007	1.0	Altium Designer 6.7 release