

# FDS6912

## Dual N-Channel Logic Level PWM Optimized PowerTrench® MOSFET

### General Description

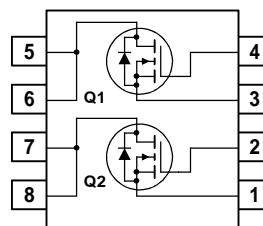
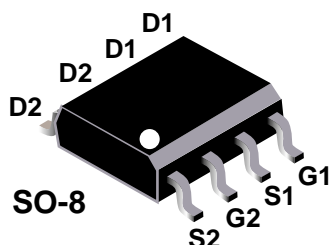
These N-Channel Logic Level MOSFETs have been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable RDS(ON) specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

### Features

- 6 A, 30 V.  $R_{DS(ON)} = 0.028 \Omega @ V_{GS} = 10 V$   
 $R_{DS(ON)} = 0.042 \Omega @ V_{GS} = 4.5 V.$
- Optimized for use in switching DC/DC converters with PWM controllers
- Very fast switching.
- Low gate charge



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	30	V
V <sub>GSS</sub>	Gate-Source Voltage	±25	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	6	A
	– Pulsed	20	
P <sub>D</sub>	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
T <sub>J</sub> , T <sub>stg</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6912	FDS6912	13"	12mm	2500 units

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		20		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55^\circ\text{C}$			1 10	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

## On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	2	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$ $T_J = 125^\circ\text{C}$		0.024 0.034	0.028 0.048	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 4.9\text{ A}$		0.035	0.042	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	20			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 6\text{ A}$		20		S

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$		740		pF
$C_{oss}$	Output Capacitance	$f = 1.0\text{ MHz}$		170		pF
$C_{rss}$	Reverse Transfer Capacitance			75		pF

## Switching Characteristics (Note 2)

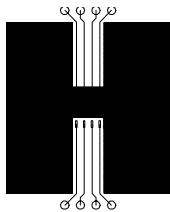
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$		8	16	ns
$t_r$	Turn–On Rise Time	$V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		13	24	ns
$t_{d(off)}$	Turn–Off Delay Time			18	29	ns
$t_f$	Turn–Off Fall Time			8	16	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 6\text{ A},$		7	10	nC
$Q_{gs}$	Gate–Source Charge	$V_{GS} = 5\text{ V}$		3.8		nC
$Q_{gd}$	Gate–Drain Charge			2.5		nC

## Drain–Source Diode Characteristics and Maximum Ratings

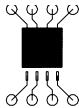
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				1.3	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)		0.75	1.2	V

### Notes:

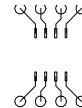
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 78 $^\circ\text{W}$  when mounted on a 0.5in<sup>2</sup> pad of 2 oz copper



b) 125 $^\circ\text{W}$  when mounted on a 0.02 in<sup>2</sup> pad of 2 oz copper



c) 135 $^\circ\text{W}$  when mounted on a minimum mounting pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

## Typical Characteristics

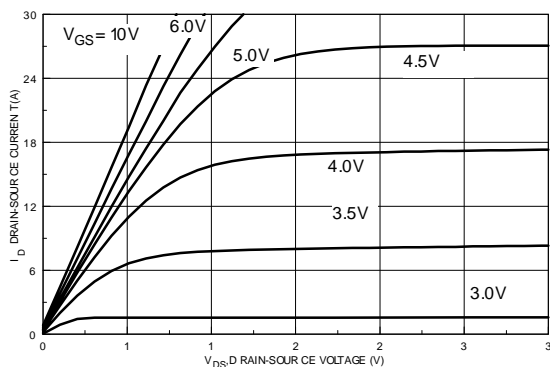


Figure 1. On-Region Characteristics.

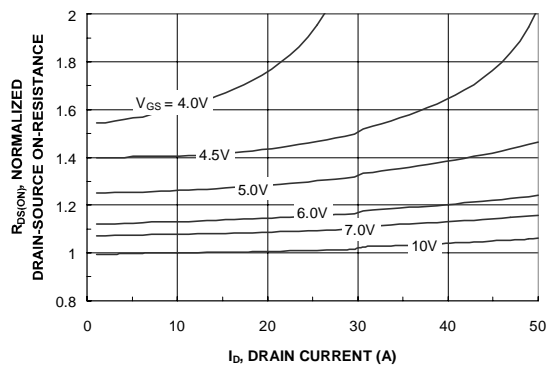


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

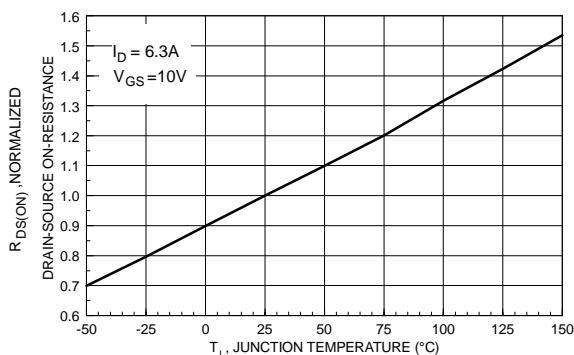


Figure 3. On-Resistance Variation with Temperature.

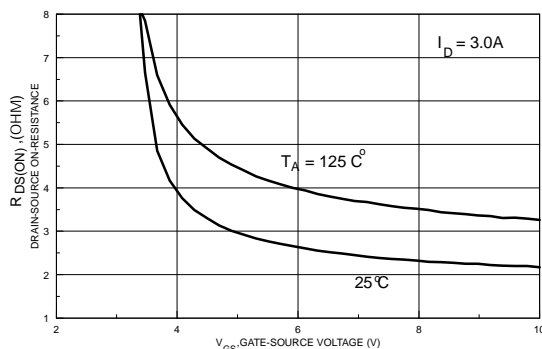


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

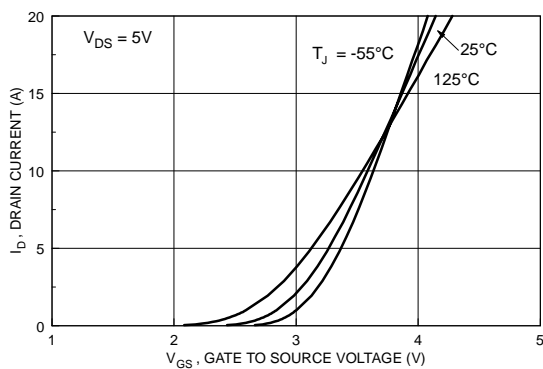


Figure 5. Transfer Characteristics.

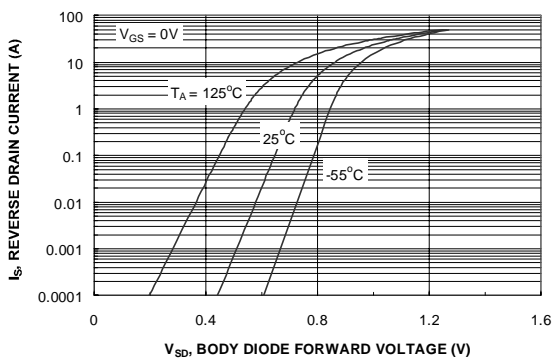


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

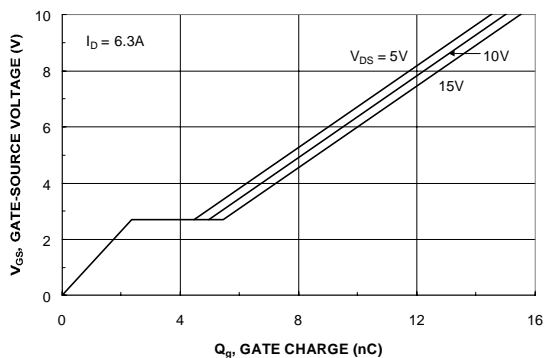


Figure 7. Gate Charge Characteristics.

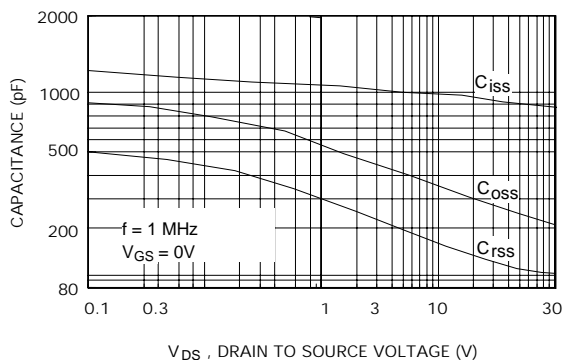


Figure 8. Capacitance Characteristics.

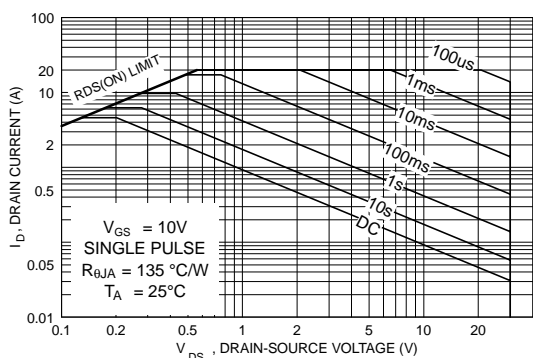


Figure 9. Maximum Safe Operating Area.

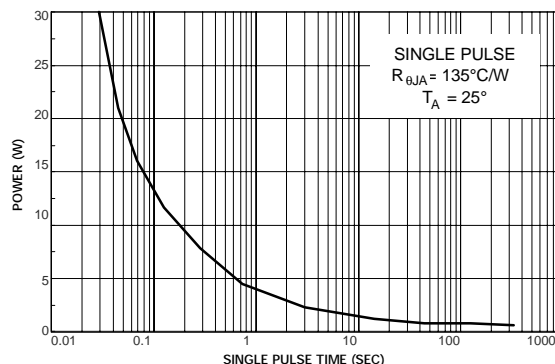


Figure 10. Single Pulse Maximum Power Dissipation.

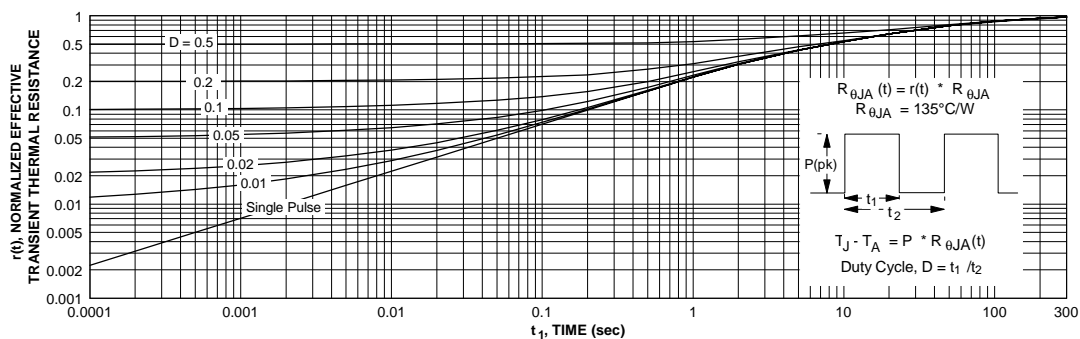


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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