Wireless Components

FM Car Radio IC with PLL

TUA 4401K V 2.1

Specification 17.02.00

DS 1

Revision History: Current Version: 02.00

Previous Version:Data Sheet 23.09.1999

Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
3-7	3-7	Functional description pin 41 corrected
3-11	3-11	Functional description pin 41 corrected
5-3	5-3	Sequence tests 310 to 317 changed (Item)
5-5	5-5	Values attack current changed
5-5	5-5	Values recovery current changed
5-5	5-5	Values detector characteristic changed

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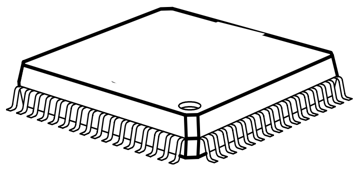
Productinfo

General Description

The TUA 4401K is the first Infineon Carradio IC using BICMOS technology.
The combination of an analog FM receiver circuit and a digital PLL synthesizer on the same chip reduces the over all pin count in comparison to two separate IC's and in addition the number of necessary external components. This gives the flexibility both for high performance and low cost applications.
The recommended applications for this device are FM only carradios and background receivers, capable for all world standards.

Package



Features

- Double balanced RF mixer with low noise figure, high IP3 and wide dynamic range
- Strictly symmetrical RF circuitry
- IF amplifier with adjustable gain
- Double frequency 1st LO option
- 7 stage limiter amplifier with dB linear fieldstrength output
- Low distortion coincidence demodulator
- Multipath detector with analog output
- CMOS PLL-Synthesizer
- Resolution between 100 kHz and 6.25kHz
- Search tuning stop with IF counter and Fieldstrength/Multipath evaluation
- ADC's for fieldstr. and multipath detector
- I^2C Bus operation

Applications

- FM only car radio receiver, background receiver

Ordering Information

Type	Ordering Code	Package
TUA 4401K		MQFP-44

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2 Product Description

Contents of this Chapter

2.1 General Description

The TUA 4401K is the first Infineon Carradio IC using BICMOS technology. The combination of an analog FM receiver circuit and a digital PLL synthesizer on the same chip reduces the over all pin count in comparison to two separate IC's and in addition the number of necessary external components. This gives the flexibility both for high performance and low cost applications.
The recommended applications for this device are FM only carradios and background receivers, capable for all world standards.

TUA 4401K features:

Frontend

- High level, high impedance mixer input with improved dynamic range
- High input / output 3rd order intercept point
- Integrated prestage AGC generation and control for PIN diodes and MOS tetrode
- Bus controlled AGC threshold
- 2 pin 1st local oscillator with improved low phase noise, internally coupled to PLL. Double frequency operation possible
- Strictly symmetrical RF parts
- PLL with fast acquisition mode
- Resolution 100 kHz, 50 kHz, 25 kHz, 12,5 kHz, 10 kHz and 6.25 kHz
- High running (61.5 MHz) crystal oscillator to avoid interference with bus controlled adjustment

IF amplification, demodulation and STS

- Low noise IF amplifier
- Gain adjust with DC control voltage or serial bus possible
- 7 stage IF limiter with extended fieldstrength range suitable for the IF frequency range of 10.7 MHz ... 21.4 MHz
- Fieldstrength DC output and ADC output available
- Low distortion coincidence demodulator (using short loop AFC principle) with MPX output
- Wideband multipath detector with analog output and ADC output
- IF counter for search tuning stop with selectable IF center frequency, window width and programmable thresholds for fieldstrength and multipath evaluation
- STS informations -in window-,-below-,-beyond- available

I^2C Bus

- I^2C bus (2 wire, fast mode device with 400 kbit/s) operation possible
- Bus interface with low threshold voltage Schmitt Trigger inputs for interfacing 3V or 5V microprocessors

2.2 Applications

- FM only car radio receiver, background receiver

2.3 Features

- Double balanced RF mixer with low noise figure, high IP3 and wide dynamic range
- Strictly symmetrical RF circuitry
- Double frequency 1st LO option
- IF amplifier with adjustable gain
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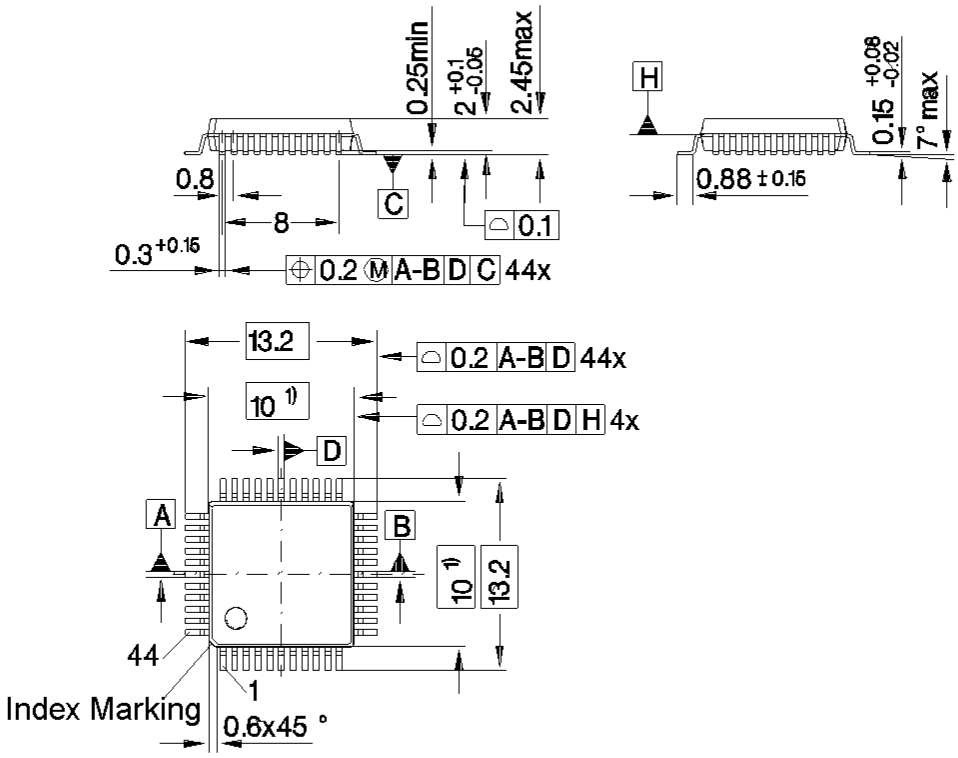
- Resolution between 100 kHz and 6.25kHz
- Search tuning stop with IF counter and Fieldstrength/Multipath evaluation
- ADC's for fieldstr. and multipath detector
- I^2C Bus operation

2.4 Package Outlines

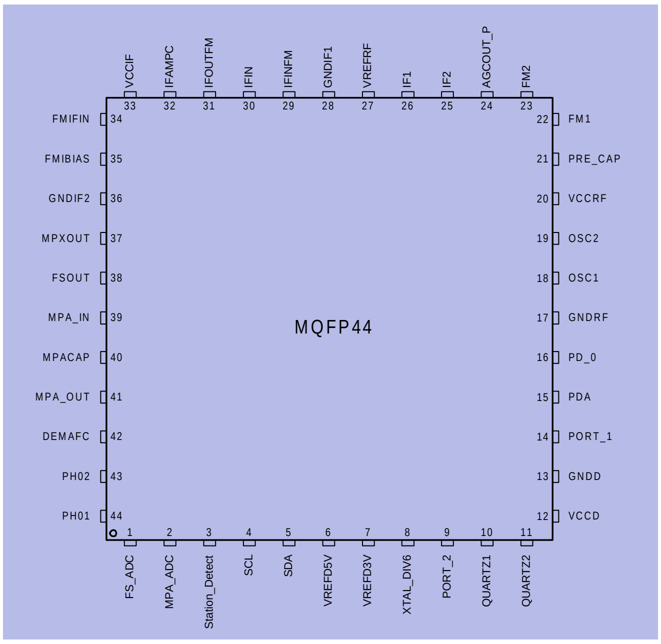
MQFP 44



3 Functional Description

Contents of this Chapter

3.1 Pin Configuration



Pin_config.wmf

Figure 3-1 IC Pin Configuration

Table 3-1 Pin Configuration

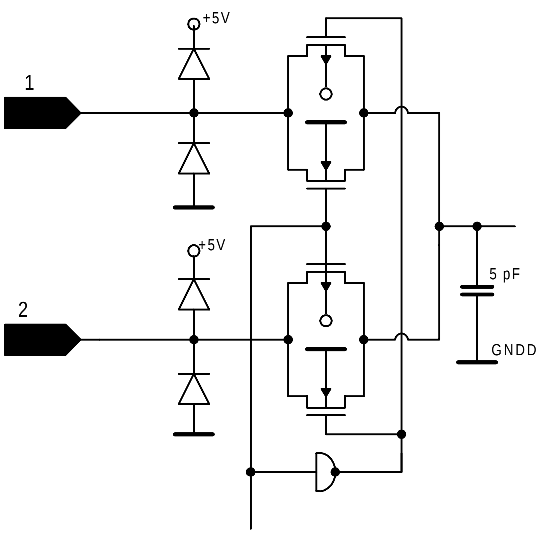
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	FS_ADC		1: ADC input fieldstrength
2	MPA_ADC		2: ADC input multipath detector

Table 3-1 Pin Configuration (continued)

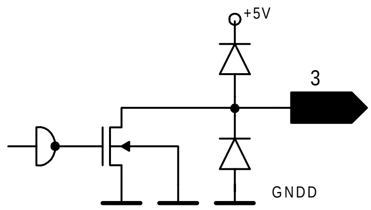
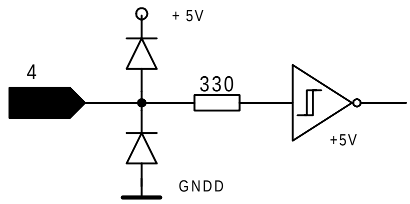
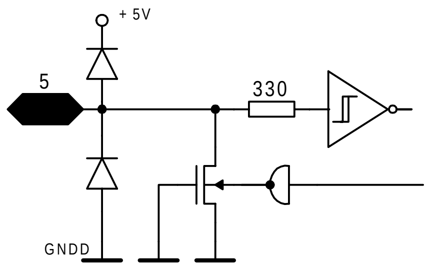
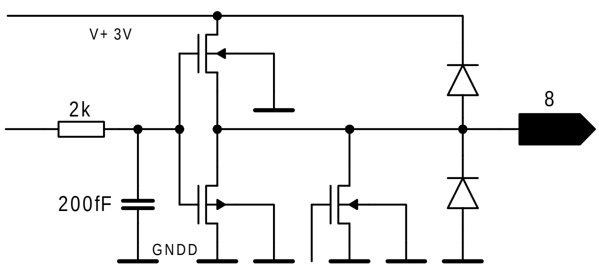
Pin No.	Symbol	Equivalent I/O-Schematic	Function
3	Station_Detect		3: IF counter output station detector
4	SCL		4: I^2C bus clock input
5	SDA		5: I^2C bus data in/output
6	VREFD5V		6: Reference voltage digital section (5V)
7	VREFD3V		7: Reference voltage digital section (3V)
8	XTAL_DIV6		8: Crystal oscillator auxiliary output (10.25 MHz)

Table 3-1 Pin Configuration (continued)

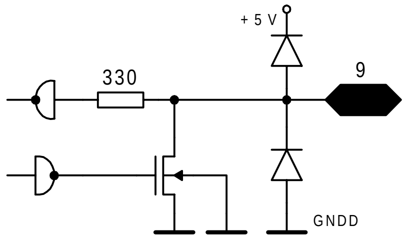
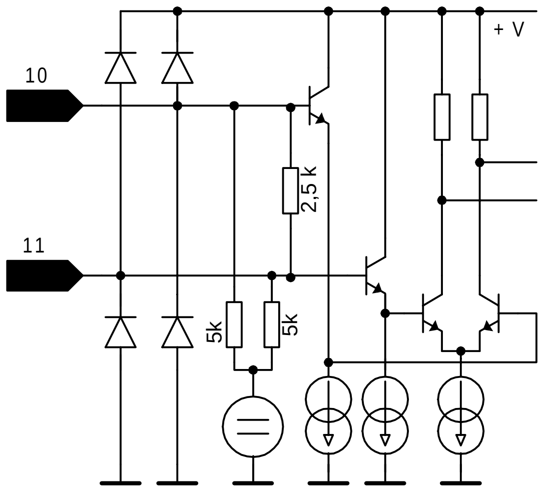
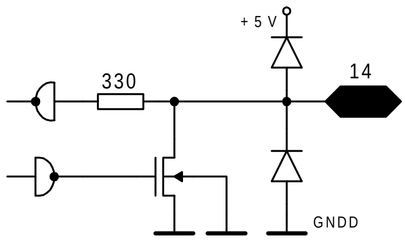
Pin No.	Symbol	Equivalent I/O-Schematic	Function
9	PORT_2		9: Switch port output 2(open drain)
10	QUARTZ1		10: Reference oscillator input / Crystal
11	QUARTZ2		11: Reference oscillator input / Crystal
12	VCCD		12: Positive power supply voltage for serial bus and synthesizer
13	GNDD		13: Ground for serial bus and synthesizer
14	PORT_1		14: Switch port output 1 (open drain)

Table 3-1 Pin Configuration (continued)

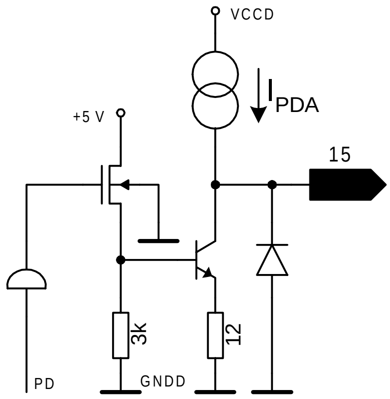
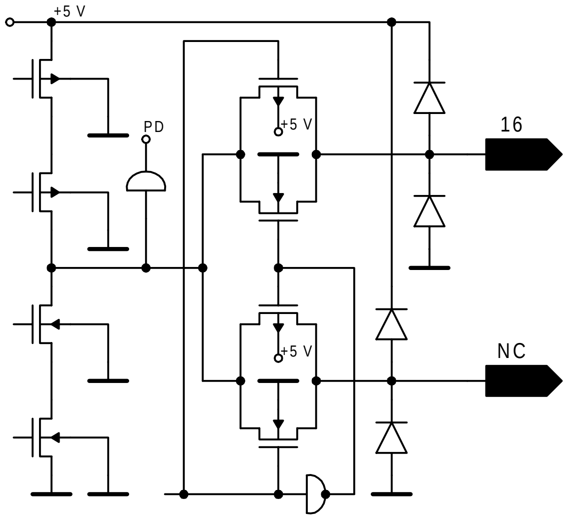
Pin No.	Symbol	Equivalent I/O-Schematic	Function
15	PDA		15: PLL phasedetector output analog (Tuningvoltage)
16	PD_0		16: PLL chargepump output (Phase detector tristate chargepump output)
17	GNDRF		17: Ground for RF part

Table 3-1 Pin Configuration (continued)

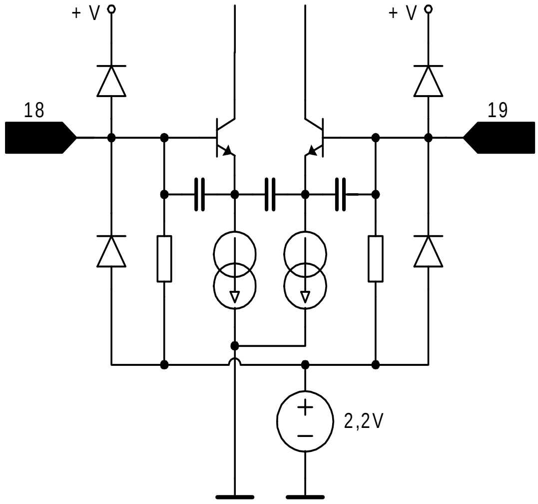
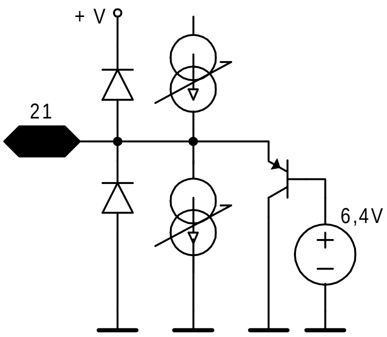
Pin No.	Symbol	Equivalent I/O-Schematic	Function
18 19	OSC1 OSC2		18: 1st local oscillator circuit 19: 1st local oscillator circuit
20	VCCRF		20: Positive power supply voltage for RF part
21	PRE_CAP		21: Prestage AGC time constant capacitor; output for MOS tetrode gate 2

Table 3-1 Pin Configuration (continued)

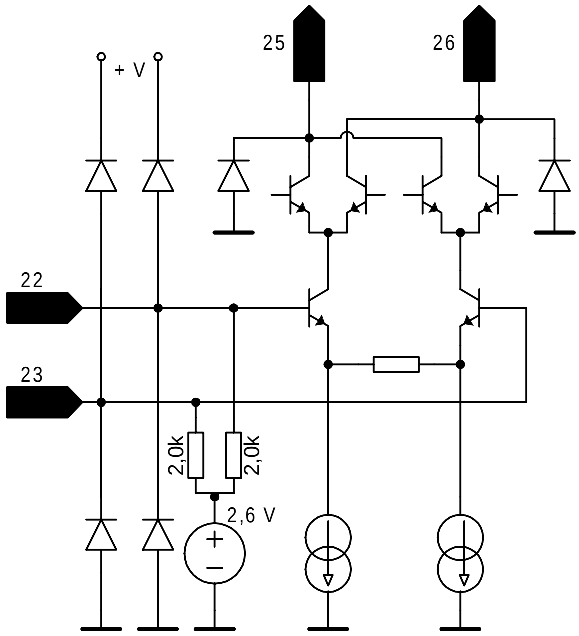
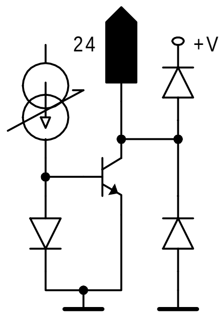
Pin No.	Symbol	Equivalent I/O-Schematic	Function
22 23	FM1 FM2		22: FM 1st mixer symmetrical input 23: FM 1st mixer symmetrical input
24	AGCOUT_P		24: Prestage AGC current output for PIN diode normal polarity

Table 3-1 Pin Configuration (continued)

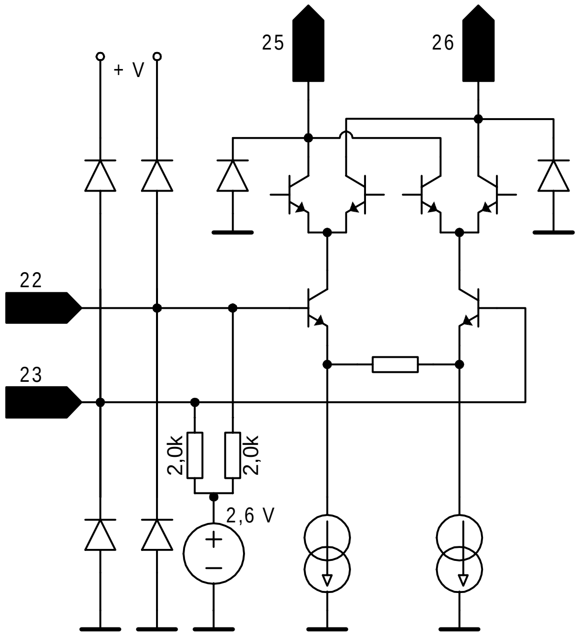
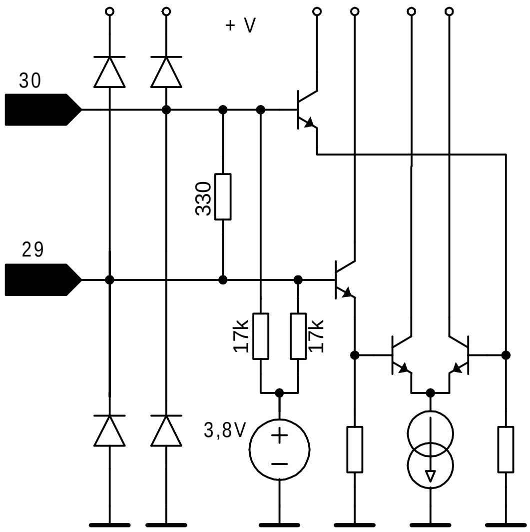
Pin No.	Symbol	Equivalent I/O-Schematic	Function
25	IF2		25: 1st mixer output (open collector)
26	IF1		26: 1st mixer output (open collector)
27	VREFRF		27: Reference voltage RF section (4.8V)
28	GNDIF1		28: Ground for IF amplifier
29	IFINFM		29: 10.7 MHz IF amplifier input
30	IFIN		30: 10.7 MHz IF amplifier operation point

Table 3-1 Pin Configuration (continued)

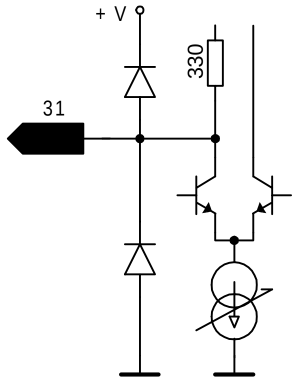
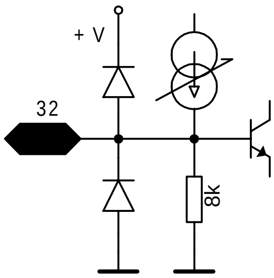
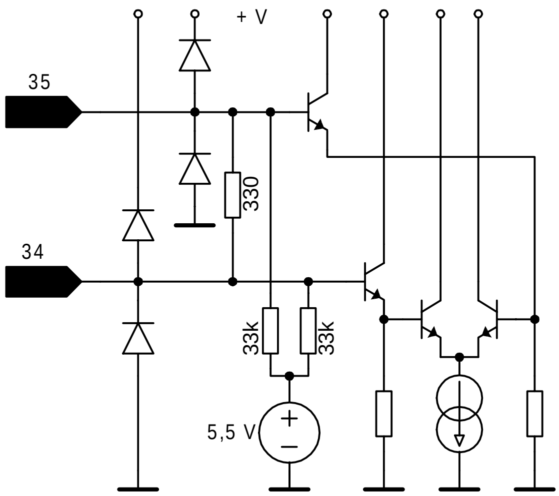
Pin No.	Symbol	Equivalent I/O-Schematic	Function
31	IFOUTFM		31: 10.7 MHz IF amplifier out-put
32	IFAMPC		32: 10.7 MHz IF amplifier DC gain control adjust block-ing capacitor
33	VCCIF		33: Positive power supply voltage for IF amplifier
34	FMIFIN		34: FM limiter input
35	FMIFBIAS		35: FM limiter input bias decoupling capacitor
36	GNDIF2		36: Ground for limiter ampli-fier

Table 3-1 Pin Configuration (continued)

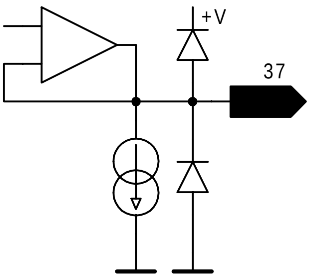
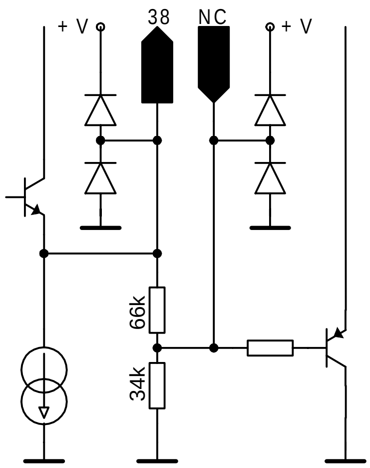
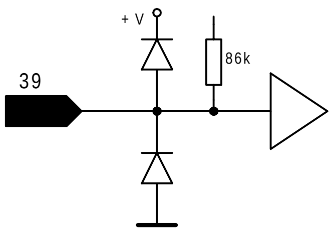
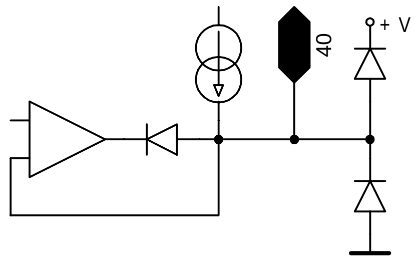
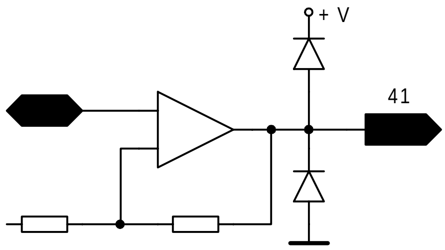
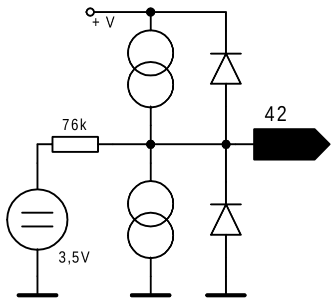
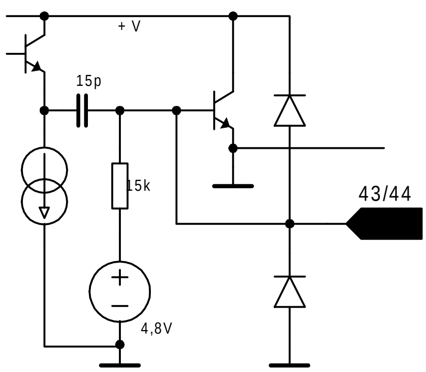
Pin No.	Symbol	Equivalent I/O-Schematic	Function
37	MPXOUT		37: FM MPX signal output
38	FSOUT		38: Fieldstrength output
39	MPA_IN		39: Multipath detector input

Table 3-1 Pin Configuration (continued)

Pin No.	Symbol	Equivalent I/O-Schematic	Function
40	MPACAP		40: Multipath detector rectifier capacitor
41	MPA_OUT		41: Multipath detector output
42	DEMAFC		42: Demodulator AFC blocking capacitor
43	PH02		43: Demodulator circuit
44	PH01		44: Demodulator circuit

3.2 Block Diagram

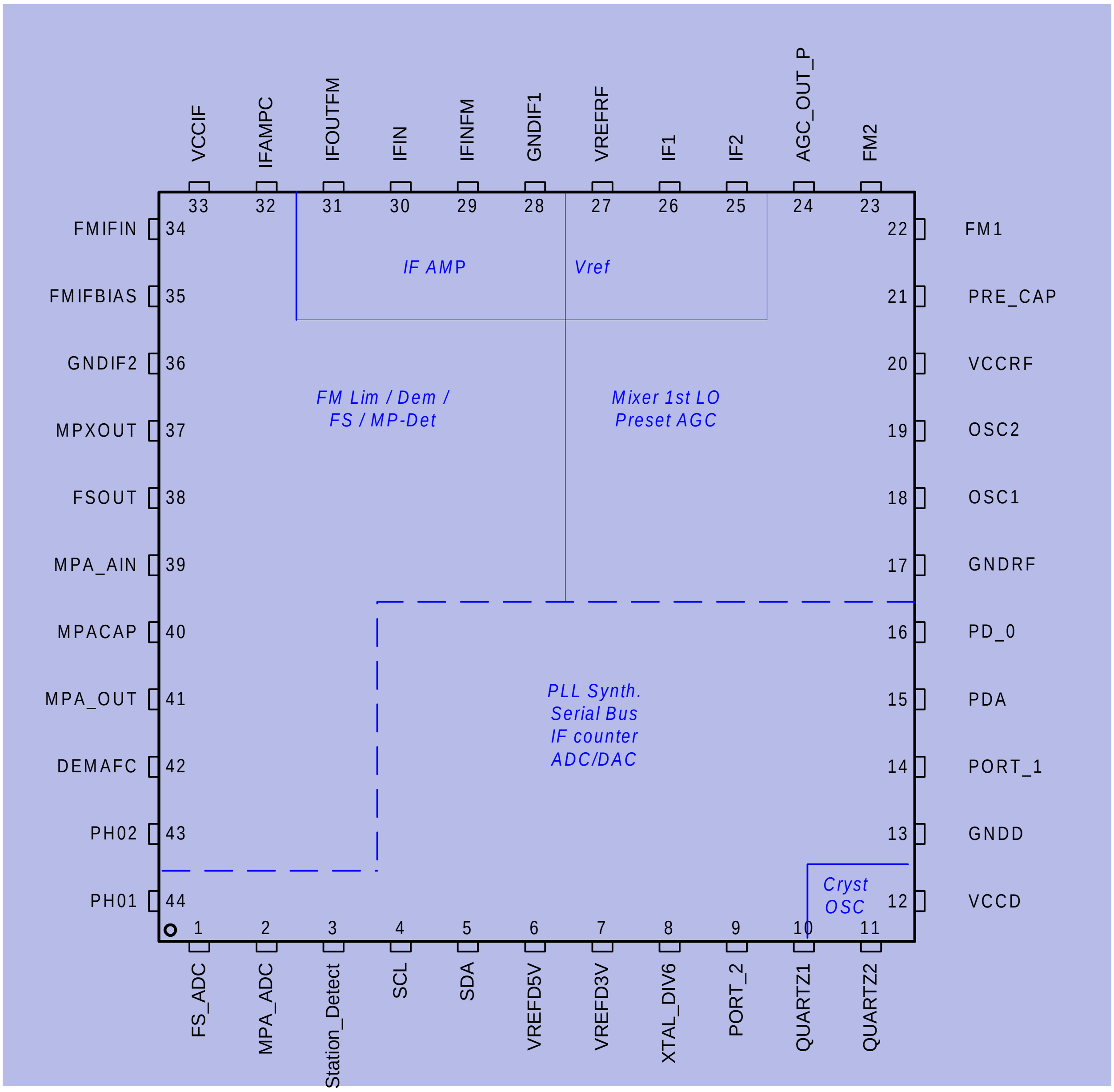


Figure 3-2 Main Block Diagram

3.3 Functional Block Diagram

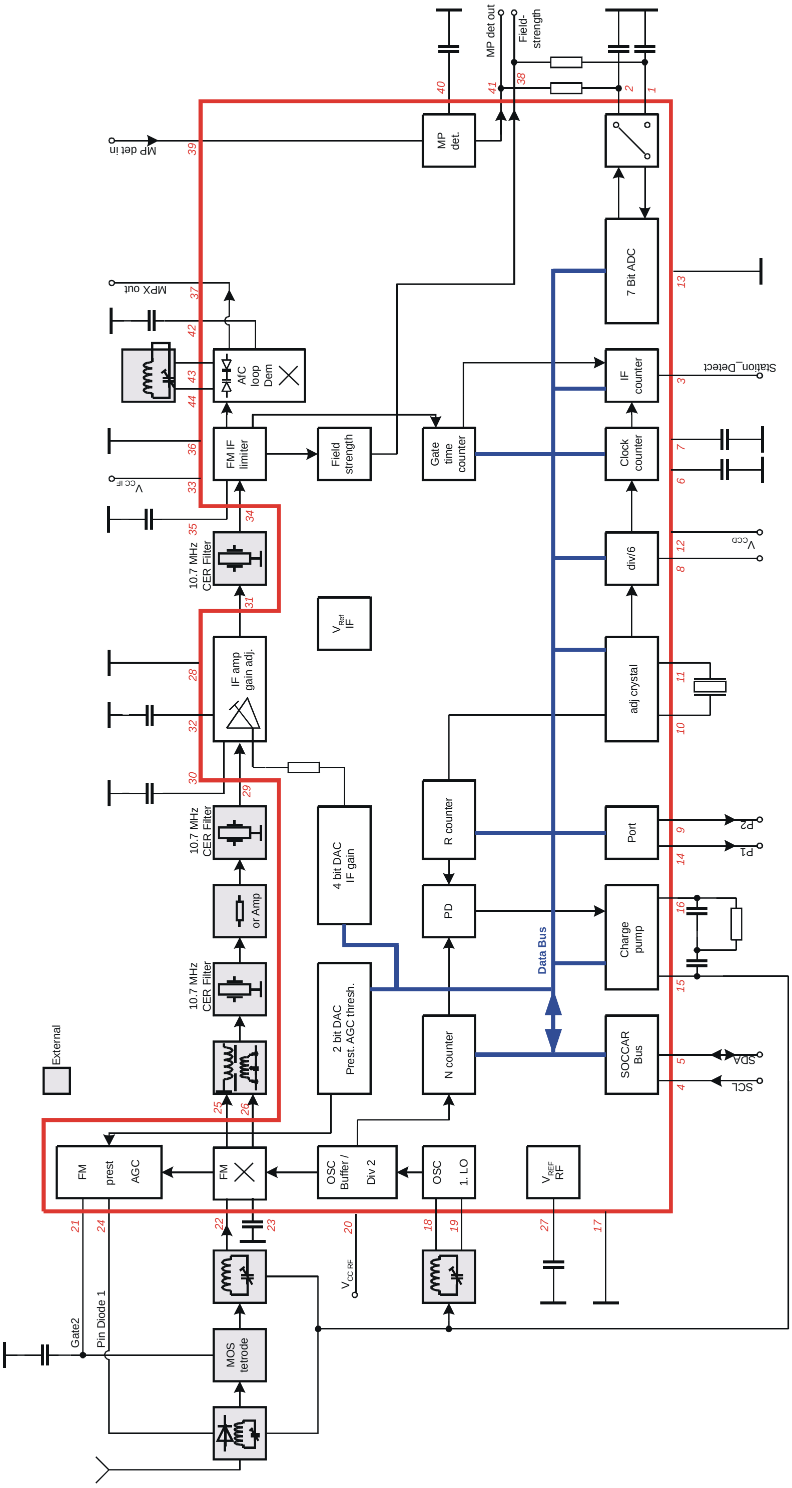


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Figure 3-3 Functional Block Diagram

3.4 Circuit Description

The TUA 4401K is a one chip FM car radio system consisting of RF frontend, gain adjustable IF amplifier, FM-IF limiter amplifier, demodulator, PLL synthesizer, IF counter for STS and ADC's for fieldstrength and multipath detector. The serial bus is a I^2C type.

1. FM frontend
   The frontend consists of a two pin varactor tuned oscillator, a double balanced mixer and a prestage AGC control circuit. The mixer has an improved intermodulation behaviour and converts the RF signal to the 10,7 MHz IF range . Two inputs allow both symmetrical and unsymmetrical operation. The integrated AGC stage for prestage control drives MOSFETS as well as PIN diodes a with cur- rent driver. The AGC threshold can be set with a serial bus controlled 2 Bit DAC. For background receiver application the oscillator is able run at double frequency, a subsequent frequency divider by 2 is activated by serial bus to provide the correct mixer frequency.

2. FM IF amplifier
   After the mixer an IF amplifier is present for IF post amplification. Input and output impedance are both 330 Ohms for matching with ceramic filters. For adjusting the over all gain the IF amplifier gain can be adjusted with a serial bus controlled 4 Bit DAC.

3. FM limiter and demodulator
   The FM IF amplifier includes a seven stage capacitive coupled limiter amplifier and a fieldstrength generator with high linearity and increased dynamic range. The coincidence demodulator has an additional AFC short loop circuit with integrated varactor diode in parallel to the external tank circuit to improve the distortion bahaviour in case of detuning.

4. Multipath detector
   A wideband multipath detector with analog output is available.

5. A/D converter for fieldstrength and multipath detector
   The 7 bit A/D converter has two input channels and works as successive approximation converter. The conversion time for both input signals is t = 32 µs. The 7-bit digital-words from both channels (14 bit) are read out together via bus into two bytes with the read subaddress 82H. The input voltage range for both channels is 0...VREFD5V.

6. IF counter and multipath/fieldstrength evaluation for STS
   FM center frequencies ar available in two ranges set by bit D7 in subaddress 05H. For D7=1 the range of centerfrequency is 20.800 MHz...22.3875 MHz in 128 steps (12.5 kHz per step). For D7=0 the range of centerfrequency is 10.400 MHz...11.1937 MHz in 128 steps (6.25 kHz per step).
   The gate time is adjustable in 8 steps from 320us...40.96ms and the tolerance of the accepted count value, the window is adjustable in 5 steps from +/- (6.25kHz...100kHz) for D7=0 in sub-address 05H and

+/- (12.5 kHz...200 kHz) for D7=1 in subaddress 05H. The results IF_CENT and IF_WINDOW are read out via bus (read-subaddress 82H&83H) or pin Station_Detect.
If the IF frequency is into the preselected window, Station_Detect goes from high to low level. If the IF frequency is outside the preselected window, Station_Detect is high. The bit IF_WINDOW is a hint IF-frequency that is to low (IF_WINDOW=high) or is to high (IF_WINDOW=low).
In addition to the frequency measurement, thresholds for multipath and field-strength voltages can be programmed via bus (subaddress 0BH).
Station_Detect will only go to low level in case of field-strength and multipath voltages are beyond the thresholds and the frequency is inside the window.
When setting the thresholds to zero multipath and fieldstrength evaluation is disabled.

7. Crystal oscillator
   A master crystal oscillator provides all necessary clock frequencies for the whole IC. A 61.5 MHz crystal is used in 3rd harmonic mode.
   The oscillator frequency can fine tuned with a serial bus controlled 4 bit D/A converter.
   The crystal frequency is used as reference frequency for the PLL oscillator and IF counter. It is also used as clock for the ADC’s. Finally the crystal frequency divided by 6 (10.25 MHz) is available at a pin as low pass filtered voltage, it can be disabled with the serial bus.

8. Output ports
   PORT_1 / 2 are NMOS Open drain outputs.

9. I^2C Bus
   The TUA4401K supports the I^2C bus protocol (2 wire). All bus pins (SCL, SDA) are Schmitt triggered input buffer for 3V or 5V µC.
   The bit stream begins with the most significant bit (MSB), is shifted in (write mode) on the low to high transition of CLK and is shifted out (read mode) on the high to low transition of CLK

   I^2C bus mode:
   Data Transition:
   Data transition on the pin SDA must only occur when the clock SCL is low. SDA transitions while SCL is high will be interpreted as start or stop condition.

   Start Condition (STA):
   A start condition is defined by a high to low transition of the SDA line while SCL is at a stable high level.This start condition must precede any command and initiate a data transfer onto the bus.

   Stop Condition (STO):
   A stop condition is defined by a low to high transition of the SDA while the SCL line is at a stable high level. This condition terminate the communication between the devices and forces the bus interface into the initial conditions.

Acknowledge (ACK):
Indicates a successful data transfer. The transmitter will release the bus after sending 8 bit of data. During the 9th clock cycle the receiver will pull the SDA line to low level to indicate it has receive the 8 bits of data correctly.

Data Transfer Write Mode:
To start the communication, the bus master must initiate a start condition, followed by the 8bit chip address (write). The chip address for the TUA 4401 is fixed as ”1100110” (MSB at first). The last bit (LSB=A0) of the chip address byte defines the type of operation to be performed:
A0=1, a read operation is selected and A0=0, a write operation is selected.
After this comparison the TUA 4401 will generate an ACK.
After this device addressing the desired subaddress byte and data bytes must be followed. The subaddresses determines which one of the 9 data bytes (00H...07H, 0BH) is transmitted first. At the end of data transition the master must be generate the stop condition.

Data Transfer Read Mode:
To start the communication in the read mode, the bus master must initiate a start condition, followed by the 8bit chip address (write: A0=0), followed by the sub address read (82H/83H), followed by the chip address (read: A0=1).
After that procedure the 16bit/8bit data register 82H/83H is read out. After the first 8 bit read out, the uP mandatory send LOW during the ACK-clock.
After the second 8 bit read out the uP mandatory send HIGH during the ACK-clock. At the end of data transition the master must be generate the stop condition.

10. PLL Synthesizer
R / N Counter
The TUA 4401K has 2 identical 16bit counter for R and N path. Input frequency for the R-counter is the buffered XTAL-frequency (61.5MHz). Tuning steps can be selected by the 16bit R-counter from f_R= 6.25kHz...100kHz.
Input frequency for the N-counter is the buffered LO-frequency (in FM mode 98.2MHz...118.7MHz).

Three State Phase Comparator
The phase comparator generates a phase error signal according to phase difference between f_R (R counter output) and f_N (N counter output).This phase error signal drives the charge pump current generator.

Charge Pump
The charge pump generates signed pulses of current. 4 current values are available.

Loop Amp
The integrated rail to rail loop amplifier allows an active loop filter design with external components.
Two modes are available with status bit D11: high speed and normal mode.

4 Applications

Contents of this Chapter

4.1 Application and Circuits

- FM only car radio receiver, background receiver

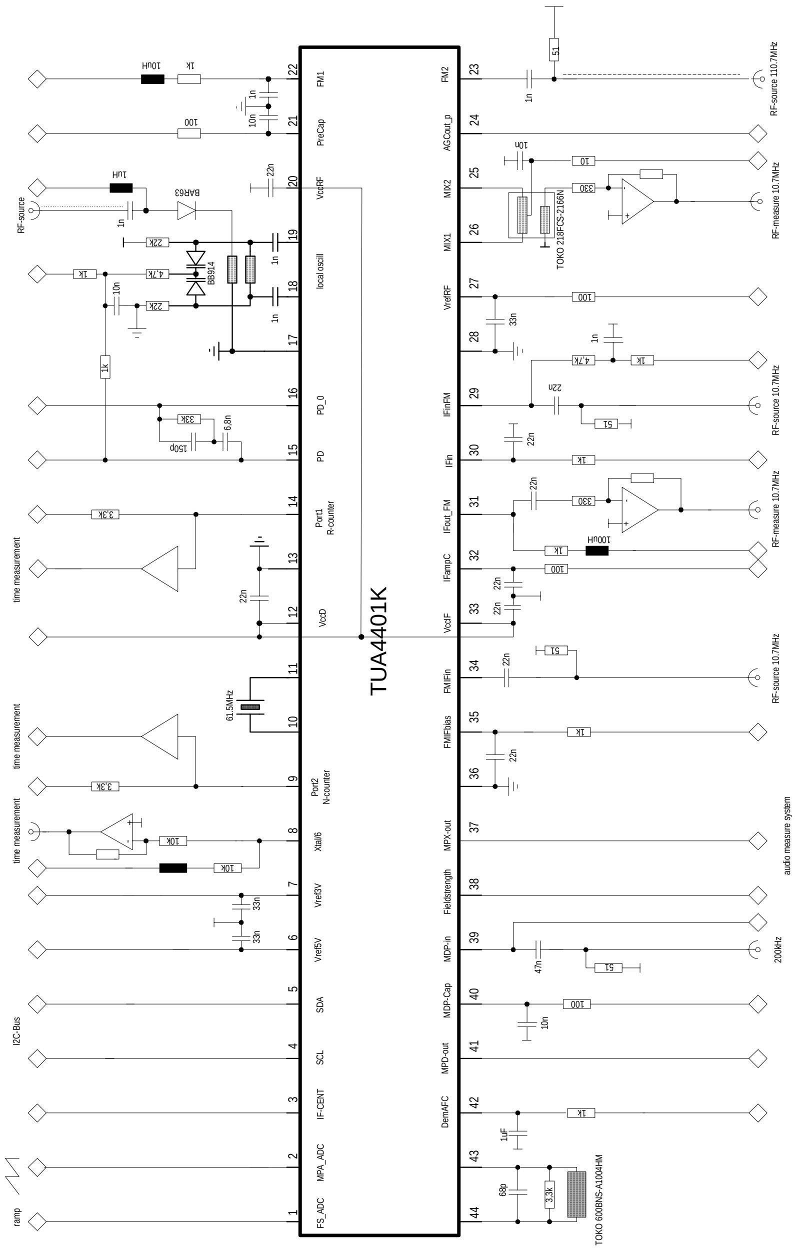
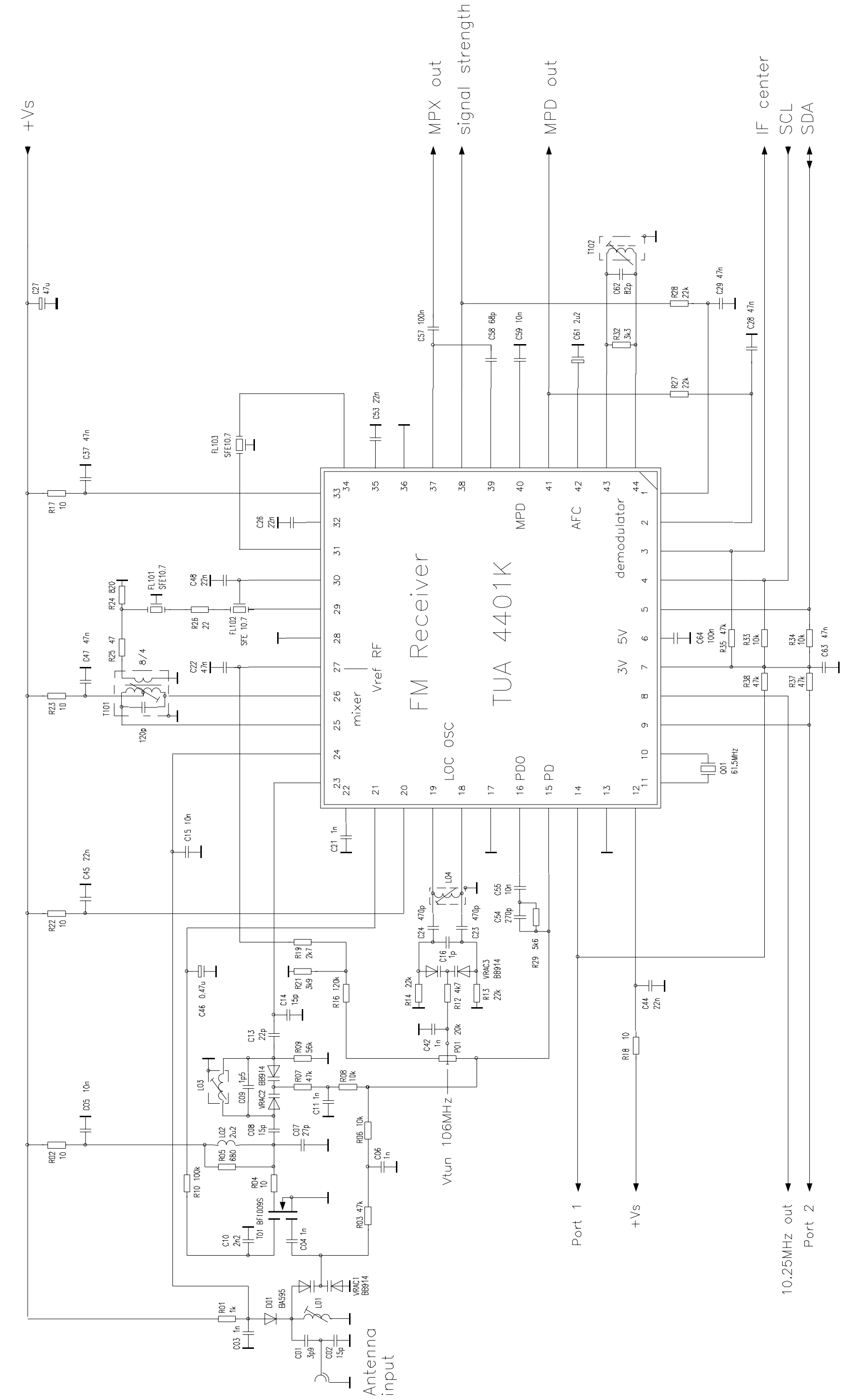


Figure 4-1 Test Circuit



4401K_SPEC.eps

Figure 4-2 Application Circuit

5 Reference

Contents of this Chapter

5.1 Electrical Data

5.1.1 Absolute Maximum Range

The maximal ratings may not be exceeded under any circumstances, not even momentary and individual, as permanent damage to the IC will result.

Table 5-1 Absolute Maximum Range

Parameter	Symbol	Limit Values min	Limit Values max	Unit
ESD-Protection all bipolar pins HBM (R=1.5kΩ , C=100pF)	V_{ESD}	- 1	1	kV
ESD-Protection all CMOS pins HBM (R=1.5kΩ , C=100pF)	V_{ESD}	-1	1	kV
Total power dissipation	P_{tot}		900	mW
Ambient temperature	T_A	- 40	85	°C
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	- 40	125	°C
Thermal resistance P-MQFP-44 (sys-air)	T_{thSA}		65	K/W

All values are referred to ground (pin), unless stated otherwise.
All currents are designated according to the source and sink principle, i.e. if the device pin is to be regarded as a sink (the current flows into the stated pin to internal ground), it has a negative sign, and if it is a source (the current flows from Vs across the designated pin), it has a positive sign.

5.1.2 Operating Range

Within the operational range the IC operates as described in the circuit description.
The AC / DC characteristic limits are not guaranteed.

Table 5-2 Operating Ratings

Parameter	Symbol	Limit Values min	Limit Values max	Unit	Test Conditions	L	Item
Supply voltage	V_{VCC}	8	9	V			
Current consumption	I_{vcc}		111	mA			
Ambient temperature	T_A	- 40	85	°C			

5.1.3 AC/DC Characteristics

AC / DC characteristics involve the spread of values guaranteed in the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 8.5 V

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Power Supply								
Total current consumption	I_{VCC}		85	111	mA			
1st local oscillator								
Frequency range	$f_{1st\ LO}$	50		250	MHz			
Frequency range	$f_{1st\ LO}$	50		150	MHz	Q factor of coil > 90		
Frequency range	$f_{1st\ LO}$	160		250	MHz	coil tbf; see SUB06h		
Negative input impedance	Z_{18-19}		- 1000		Ω	f = 100 MHz	L	
RF mixer								
Mixer current	Imix	11	14	17	mA			101
Input frequency	f_{22-23}	60		140	MHz			
Max input RF level	V_{22-23}	120			dBµV			
Input impedance single ended	R_{22-23}		1.8		kΩ		L	
	C_{22-23}		2.5		pF		L	
Mixer gain	A_{mix}	12	15	18	dB			259
Input IP3			126		dBµV	IM = 60 dB	L	
Noise Figure	F		6		dB		L	
Reference voltage RF section	V_{27}	4.3	4.8	5.3	V			104
Prestage AGC outputs								
AGC threshold range	V_{22-23}	48	60	72	mV	see diagram SUB06h		310 311
AGC threshold range	V_{22-23}	36	45	54	mV	see diagram SUB06h		312 313
AGC threshold range	V_{22-23}	24	30	36	mV	see diagram SUB06h		314 315
AGC threshold range	V_{22-23}	10	15	20	mV	see diagram SUB06h		316 317
AGC voltage for MOSFET Gate 2	V_{21}	5.7	6.4		V	V_{22-23} = 0 mV		106
AGC voltage for MOSFET Gate 2	V_{21}			0.1	V	V_{22-23} = 200 mV		300
AGC current normal polarity	I_{24}	10	13		mA	V_{22-23} = 0 mV		115

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 8.5 V (continued)

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
AGC current normal polarity	I_{24}			0.1	mA	$V_{22\text{-}23}$ = 200 mV		301
Integrator current	I_{21}	-75	-50	-25	µA	$V_{22\text{-}23}$ = 0 mV; Vm = 3V		117
Integrator current	I_{21}	25	50	75	µA	$V_{22\text{-}23}$ = 200 mV; Vm = 3V		303
IF amplifier								
DC input voltage	V_{29}	3.4	3.7	4.0	V			108
Input resistance	R_{29}		330		Ω		L	
Output resistance	R_{31}		330		Ω		L	
Max. Voltage gain	$A_{31\text{-}29}$	23	26	29	dB	see diagram SUB07h		403
Min. Voltage gain	$A_{31\text{-}29}$	10	13	16	dB	see diagram SUB07h		405
Noise figure	F		7		dB	R_G = 330 Ω		
IF limiter amplifier / fieldstrength generator								
Input voltage for limiter threshold	V_{34}		25	45	μV_{rms}	f_{in} = 10.7 MHz; V_{37} - 3 dB		470
AM suppression	A_{AM}	70	80		dB	m = 30 %, V_{34}=100mV		469
Fieldstrength voltage	V_{38}		0.4	0.8	V	V_{34} = 0 mV_{rms}		450
Fieldstrength voltage	V_{38}	1.5	1.9	2.3	V	V_{34} = 1 mV_{rms}		451
Fieldstrength voltage	V_{38}	2.4	2.9	3.4	V	V_{34} = 10 mV_{rms}		452
Fieldstrength voltage	V_{38}	3.6	4.2	4.8	V	V_{34} = 200 mV_{rms}		471
Fieldstrength dynamic range	V_{38dyn}		90		dB			
Fieldstrength linearity	V_{38lin}		±1		dB			
Fieldstrength temperature drift	V_{38temp}			±3	dB			
FM demodulator								
AF output voltage	V_{37}	500	600	720	mV_{rms}	ΔF = 75 kHz; f_{IF}=10.7 MHz		455
AF output voltage	V_{37}		300		mV_{rms}	ΔF = 75 kHz; f_{IF}= 21.4 MHz	L	
Total harmonic distortion	THD_{37}		0.3	0.6	%	ΔF = 75 kHz		456
Total harmonic distortion detuned	THD_{37}			0.8	%	f_{in} = 10.7 MHz ± 50 kHz; ΔF = 75 kHz		457

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 8.5 V (continued)

	Symbol	Limit Values min	typ	max	Unit	Test Conditions	L	Item
Multipath detector								
Attack current	I_{40}*)	700	900	1200	µA	V_{39} = 350 mV_{rms}; V_m = 5 V		801
Recovery current	I_{40}*)	-8	-13	-18	µA	V_{39}= 0 V_{rms}; V_m = 3.6 V		802
Start voltage	V_{41Def}		4.7		V	V_{39} = 0 V_{rms}		114
Detector characteristic	V_{41}	V_{41Def} -3.1 V	V_{41Def} -2.8 V	V_{41Def} -2.5 V	V	f_{39} = 200 kHz V_{39} = 40 mV_{rms}		800

*) Detector currents are measured between the output pin (-pole) and a voltage source V_m

	Symbol	min	typ	max	Unit	Test Conditions	L	Item
Crystal oscillator								
Operating frequency	f_{10-11}		61.5		MHz	3rd harmonic		
Negative input impedance	Z_{10-11}		- 250		Ω	f = 61.5 MHz		
Negative input impedance	Z_{10-11}		1.4		kΩ	f = 20.5 MHz		
Input impedance crystal	R_{cr}			70	Ω	3rd harmonic		
Spurious harmonics crystal	a_{sp}			- 20	dB	f < 200 MHz		
Bus controlled adjust range	Δf_{adj}		± 40		ppm	see diagram SUB06h		
Bus controlled output XTAL_DIV6	V_{XTAL_DIV6} on AC		500		mV_{pp}	f = 10.25 MHz, C_{load} = 10 pF		
Bus controlled output XTAL_DIV6	V_{XTAL_DIV6} on DC	1.0	1.5	2.0	V_{DC}	f = 10.25 MHz, C_{load} = 10 pF		180
Bus controlled output XTAL_DIV6	V_{XTAL_DIV6} off DC			50	mV_{DC}	C_{load} = 10 pF		197
Chargepump output (Loopfilter input)								
DC voltage	V_{PD_0}	2.3	2.5	2.7	V	locked		251 252
DC current	± I_{PD_03}	3.2	4	5.2	mA	see Status, Subaddress 00H, bit D1, D2 V_{PD_0} = 2.5V		220 to 227
DC current	± I_{PD_02}	1.6	2	2.6	mA			
DC current	± I_{PD_01}	0.8	1	1.3	mA			
DC current	± I_{PD_00}	400	500	700	uA			
Tristate output current	± I_{PD_0OFF}		0.1	10	nA	V_{PD_0} = 2.5V , guaranteed by design		228
Loop amplifier tuningvoltage output (Loopfilter output)								
LOW output voltage	V_{PDA_L}	0		400	mV	I_{TUNE} = 100 uA		231
HIGH output voltage	V_{PDA_H}	V_{VCC} -0.5V		V_{CC}	mV	I_{TUNE} = -100 uA		230

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 8.5 V (continued)

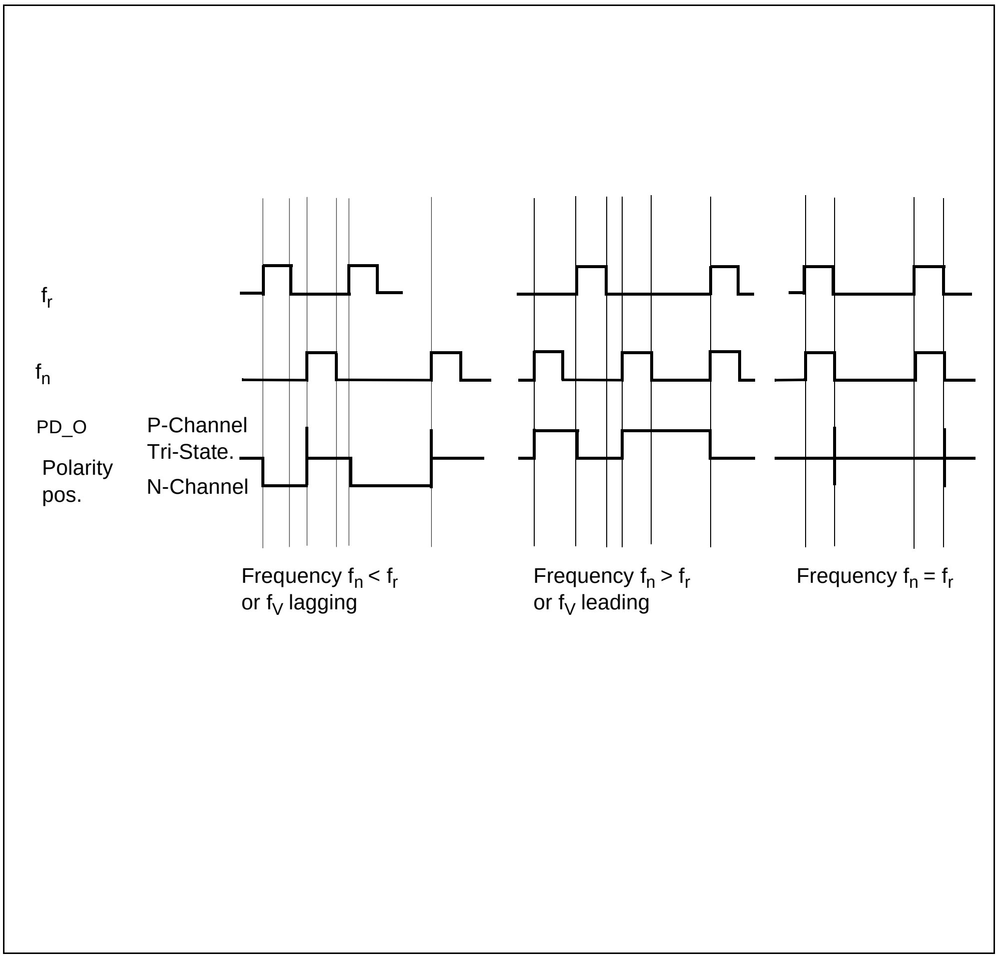
	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
HIGH output current source	I_{PDA_H}	-1.9	-2.4	-2.9	mA	V_{TUNE} = 4V, V_{PD_0} = 0V (see Status, Subaddress 00H, bit D11)		232
LOW output current source	I_{PDA_L}	-0.9	-1.2	-1.5	mA			233
PLL for synthesizer (see PLL Synthesizer on page 3-16)								
PLL / VCO step size (programmable via R-counter)	f_{ref}	6.25		100	kHz	$f_{crystal}$ = 61.5 MHz		
N-counter divide ratio	N	2		65535		16-Bit		200 to 207
R-counter divide ratio	R	2		65535		16-Bit		210 to 216
Port outputs, PORT_1, PORT_2, IF_CENT, IF_WINDOW (see Output ports on page 3-15)								
LOW output voltage	V_P	0	100	400	mV	I_P = 1 mA		*1)
HIGH Leakage current	I_{P_LEACK}	0		100	nA	V_P = 5 V		*2)

*1) 830, 840, 831, 834
*2) 118, 119, 124, 125

I^2C bus (SCL, SDA) (see I2C Bus Timing on page 5-12 and Bus Data Format on page 3-15)								
H-input voltage	V_{IH}	2.10		5.50	V			150
L-input voltage	V_{IL}	-0.5		0.90	V			150
Hysteresis of Schmitt trigger inputs (SCL, SDA)	V_{hys}	0.30			V			
Input capacity	C_I			5	pF			
I^2C bus leakage current	$I_{\_LEACK}$	0		1	µA	Values only valid for applied V_{CC}	L	

Ref voltages								
Ref voltage	V_6	4.5	5.0	5.5	V			102
Ref voltage	V_7	2.7	3.0	3.3	V			103

5.2 Phase detector outputs



5.3 Bus Interface

1. Bus Interface

I^2C Bus

2. Bus Data Format

I^2C Bus Write Mode

	MSB	CHIP ADDRESS (WRITE)						LSB		MSB	SUB ADDRESS (WRITE) 00H...07H, 0BH						LSB		MSB	DATA IN X...0 (X=7 or 15)						LSB		
STA	1	1	0	0	1	1	0	0	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	DX	...	D5	D4	D3	D2	D1	D0	ACK	STO

I^2C Bus Read Mode

	MSB	CHIP ADDRESS (WRITE)						LSB		MSB	SUB ADDRESS (READ) 82H/83H						LSB			MSB	CHIP ADDRESS (READ)						LSB	
STA	1	1	0	0	1	1	0	0	ACK	1	0	0	0	0	0	1	0	ACK	STA	1	1	0	0	1	1	0	1	ACK

MSB	DATA OUT FROM SUB ADD 82H						LSB		MSB	DATA OUT FROM SUB ADD 82H/83H						LSB		
R15	R14	R13	R12	R11	R10	R9	R8	ACK[1)]	R7	R6	R5	R4	R3	R2	R1	R0	ACK[2)]	STO

1): mandatory LOW send by uP, 2): mandatory HiGH send by uP

Chipaddress Organisation

Chip Address								
MSB							LSB	Function
1	1	0	0	1	1	0	0	Chip Address Write
1	1	0	0	1	1	0	1	Chip Address Read

Subaddress Organisation

Sub Addresses of Data Registers Write									
MSB	Bin						LSB	Hex	Function
0	0	0	0	0	0	0	0	00H	Status
0	0	0	0	0	0	0	1	01H	R_Counter
0	0	0	0	0	0	1	0	02H	N_Counter
0	0	0	0	0	0	1	1	03H	Mute_DAC7
0	0	0	0	0	1	0	0	04H	IF_COUNT_P1
0	0	0	0	0	1	0	1	05H	IF_COUNT_P2
0	0	0	0	0	1	1	0	06H	Specials
0	0	0	0	0	1	1	1	07H	Gain_DAC4
0	0	0	0	1	0	1	1	0BH	COMP-PRESET

Sub Address of Data Register Read									
MSB	Bin						LSB	Hex	Function
1	0	0	0	0	0	1	0	82H	Result Multipath, Fieldstrength, IF_Window and IF_Center
1	0	0	0	0	0	1	1	83H	Result-MISC

Data Byte Specification

Status Subaddress 00H	
Bit	Function
MSB D15	not used (must be=0)
D14	Port_2 (0=low, 1=high)
D13	Port_1 (0=low, 1=high)
D12	not used (must be=0)
D11	Loopamp current
D10	not used (must be=0)
D9	not used (must be=0)
D8	not used (must be=0)
D7	ADC_Single
D6	ADC_Mode
D5	ADC_ON
D4	IF_DAC4
D3	not used (must be=0)
D2	CP_Current 2
D1	CP_Current 1
D0 LSB	CP_Mode

R_Counter Subaddress 01H	
Bit	Function
MSB D15	2^{15}
D14	2^{14}
D13	2^{13}
D12	2^{12}
D11	2^{11}
D10	2^{10}
D9	2^{9}
D8	2^{8}
D7	2^{7}
D6	2^{6}
D5	2^{5}
D4	2^{4}
D3	2^{3}
D2	2^{2}
D1	2^{1}
D0 LSB	2^{0}

N_Counter Subaddress 02H	
Bit	Function
MSB D15	2^{15}
D14	2^{14}
D13	2^{13}
D12	2^{12}
D11	2^{11}
D10	2^{10}
D9	2^{9}
D8	2^{8}
D7	2^{7}
D6	2^{6}
D5	2^{5}
D4	2^{4}
D3	2^{3}
D2	2^{2}
D1	2^{1}
D0 LSB	2^{0}

Results Fieldstrength, Multipath and IF counter Subaddress 82H (read address)	
Bit	Function
MSB D15	IF_window
D14	Multipath_2^{6}
D13	Multipath_2^{5}
D12	Multipath_2^{4}
D11	Multipath_2^{3}
D10	Multipath_2^{2}
D9	Multipath_2^{1}
D8	Multipath_2^{0}
D7	IF_center
D6	Fieldstrength_2^{6}
D5	Fieldstrength_2^{5}
D4	Fieldstrength_2^{4}
D3	Fieldstrength_2^{3}
D2	Fieldstrength_2^{2}
D1	Fieldstrength_2^{1}
D0 LSB	Fieldstrength_2^{0}

Mute_DAC7 Subaddress 03H	
Bit	Function
MSB D7	Enable
D6	MDAC_6
D5	MDAC_5
D4	MDAC_4
D3	MDAC_3
D2	MDAC_2
D1	MDAC_1
D0 LSB	MDAC_0

IF_Count_P1 Subaddress 04H	
Bit	Function
MSB D7	Enable
D6	not used
D5	Win_2
D4	Win_1
D3	Win_0
D2	Gate_2
D1	Gate_1
D0 LSB	Gate_0

IF_Count_P2 Subaddress 05H	
Bit	Function
MSB D7	CF_Mod e
D6	CF_6
D5	CF_5
D4	CF_4
D3	CF_3
D2	CF_2
D1	CF_1
D0 LSB	CF_0

Specials Subaddress 06H	
Bit	Function
MSB D7	XTAL_DIV6
D6	VCO_2
D5	AGC_1
D4	AGC_0
D3	XTAL_3
D2	XTAL_2
D1	XTAL_1
D0 LSB	XTAL_0

IF_DAC4 Subaddress 07H	
Bit	Function
MSB D7	not used
D6	not used
D5	not used
D4	not used
D3	GDAC_3
D2	GDAC_2
D1	GDAC_1
D0 LSB	GDAC_0

COMP_PRESET Subaddress 0BH	
Bit	Function
MSB D15	not used
D14	Fieldstrength_2^{6}
D13	Fieldstrength_2^{5}
D12	Fieldstrength_2^{4}
D11	Fieldstrength_2^{3}
D10	Fieldstrength_2^{2}
D9	Fieldstrength_2^{1}
D8	Fieldstrength_2^{0}
D7	not used
D6	Multipath_2^{6}
D5	Multipath_2^{5}
D4	Multipath_2^{4}
D3	Multipath_2^{3}
D2	Multipath_2^{2}
D1	Multipath_2^{1}
D0 LSB	Multipath_2^{0}

Result Misc Subaddress 83H	
Bit Function	
MSB D7	IF_Window
D6	IF_Center
D5	Fieldstrength_Comp
D4	Multipath_Comp
D3	Res
D2	Res

D1	Res
D0 LSB	Res

Status, Subaddress 00H																
MSB							LSB	MSB							LSB	Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0			0		0	0	0					0				these bits must be = 0
0	1															opendrain Port_2 output = high level
0	0															opendrain Port_2 output = low level
0		1														opendrain Port_1 output = high level
0		0														opendrain Port_1 output = low level
0				1												Loopamp currentsource high ($I_{LOOPAMP}$=2.4mA) for high speed tuning
0				0												Loopamp currentsource low ($I_{LOOPAMP}$=1.2mA)
0								0	0	1						7 bit AD Converter enabled for single mode, stop
0								1	0	1						7 bit AD Converter enabled for single mode start. To restart single mode write the same bits once more.
0								0	1	1						7 bit AD Converter enabled for continuous mode run.
0								x	x	1						7 bit AD Converter enabled for single or continuous mode
0								x	x	0						7 bit AD Converter disabled for single and continuous mode
0											1					IF_DAC4 enabled (see subaddress 07H)
0											0					IF_DAC4 disabled (see subaddress 07H)
0													1	1		Chargepump current I_{cp3} = 4mA
0													1	0		Chargepump current I_{cp2} = 2mA
0													0	1		Chargepump current I_{cp1} = 1mA
0													0	0		Chargepump current I_{cp0} = 500uA
0															1	Chargepump enabled
0															0	Chargepump disabled

Subaddress 01H, R_Counter and Subaddress 02H, N_Counter																
MSB							LSB	MSB							LSB	Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Divider by 65535
0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	Divider by 2000
0	0	0	0	0	1	0	0	1	1	0	0	1	1	1	0	Divider by 1230
0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	Divider by 1000
0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	1	Divider by 615
0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	Divider by 100
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	Divider by 10
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	Divider by 2

Subaddress 03H, Mute_DAC7								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	1	1	not used (must be 1)

Subaddress 04H, IF_Count_P1								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1								IF_Count enabled
0								IF_Count disabled
	0							not used (must be=0)
		1	0	0				Window=+/-100kHz*
		0	1	1				Window=+/-50kHz*
		0	1	0				Window=+/-25kHz*
		0	0	1				Window=+/-12.5kHz*
		0	0	0				Window=+/-6.25kHz*
					1	1	1	Gatetime= 40.96ms
					1	1	0	Gatetime= 20.48ms
					1	0	1	Gatetime= 10.24ms
					1	0	0	Gatetime= 5.12ms
					0	1	1	Gatetime= 2.56ms
					0	1	0	Gatetime= 1.28ms
					0	0	1	Gatetime= 640us
					0	0	0	Gatetime= 320us

* Valid for D7= 0 in subaddress 05H

Multiply window value with 2 for D7= 1 in subaddress 05H

(e. g. D7= 0 Window =+/- 6.25 kHz

D7= 1 Window =+/- 12.5 kHz)

Subaddress 05H, IF_Count_P2, Centerfrequency = CF, CF_{step}= 6.25kHz) / 12.5 kHz								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1								Centerfrequency CF1
0								Centerfrequency CF0
1	1	1	1	1	1	1	1	CF1= 22.3875 MHz
0	1	1	1	1	1	1	1	CF0= 11.1937 MHz
1	1	0	0	0	0	0	0	CF1= 22.600 MHz
0	1	0	0	0	0	0	0	CF0= 10.800 MHz
1	0	1	1	0	0	0	1	CF1= 21.4125 MHz
0	0	1	1	0	0	0	1	CF0= 10.70625 MHz
1	0	1	1	0	0	0	0	CF1= 21.400 MHz
0	0	1	1	0	0	0	0	CF0= 10.700 MHz
1	0	1	0	1	1	1	1	CF1= 21.3875 MHz
0	0	1	0	1	1	1	1	CF0= 10.69375 MHz
1	0	1	0	0	0	0	0	CF1= 21.200 MHz
0	0	1	0	0	0	0	0	CF0= 10.600 MHz
1	0	0	1	0	0	0	0	CF1= 21.000 MHz
0	0	0	1	0	0	0	0	CF0= 10.500 MHz
1	0	0	0	0	0	0	0	CF1= 20.800 MHz
0	0	0	0	0	0	0	0	CF0= 10.400 MHz

Centerfrequencies for

D7=1 CF1= 20.800 MHz +n*12.5 kHz, CF_{Step}=12.5 kHz

D7=0 CF0= 10.400 MHz +n*6.25 kHz, CF_{Step}=6.25 kHz

n=0...127

Subaddress 06H, Specials								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1								XTAL_DIV6 enabled
0								XTAL_DIV6 disabled
	1							1st LO divided by 1
	0							1st LO divided by 2
		0	0					Prest. AGC threshold typ. 15 mV
		0	1					Prest. AGC threshold typ. 30 mV
		1	0					Prest. AGC threshold typ. 45 mV
		1	1					Prest. AGC threshold typ. 60 mV
				1	1	1	1	XTAL_adjust C_L = 15 pF
				1	1	1	0	XTAL_adjust C_L = 14pF
				1	1	0	1	XTAL_adjust C_L = 13 pF
				1	1	0	0	XTAL_adjust C_L = 12 pF
				1	0	1	1	XTAL_adjust C_L = 11 pF
				1	0	1	0	XTAL_adjust C_L = 10 pF
				1	0	0	1	XTAL_adjust C_L = 9 pF *)
				1	0	0	0	XTAL_adjust C_L = 8 pF *)
				0	1	1	1	XTAL_adjust C_L = 7 pF
				0	1	1	0	XTAL_adjust C_L = 6 pF
				0	1	0	1	XTAL_adjust C_L = 5 pF
				0	1	0	0	XTAL_adjust C_L = 4 pF
				0	0	1	1	XTAL_adjust C_L = 3 pF
				0	0	1	0	XTAL_adjust C_L = 2 pF
				0	0	0	1	XTAL_adjust C_L = 1pF
				0	0	0	0	XTAL_adjust C_L = 0pF

Subaddress 07H, IF_DAC4								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
x	x	x	x					not used
				1	1	1	1	IF_DAC Gain adj. typ. 16 dB
				1	1	1	0	IF_DAC Gain adj.
				1	1	0	1	IF_DAC Gain adj.
				1	1	0	0	IF_DAC Gain adj.
				1	0	1	1	IF_DAC Gain adj. typ. 21 dB
				1	0	1	0	IF_DAC Gain adj.
				1	0	0	1	IF_DAC Gain adj.
				1	0	0	0	IF_DAC Gain adj.
				0	1	1	1	IF_DAC Gain adj.
				0	1	1	0	IF_DAC Gain adj.
				0	1	0	1	IF_DAC Gain adj.
				0	1	0	0	IF_DAC Gain adj. typ. 24 dB
				0	0	1	1	IF_DAC Gain adj.
				0	0	1	0	IF_DAC Gain adj.
				0	0	0	1	IF_DAC Gain adj.
				0	0	0	0	IF_DAC Gain adj. typ. 26 dB

*) For continuous tuning characteristic it is recommended to skip steps 8 and 9

Subaddress 0BH, Comp preset																
MSB							LSB	MSB							LSB	Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
X								X								not used
	$FP2^6$	$FP2^5$	$FP2^4$	$FP2^3$	$FP2^2$	$FP2^1$	$FP2^0$									Preset value Fieldstrength
									$MP2^6$	$MP2^5$	$MP2^4$	$MP2^3$	$MP2^2$	$MP2^1$	$MP2^0$	Preset value Multipath

Subaddress 82H, Read results from Fieldstrength, Multipath and IF counter																
MSB							LSB	MSB							LSB	Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1								1								IF_counter result: IF frequency is outside the desired window. IF frequency is lower as the desired IF frequency.
0								1								IF_counter result: IF frequency is outside the desired window.IF frequency is higher as the desired IF frequency.
x								0								IF_counter result: IF frequency is inside the desired window
	$M2^6$	$M2^5$	$M2^4$	$M2^3$	$M2^2$	$M2^1$	$M2^0$									Result multipath byte M6...M0
									$F2^6$	$F2^5$	$F2^4$	$F2^3$	$F2^2$	$F2^1$	$F2^0$	Result fieldstrength byte F6...F0

Subaddress 83H, Read results misc								
MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1	1			Res	Res	Res	Res	IF_counter result: IF frequency is outside the desired window. IF frequency is lower as the desired IF frequency.
0	1			Res	Res	Res	Res	IF_counter result: IF frequency is outside the desired window.IF frequency is higher as the desired IF frequency.
x	0			Res	Res	Res	Res	IF_counter result: IF frequency is inside the desired window
		1						Fieldstrength is higher as the preseted value in subaddress 0BH (D8...D14)
		0						Fieldstrength is lower as the preseted value in subaddress 0BH (D8...D14)
			1					Multipathsignal is higher as the preseted value in subaddress 0BH (D0...D6)
			0					Multipathsignal signal is lower as the preseted value in subaddress 0BH (D0...D6)

5.4 I²C Bus Timing

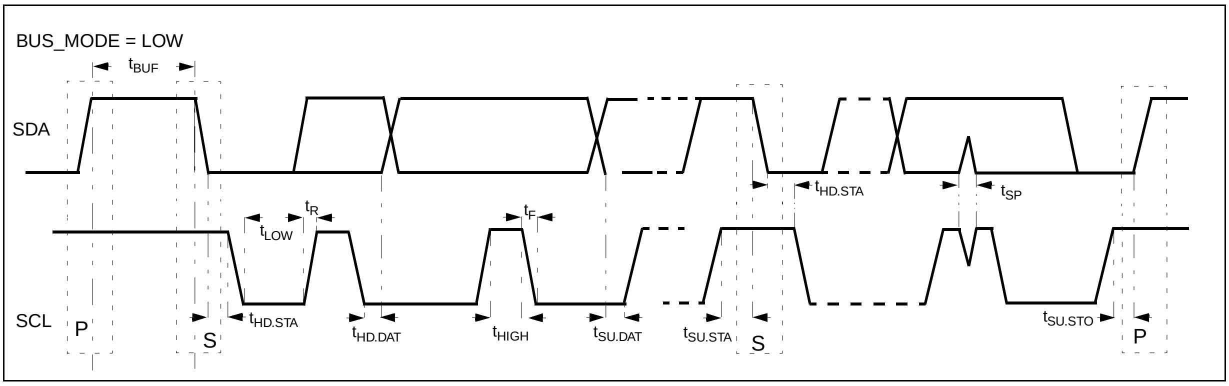


Table 5-4				
Parameter	**Symbol**	**min**	**max**	**Unit**
LOW level input voltage (SDA, SCL)	V_{IL}	-0.5	0.90	V
HIGH level input voltage (SDA, SCL)	V_{IH}	2.10	5.50	V
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
LOW level output voltage 3mA sink current (SDA)	V_{OL}	0	0.40	V
Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10pF to 400pFwith up to 3mA	t_{OF}	$20+0.1C_b$ [2)]	250	ns
SCL clock frequency	f_{SCL}	0	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	1.3		µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HO.STA}$	0.6		µs
LOW period of the SCL clock	t_{LOW}	1.3		µs
HIGH period of the SCL clock	t_{HIGH}	0.6		µs
Set-up time for a repeated START condition	$t_{SU.STA}$	0.6		µs
Data hold time	$t_{HD.DAT}$	0		ns
Data set -up time	$t_{SU.DAT}$	100		ns
Rise, fall time of both SDA and SCL signals	t_R, t_F	$20+0.1C_b$ [2)]	300	ns
Set-up time for STOP condition	$t_{SU.STO}$	0.6		µs
Capacitive load for each bus line	C_b		400	pF

[2)] C_b= capacitance of one bus line in pF.
Note that the maximum t_F for the SDA and SCL bus lines quoted at 300ns is longer than the specified maximum t_{OF} for the output stages (250ns).This allows series protection resistors to be connected between the SDA / SCL pins and the SDA /SCL bus lines without exceeding the maximum specified t_F.