MOTOROLA
Semiconductors
Avenue Général-Eisenhower - 31023 Toulouse CEDEX - FRANCE

UAA2022

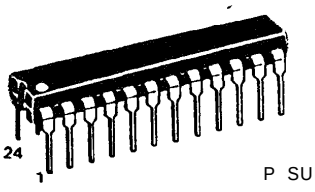
16 SEGMENT LED DRIVER

The UAA2022 is a 16-bit serial data input to a 16-segment LED driver. Brightness control of common anode LED's from an external control voltage is possible. The UAA2022 is particularly suitable for Hi-Fi applications and is implemented in I^2L linear technology.

- LED brightness control voltage
- Current source Segment driver Outputs
- No external resistors for Segment currents
- Non-multiplexed, therefore no RFI
- Cascadable

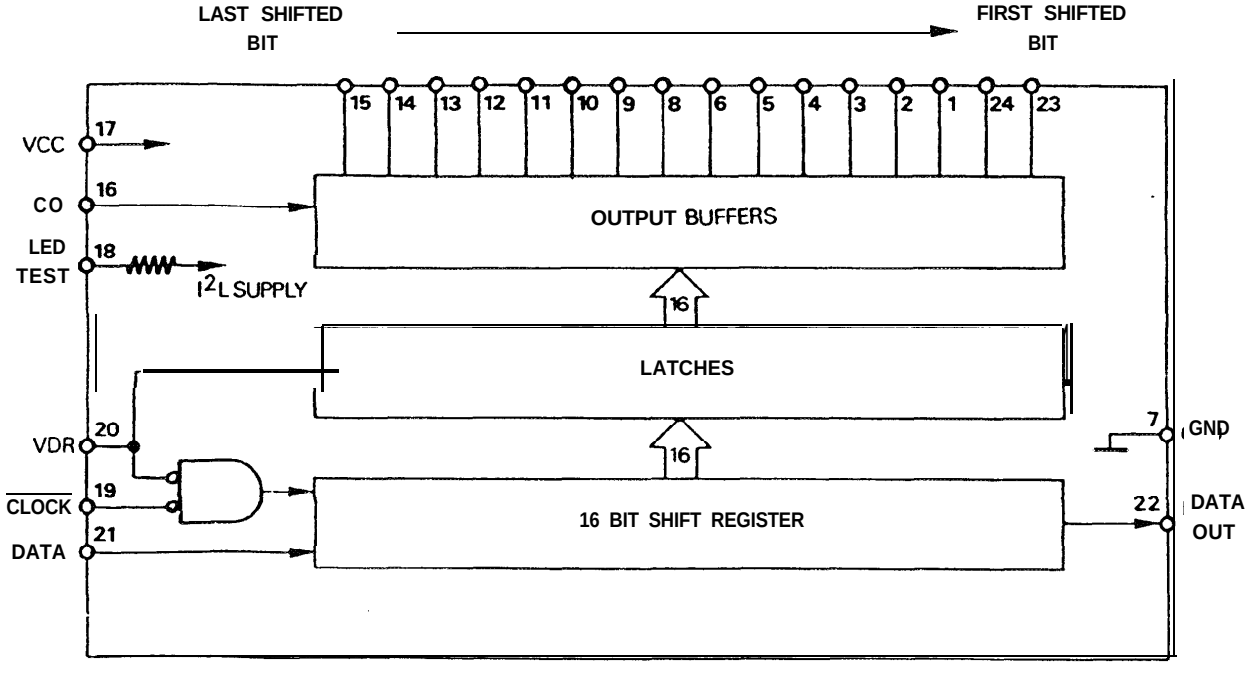
16 SEGMENT LED DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT



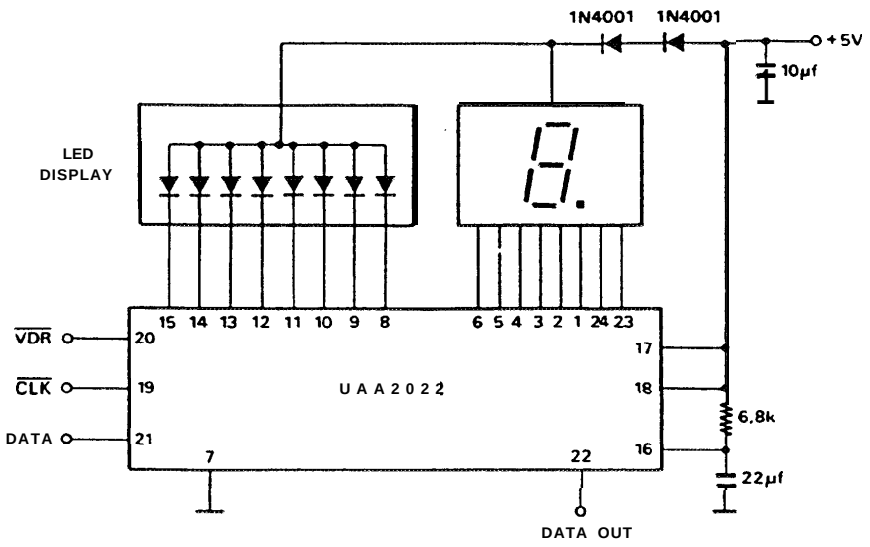
P SUFFIX
PLASTIC PACKAGE
CASE 724

FIGURE 1 -BLOCK DIAGRAM AND **PIN** ASSIGNMENT



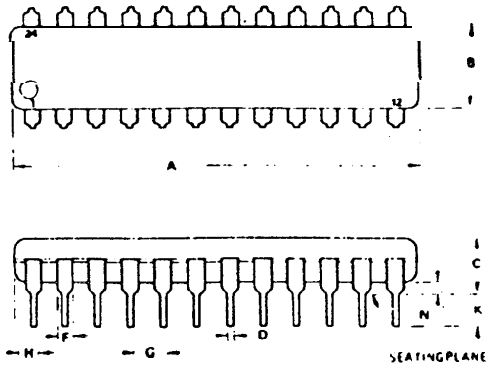
July 1983

FIGURE 4 — TYPICAL **APPLICATION**



OUTLINE DIMENSIONS

P SUF FIX
PLASTIC PACKAGE
CASE 724



NOTE:
1. LEADS, TAUE POSITIONED WITHIN 0.25 mrn (0.010) OIA ATSEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM. "0")

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.13	1.260	1.286
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.35	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040

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Avenue **Général-Eisenhower** - 31023 **Toulouse** CEDEX - FRANCE
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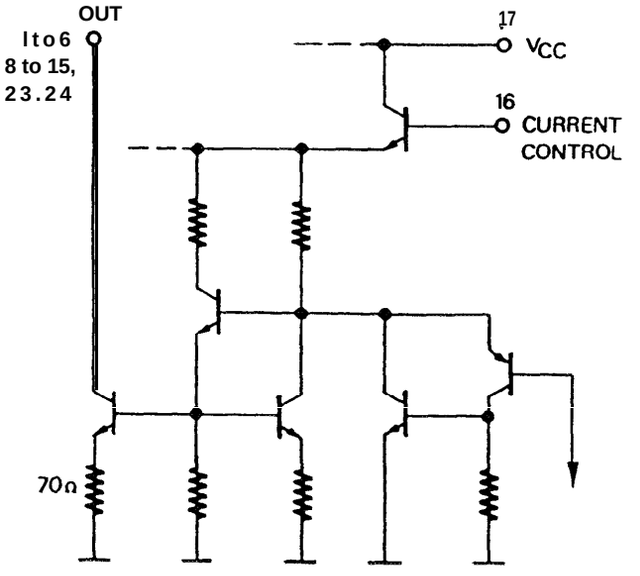
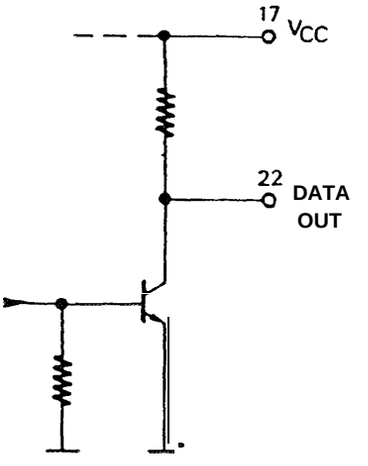
FIGURE 2 – CIRCUIT CONFIGURATIONS

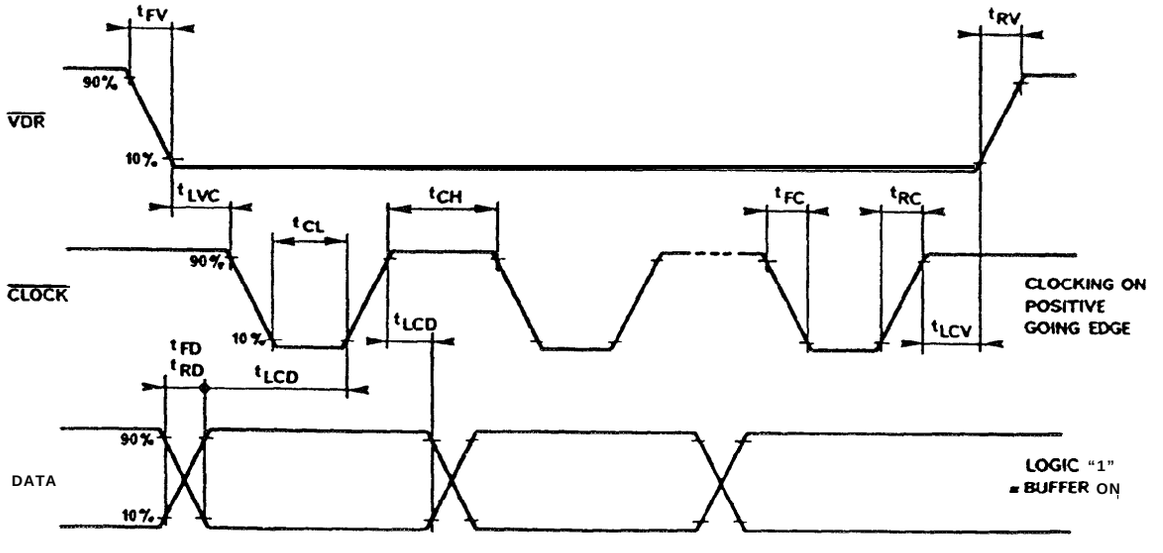


a) Output Buffers for LED's



b) Output Stage of Data Output

FIGURE 3 -DEFINITION OF SWITCHING TIMES



CIRCUIT DESCRIPTION

he UAA2022 is intended to control common anode ED's and allows brightness Variation from an external ontrol voltage. Since it is not multiplexed it is particularly ıited for hi-fi applications etc.

'he circuit receives 16 bit serial data by means of the igital inputs $\overline{VDR}$ (chip select), $\overline{Clock}$ and Data (TTL-evels). The information is fed into a shift-register, and nen is stored in latches which in turn control the output uffers. These output buffers (segment drivers) have urrent source characteristics (see figure 2a), thus no xternal resitors are needed to set up the Segment currents for 100 % luminosity).

'igure 3 shows the timing diagram of the circuit. On the ıegative going VOR-edge the latches are disconnected from the shift register and new information is shifted in. On the positive VDR-edge the latches are reconnected, thus transferring new information to the Outputs. (See f igure 2a.)

The shift register also has a data output. (See figure 2b.) This allows the microprocessor to pass data through the UAA 2022, and thus drive further circuits from the same data and chip-select pins. The UAA 2022 shifts and Outputs data on the positive going clock edge. Thus for reliable data transfer, it has to be the first circuit in the line, when connected in series with circuits which shift on the negative going clock edge. The circuit is cascadable and can be cascaded with the UAA2000 and UAA2001/2010.

INPUT/OUTPUT FUNCTIONS

3UFFER OUTPUTS —(pins 1 to 6, 8 to 15, 23, 24)

These Outputs have current source characteristics to drive :he LED segments without external resistances.

CURRENT CONTROL — (pin 16)

Serves to vary the output currents of the buffers. This pin has to be connected to VCC (pin 17) for maximum iuminosity. The buffer currents decrease linearly with the control voltage, going down to zero at about 2V.

LED — TEST —(pin 18)

This pin supplies the logic section of the circuit, when connected to ground all output buffers are switched on.

CLOCK — (pin 19)

This pin delivers the clock signal to the shift register, which accepts shifts and Outputs data on the positive going edge. It should be noted that within the $\overline{VDR}$-window, when $\overline{VDR}$ is low, the clock has to be high at the beginning and the end of the clock pulse train.

$\overline{VDR}$ —(pin 20)

This pin is the chip select and is active when low.

DATA — (pin 2 1)

Data is entered into the device serially via this pin and passed directly into the shift register- In turn, this controls the latches and output buffers. (Logic "1" = Buffer ON)

DATA OUT —(pin 22)

Is the data output of the shift register- Allows cascading with circuits operating on the same $\overline{VDR}$ and clock signals.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, T_A=25°C)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Logic Input Levels, $\overline{VDR}$, $\overline{Clock}$, Data	19, 20, 21	V_{LOG}				
Low State			0		0.8	V
High State			2		6	V
Logic Input Currents		I_{LOG}				
Low State					− 100	μA
High State					10	μA
Control Voltage Range[1]	16	V_{CO}	0		V_{CC}	
Supply Voltage	17	V_{CC}	4.5		5.5	V
Control Current	16	I_{CO}			1	mA
Control Voltage, LED Test	18	V_{LE}				
Low Level (no Logic Supply, all Buffers ON)			0		0.5	V
High Level (normal Operation)			4.5V		V_{CC}	
Data Out (figure 2)						
Output Voltage, Logic "0" (1mA)	V_D				0.5	V
Internal Pull-Up Resistor					15	kΩ
Buffers	1 to 6, 8 to 15, 23, 24					
Mean Value of min. and max. Buffer Currents (V_{CO} = V_{CC}, V_{LE} = 0)		I_{BB}	9	11	13	mA
Buffer Current Variation around I_{BB}			− 7 %		+ 7 %	
Saturation Voltage		V_S		1.2	1.8	V
Output Impedance		r_{out}		100		kΩ
Leakage Current (V_{BB}=5V)		I_{BL}			10	μA
Supply Current LED-Test (V_{LE} = 5V)	18	I_{LE}	3	4.3	6	mA
Supply Current	17	I_{CC}	18		50	mA
Power Dissipation, all Buffers ON (V_{CO} = V_{LE} = V_{CC}) at V_{BB} = 2.9V				650		mW
Ambient Temperature		T_A	0		70	°C
Package Thermal Resistance		R_{th}		70		°C/W

All Voltages referenced to ground (Pin 7)

1) Brightness goes to zero at 2V

MAXIMUM RATINGS (TA= 25°C)

Rating	Pin	Symbol	Value	Unit
Logic Input Voltages	19, 20, 21	V_{LOG}	10	V
Con trol Vol tage	16	V_{CO}	10	V
Supply Voltage	17	V_{CC}	10	V
Control Voltage	18	V_{LE}	10	V
Data-Out, max. Voltage (I_D = 2mA)	22	V_D	10	V
Buffers Output Voltage (V_{CC} = V_{CO} = 5.5V) All Buffers ON	1 to6 8to 15 23, 24	V_{BB}	6	V
Storage Temperature		T_{STG}	−50 to +150	°C
Operating Ambient Temperature		T_A	0 to 70	°C

All voltages referenced to ground (Pin 7)

SWITCHING CHARACTERISTICS (TA= 0 to 70°C, see figure 3)

Characteristic	Symbol	Min	Max	Unit
Clock "High"-Time	t_{CH}	3		µs
Clock "Low"-Time	t_{CL}	3		µs
Negative going $\overline{VDR}$ Edge to first Clock Edae	t_{LVC}	10		µs
Last Clock Edge to positive going $\overline{VDR}$ Edge	t_{LCV}	1		µs
Data Change to positive going Clock Edge	t_{LDC}	1		µs
Positive going Clock Edge to Data Change	t_{LCD}	3		µs
Rise Times of Digital Inputs $\overline{VDR}$, $\overline{Clock}$, Data	t_{RV}, t_{RC}, t_{RD}		2	µs
Fall Timet of Digital Inputs $\overline{VDR}$, $\overline{Clock}$, Data	t_{FV}, t_{FC}, t_{FD}		2	µs