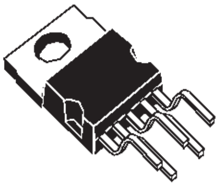
TDA2030

14W Hi-Fi AUDIO AMPLIFIER

DESCRIPTION

The TDA2030 is a monolithic integrated circuit in Pentawatt® package, intended for use as a low frequency class AB amplifier. Typically it provides 14W output power (d = 0.5%) at 14V/4Ω; at ± 14V or 28V, the guaranteed output power is 12W on a 4Ω load and 8W on a 8Ω (DIN45500).
The TDA2030 provides high output current and has very low harmonic and cross-over distortion.
Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shut-down system is also included.



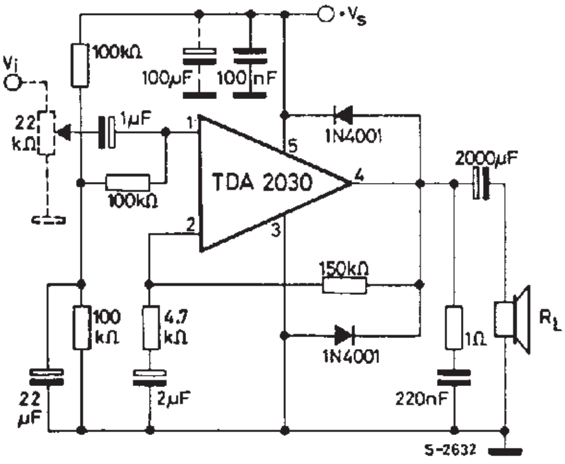
Pentawatt

ORDERING NUMBERS : TDA2030H
TDA2030V

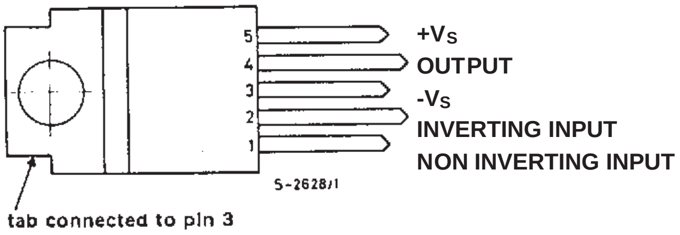
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply voltage	± 18 (36)	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Output peak current (internally limited)	3.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Stoprage and junction temperature	-40 to 150	°C

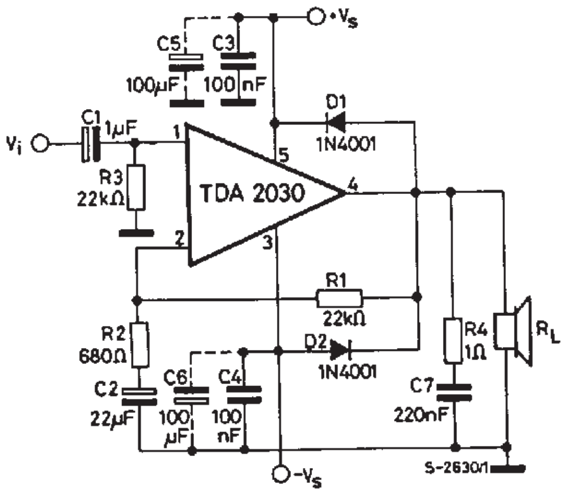
TYPICAL APPLICATION



PIN CONNECTION (top view)



TEST CIRCUIT



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-case max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = \pm 14V$, $T_{amb} = 25°C$ unless otherwise specified) for single Supply refer to fig. 15 Vs = 28V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 6 12		± 18 36	V
I_d	Quiescent drain current	$V_s = \pm 18V$ (Vs = 36V)		40	60	mA
I_b	Input bias current			0.2	2	μA
V_{os}	Input offset voltage			± 2	± 20	mV
I_{os}	Input offset current			± 20	± 200	nA
P_o	Output power	d = 0.5% $G_v = 30$ dB f = 40 to 15,000 Hz $R_L = 4\Omega$ $R_L = 8\Omega$	12 8	14 9		W W
		d = 10% $G_v = 30$ dB f = 1 KHz $R_L = 4\Omega$ $R_L = 8\Omega$		18 11		W W
d	Distortion	$P_o = 0.1$ to 12W $R_L = 4\Omega$ $G_v = 30$ dB f = 40 to 15,000 Hz		0.2	0.5	%
		$P_o = 0.1$ to 8W $R_L = 8\Omega$ $G_v = 30$ dB f = 40 to 15,000 Hz		0.1	0.5	%
B	Power Bandwidth (-3 dB)	$G_v = 30$ dB $P_o = 12W$ $R_L = 4\Omega$	10 to 140,000			Hz
R_i	Input resistance (pin 1)		0.5	5		MΩ
G_v	Voltage gain (open loop)			90		dB
G_v	Voltage gain (closed loop)	f = 1 kHz	29.5	30	30.5	dB
e_N	Input noise voltage	B = 22 Hz to 22 KHz		3	10	μV
i_N	Input noise current			80	200	pA
SVR	Supply voltage rejection	$R_L = 4\Omega$ $G_v = 30$ dB $R_g = 22$ kΩ $V_{ripple} = 0.5\ V_{eff}$ $f_{ripple} = 100$ Hz	40	50		dB
I_d	Drain current	$P_o = 14W$ $R_L = 4\Omega$ $P_o =$ W $R_L = 8\Omega$		900 500		mA mA

Figure 1. Output power vs. supply voltage

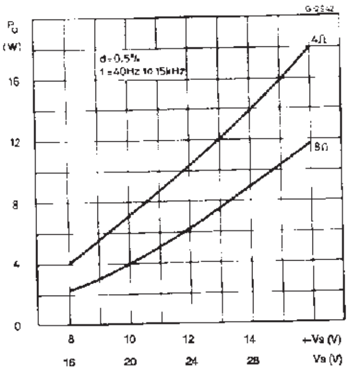


Figure 2. Output power vs. supply voltage

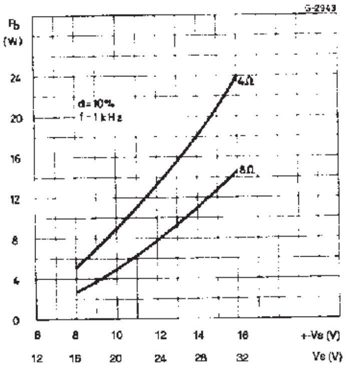


Figure 3. Distortion vs. output power

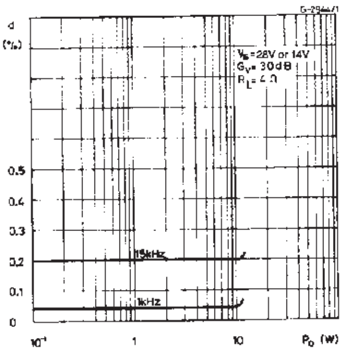


Figure 4. Distortion vs. output power

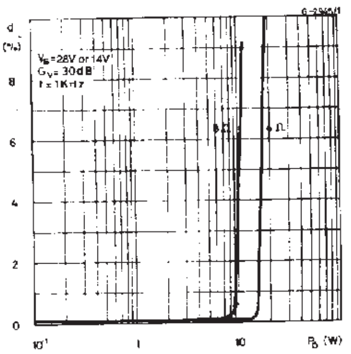


Figure 5. Distortion vs. output power

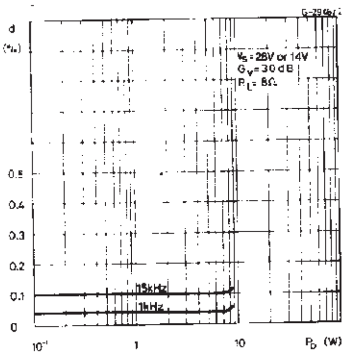


Figure 6. Distortion vs. frequency

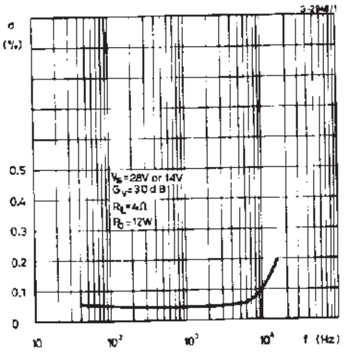


Figure 7. Distortion vs. frequency

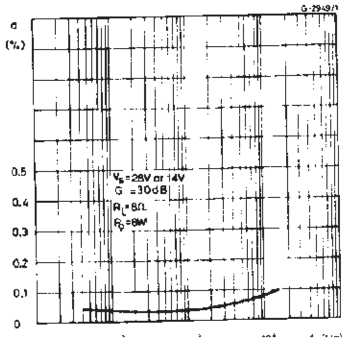


Figure 8. Frequency response with different values of the rolloff capacitor C8 (see fig. 13)

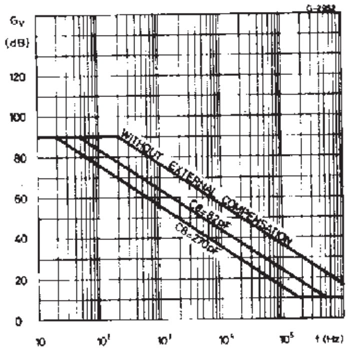


Figure 9. Quiescent current vs. supply voltage

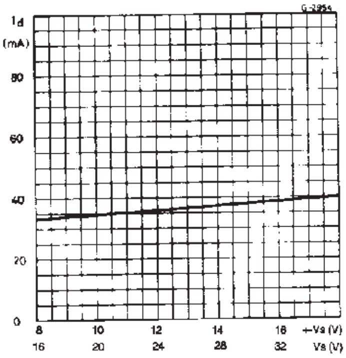


Figure 10. Supply voltage rejection vs. voltage gain

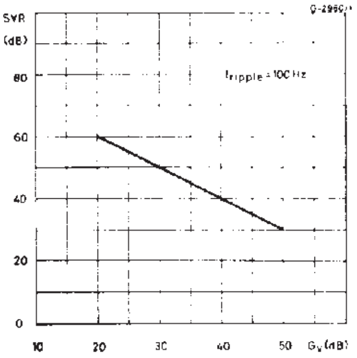


Figure 11. Power dissipation and efficiency vs. output power

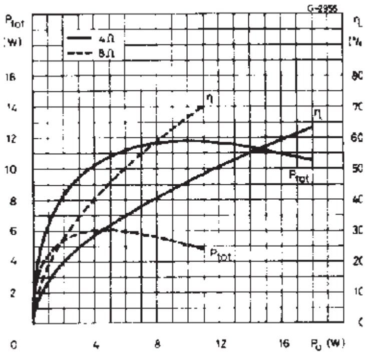
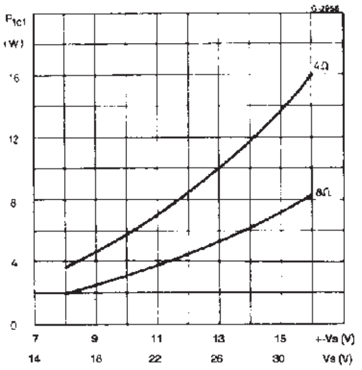


Figure 12. Maximum power dissipation vs. supply voltage (sine wave operation)



APPLICATION INFORMATION

Figure 13. Typical amplifier with split power supply

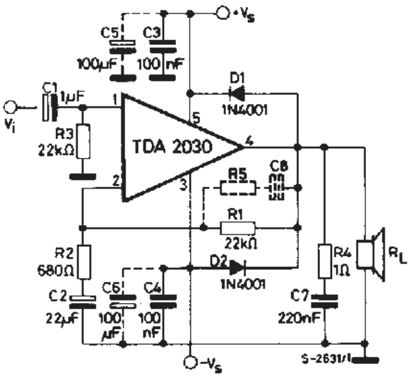
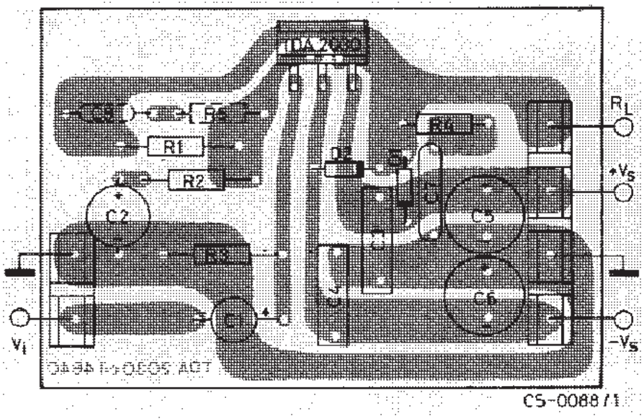


Figure 14. P.C. board and component layout for the circuit of fig. 13 (1 : 1 scale)



APPLICATION INFORMATION (continued)

Figure 15. Typical amplifier with single power supply

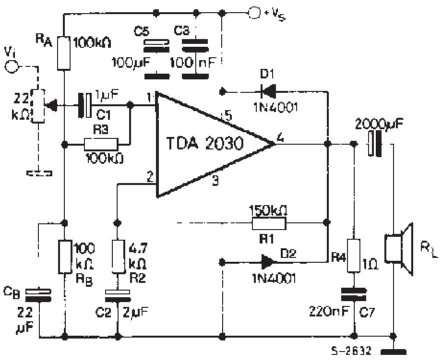


Figure 16. P.C. board and component layout for the circuit of fig. 15 (1 : 1 scale)

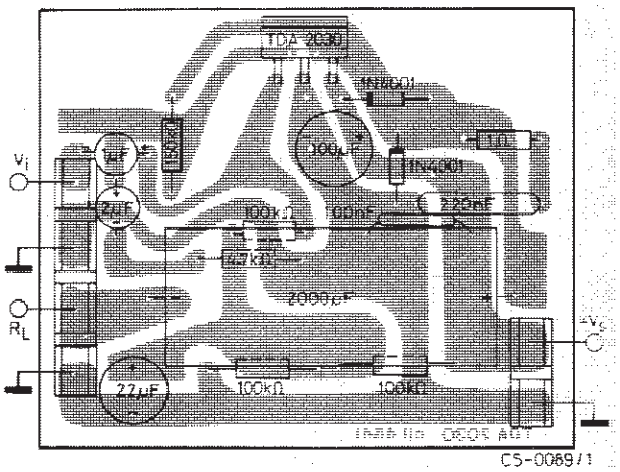
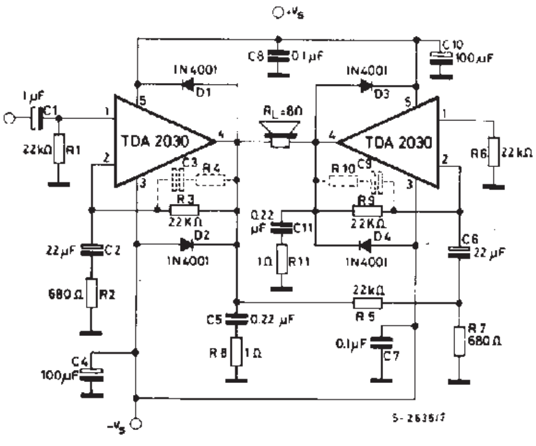


Figure 17. Bridge amplifier configuration with split power supply (P_O = 28W, V_S = ±14V)



PRACTICAL CONSIDERATIONS

Printed circuit board

The layout shown in Fig. 16 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

Assembly suggestion

No electrical isolation is needed between the package and the heatsink with single supply voltage configuration.

Application suggestions

The recommended values of the components are those shown on application circuit of fig. 13. Different values can be used. The following table can help the designer.

Component	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value
R1	22 kΩ	Closed loop gain setting	Increase of gain	Decrease of gain (*)
R2	680 Ω	Closed loop gain setting	Decrease of gain (*)	Increase of gain
R3	22 kΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R4	1 Ω	Frequency stability	Danger of osccilat. at high frequencies with induct. loads	
R5	≅ 3 R2	Upper frequency cutoff	Poor high frequencies attenuation	Danger of oscillation
C1	1 µF	Input DC decoupling		Increase of low frequencies cutoff
C2	22 µF	Inverting DC decoupling		Increase of low frequencies cutoff
C3, C4	0.1 µF	Supply voltage bypass		Danger of oscillation
C5, C6	100 µF	Supply voltage bypass		Danger of oscillation
C7	0.22 µF	Frequency stability		Danger of oscillation
C8	$\cong \frac{1}{2\pi \ B \ R1}$	Upper frequency cutoff	Smaller bandwidth	Larger bandwidth
D1, D2	1N4001	To protect the device against output voltage spikes		

(*) Closed loop gain must be higher than 24dB

SINGLE SUPPLY APPLICATION

Component	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value
R1	150 kΩ	Closed loop gain setting	Increase of gain	Decrease of gain (*)
R2	4.7 kΩ	Closed loop gain setting	Decrease of gain (*)	Increase of gain
R3	100 kΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R4	1 Ω	Frequency stability	Danger of osccilat. at high frequencies with induct. loads	
R_A/R_B	100 kΩ	Non inverting input Biasing		Power Consumption
C1	1 µF	Input DC decoupling		Increase of low frequencies cutoff
C2	22 µF	Inverting DC decoupling		Increase of low frequencies cutoff
C3	0.1 µF	Supply voltage bypass		Danger of oscillation
C5	100 µF	Supply voltage bypass		Danger of oscillation
C7	0.22 µF	Frequency stability		Danger of oscillation
C8	$\cong \frac{1}{2\pi\ B\ R1}$	Upper frequency cutoff	Smaller bandwidth	Larger bandwidth
D1, D2	1N4001	To protect the device against output voltage spikes		

(*) Closed loop gain must be higher than 24dB

SHORT CIRCUIT PROTECTION

The TDA2030 has an original circuit which limits the current of the output transistors. Fig. 18 shows that the maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area (Fig. 2). This function can therefore be considered as being peak power limiting rather than simple current limiting.

It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

Figure 18. Maximum output current vs. voltage [V_{CEsat}] across each output transistor

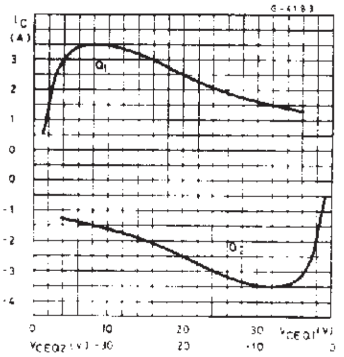
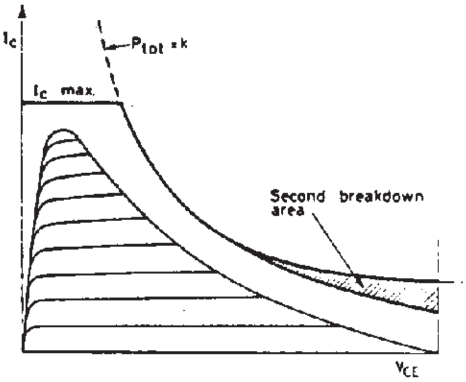


Figure 19. Safe operating area and collector characteristics of the protected power transistor



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1. An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2. The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation at the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 22 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Figure 20. Output power and drain current vs. case temperature ($R_L = 4\Omega$)

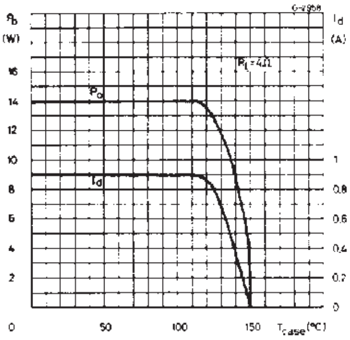


Figure 21. Output power and drain current vs. case temperature ($R_L = 8\Omega$)

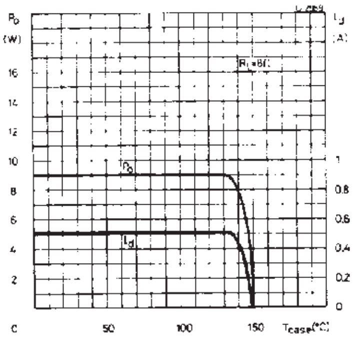


Figure 22. Maximum allowable power dissipation vs. ambient temperature

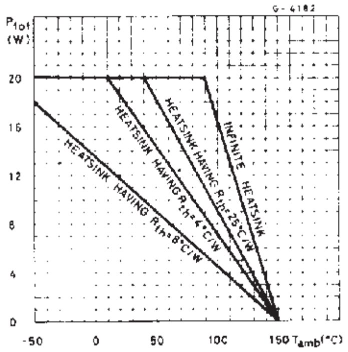
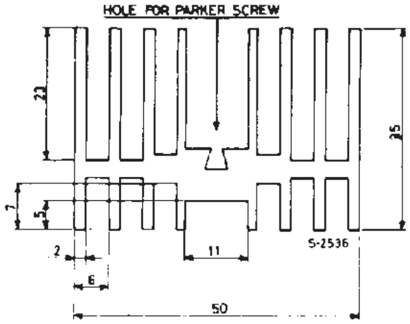


Figure 23. Example of heat-sink



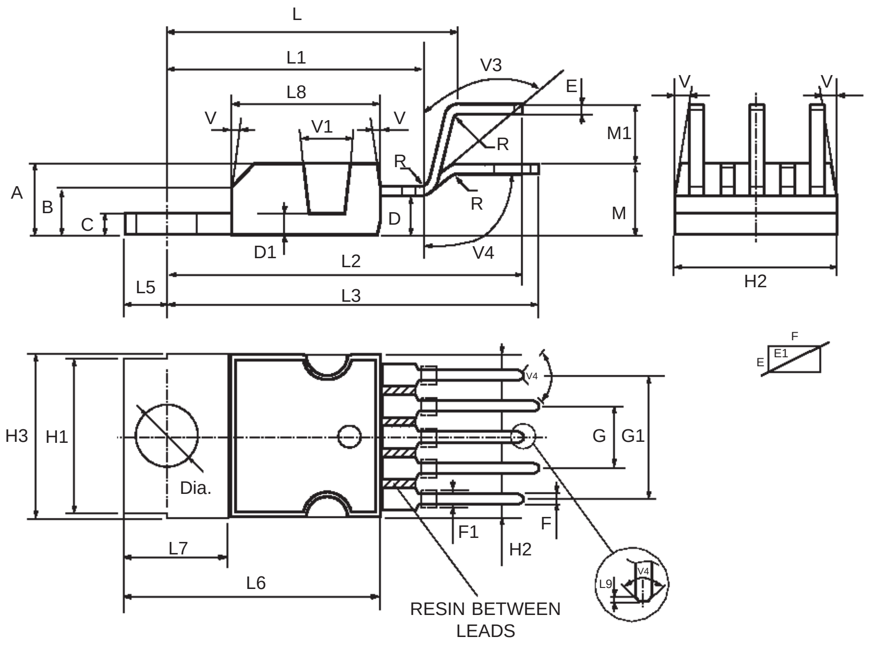
Dimension : suggestion.

The following table shows the length that the heatsink in fig. 23 must have for several values of P_{tot} and R_{th}.

Ptot (W)	12	8	6
Length of heatsink (mm)	60	40	30
Rth of heatsink (° C/W)	4.2	6.2	8.3

PENTAWATT PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
E1	0.76		1.19	0.030		0.047
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G	3.2	3.4	3.6	0.126	0.134	0.142
G1	6.6	6.8	7	0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L	17.55	17.85	18.15	0.691	0.703	0.715
L1	15.55	15.75	15.95	0.612	0.620	0.628
L2	21.2	21.4	21.6	0.831	0.843	0.850
L3	22.3	22.5	22.7	0.878	0.886	0.894
L4			1.29			0.051
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
L9		0.2			0.008	
M	4.23	4.5	4.75	0.167	0.177	0.187
M1	3.75	4	4.25	0.148	0.157	0.167
V4	40° (typ.)					
Dia	3.65		3.85	0.144		0.152



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