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DESIGN TIP

DT 98-1

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Variable Frequency Drive using IR215x Self-Oscillating IC's

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Purpose of this Design Tip

Applications such as high quality Electronic Ballast and Power Supply circuits often require continuous switch frequency control over a specific range. Alternatively, the need may arise to dynamically select one of several discrete drive frequencies using digital control signals. Both IR215x self-oscillating control IC's and IR5xHxxx Hybrid circuits are ideal for use in such areas and offer several advantages over traditional bridge drive methods. This design tip describes operation of the integral oscillator and shows how simple techniques and inexpensive peripheral circuitry may be utilized for variable frequency drive.

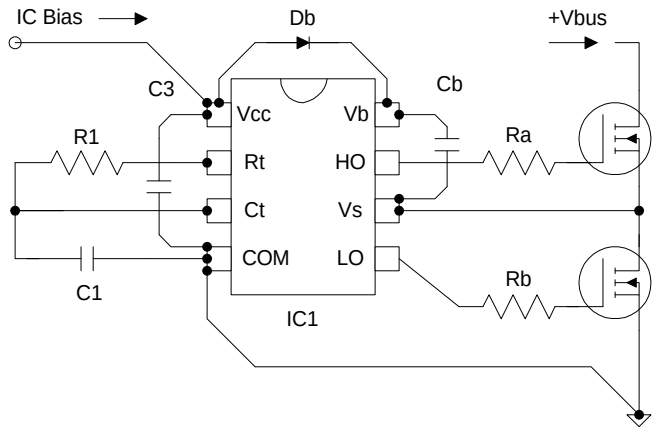
Topics Covered

1. *Operation of Typical Fixed Frequency Circuit*
2. *Dynamic Frequency Selection by Switched Capacitor Method*
3. *Continuous Frequency Control by Offset Voltage Method*

1 Operation of Typical Fixed Frequency Circuit

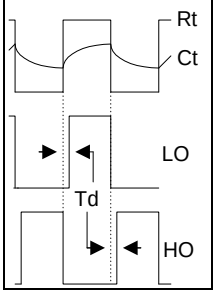
In perhaps the simplest implementation, self-oscillating control IC's are configured with a single resistor and timing capacitor in the circuit shown by figure 1a. This circuit exhibits 50% duty cycle and fixed frequency determined by equation 1, in which the 75 Ohm term accounts for resistance of the oscillator output pin, Rt. In later sections of this design tip, bootstrap components D1,Cb, power switches and gate resistors Ra and Rb are omitted for clarity. Figure 1b shows the operating waveforms to be expected using the IR2153 control IC. The Rt output pin behaves as a voltage source switching between Vcc and Ground. Rt is pulled low as the Ct pin rises to a threshold of 2/3 Vcc and switches high when Ct -falls to 1/3 Vcc. Note that Ct switching thresholds are set at a fixed proportion of Vcc and derived from a ratiometric divider network within the IC.

Fig 1a. IR215x in Typical Fixed Frequency Application



$$f = \frac{1}{1.38(R1 + 75)C1} \qquad \textbf{(1)}$$

Fig 1b. IR2153 Waveforms



2 Frequency Control using Series/Parallel Switched Capacitor Method

2.1 Operation

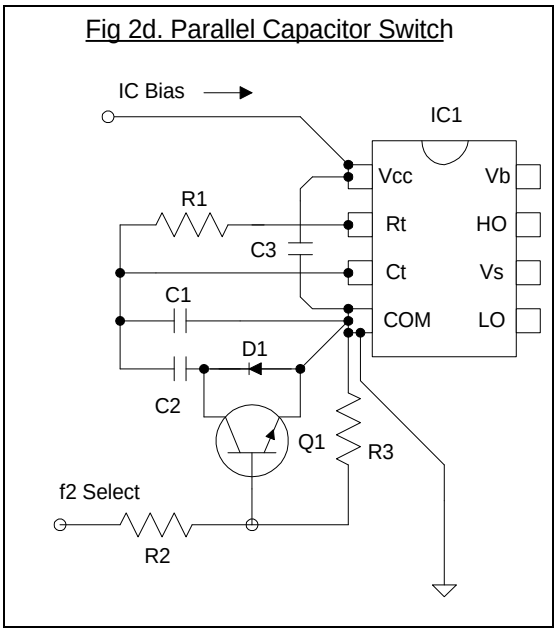
One of two or more running frequencies may be easily selected using either of circuits discussed in sections 2.2 and 2.3. In both cases, a small signal NPN transistor is used to add or bypass one of two capacitors in series or parallel. This results in a change in frequency by altering the effective capacitance seen by the Ct node of the IC.

2.2 Parallel Capacitor Switch

The circuit of figure 2d shows how a small-signal transistor may be employed to connect an auxiliary capacitor to the oscillator on command. When the transistor is in the off-state, diode D1 is blocking and C2 is out of circuit, so the oscillator frequency is high. When Q1 is turned on, it carries charging current for C1 and the diode D1 provides the discharge path. This effectively places C1 and C2 in parallel, increasing the capacitance seen at the Ct node and reducing switch frequency. Resistors R2 and R3 should be chosen such that Q1 is in saturation when the 'f2' select input is high. Dividing the control signal in this manner is recommended over a single base resistor because noise immunity of the control signal is improved. This is especially important in cases where the control signal ground is distant from the COM pin of IC1. Note the star point return to COM.

$$f1 = \frac{1}{1.38(R1+75)C1} \quad f2 \approx \frac{1}{1.38(R1+75)(C1+C2)}$$

Fig 2d. Parallel Capacitor Switch

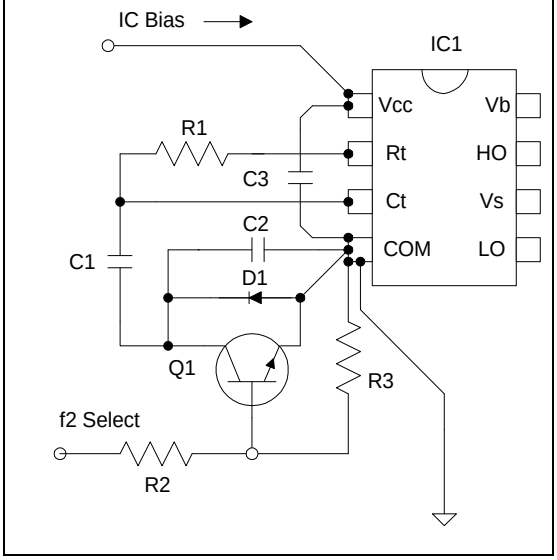


2.3 Series Capacitor Bypass

The circuit of figure 2e shows how a small signal transistor may be employed to bypass one of two capacitors connected in series. When the transistor is in the off-state, diode D1 is blocking and timing capacitors C1 and C2 are in series connection so the switch frequency is high. In the on-state, the transistor carries charging current for C1 and the diode D1 provides the discharge path. This effectively removes C2 from circuit, increasing the capacitance seen at the Ct node and reducing switch frequency. Resistors R2 and R3 should be chosen such that Q1 is in saturation when the 'f2' select input is high. Note the star point return to COM implied in the diagram.

$$f1 = \frac{C1.C2}{1.38(R1+75)(C1+C2)} \quad f2 \approx \frac{1}{1.38(R1+75)C1}$$

Fig 2e. Series Capacitor Bypass



2.4 Circuit Variation

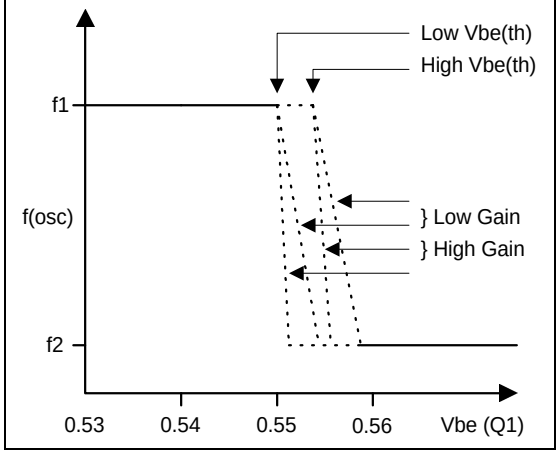
If desired, both diode and bipolar transistor may be replaced with a single, N-channel MOSFET since the internal body drain diode will serve the function of D1. In this case it may be necessary to account for output capacitance (Coss) of the switch when in the off sate. MOSFET output capacitance is highest when the drain to source voltage is low, as in this application and therefore it is preferable to select the smallest device available. If a small signal bipolar transistor is used as shown in the circuits proposed here, output capacitance of the switch can usually be neglected. Various combinations of series and parallel switch may be deployed as necessary to provide the required number of selectable run frequencies.

2.5 Limitations of Switched Capacitor Circuits

2.5.1 Repeatability

Both series and parallel methods give good results if one of two distinct switch frequencies must be dynamically selected. However, if continuous frequency control is needed, some limitations appear. Continuous frequency variation using either circuit requires that the transistor be operated in the linear mode between limits. Unfortunately, oscillator frequency in this region is a function of both small-signal gain and switch threshold as portrayed in figure 5f . Transistor selection or trimming may help increase repeatability in volume manufacture, however in general, neither are appealing options. In such cases, continuous frequency adjustment by offset voltage control may be a preferable alternative. This topic is covered in section 3.

Fig 2f. Effect of Q1 parametric spread on circuit of fig 2e.



2.5.2 Duty Cycle Disturbance and Possible Effects

During the transition when Q1 enters the linear region and frequency starts to change, the duty cycle at the output will temporarily deviate from its 50% nominal value. This statement applies to both circuits of figure 2d and figure 2e. When C2 starts to switch either in or out of circuit, the average potential across C1 must change to compensate for the reduction or increase in the average voltage across C2. The charge required to do this can only be acquired by inequality between Rt on and Rt off time, resulting in Ct asymmetry and subsequent duty cycle change at the output. Fortunately, this effect is temporary and in the typical case,where timing capacitors C1 and C2 are either equal or of a similar magnitude, duty cycle deviation will be minimal and remain for only a few switch cycles. If however, the ratio between C1 and C2 is high, then many switch cycles may be required for the average voltage on the larger of the two capacitors to be restored and for the duty cycle to return to its nominal value.

In a half bridge drive, duty cycle variation changes the average voltage at the output, in the same manner as would a PWM circuit. The result is a low frequency transient superimposed on the much higher switch frequency. Certain types of load, such as the series resonant LC circuit used in electronic ballasts may react unfavorably to the resulting voltage transient if it is sufficiently extreme. If any type of resonant load is deployed, circuit parameters should be verified in as the linear region starts. In particular, check current in magnetic components for saturation with the equipment at expected operating temperature.

3 Continuous Frequency Control by Offset Voltage Method

If the oscillator frequency must be continuously variable between two limits and programmable by an external voltage sourced signal, the method described here may be applicable. The concept is introduced below and circuits with a more practical bias follow later in the document.

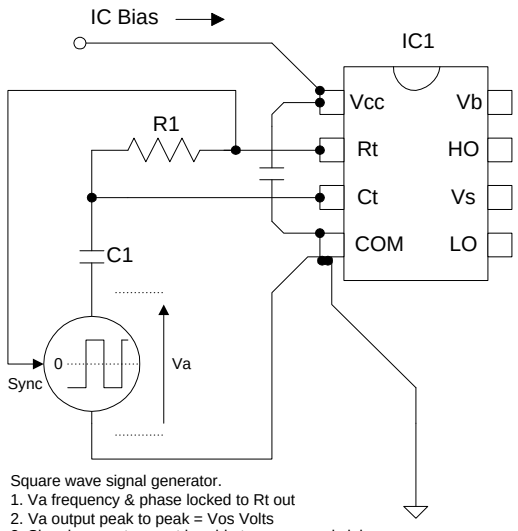
3.1 Explanation of Offset Voltage Control

3.1.1 Test Circuit

For the purpose of this description, consider the 'test circuit' portrayed in figure 3a. This circuit serves only to aid explanation and is not offered as a practical implementation. Note the lower plate of the timing capacitor, C1 is attached to the output of a signal generator which produces a square wave output.

The signal generator output (Va) is synchronized in both frequency and phase to the Rt pin of IC1 and set for positive peak of V1 volts and a negative peak of V2 volts with respect to COM. The signal generator output sums with the lower plate of C1, therefore we shall refer to the peak-to peak value of Va as the offset voltage Vos, where Vos=V1+(-V2). This configuration will yield the waveforms of fig 3b.

Fig 3a. Offset Voltage Control Test Circuit



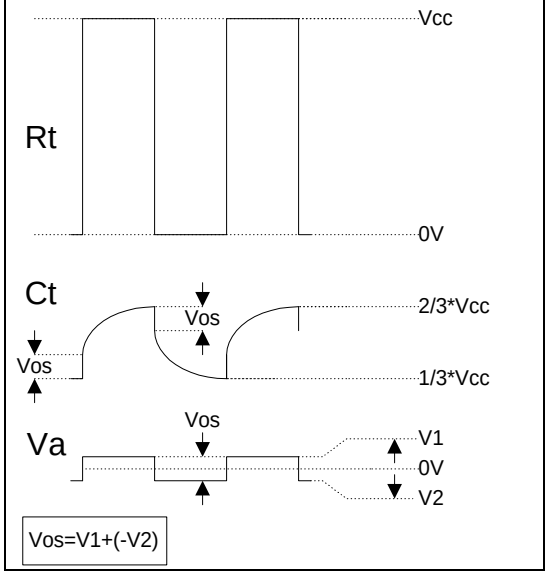
Square wave signal generator.
1. Va frequency & phase locked to Rt out
2. Va output peak to peak = Vos Volts
3. Signal generator must be able to source and sink current through C1 without distortion

3.1.2 Operation of Test Circuit

Assuming the Rt output has negligible rise and fall times, as Rt switches to Vcc, the signal generator output immediately 'adds' 1xVos to the lower plate of C1 and consequently the potential seen at the Ct pin also increases by 1xVos. This reduces the total charge (and time) required to raise Ct from 1/3*Vcc to the 2/3*Vcc switch threshold set internally by IC1. - When Ct reaches the upper threshold, Rt immediately switches state to 0V and the signal generator output Va switches from V1 (+) to V2 (-). The difference (Vos) is now 'subtracted' from C1 lower plate and consequently, the Ct pin. Again, the total charge required to take Ct between thresholds is reduced.

The oscillator frequency is therefore higher than would be the case in the typical RC configuration of figure 1a. Furthermore, since charge and discharge times are affected equally, the oscillator duty cycle remains fixed at 50%.

Fig 3b. Results from circuit of Fig3a.



Equation 3 below shows that the free run frequency is a function of both Vcc and the peak-to-peak offset voltage, Vos. Although in this example, V1 and V2 are equal, this is not a requirement for the circuit to function correctly as the run frequency is independent of Va displacement relative to ground.

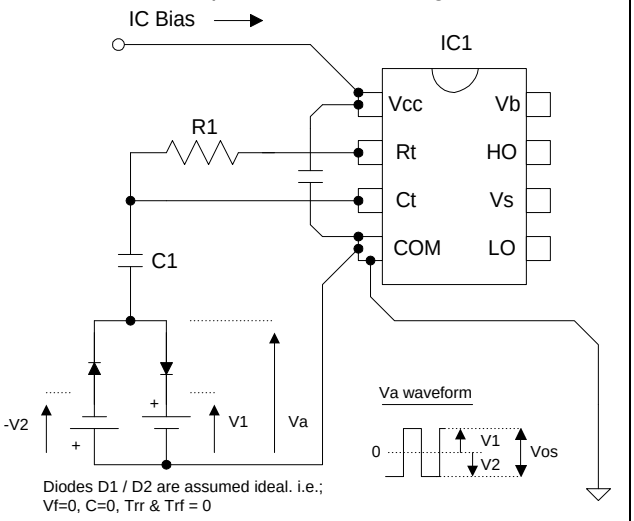
3.2 Implementation of Offset Voltage Control

$$f = \frac{1}{-2C1(R1+75).Ln\left[\frac{Vcc}{2Vcc-3Vos}\right]} \qquad \textbf{(3)}$$

In figure 3a, when the Rt output is high, the signal generator sinks charging current for C1 and holds Va=V1. Conversely, when Rt is low, the signal generator sources current and holds Va=V2. In both cases the signal generator plays a passive role and serves only to clamp the lower plate of C1.

This means that the signal generator shown in figure 3a can be reduced to the simple bipolar voltage clamp depicted in the equivalent circuit of figure 3c. Running frequency is dependent only on Vcc and Vos and both can be controlled, therefore several derivatives of this simple circuit are possible.

Fig 3c. Offset Voltage Control
Equivalent Circuit to fig 3a.



3.3 Frequency Control by Vcc Adjustment

In the circuit of figure 3d, the offset voltage is fixed using a small signal zener diode ZD1, where; Vos=Vz-(-0.6). Fixing the offset voltage in this way engineers a relationship between oscillator frequency and Vcc so the IC bias supply doubles as the control signal itself.

Substituting arbitrary values for C1,R1 reveals the oscillator response to Vcc changes as shown in figure 3e. Note that switching starts at a high frequency as Vcc passes the positive going under-voltage lockout threshold (UVLO+). As Vcc continues to rise, the run frequency falls until the internal zener clamp of the IR2153 avalanches preventing further change. An external zener diode can be used to modify the Vcc limit and fix the final run frequency as required. If the Vcc start-up waveform rises in a predictable manner or can be made to do so, this technique can be very useful as the basis for frequency sweep in a warm-start fluorescent electronic ballast.

Fig 3d. Frequency Control by Vcc Adjustment

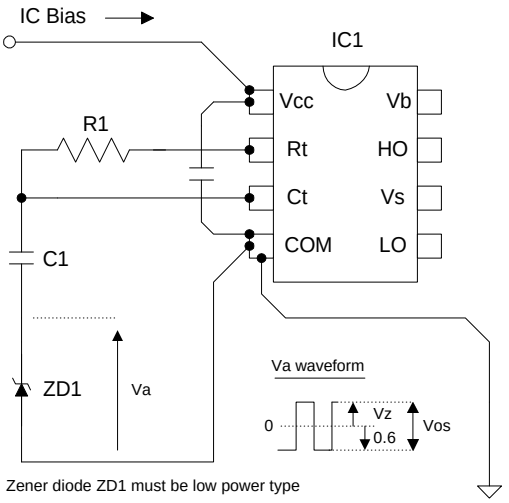
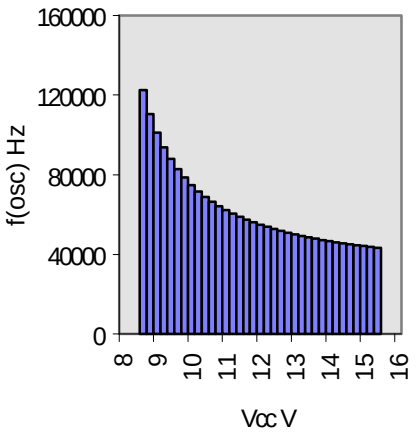


Fig 3e. Oscillator Vcc dependance
C1=1nF,R1=27K,Vz=1.8V using cct. 3d.



3.4 Frequency Control by Vos Adjustment - A Simple Non-Linear VCO

Fixing Vcc and adjusting the offset voltage will also cause frequency change. This allows a simple, non-linear voltage controlled oscillator to be easily constructed using the circuit of figure 3f. In this example, the negative clamp voltage, V2 is set by the forward voltage drop of D1. The positive clamp voltage, V1 is set by a control voltage applied to the base of Q1. This small signal PNP transistor behaves as an emitter follower and provides sufficient current gain to allow the control voltage to be driven from a comparatively weak source. Capacitor C2 is presented between base and collector of Q1 and helps to provide a solid V1 clamp and filter noise voltage on the control input. C2 should be of the order of 100pF or less. If a low-impedance control voltage source is available, then Q1 may be replaced with a single low voltage silicon diode of the same type as D1.

Fig 3f. Frequency Control by Vos Adjust

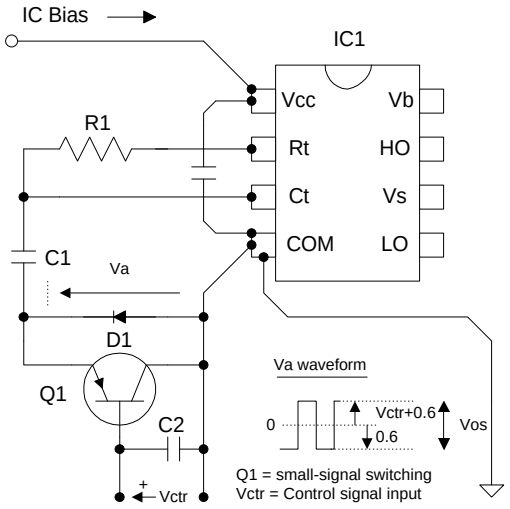
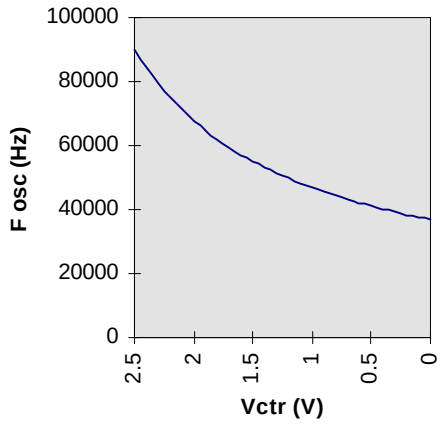


Fig 3g. Frequency Control by Vos Adjustment
Vcc=15V,Rt=24K,Ct=1nF Circuit of fig.3f



3.5 Limitations of Offset Voltage based Circuits

3.5.1 Frequency Error due to Clamp Non-Linearity.

Ideally, the bi-directional voltage clamp should source/sink current at precisely at V1/V2 clamp irrespective of the current passed and should exhibit infinite impedance between these limits, however in practice, this is not the case. Although similar limitations will exist to some degree in any implementation of offset voltage control, for the purpose of example, imperfections in the zener diode clamp of figure 3d are highlighted as follows;

a. The diode will pass a reverse leakage current prior to the zener limit.
b. There is a recovery time from both forward and reverse conduction (inequality will also change duty cycle)
c. The diode has a small equivalent parallel capacitance.

Limitations a,b and c cause distortion of the Va waveform in the form of “rounding” and reduced dv/dt during Rt transitions. The overall effect is to introduce small errors in equation 3. This presents as a reduction in frequency change with a given change in Vcc, however, some steps can be taken to improve the results. Choosing a small signal zener diode with a power rating of 250mW or less is highly recommended and will generally reduce errors in the frequency/Vcc performance to an acceptable level. Alternatively, the zener diode may be replaced with a number of small signal silicon diodes in series configuration to produce the required clamp threshold by summing Vf drops.

3.5.2 Frequency Error due to Clamp Threshold Changes.

In both implementations of offset voltage control presented here, the clamp thresholds V1 and V2 fix the offset voltage Vos, which in conjunction with Vcc determines the run frequency. In practice, both clamp thresholds will vary slightly. For this example, we will again consider limitations of the zener-diode based circuit of figure 3d, though the underlying principles are equally applicable to any implementation of offset voltage control;

d. Both Vz and forward conduction threshold Vf are dependent on temperature.
e. Equivalent series resistance is not zero and so V1 and V2 will vary slightly with charge/discharge current.

Limitations d and e introduce small errors into equation 3, however, since temperature coefficients of Vz and Vf are reasonably predictable, the overall frequency error can be easily calculated. In general, since the charge/discharge current is very low, series resistance of the clamp does not cause significant error. Variation in leakage current discussed in 3.5.1 represents a more significant source of error in this regard.

3.5.3 Noise Considerations and PCB Layout Requirements.

The oscillator trigger thresholds are a function of Vcc referenced to the COM pin. Since the Ct pin is noise sensitive, all circuits connected directly or indirectly to the Ct pin MUST be returned either the Vcc or COM node at the IC. Such PCB tracks used for this purpose should not be allowed to carry high currents from the load circuit or current from other noisy sources. This is especially important with offset voltage control is being used since the noise margin is reduced as Vos becomes an increasing proportion of Vcc. Tracks returning to COM should be as short and direct as possible.