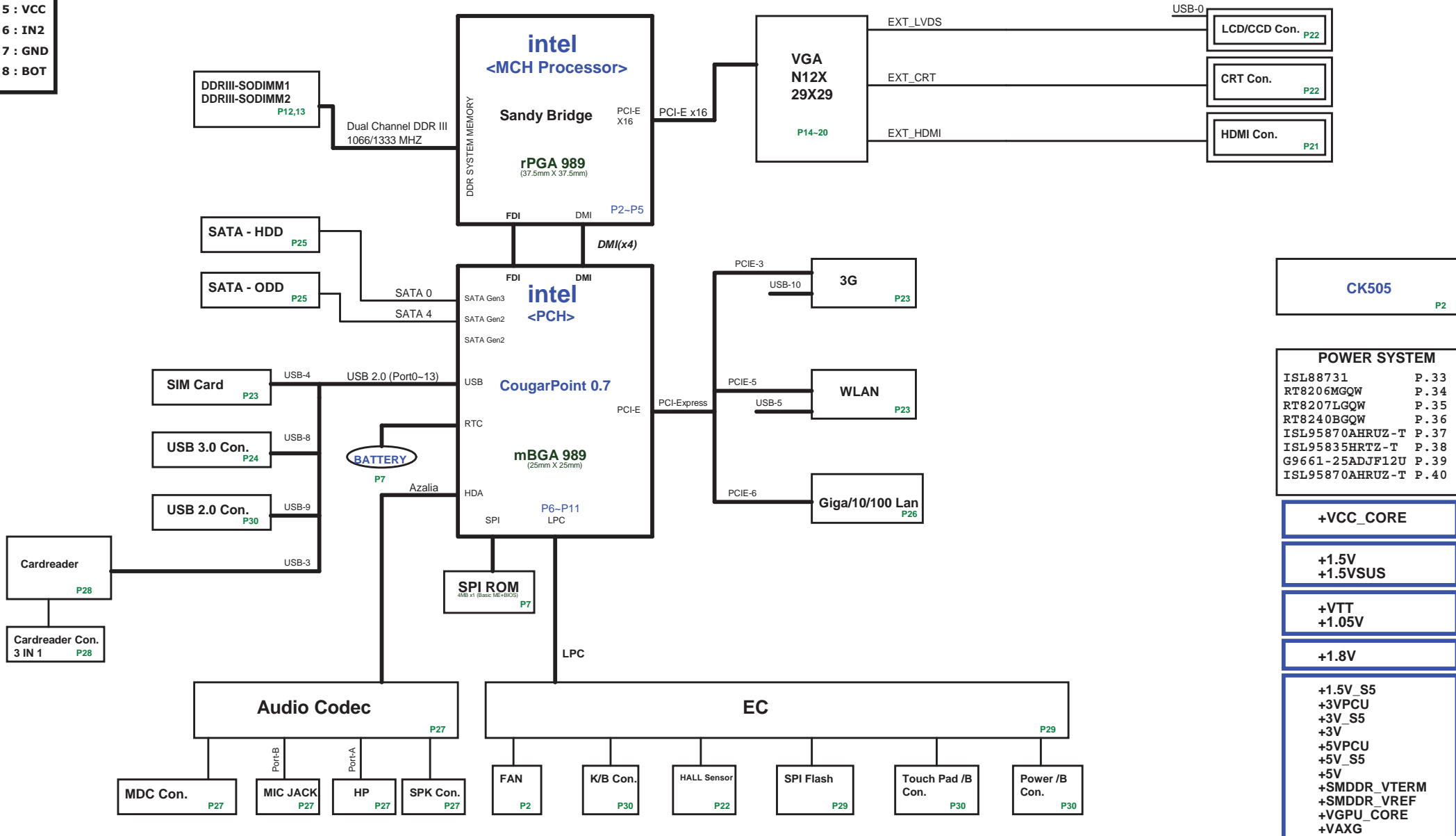


BLBD Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : GND
- LAYER 5 : VCC
- LAYER 6 : IN2
- LAYER 7 : GND
- LAYER 8 : BOT



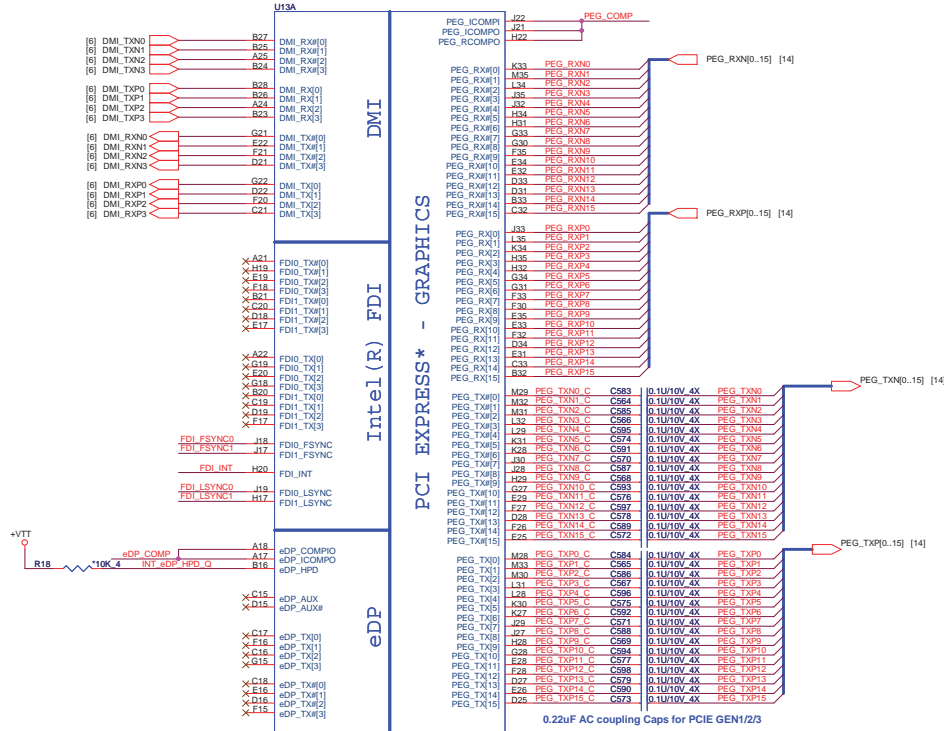
POWER SYSTEM

ISL88731	P. 33
RT8206MGQW	P. 34
RT8207LGQW	P. 35
RT8240BGQW	P. 36
ISL95870AHRUZ-T	P. 37
ISL95835HRTZ-T	P. 38
G9661-25ADJF12U	P. 39
ISL95870AHRUZ-T	P. 40

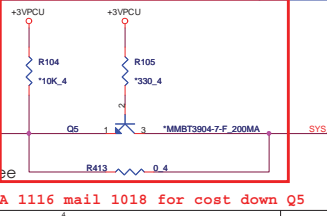
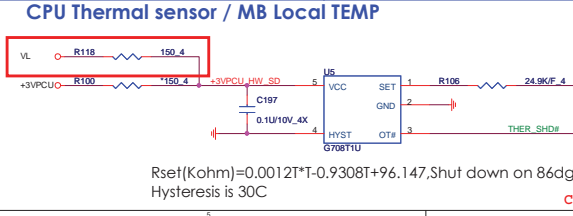
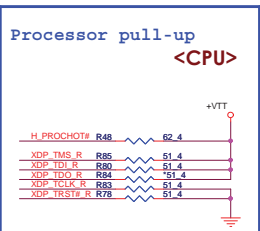
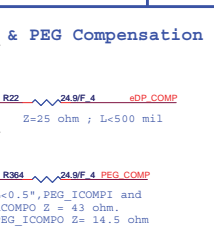
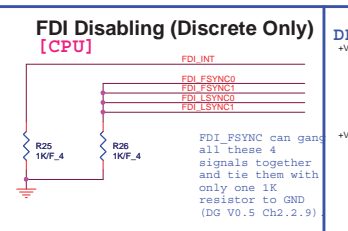
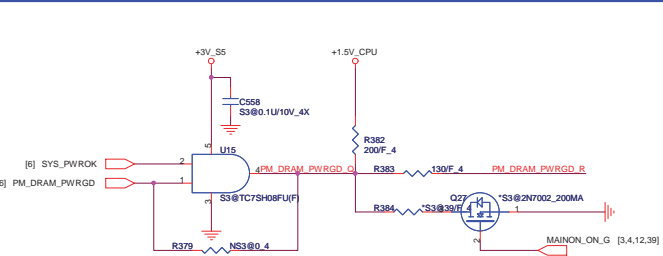
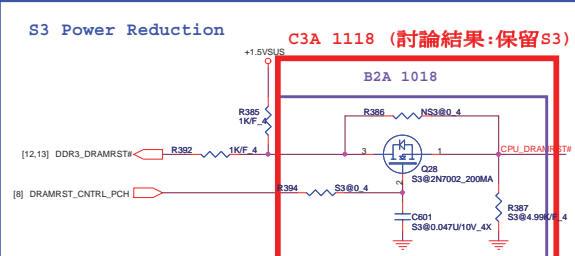
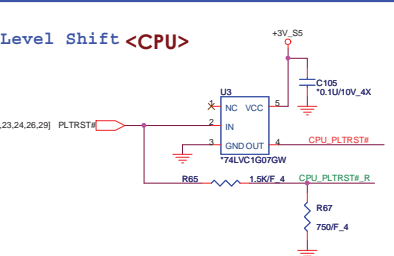
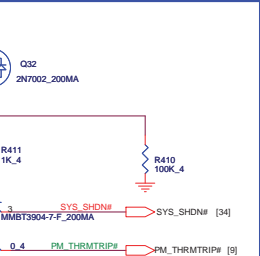
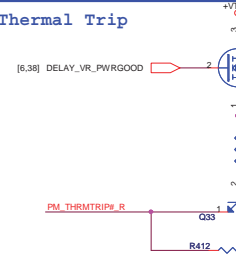
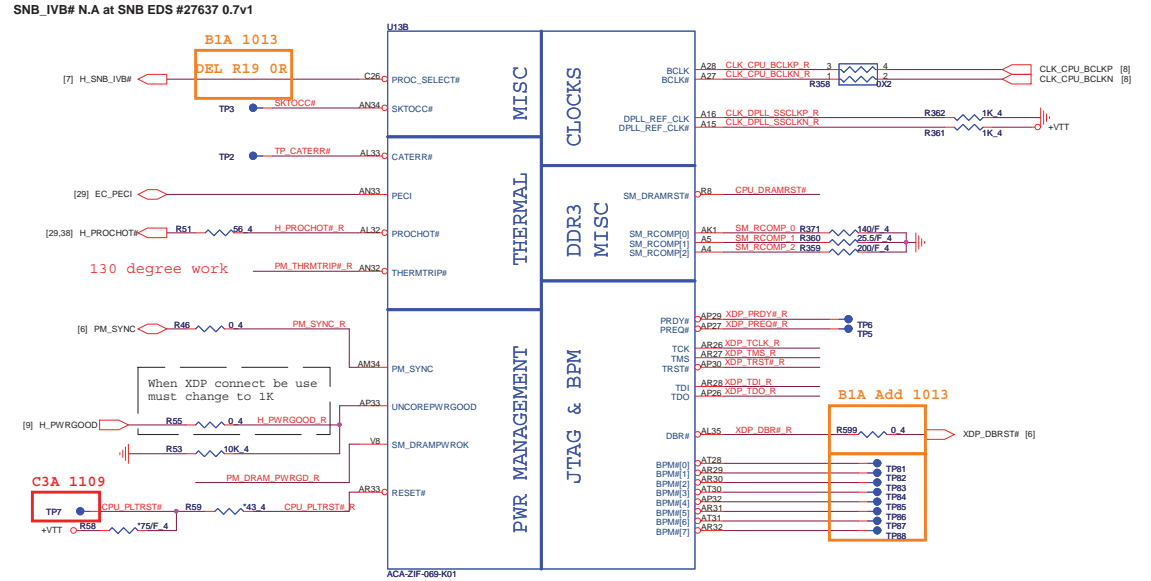
- +VCC_CORE
- +1.5V
+1.5VSUS
- +VTT
+1.05V
- +1.8V
- +1.5V_S5
- +3VPCU
- +3V_S5
- +3V
- +5VPCU
- +5V_S5
- +5V
- +SMDDR_VTERM
- +SMDDR_VREF
- +VGPU_CORE
- +VAXG

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Sandy Bridge Processor (DMI, PEG, FDI)

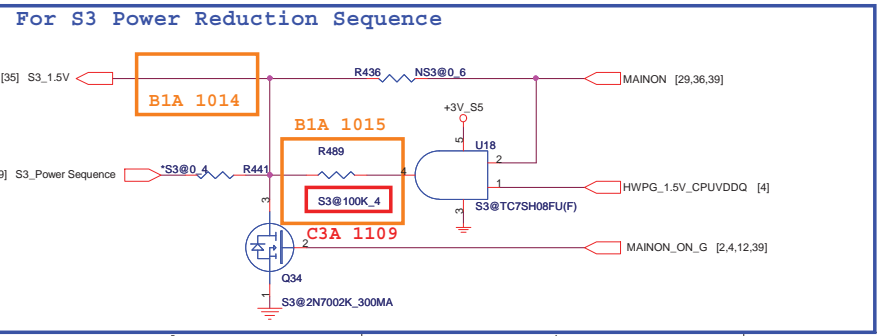
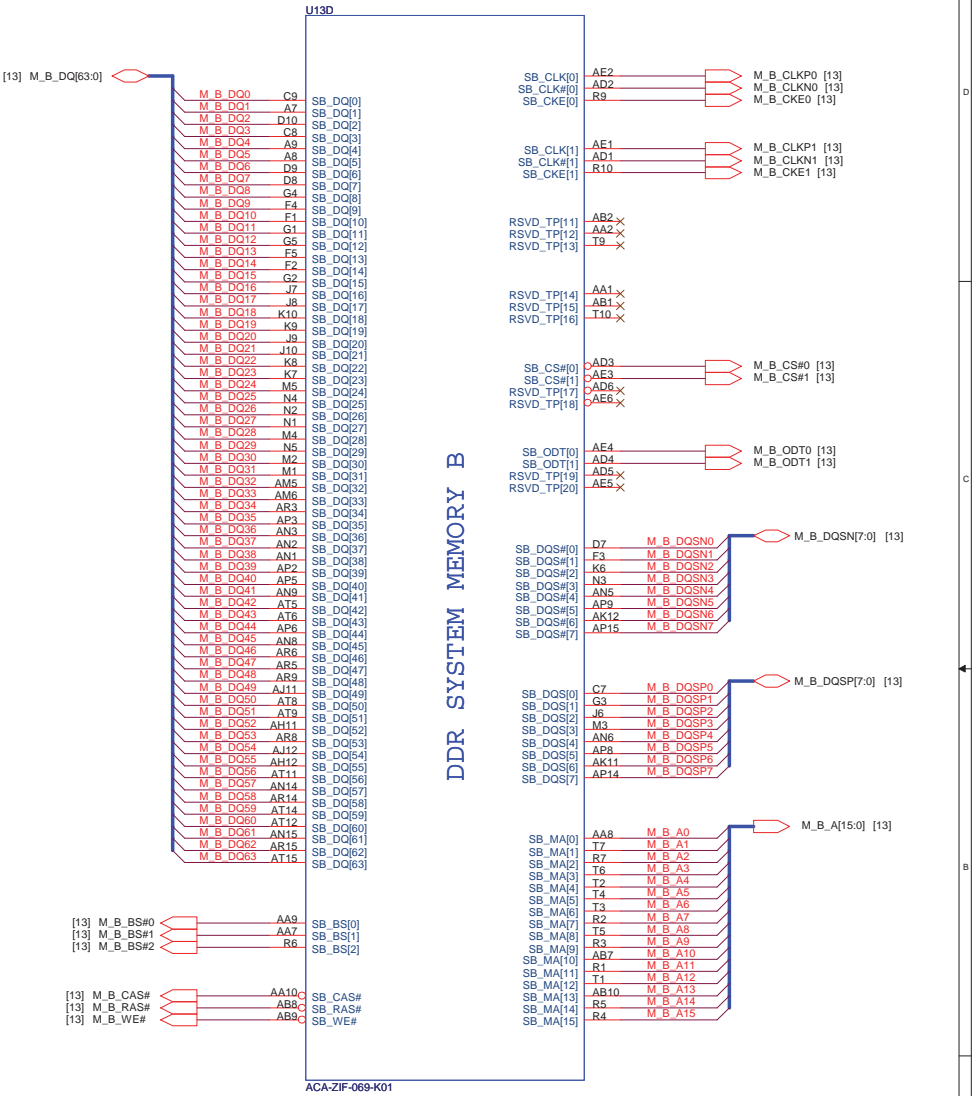
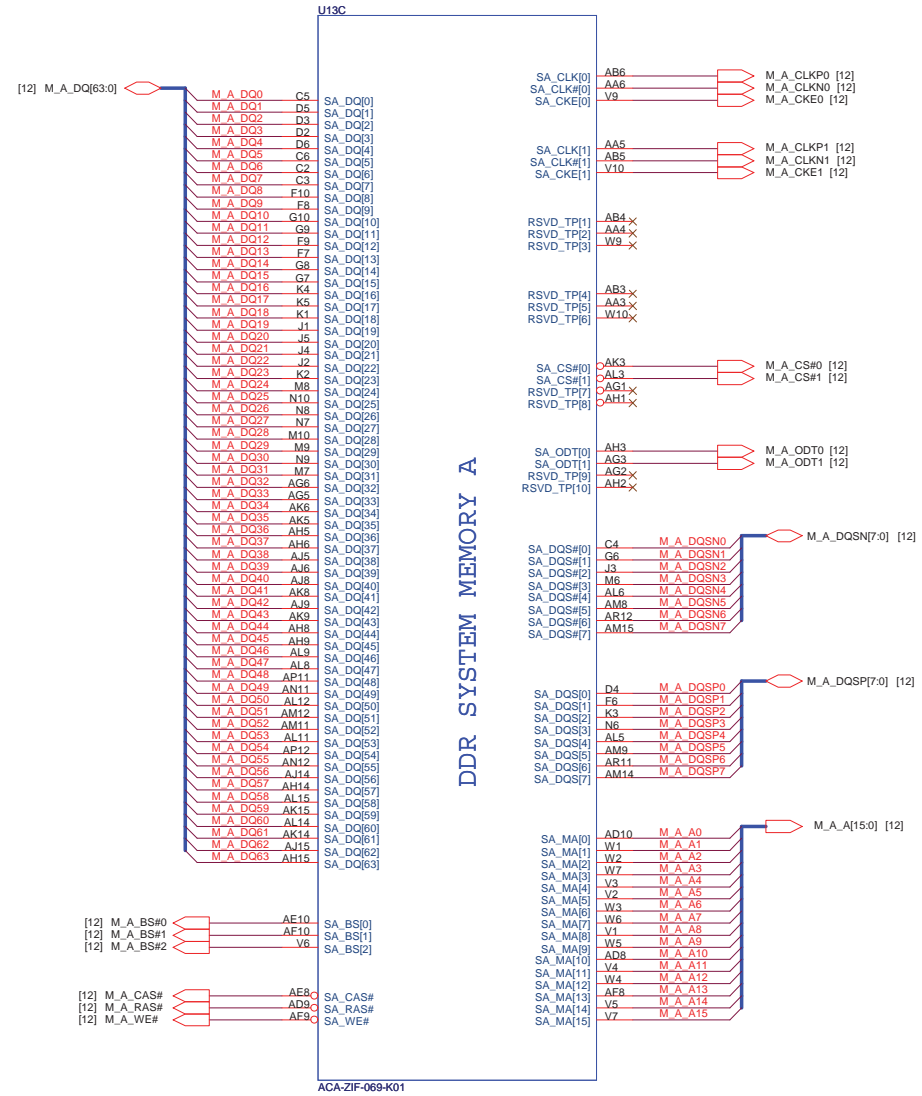


Sandy Bridge Processor (CLK, MISC, JTAG)



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Sandy Bridge Processor (DDR3)



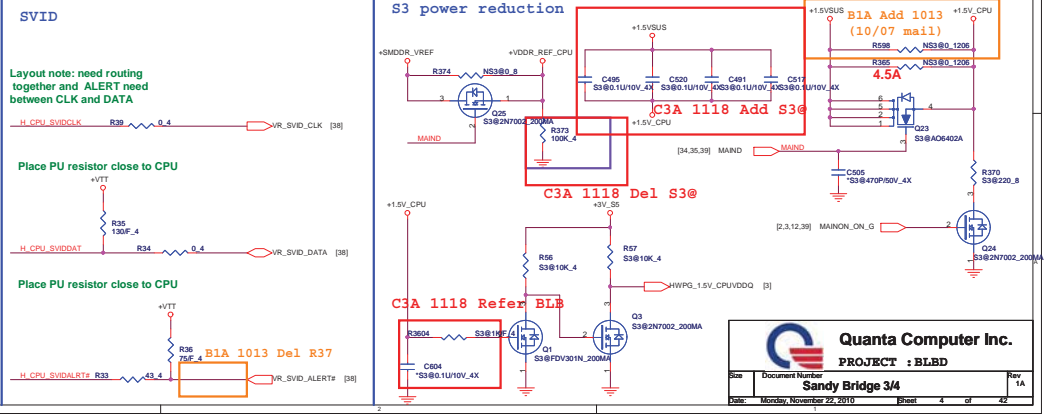
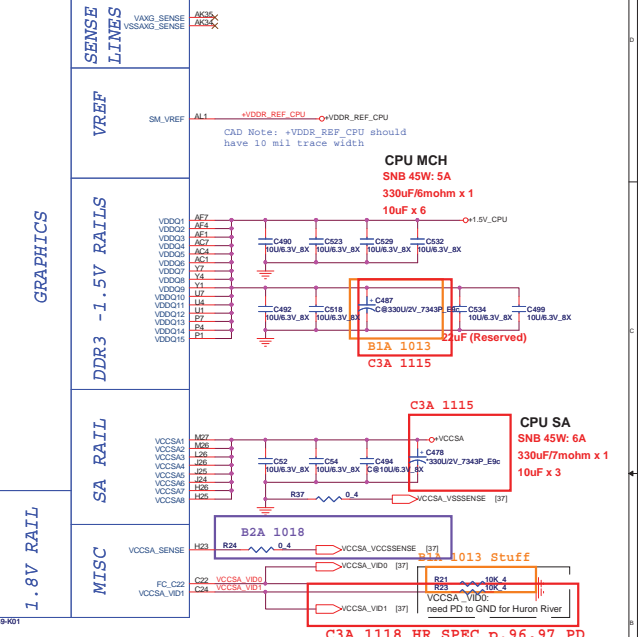
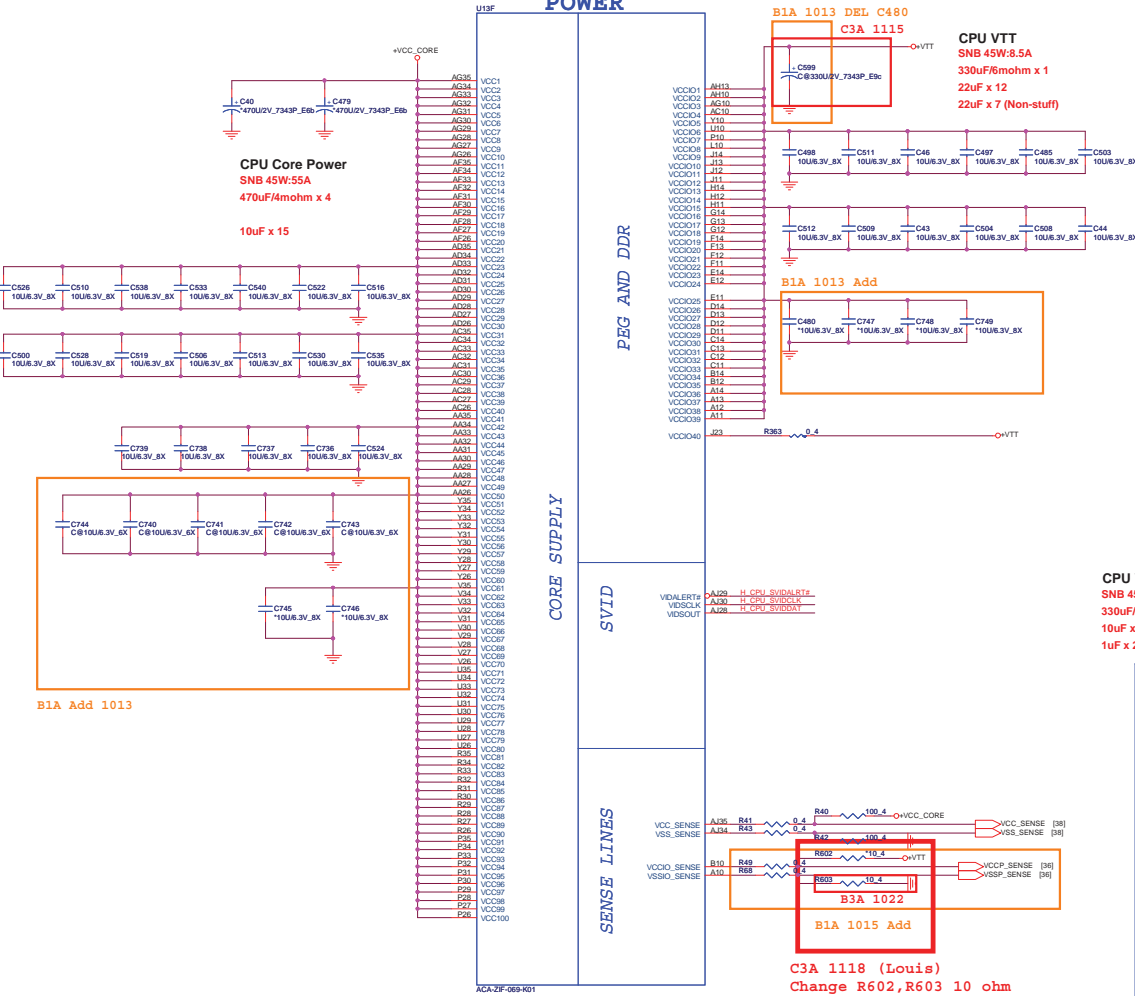
<http://hobi-elektronika.net>

Quanta Computer Inc.
PROJECT : BLBD

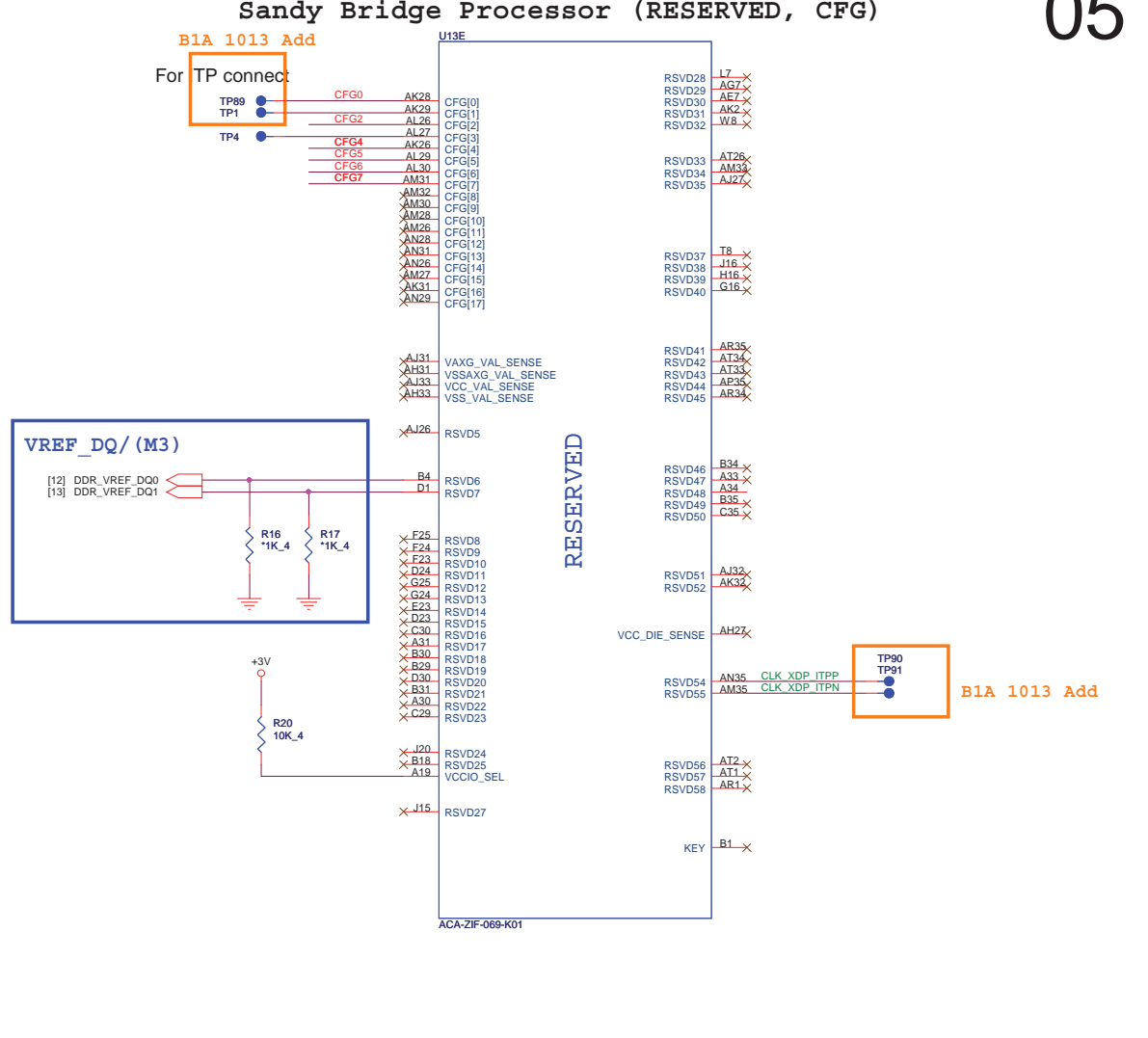
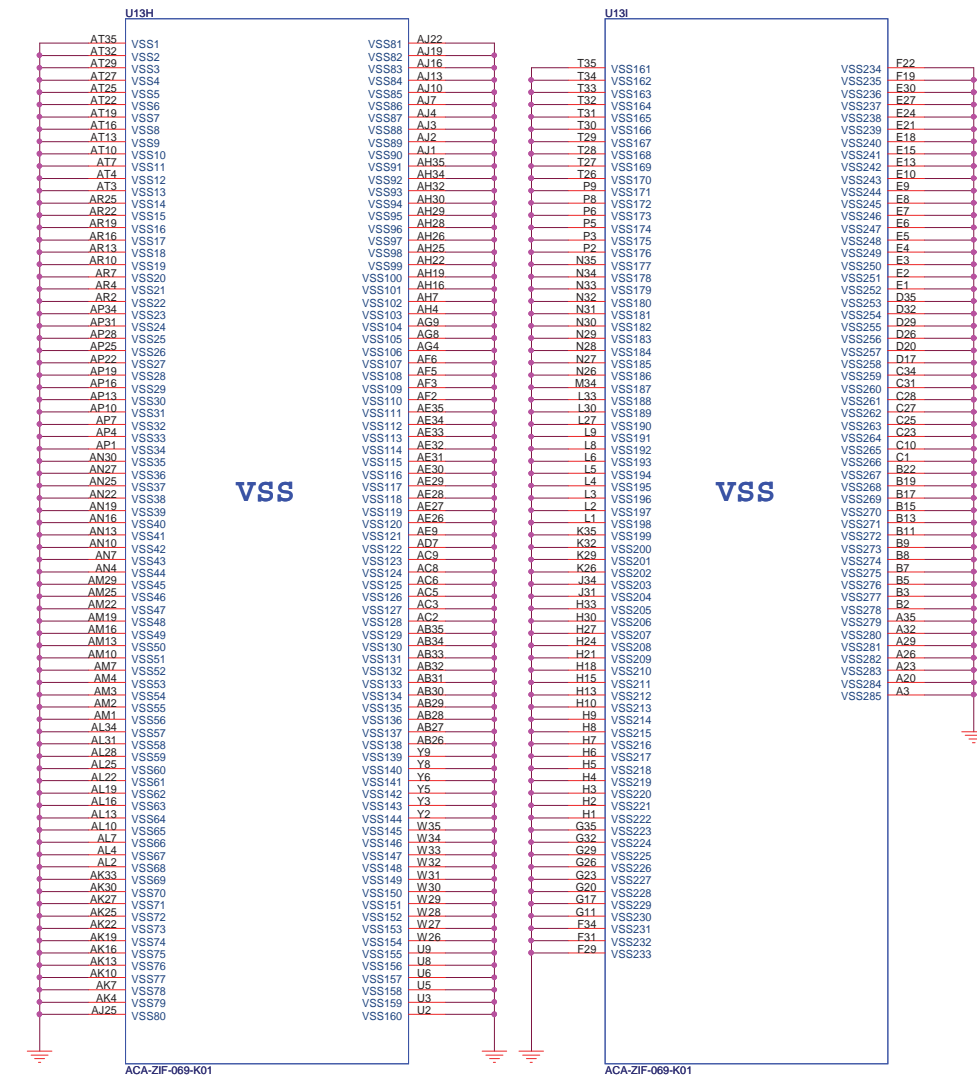
Size	Document Number	Rev
	Sandy Bridge 2/4	1A
Date:	Monday, November 22, 2010	Sheet 3 of 42

POWER

POWER



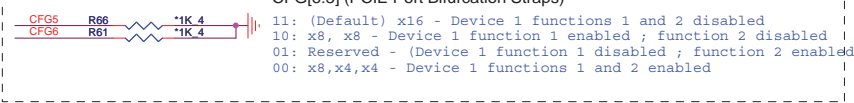
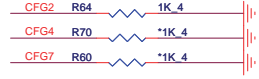
Quanta Computer Inc.
PROJECT : BLBD
Sandy Bridge 3/4
Date: Monday, November 22, 2010 Sheet 4 of 42



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

CFG	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

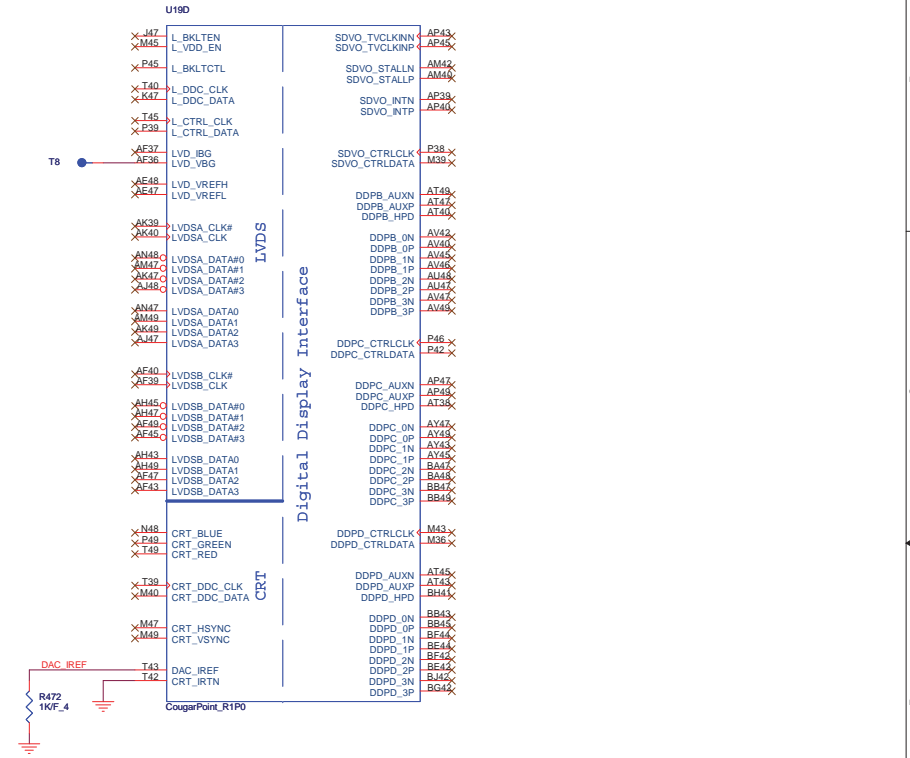
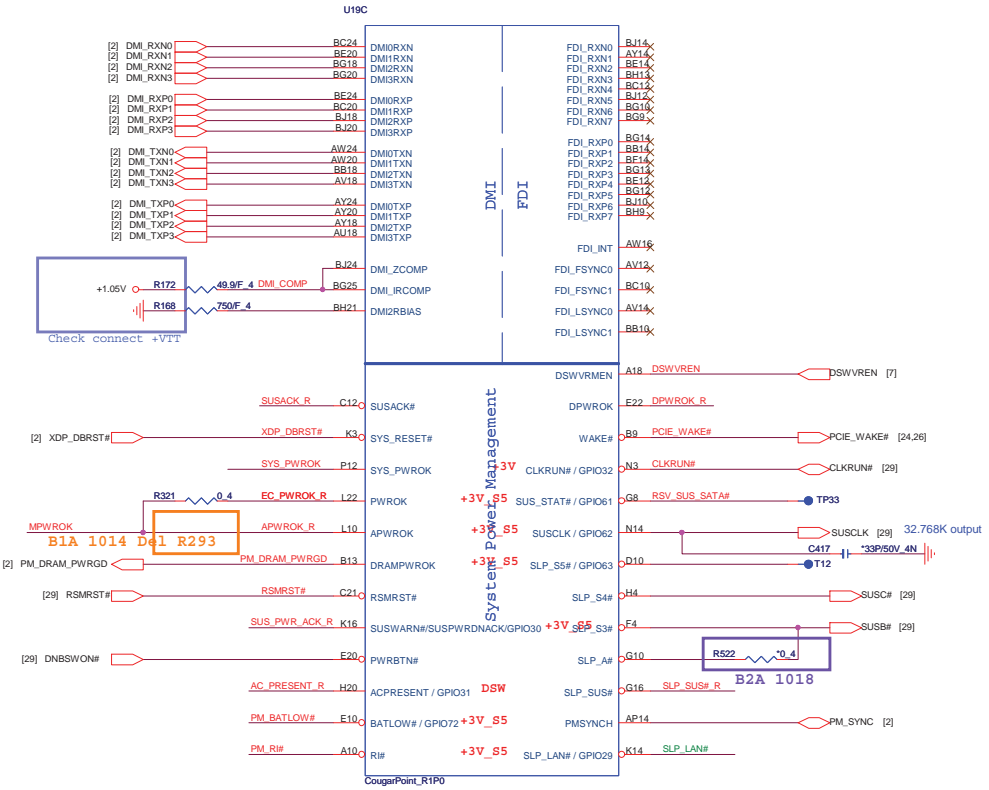


Size Document Number
 Sandy Bridge 4/4
 Rev 1A

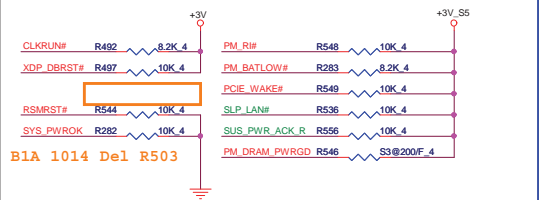
Date: Monday, November 22, 2010 Sheet 5 of 42

Cougar Point (DMI, FDI, PM)

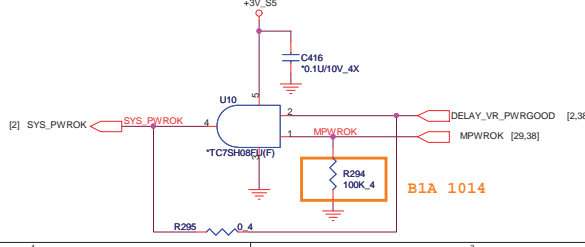
Cougar Point (LVDS, DDI)



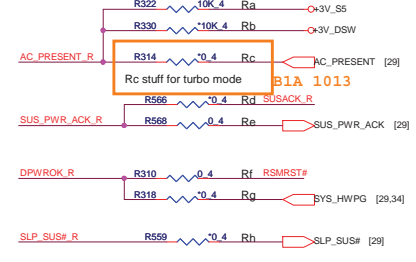
PCH Pull-high/low (CLG)



System PWR_OK (CLG)



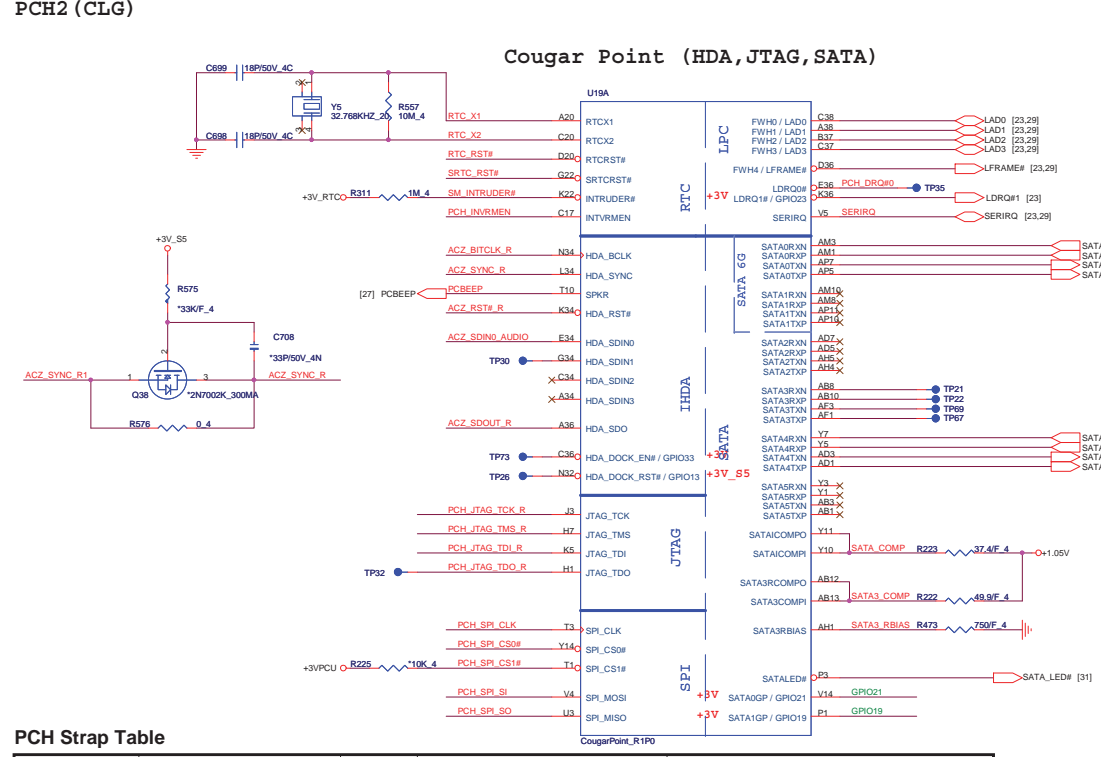
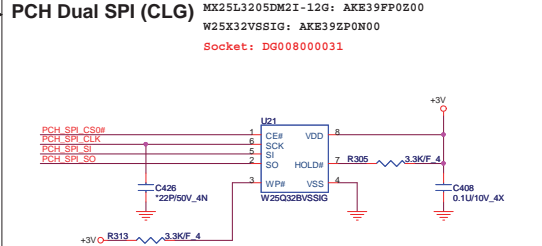
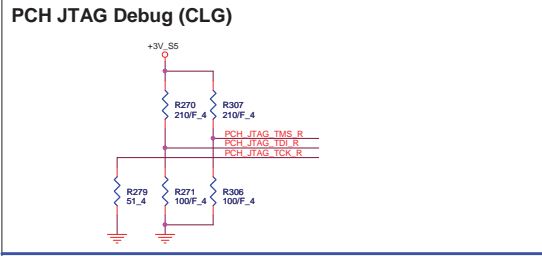
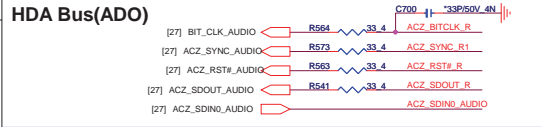
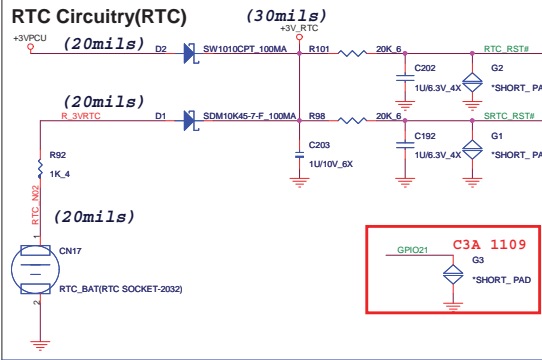
Deep Sx



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb, Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

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PROJECT : BLBD

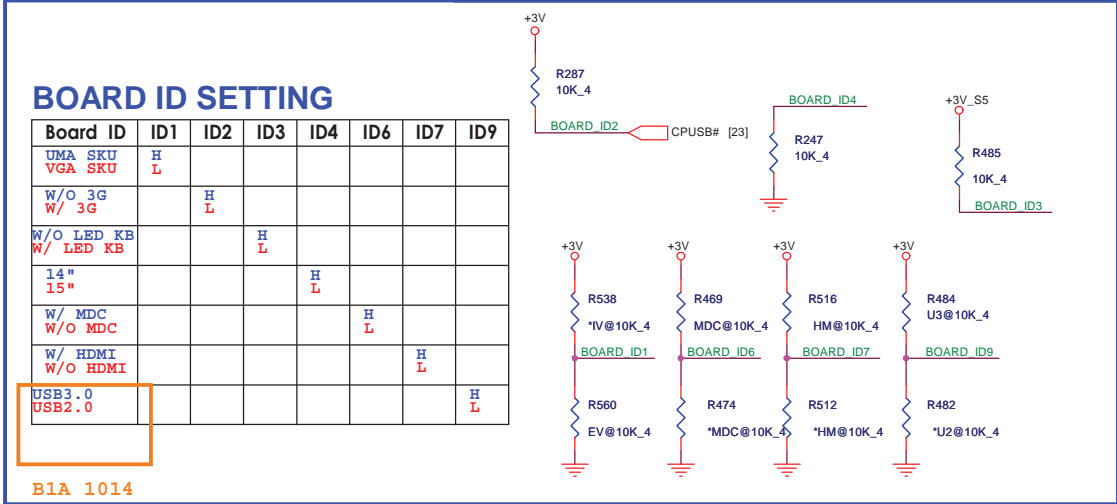
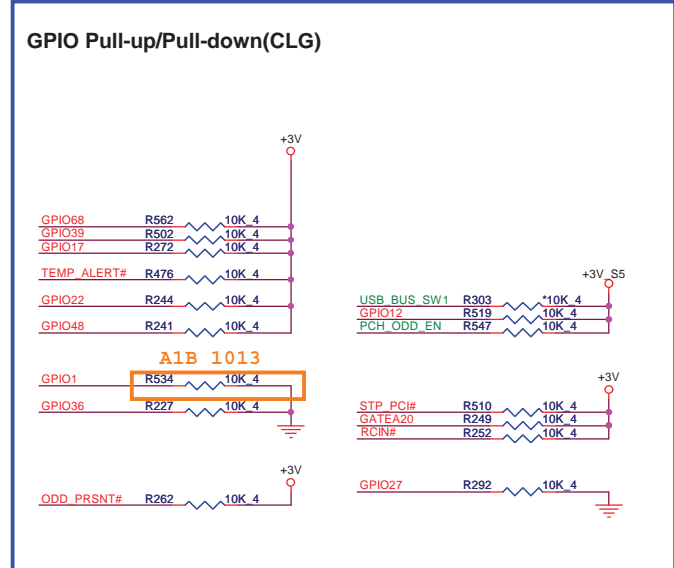
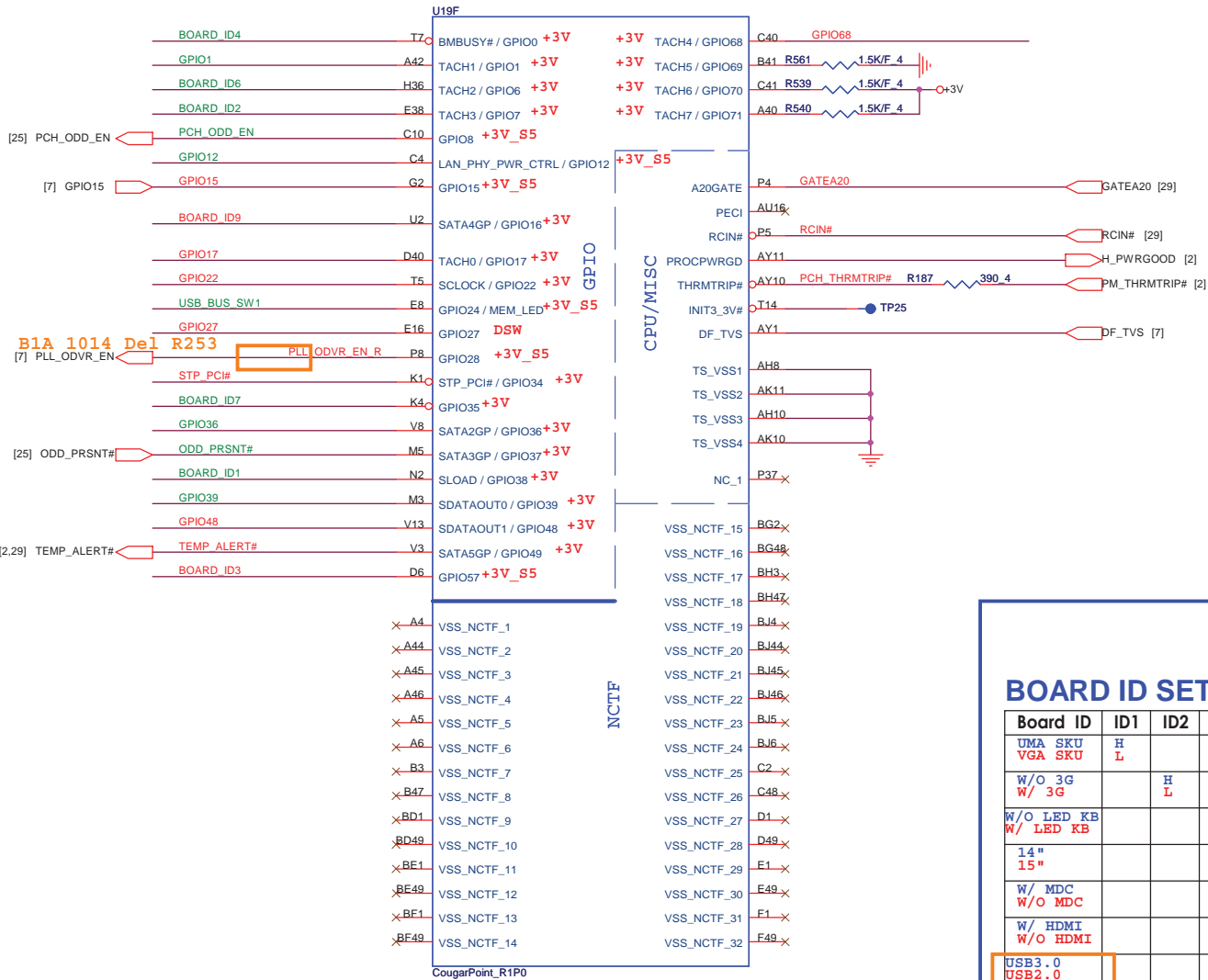
Size	Document Number	Rev
	Cougar Point 1/6	1A
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PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V_O --- R245 --- 1K_4 --- PCBEEP									
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low, leave as No Connect									
GNT3#/GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R531 --- 1K_4 --- PCL_GNT3# [8]									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC --- R545 --- 330K_4 --- PCH_INVRMEN									
GNT1#/GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
SATA1GP/GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R527 --- 1K_4 --- GNT1 [8] R490 --- 1K_4 --- GPIO19									
GNT2#/GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile									
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Default (weak pull-up 20K) 1 = Override	+3V_O --- R542 --- 1K_4 --- ACZ_SDOUT_R --- ACZ_SDOUT_R [29]									
DF_TV5	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R448 --- 2.2K_4 --- O+1.8V R447 --- 4.7K_4 --- DF_TV5 [9] H_SNB_IV5M [2]									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R248 --- 1K_4 --- PLL_ODVR_EN [9]									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Default. Support by 1.8V 1 = Support by 1.5V	+3V_S5 --- R577 --- 1K_4 --- ACZ_SYNC_R									
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	+3V_S5 --- R518 --- 1K_4 --- GPIO15 --- GPIO15 [9]									
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V									
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V									
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
DDPD_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	+3V_RTC --- R537 --- 330K_4 --- DSWVRMEN [6] R562 --- 330K_4									
SATA2GP/GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									
SATA3GP/GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									

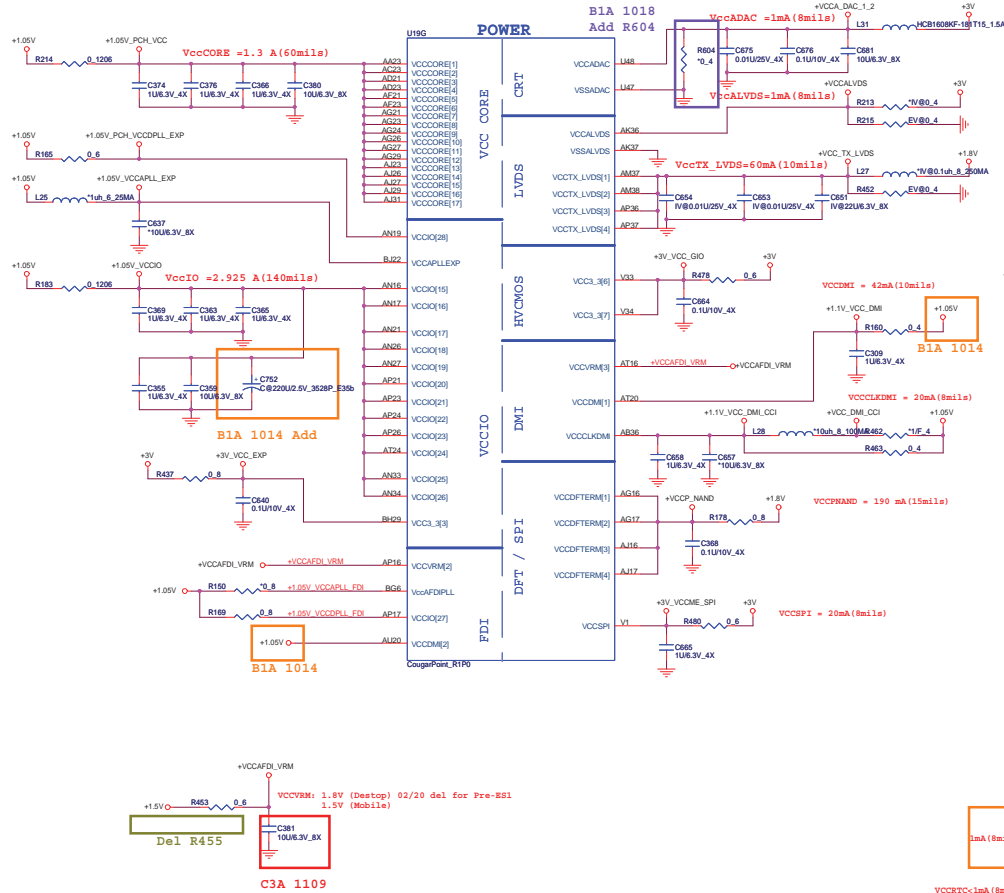
Cougar Point (GPIO,VSS_NCTF,RSVD)



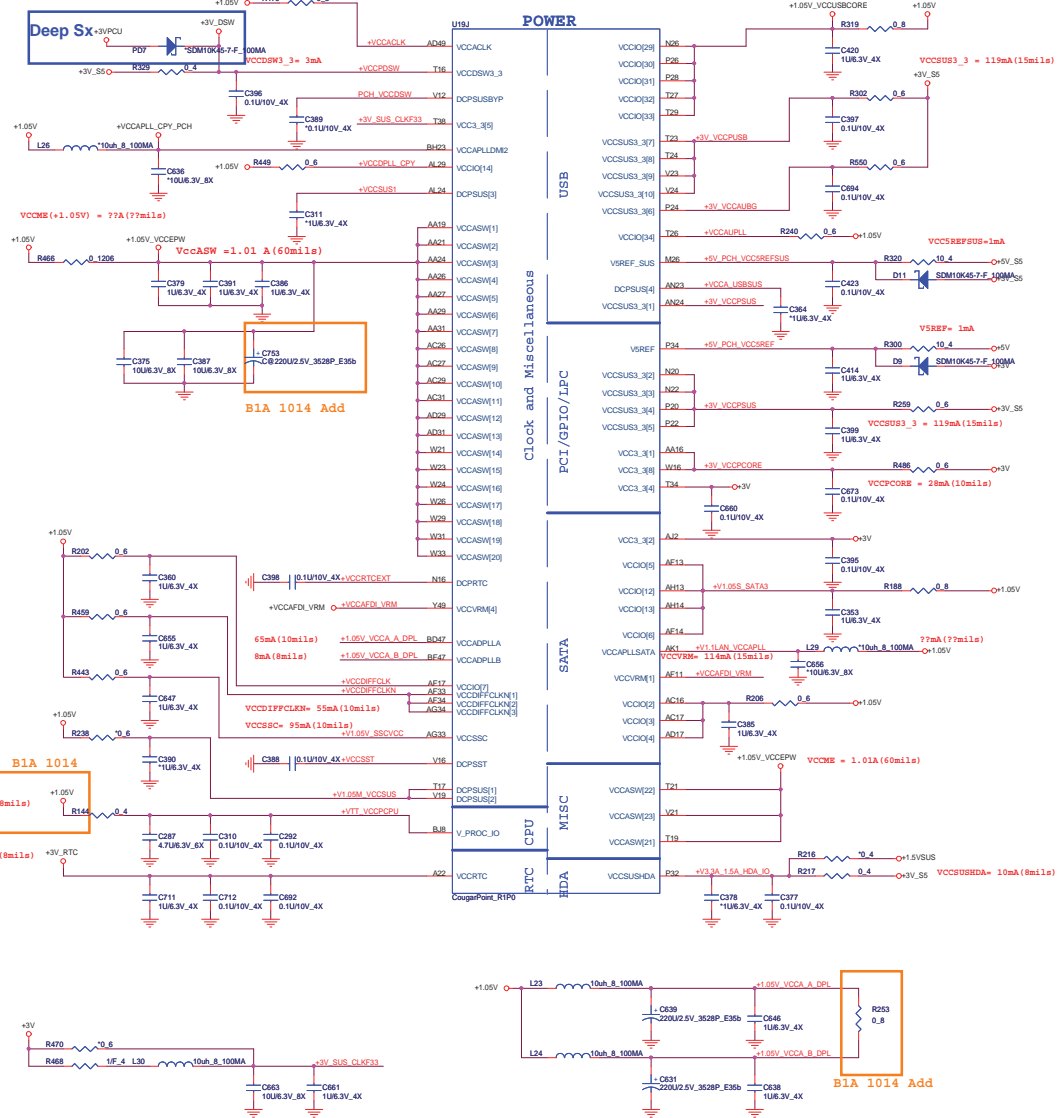
Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	Cougar Point 4/6	1A
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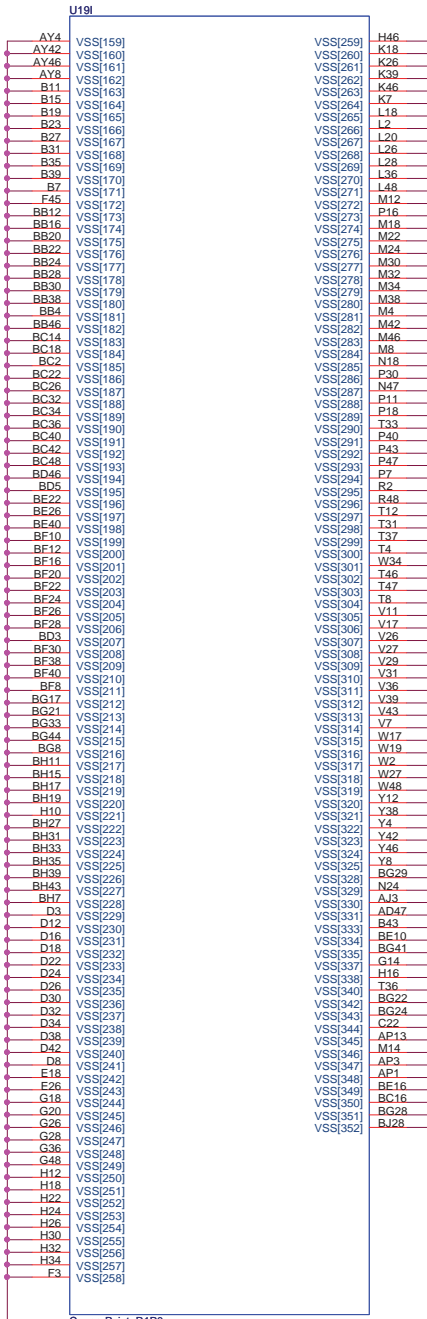
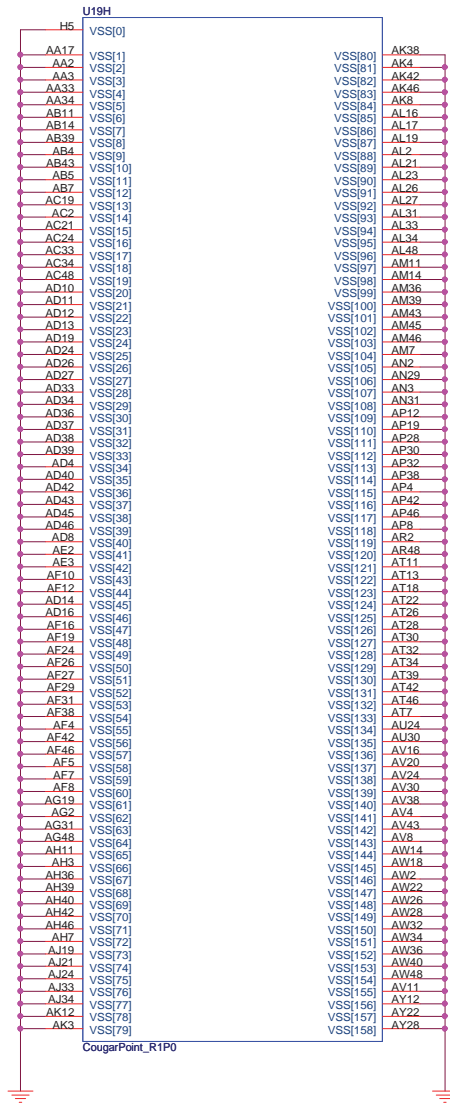
COUGAR POINT (POWER)




Cougar Point-M (POWER)



IBEX PEAK-M (GND)

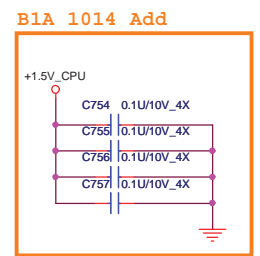
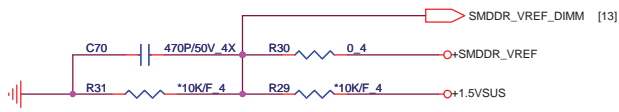
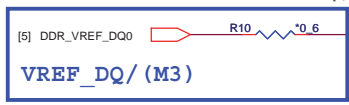
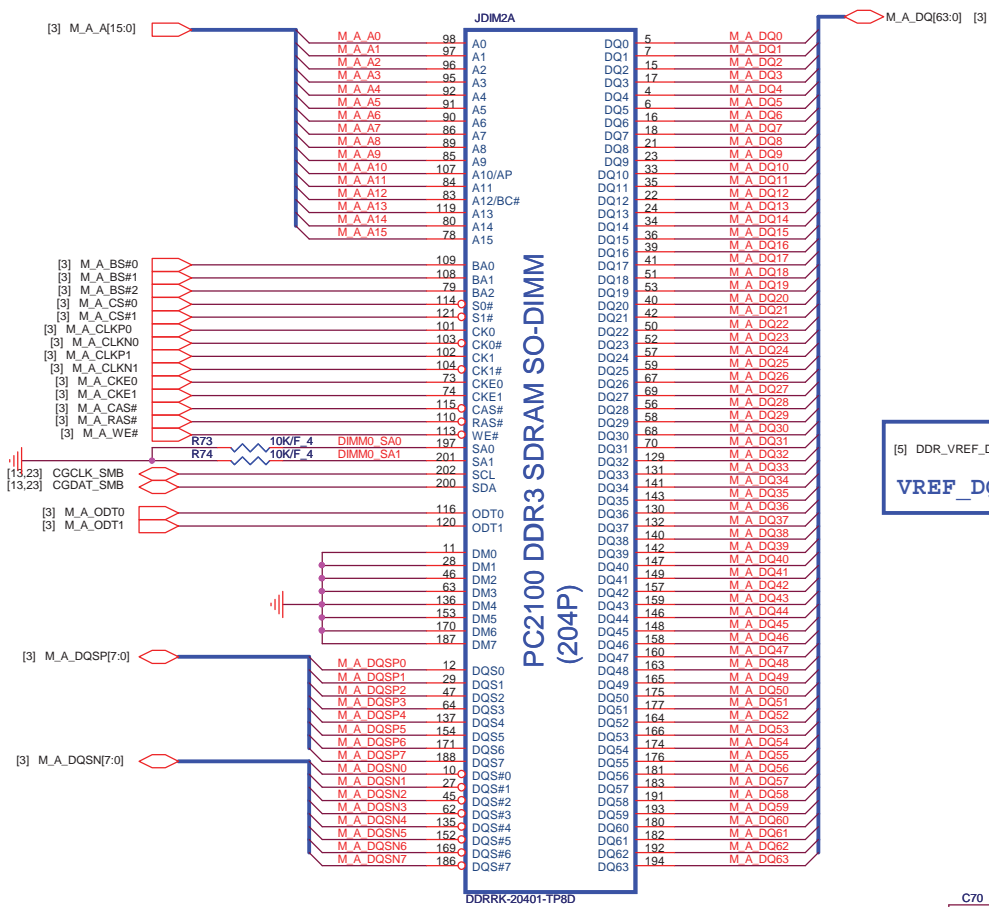


<http://hobi-elektronika.net>

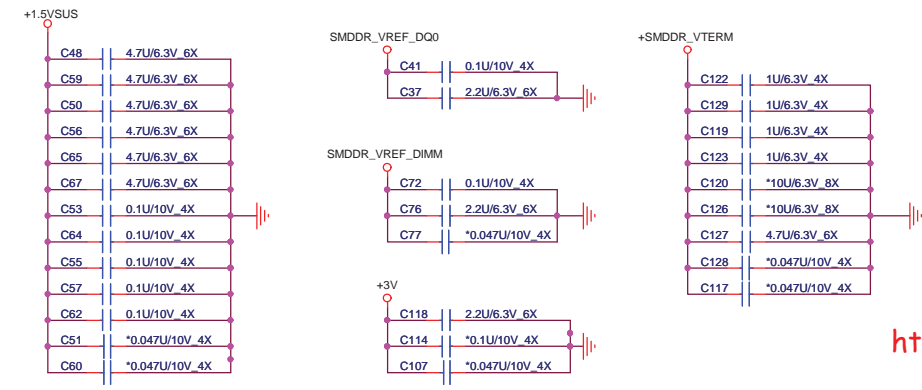
 **Quanta Computer Inc.**
PROJECT : BLBD

Size	Document Number	Rev
	Cougar Point 6/6	1A
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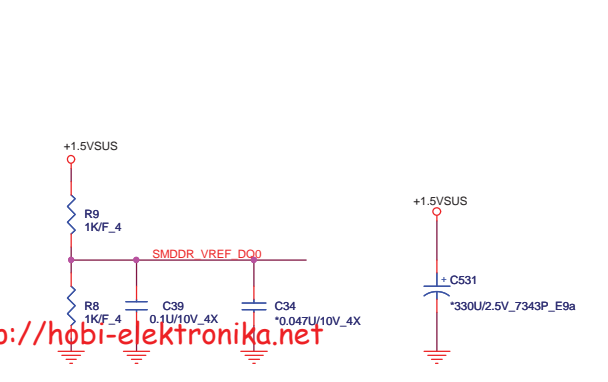
H=4



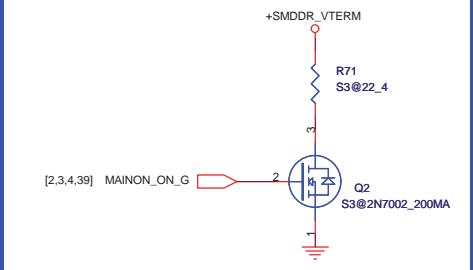
Place these Caps near So-Dimm0.



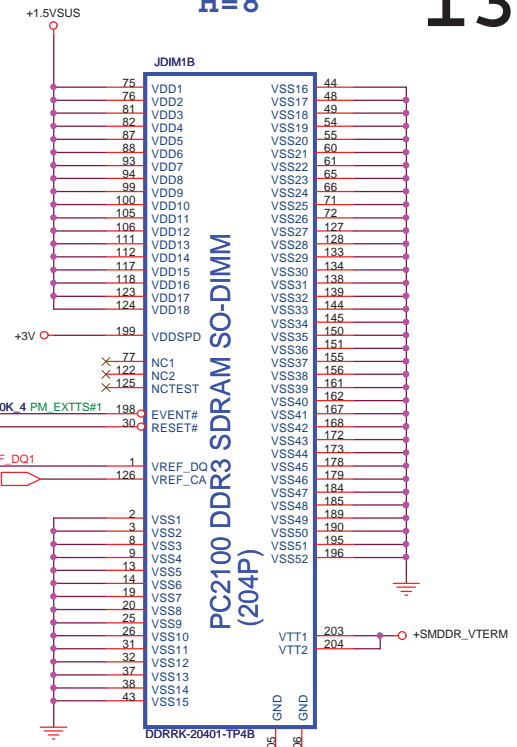
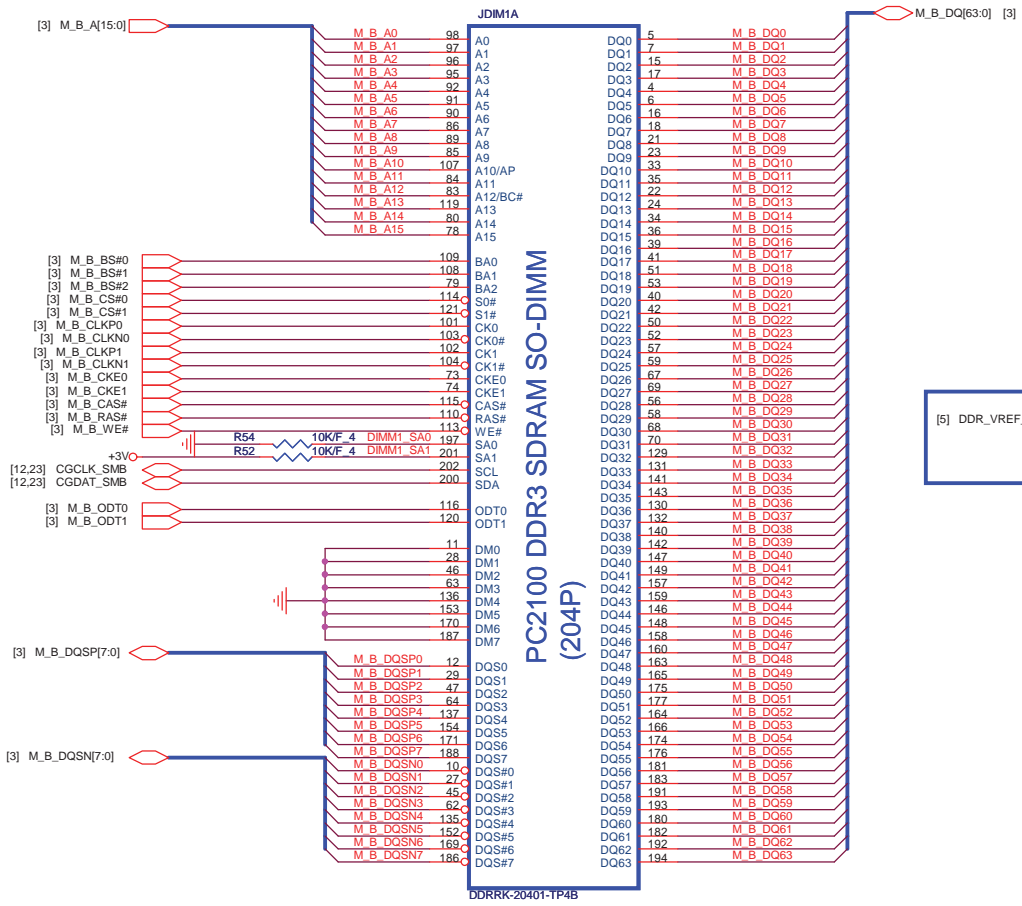
VREF_DQ/ (M1)



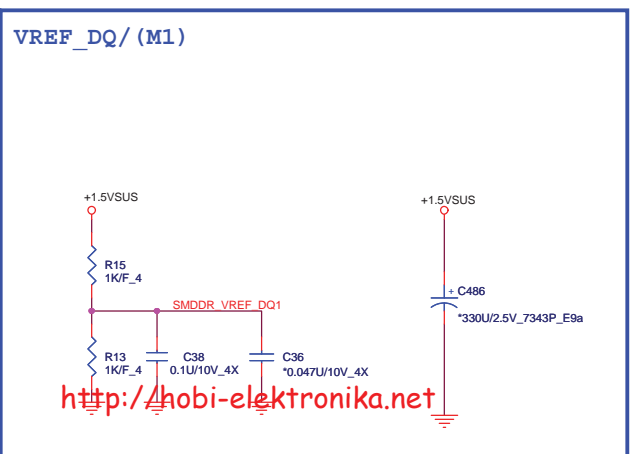
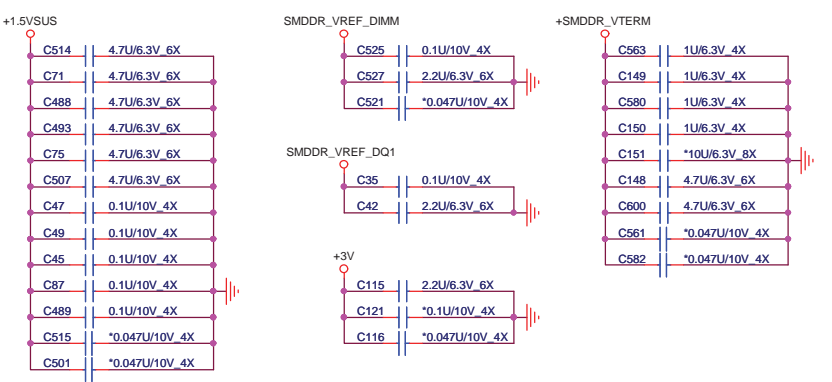
S3 Power Reduction



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Place these Caps near So-Dimm1.

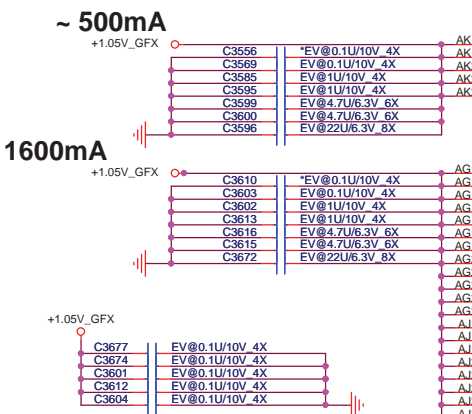


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Size	Document Number	Rev
	DDR3 DIMM-1	1A
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<http://hobi-elektronika.net>

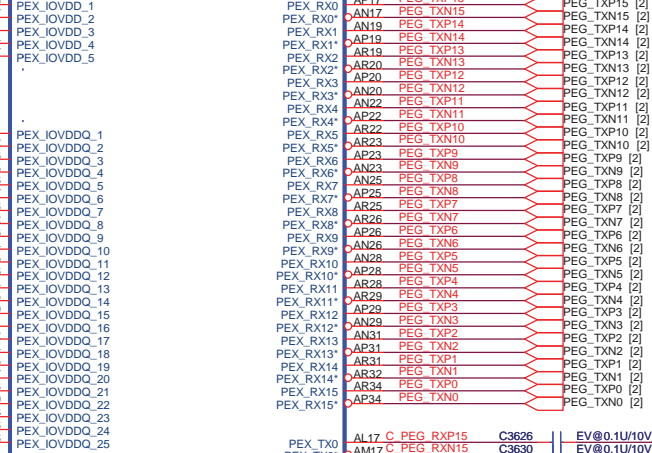
PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A



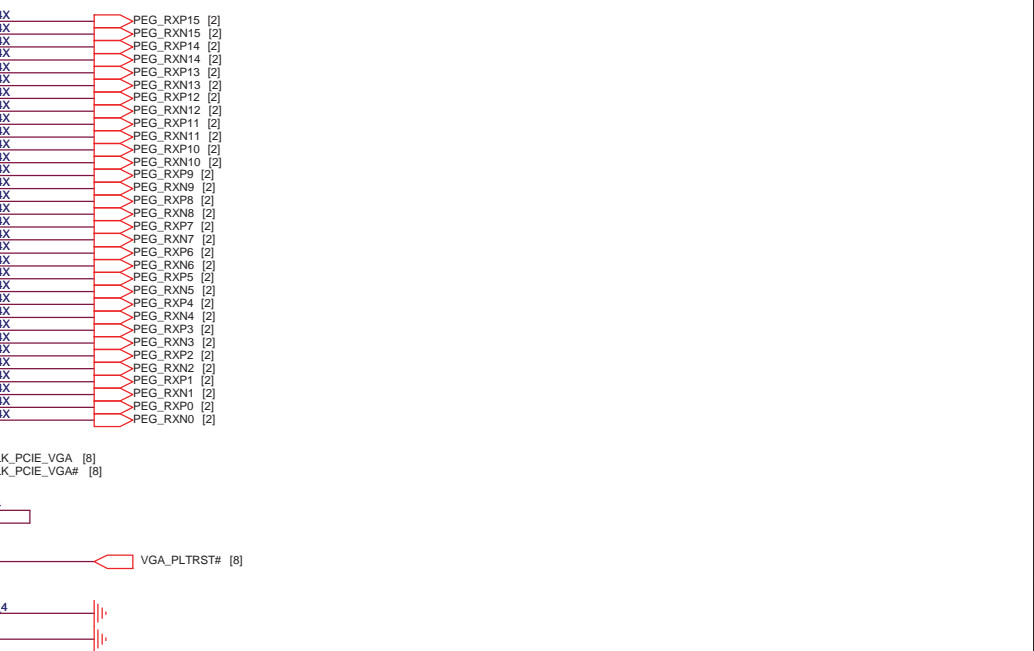
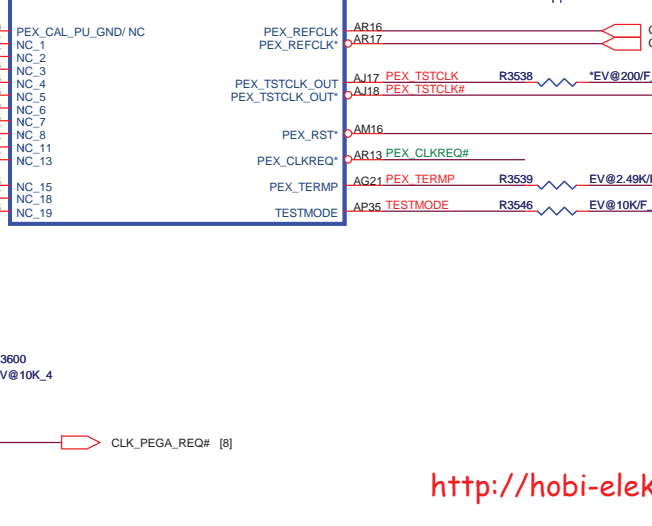
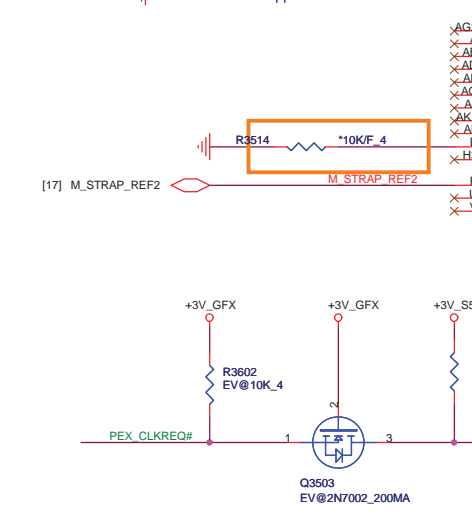
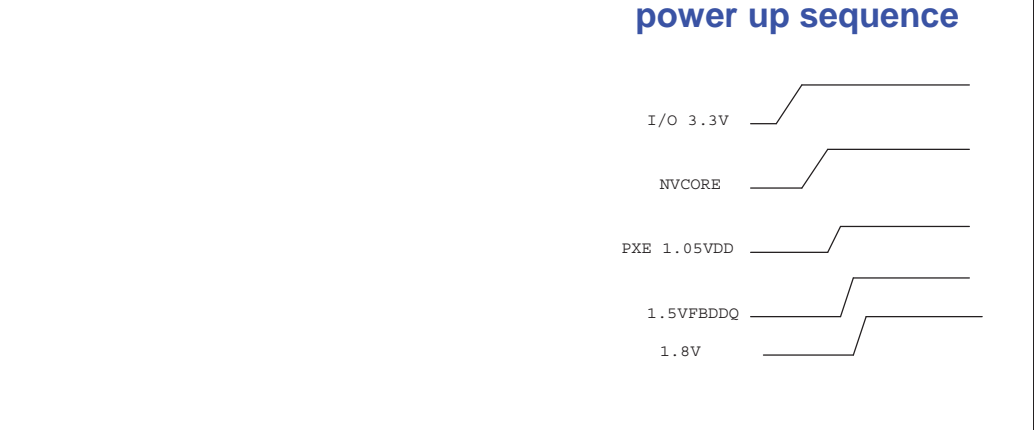
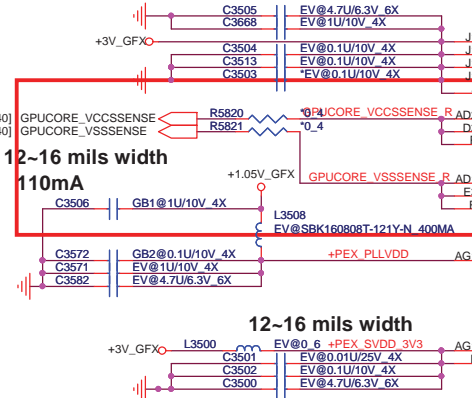
GPU3500A

fdg973-nvidia-n11p-es-a1

COMMON



PCI EXPRESS



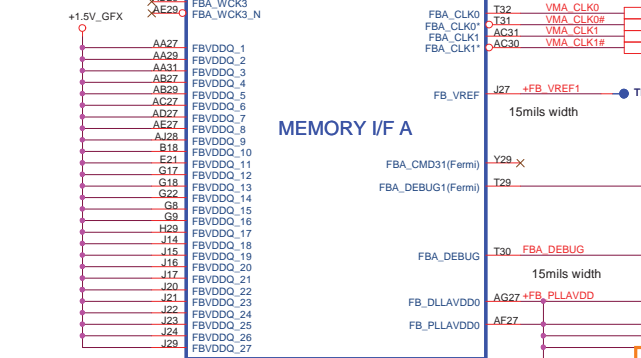
Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	N12x-Fermi PCIe	1A
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GPU3500B

Table of pin connections for GPU3500B, listing pins like FBA_CMD0 to FBA_CMD30 and VMA_DM0 to VMA_DM7.

Table of pin connections for GPU3500B, listing pins like VMA_WDQ0 to VMA_WDQ7 and VMA_RDQ0 to VMA_RDQ7.

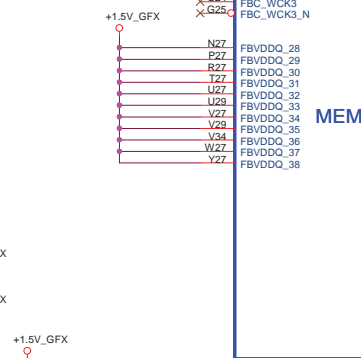


MEMORY I/F A

GPU3500C

Table of pin connections for GPU3500C, listing pins like FBC_CMD0 to FBC_CMD30 and VMC_DM0 to VMC_DM7.

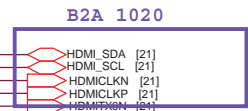
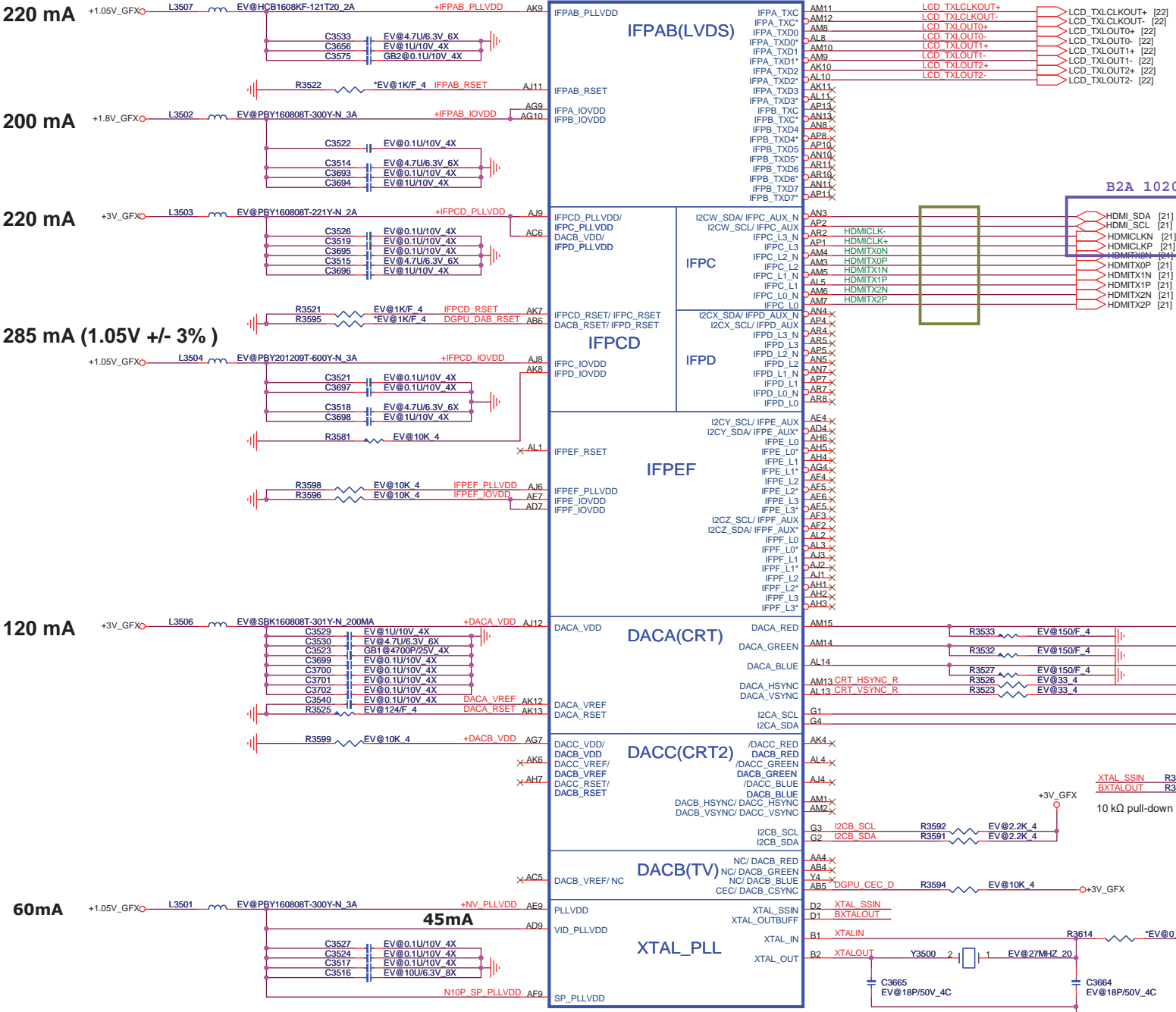
Table of pin connections for GPU3500C, listing pins like VMC_WDQ0 to VMC_WDQ7 and VMC_RDQ0 to VMC_RDQ7.



MEMORY I/F C

Quanta Computer Inc. PROJECT : BLBD N12x-Fermi (MEM I/F) Date: Monday, November 22, 2010 Sheet 15 of 42


GPU1500D
fcbg973-nvidia-n11p-es-a1
COMMON



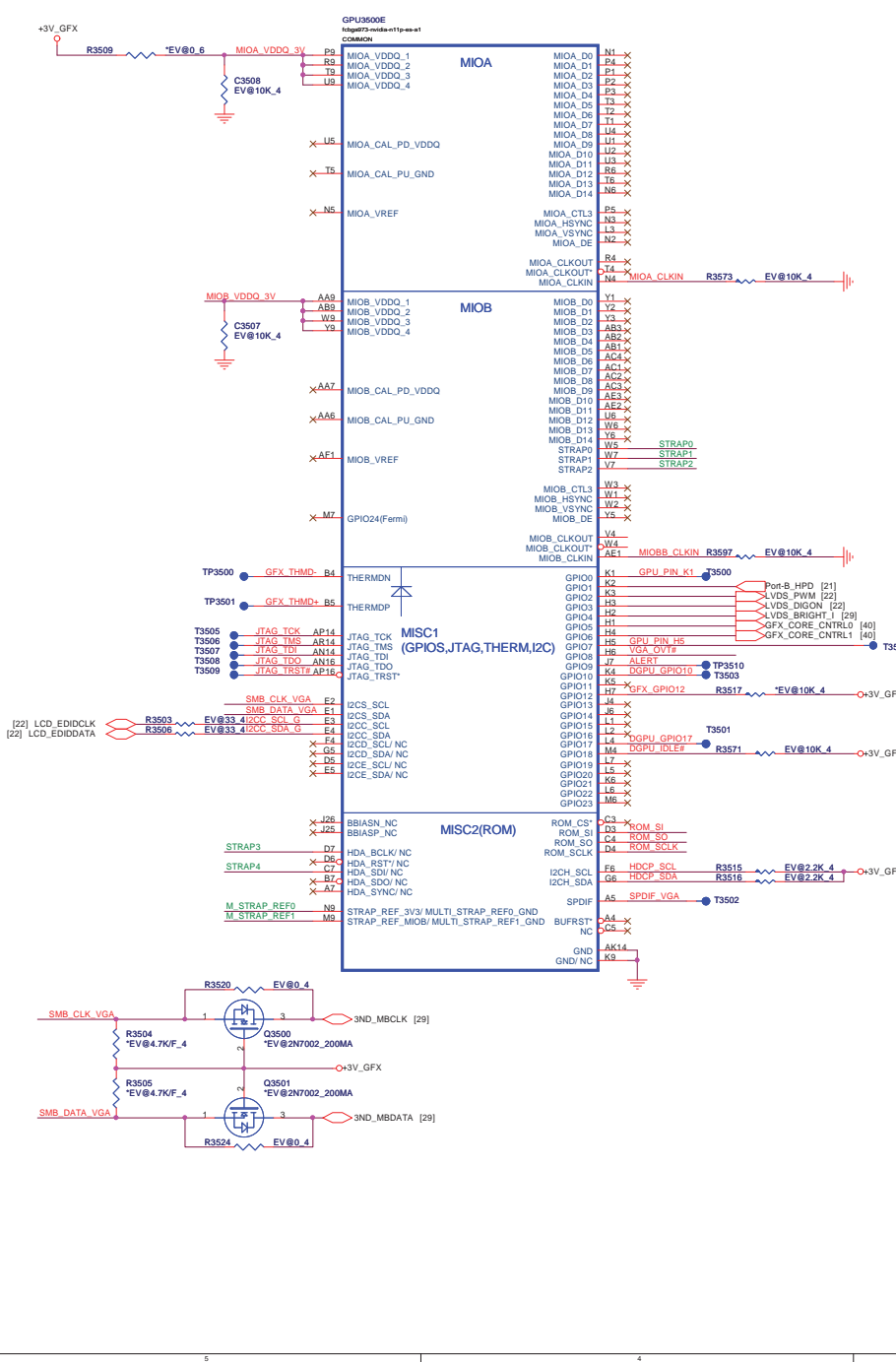
XTAL_SSN R3584 EV@10K_4
BXTALOUT R3593 EV@10K_4
10 kΩ pull-down only if no spread chip used.

STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED

<http://hobi-elektronika.net>

 **Quanta Computer Inc.**
PROJECT : BLBD

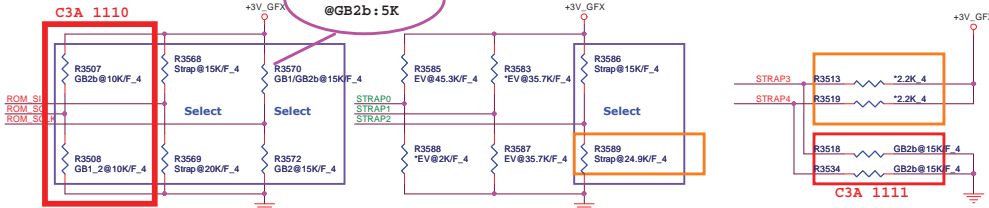
Size	Document Number	Rev
	N12x-Fermi (DISPLAY)	1A
Date:	Monday, November 22, 2010	Sheet 16 of 42



Strappin Model select

MODE	M_STRAP_REF0	M_STRAP_REF1	M_STRAP_REF2
Multi-level	40.2K/F_4 PD	40.2K/F_4 PD	40.2K/F_4 PD

MULTI level strap select



18-V

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	N12M-GB @GB1	N12P-GV @GB2b	N12P-LP @GB2	
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010(15KPU)	1000(5KPU)	0010(15KPD)	
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	RAMCFG T	RAMCFG T	RAMCFG T	
ROM_SO	GB1/2	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001(10KPD)	1001(10KPU)	0001(10KPD)
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111(45KPU)	1111(45KPU)	1111(45KPU)	
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110(35KPD)	0110(35KPD)	0110(35KPD)	
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1010(15KPU)	0000(5KPD)	1100(25KPU)	
STRAP3(Only GB2B)	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED		0010(15KPD)		
STRAP4(Only GB2B)	Reserve	Reserve	PCIE_MAX_SPEED	PD_PLL_VDD33V		0010(15KPD)		

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI	
b30 0000					
b31 0001					
b32 0010	DDR3 64Mx16x8, 128bit, 1GB	Hynix	H5TQ1G63DFR-12C(800MHz) / H5TQ1G63DFR-11C(900MHz)	AKD5LZWTW02	PD 15K PD 20K
b33 0111	DDR3 64Mx16x8, 128bit, 1GB	Samsung	K4W1G1646E-HC12(800MHz) / K4W1G1646E-HC11(900MHz)	AKD5LGH7500	
b34 0101					
b35 0110	DDR3 128Mx16x8, 128bit, 2GB	Hynix	H5TQ2G63BFR-12C(800MHz) / H5TQ2G63BFR-11C(900MHz)		PD 35K PD 45K
b36 0110	DDR3 128Mx16x8, 128bit, 2GB	Samsung	K4W2G1646C-HC1(800MHz) / K4W2G1646C-HC11(900MHz)		
b37 0111					

N12M-GE(QS)
Device Id=0x0A7A
STRAP2 =15K PU
ROM_SCLK=15K PU

N12P-GV(QS)
Device Id=-x1050
STRAP2 =5K PD
ROM_SCLK=5K PU

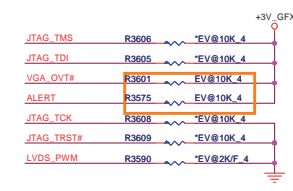
N12P-LP(QS)
Device Id=0x0DEC
STRAP2=25K PU
ROM_SCLK=15K PD

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

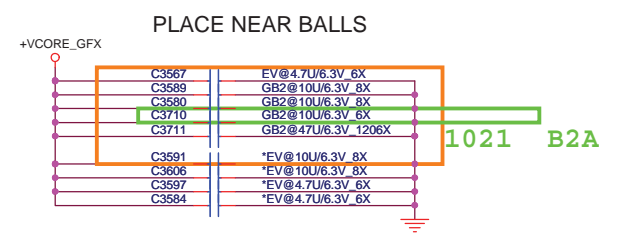
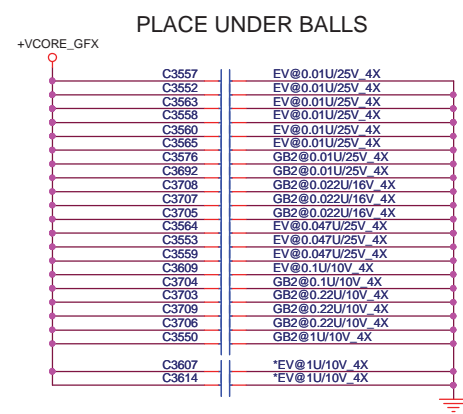
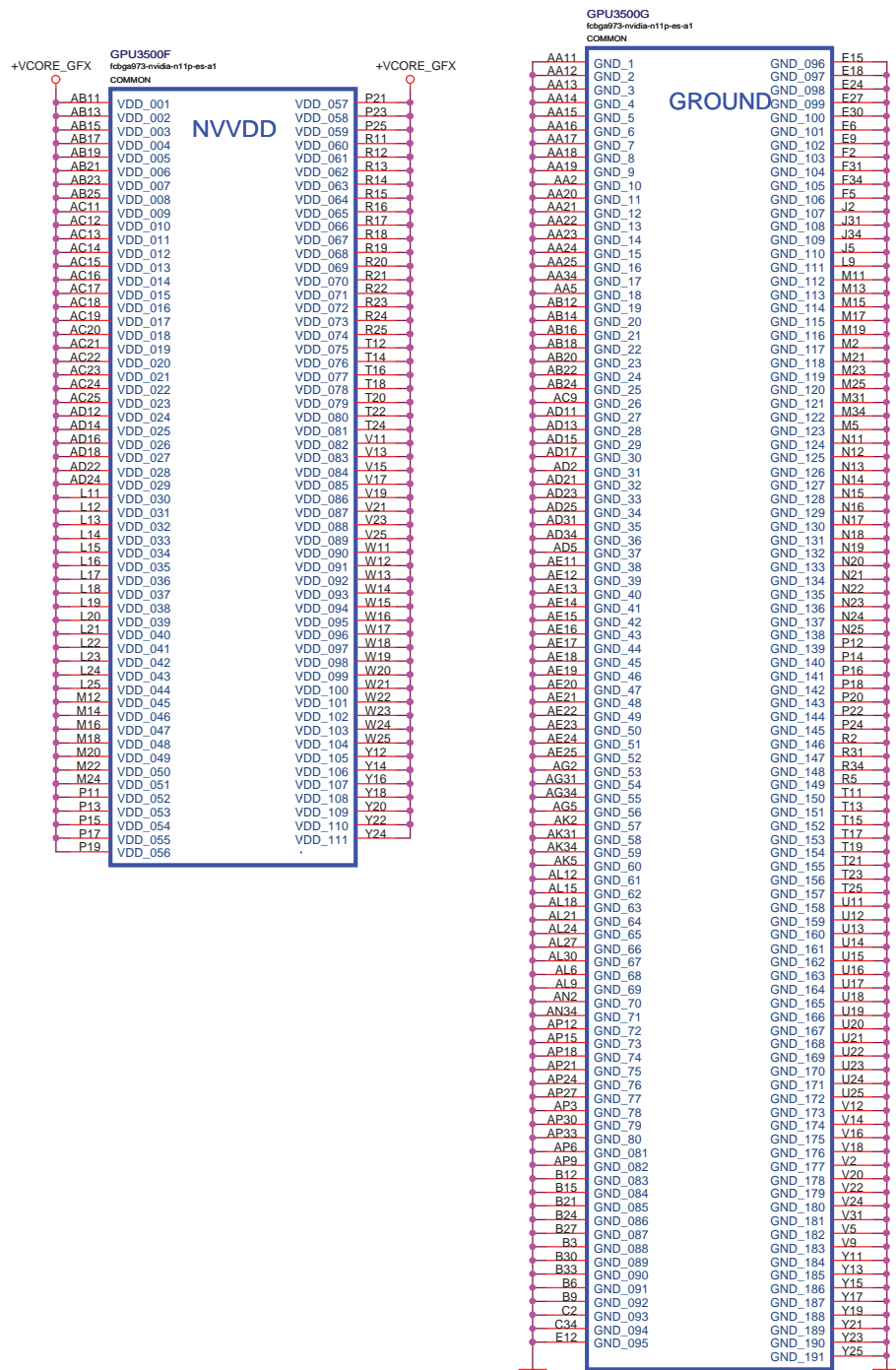
Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



Quanta Computer Inc.
PROJECT : BLBD

Size Document Number N12x-Fermi (GND&Str&Ther) Rev 1A
Date: Monday, November 22, 2010 Sheet 17 of 42



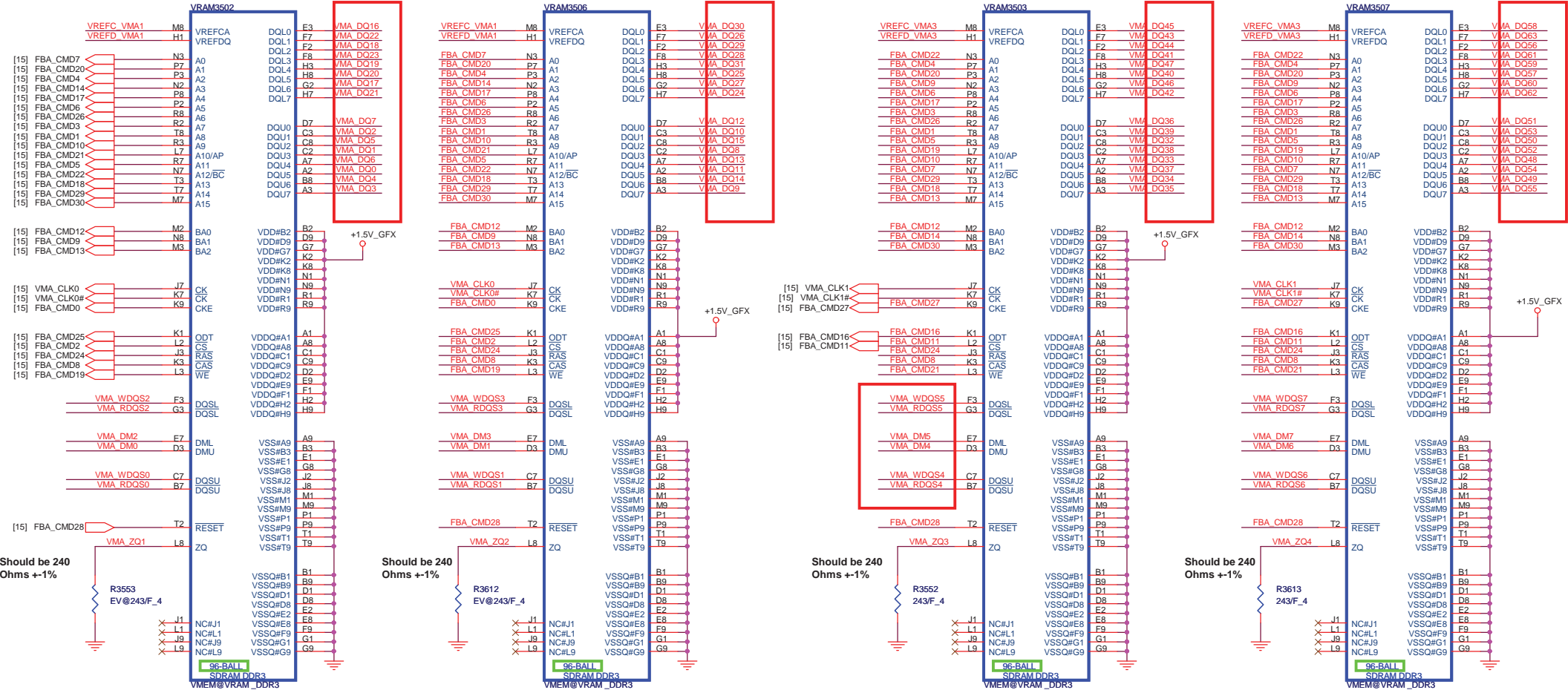
<http://hobi-elektronika.net>

Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	N12x-Fermi (GND/Power)	1A
Date:	Monday, November 22, 2010	Sheet 18 of 42

CHANNEL A: 256MB/512MB DDR3

[15] VMA_DQ[63..0]
[15] VMA_DM7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

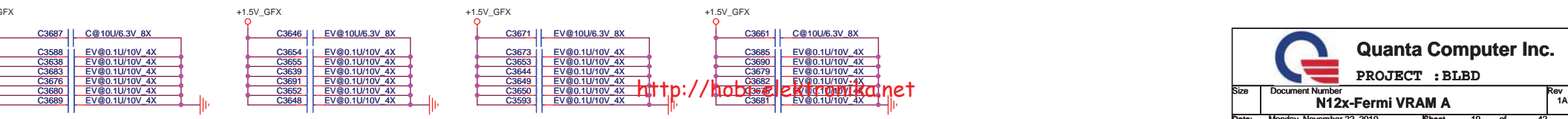
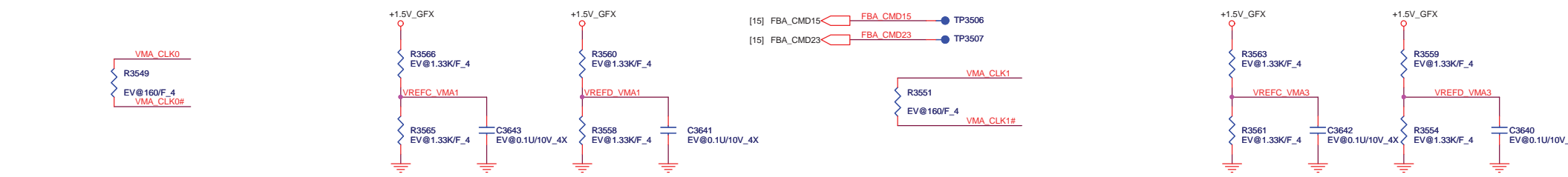


Should be 240 Ohms +-1%

Should be 240 Ohms +-1%

Should be 240 Ohms +-1%

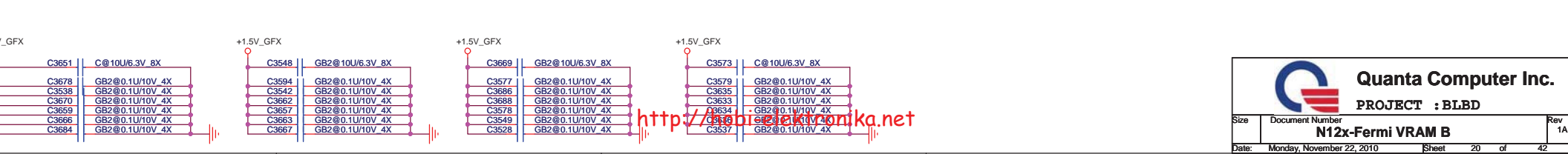
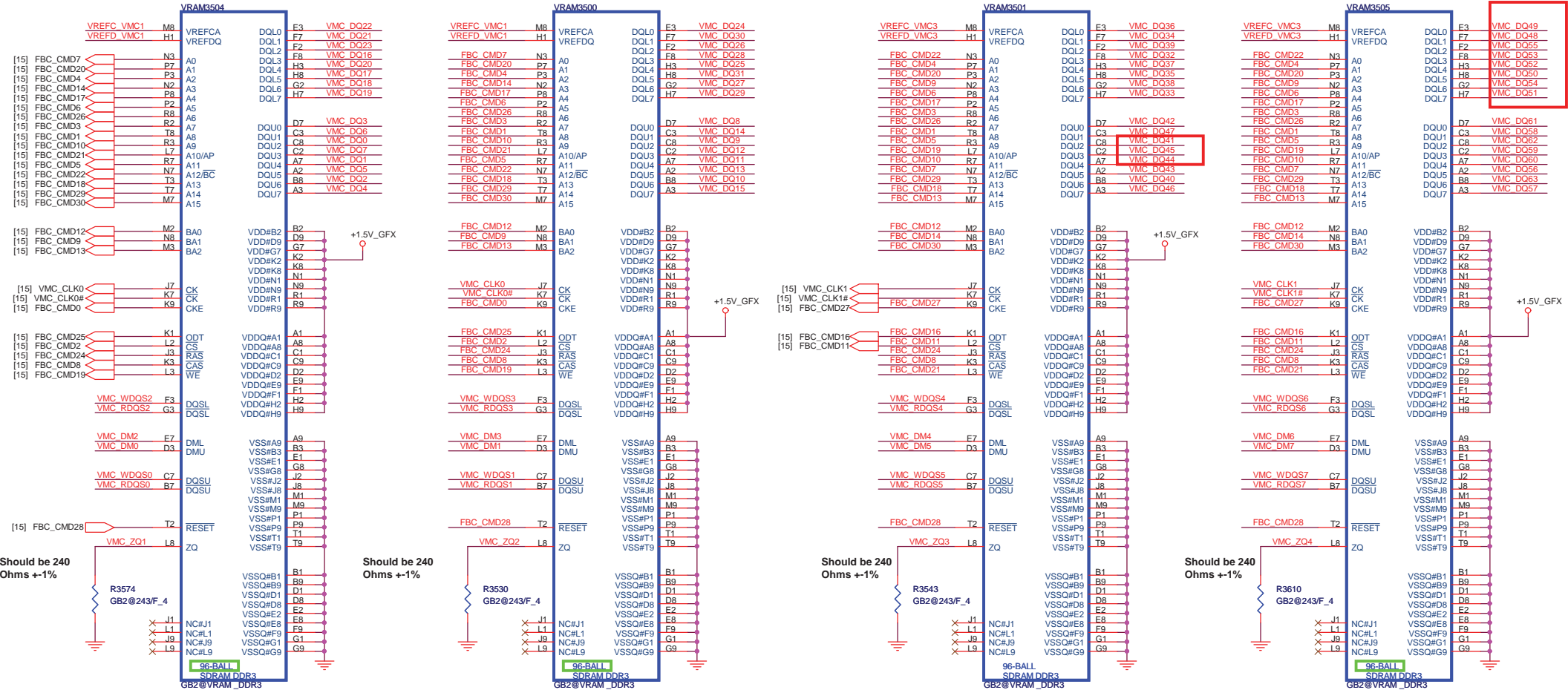
Should be 240 Ohms +-1%



http://hobbyelectronics.net

Quanta Computer Inc. PROJECT : BLBD 112x-Fermi VRAM A Rev 1A Date: Monday, November 22, 2010 Sheet 19 of 42

CHANNEL B: 256MB/512MB DDR3



Quanta Computer Inc.
PROJECT : BL2B

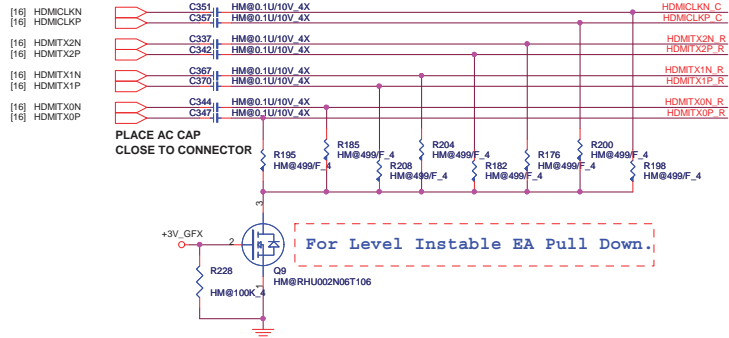
Size	Document Number	Rev
	N12x-Fermi VRAM B	1A
Date:	Monday, November 22, 2010	Sheet 20 of 42

http://www.newsonika.net

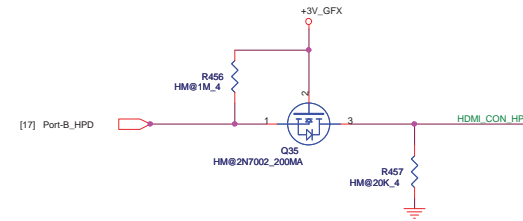
VGA HDMI
HDMI-passive level shift <HMP/HMG>

HDMI Interface

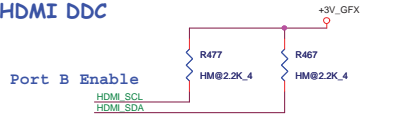
Angelo 0921



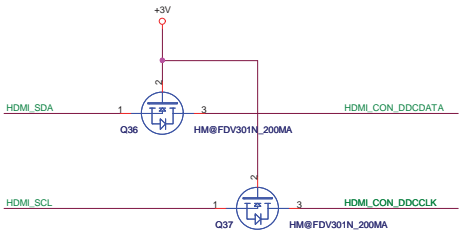
HDMI HPD



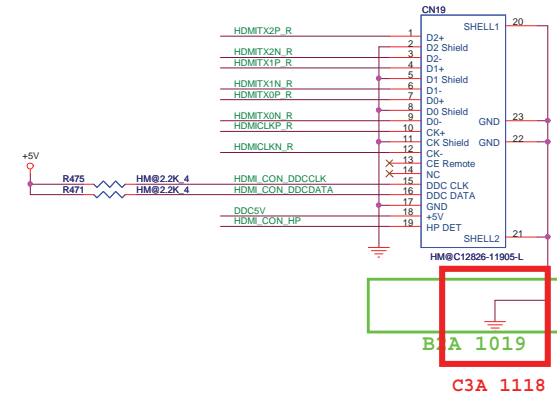
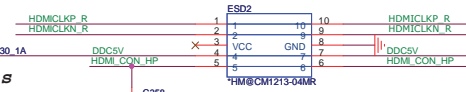
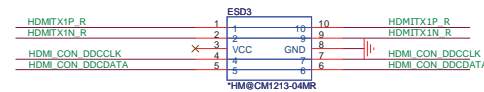
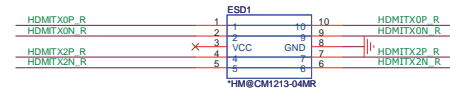
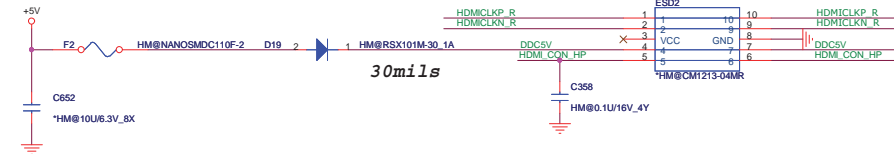
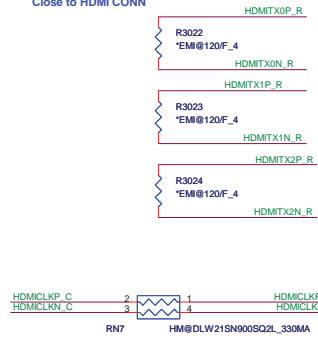
HDMI DDC



[16] HDMI_SCL
[16] HDMI_SDA



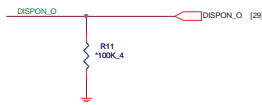
Close to HDMI CONN



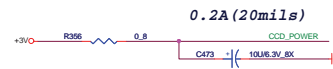
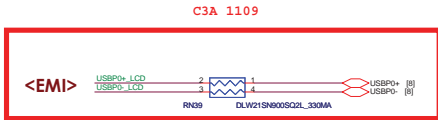
Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	HDMI CONN	1A
Date:	Monday, November 22, 2010	Sheet 21 of 42

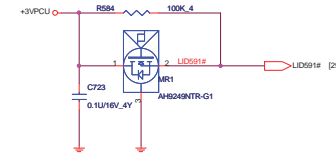
Panel backlight control <LDS>



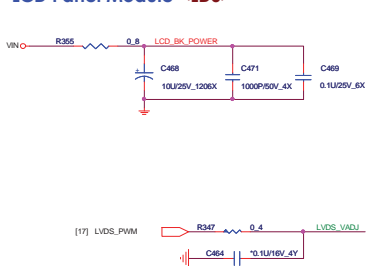
CCD <CCD>



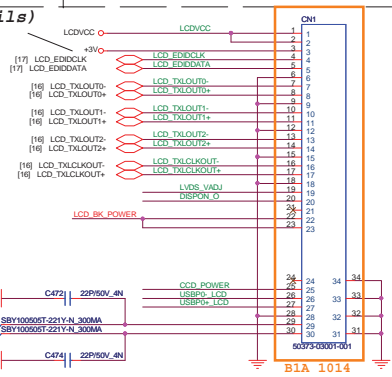
HALL SENSOR&BACK LIGHT SWITCH <HSR>



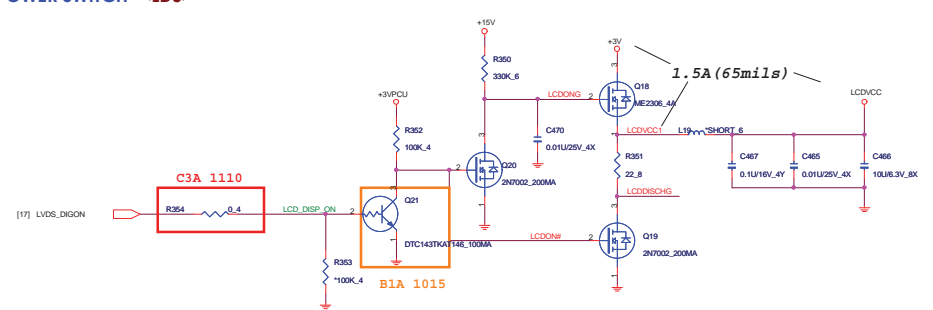
LCD Panel Module <LDS>



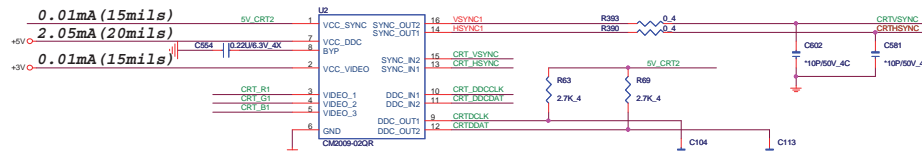
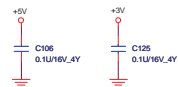
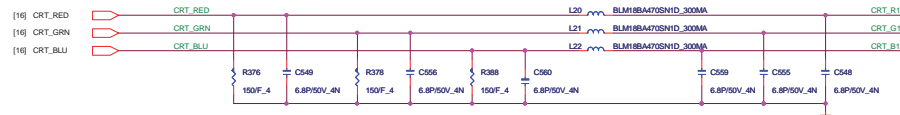
0.3A (20mils)



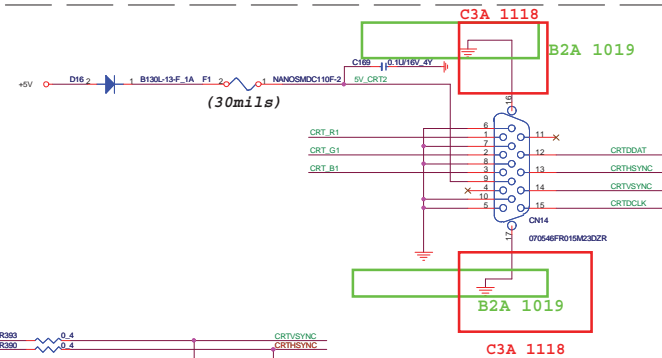
LCD POWER SWITCH <LDS>



CRT <CRT>

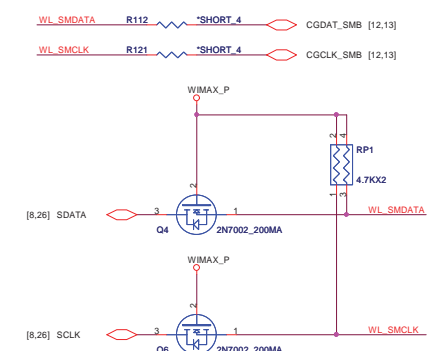
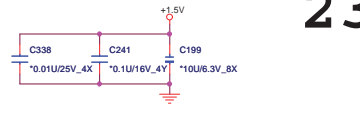
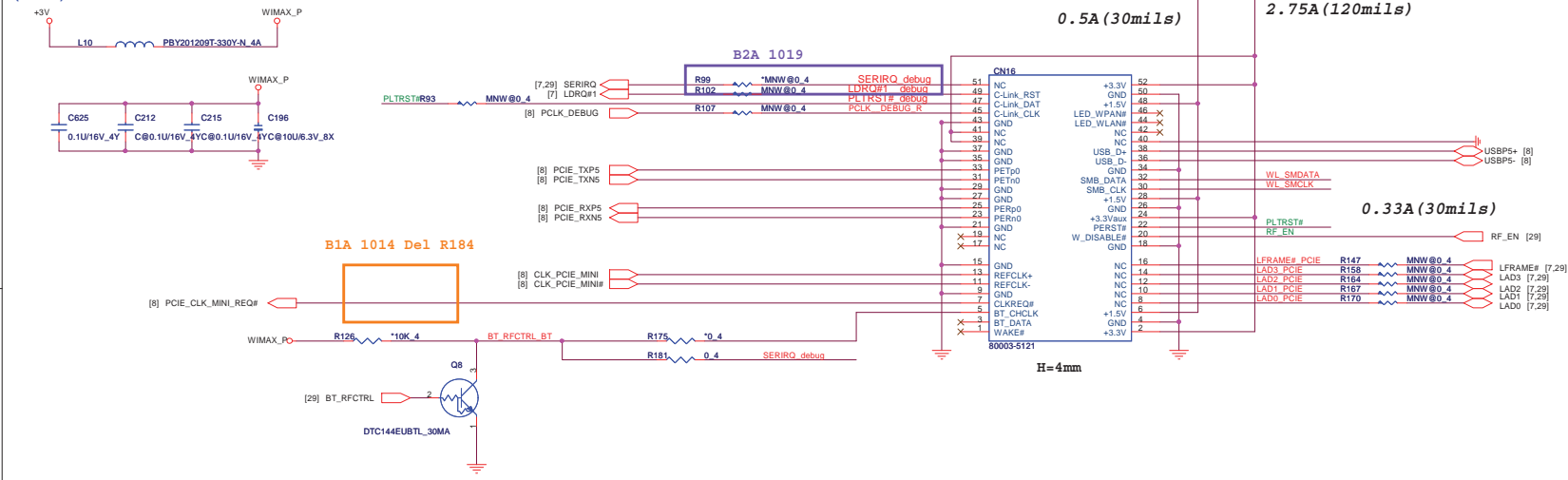


<DPP>

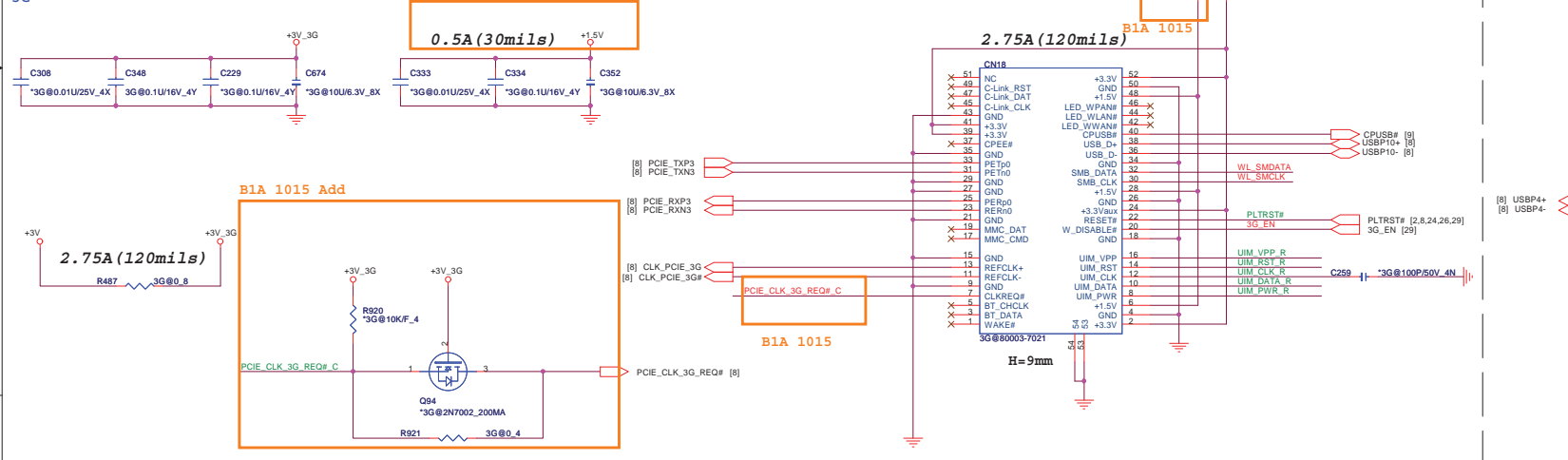


Quanta Computer Inc.
 PROJECT : BLBD
 Sheet 22 of 42
 Date: Monday, November 22, 2010

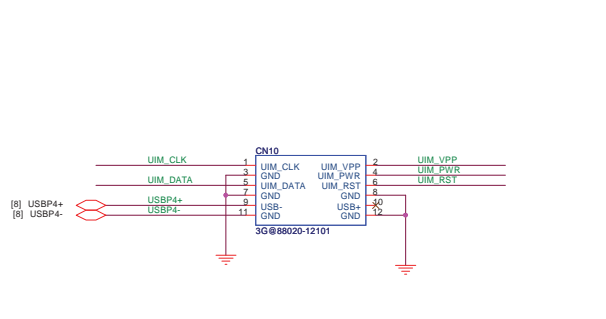
MINI Card Slot#1 <MNV>



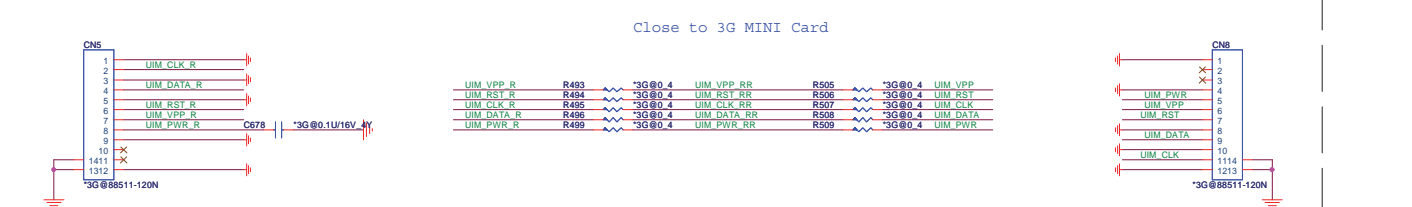
MINI Card Slot#2 <MNT>



SIM CARD board to board <MNT>



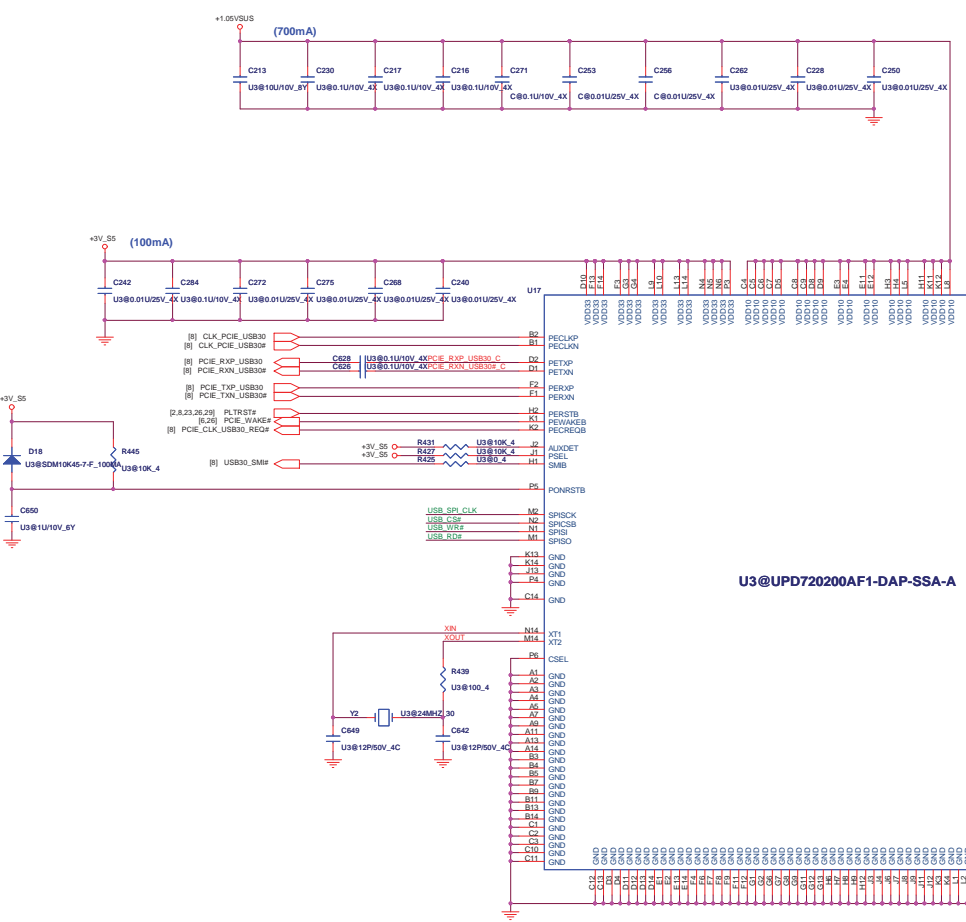
3G CONN <MNT>



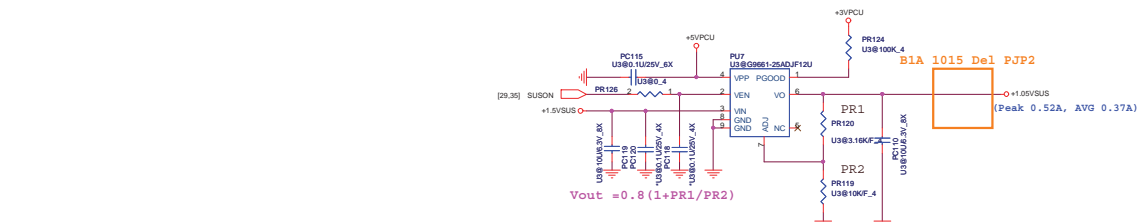
Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	MINI CARD(WLAN/3G/SIM Card)	1A
Date	Manday, November 22, 2010	Sheet 23 of 42

USB 3.0 Controller <U3B>

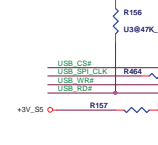


U3@UPD720200AF1-DAP-SSA-A

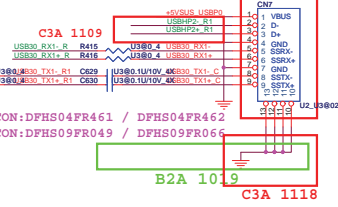


USB 3.0 Power switch

EEPROM <U3B>

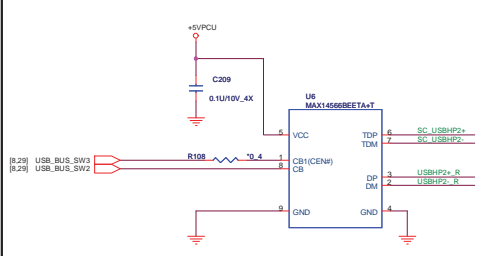


USB 3.0 CONN <U3B> <USB>



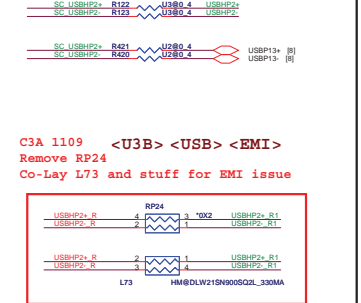
C3A 1115 Jianfa mail modify footprint

USB w S&C MAXIM solution <SLC>



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through (USB) mode: Connect DP/DM to TDP/TDM

USB 2.0 Colay <U3B> <U2B>

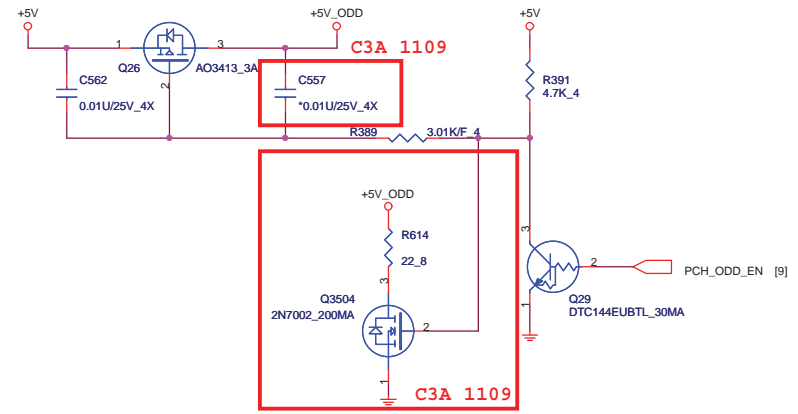
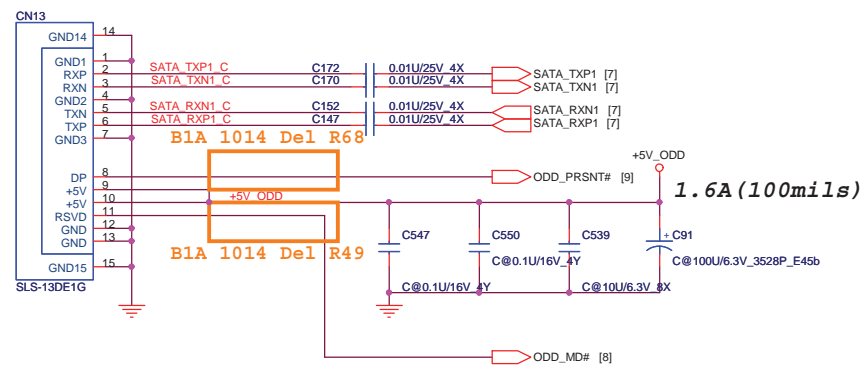


C3A 1109 <U3B> <USB> <EMI> Remove RP24 Co-Lay L73 and stuff for EMI issue

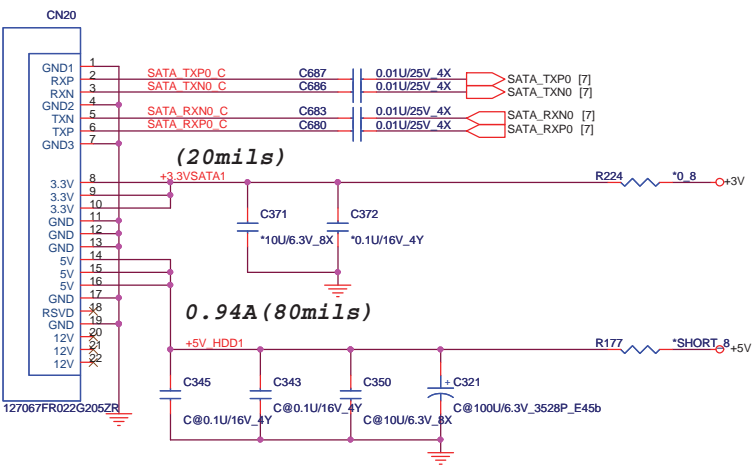


ODD Zero power . (Only for Intel) <OZP>

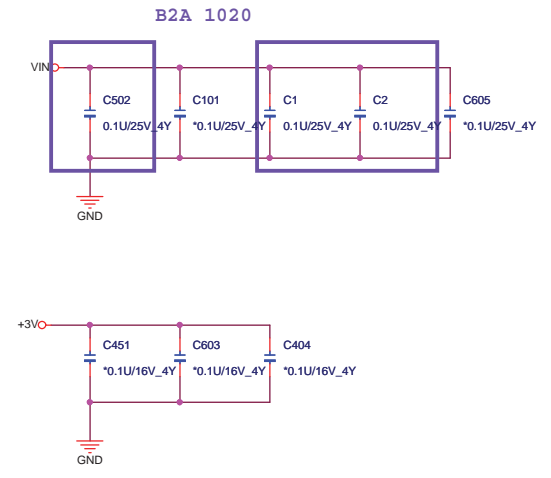
SATA ODD



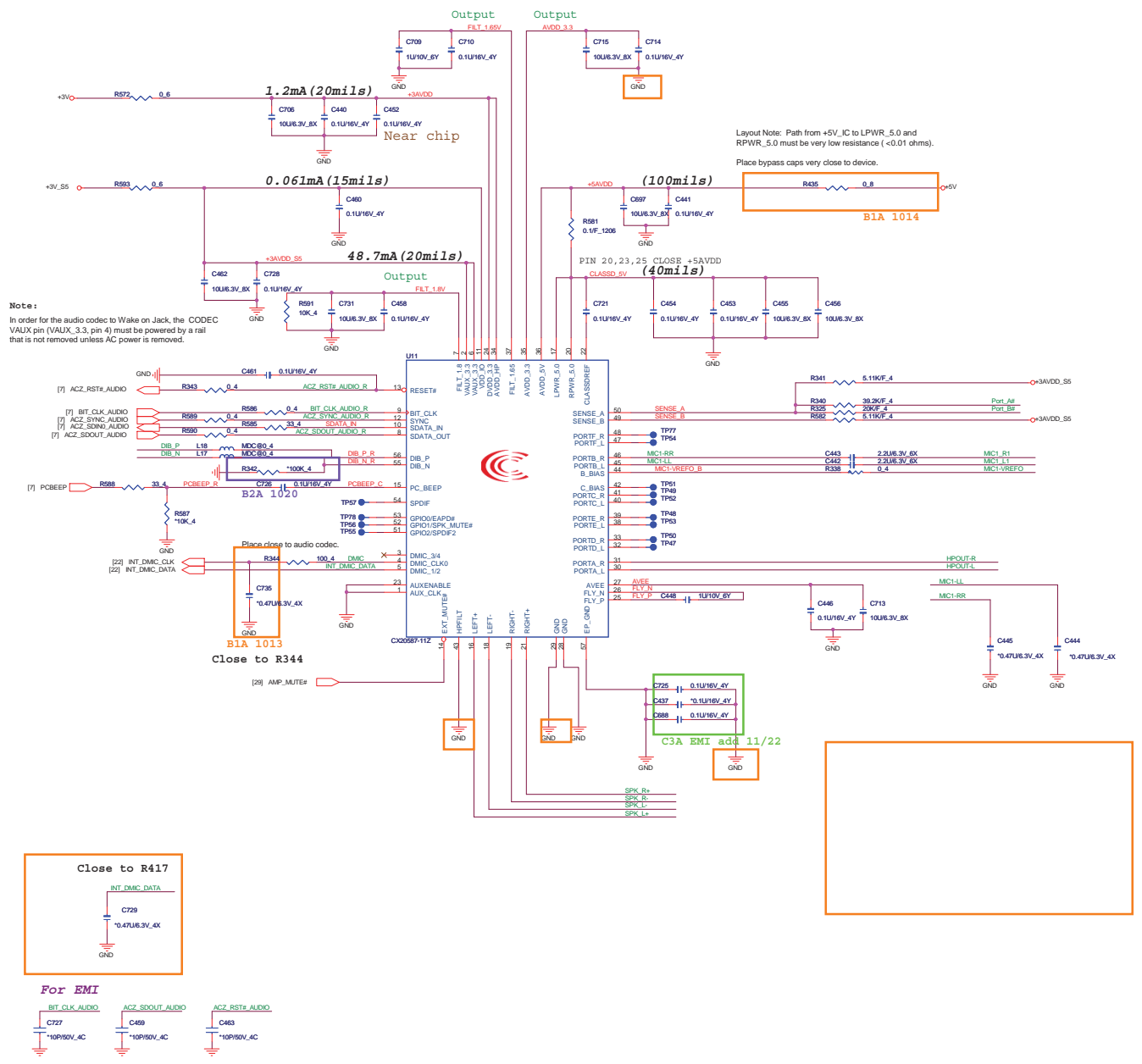
SATA HDD



EMI

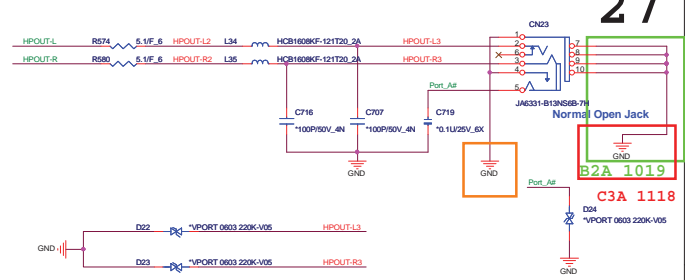


<http://hobi-elektronika.net>

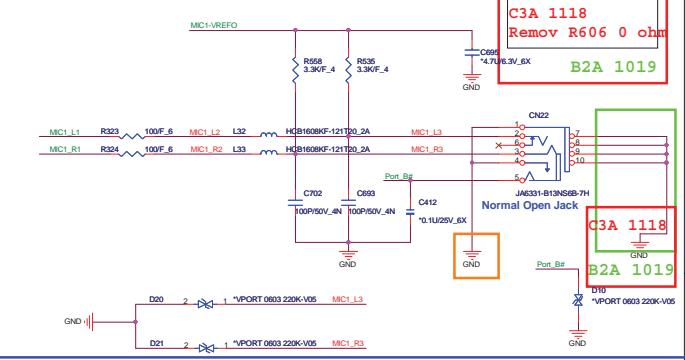


Earphone

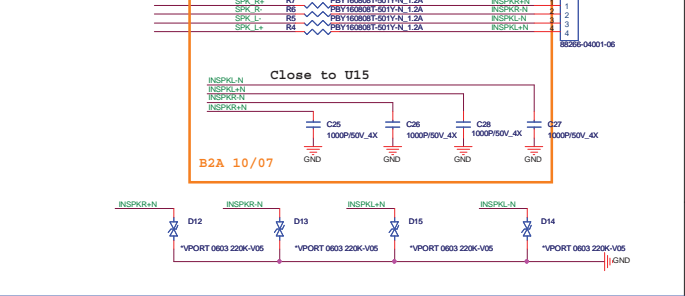
27



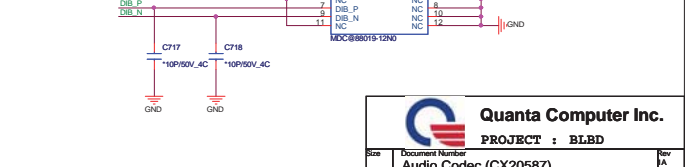
External MIC



Internal Speaker

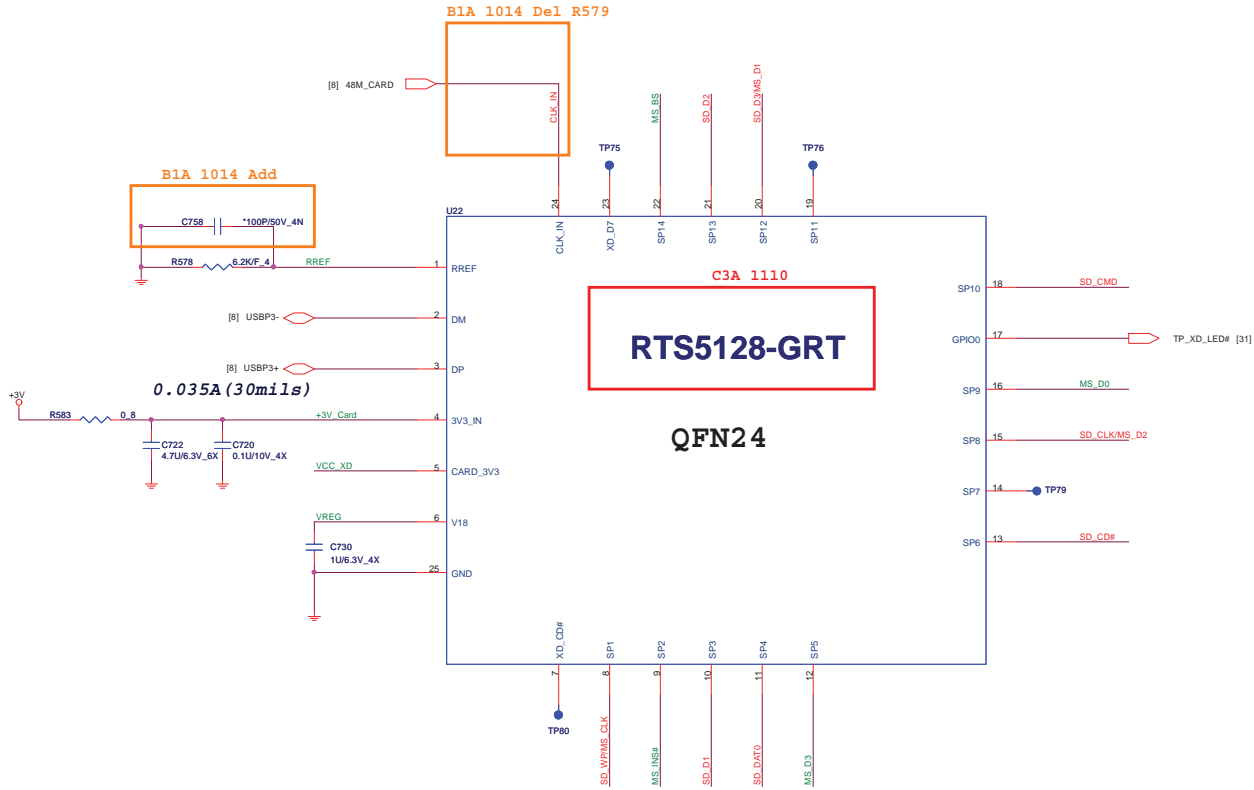


MDC <MDM>



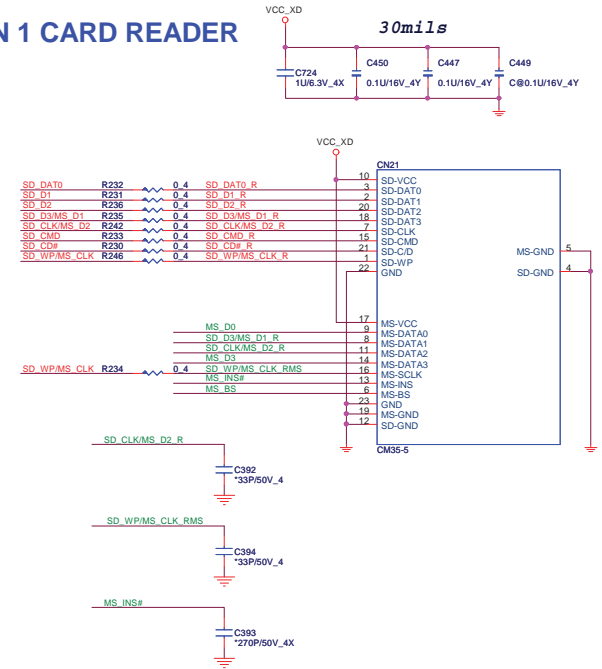
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3 IN 1 CARD READER

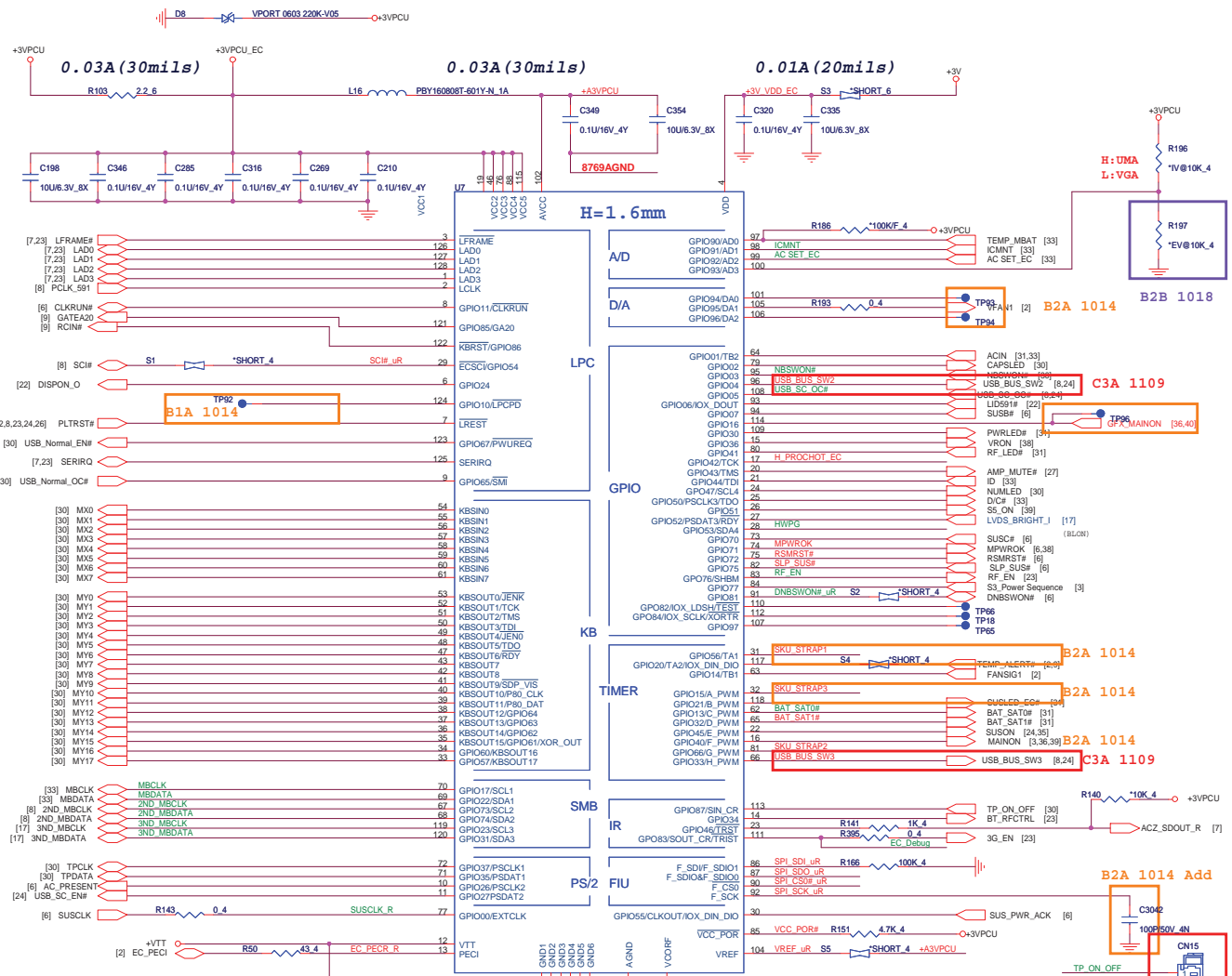


AL005128001 IC CTRL(24P) RTS5128-GRT(QFN)

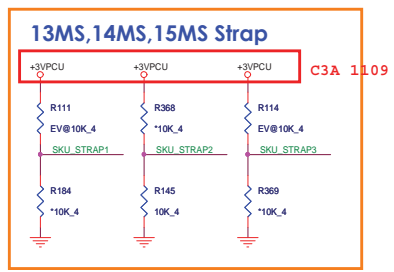
3 IN 1 CARD READER




Quanta Computer Inc.
 PROJECT : BLBD
 Document Number
RTS5159 (Card Reader)
 Date: Monday, November 22, 2010 Sheet 28 of 42 Rvw 1A

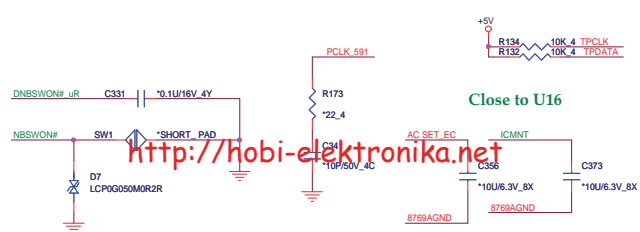


MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3
13" UMA	0	0	0
13" DIS	0	0	1
14" UMA	0	1	0
14" DIS	0	1	1
15" UMA	1	0	0
15" DIS	1	0	1

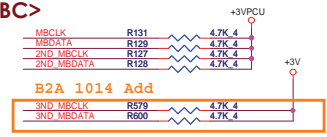


SMBUS Table

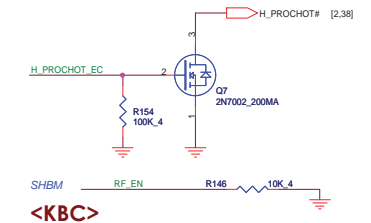
SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	EC EEPROM	A0H
	VGA Board Thermal Sensor	98H
3		



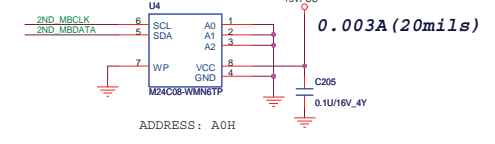
SM BUS PU <KBC>



Intel Turbo mode only <CPU>

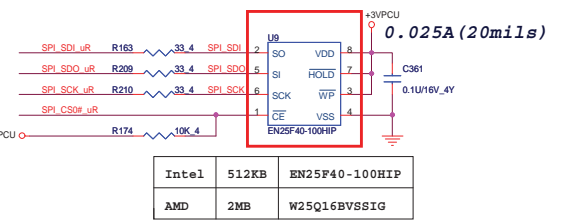


ID <KBC>

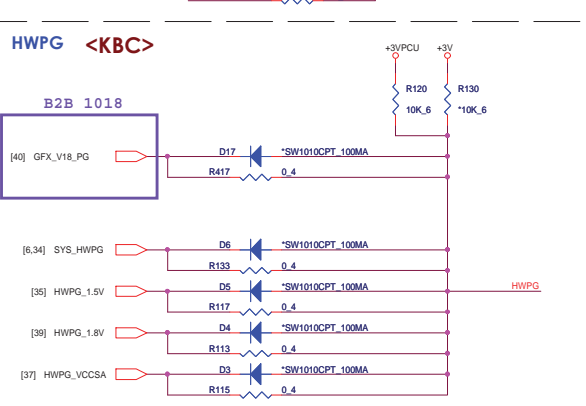


SPI FLASH <KBC>

C3A 1119 Change P/N avoid the same with USB30 portion

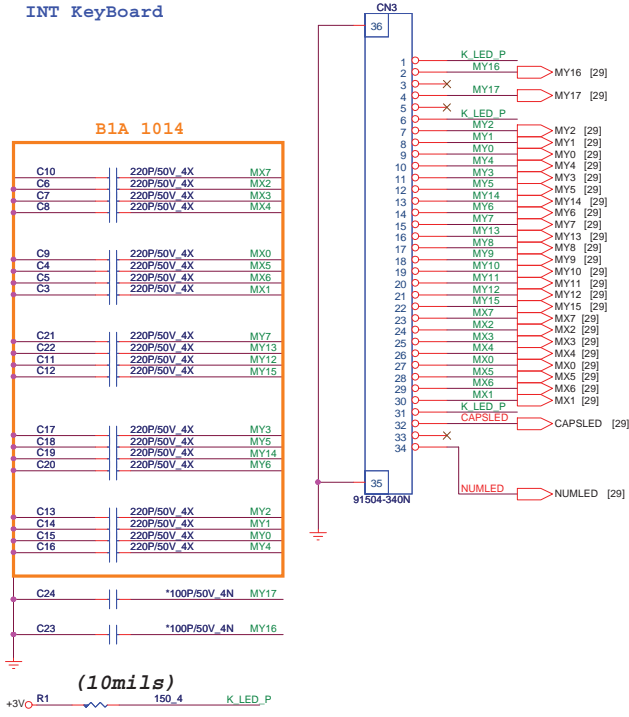


INTERNAL KEYBOARD STRIP SET <KBC>

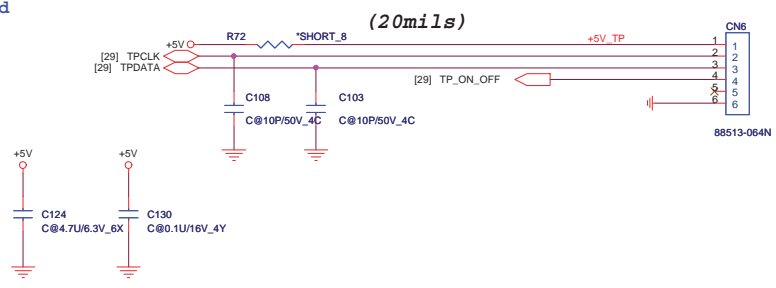


HWPG <KBC>

INT Keyboard

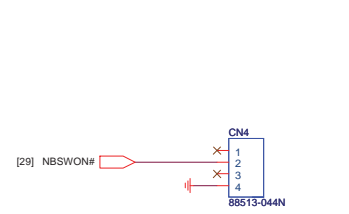


TP board

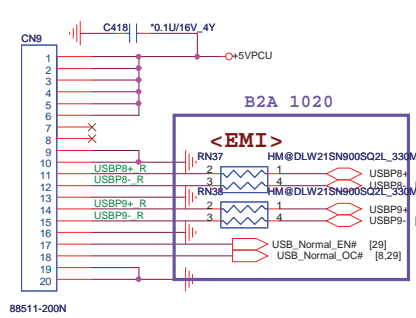


Bluetooth

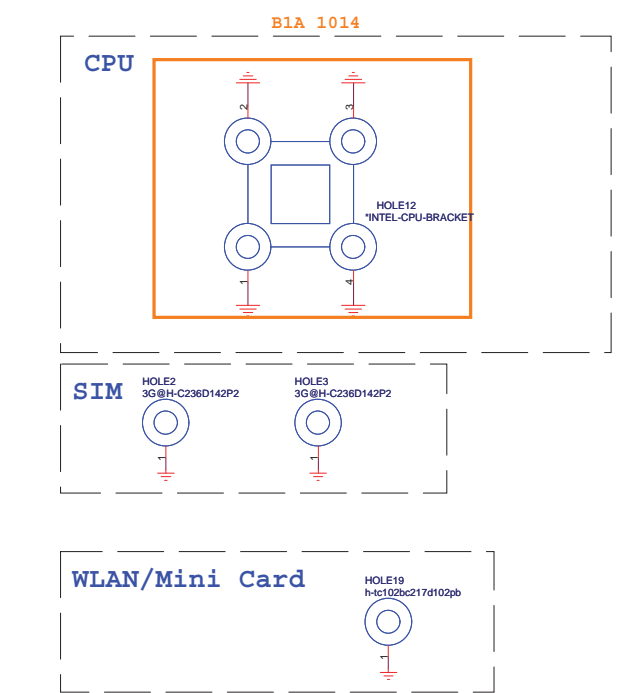
Power board



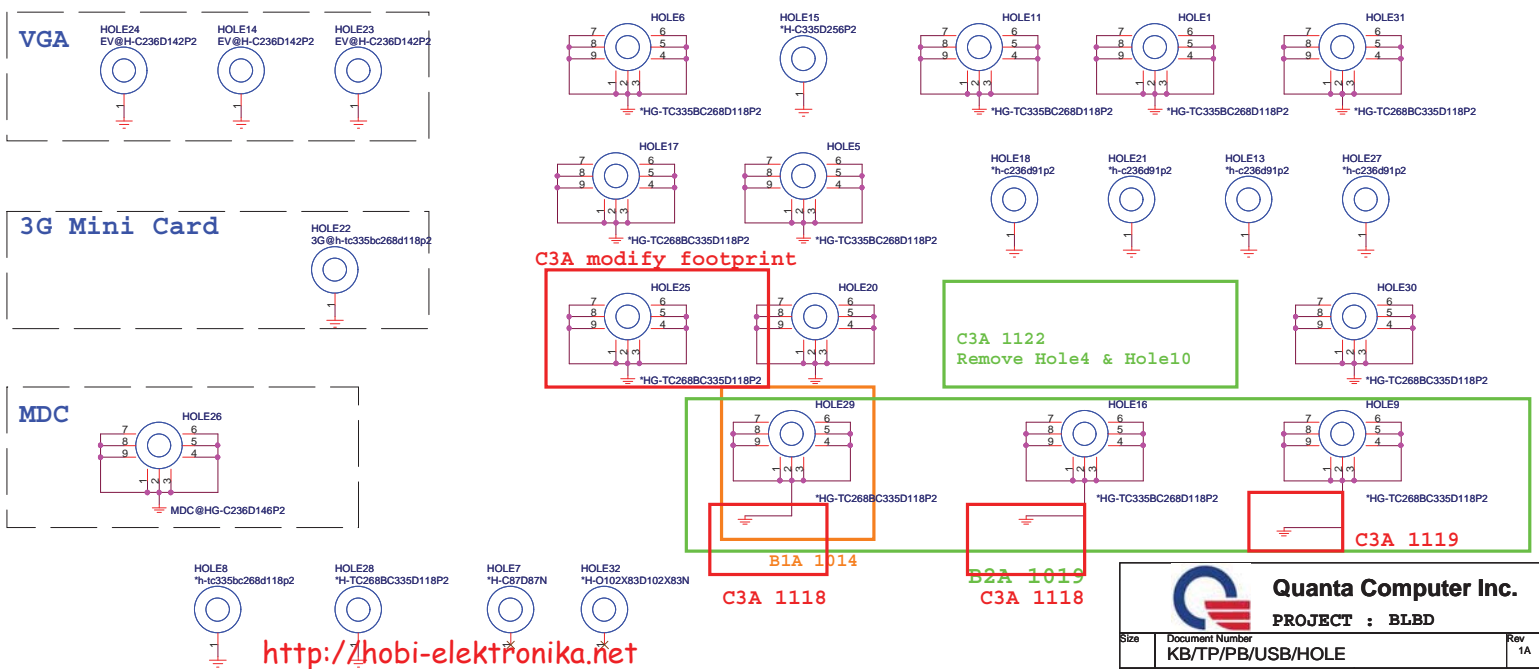
USB board



NUM



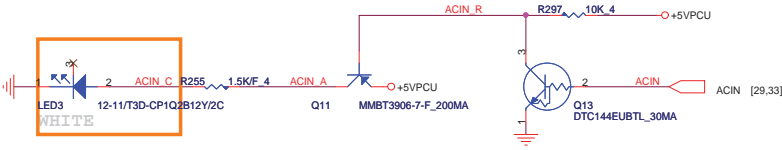
HOLE



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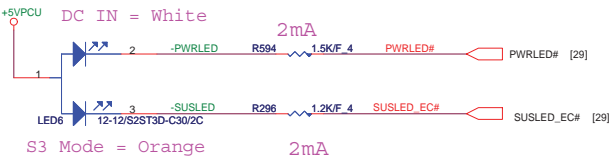
LED

AC-IN



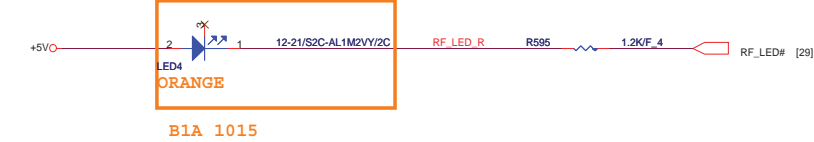
B1A 1015

POWER



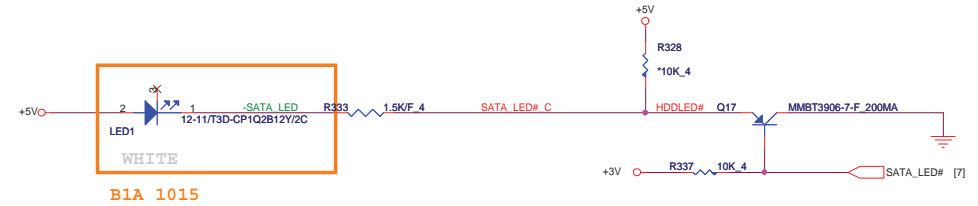
S3 Mode = Orange 2mA

RF LED



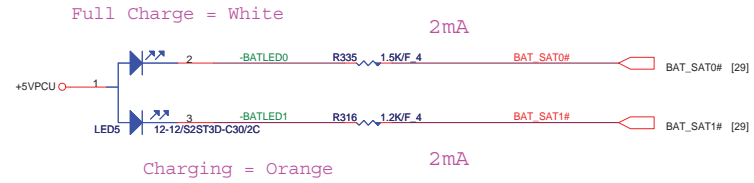
B1A 1015

HDD/ODD



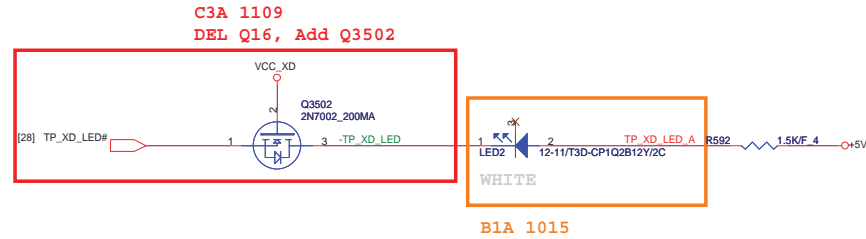
B1A 1015

BATTERY



Full Charge = White
Charging = Orange 2mA

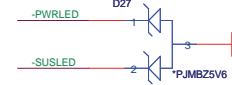
CARDREADER



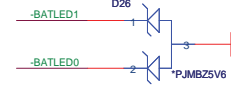
B1A 1015

ESD Protect

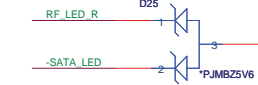
FOR POWER LED



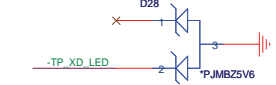
FOR BATTERY LED




FOR HDD/RF LED

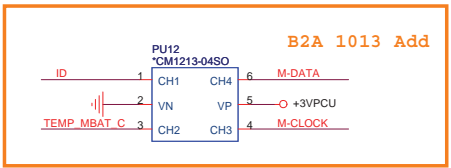
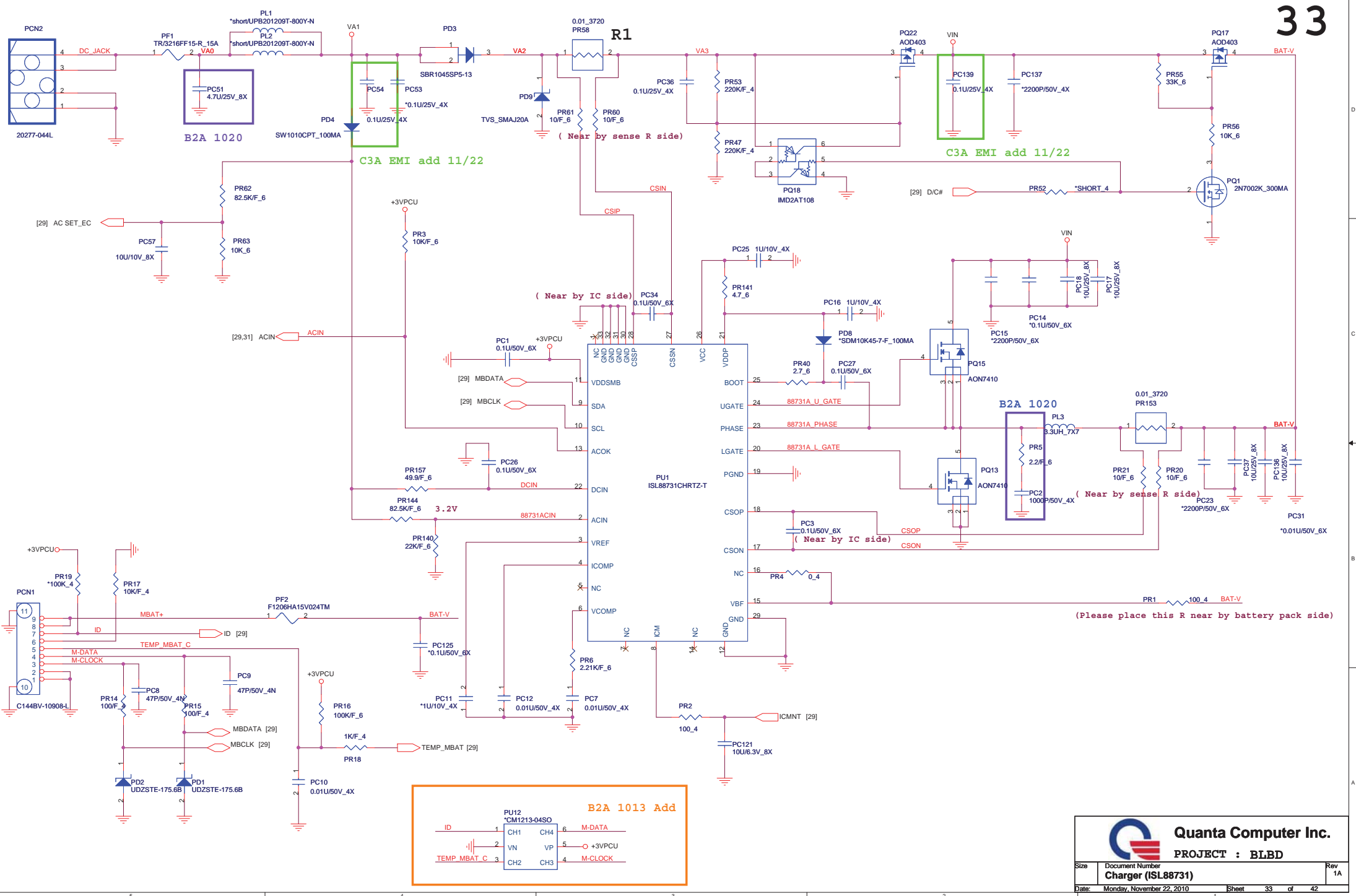


FOR CARDREADER LED



BLANK

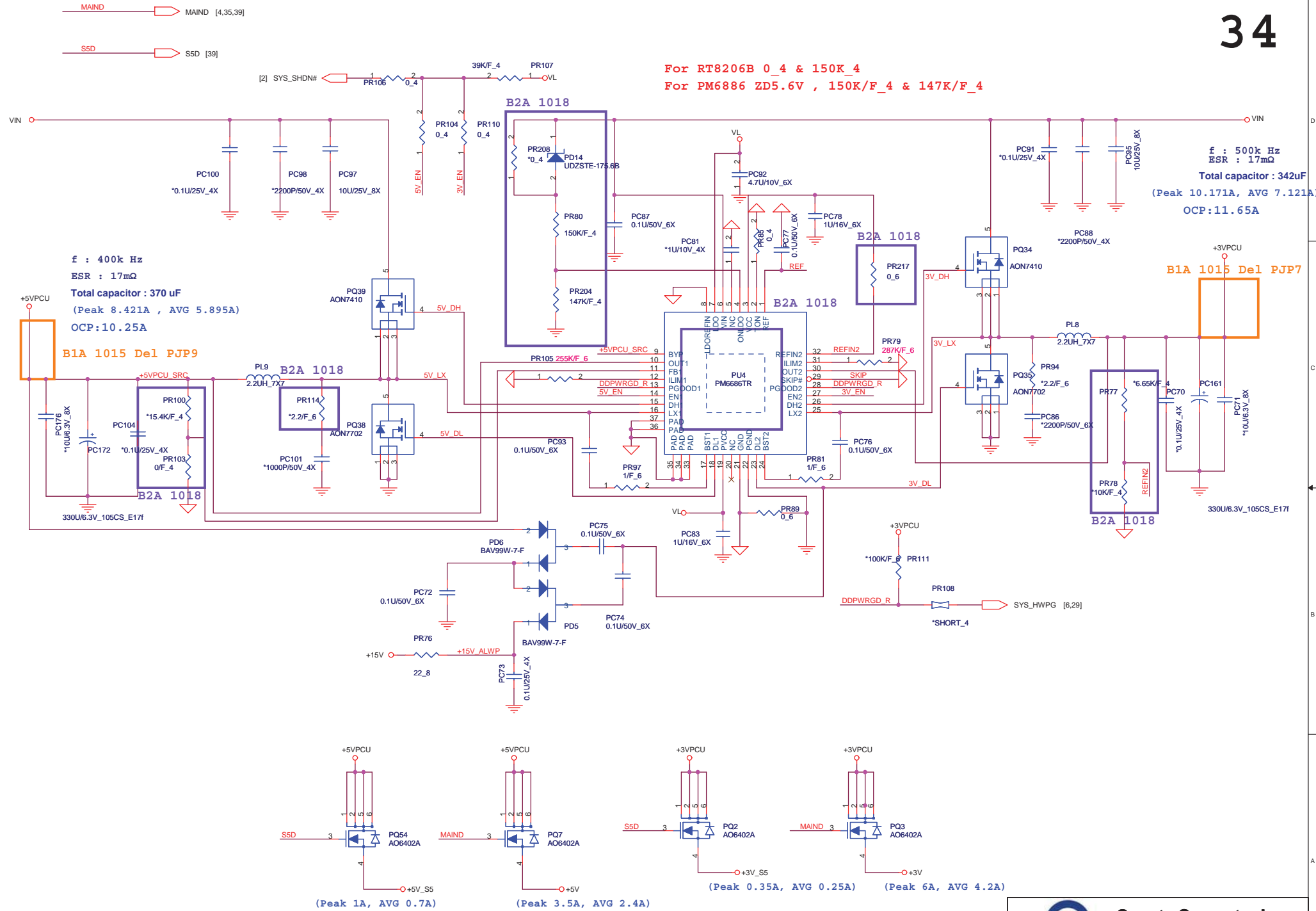
		Quanta Computer Inc.
		PROJECT : BLBD
Size	Document Number	Rev
	NVRAM Connector	1A
Date:	Monday, November 22, 2010	Sheet 32 of 42



Quanta Computer Inc.
PROJECT : BLBD

Size: Document Number
Charger (ISL88731) Rev 1A

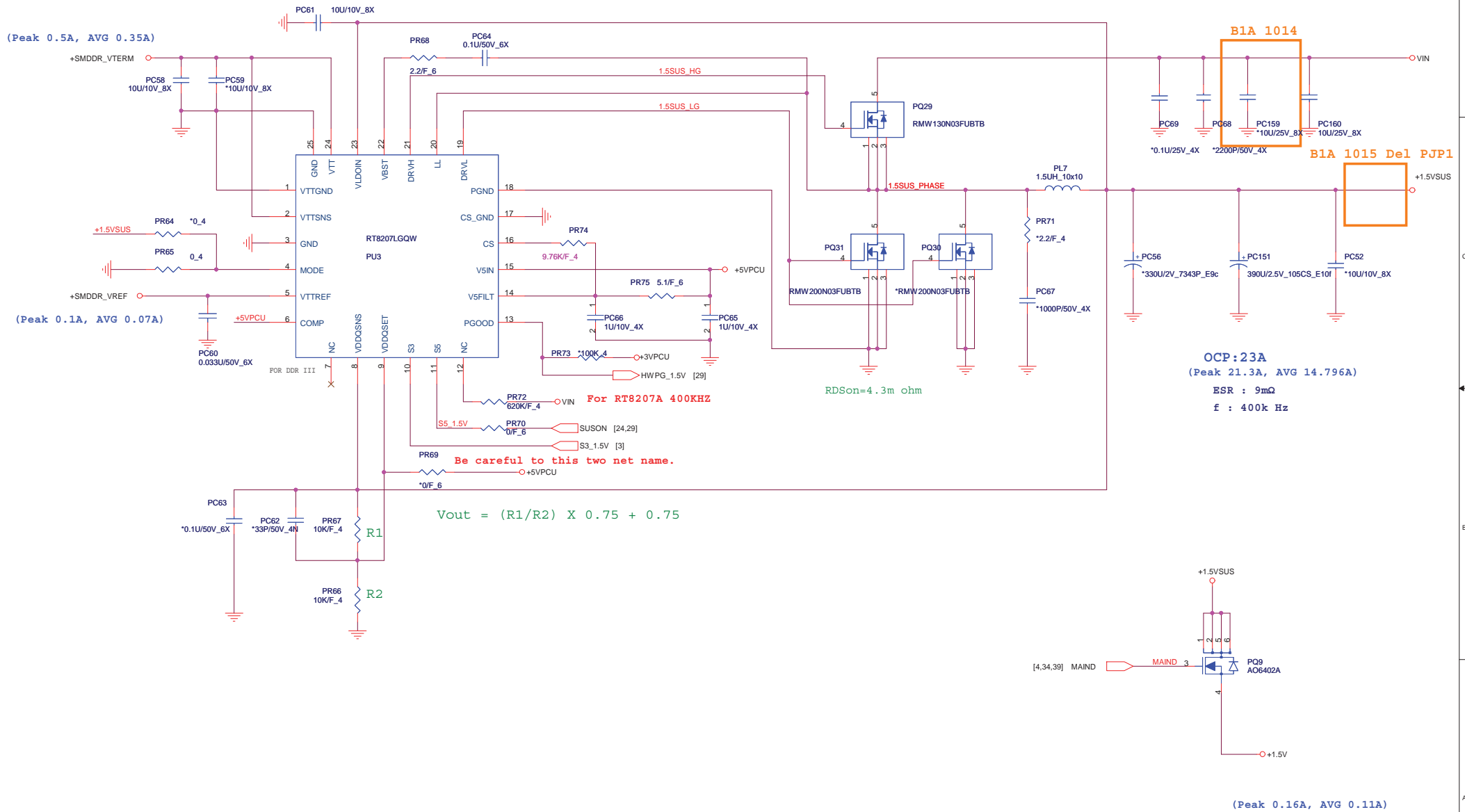
Date: Monday, November 22, 2010 Sheet 33 of 42

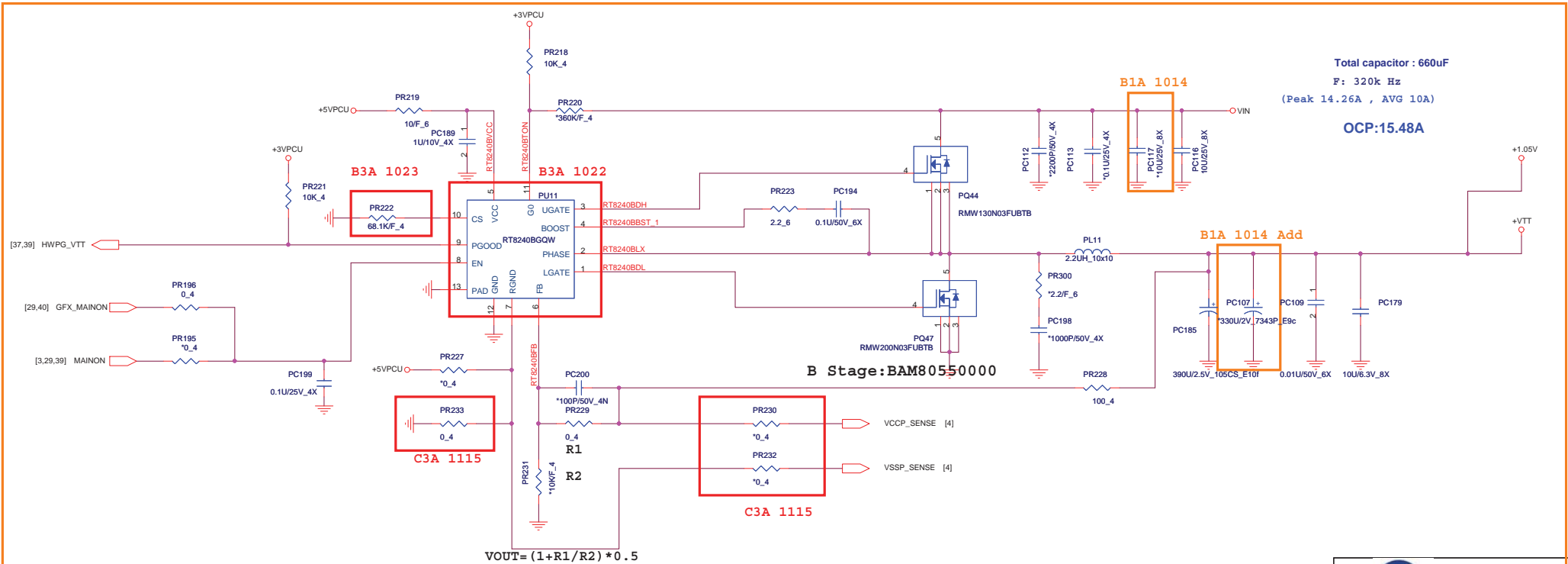


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Quanta Computer Inc.
PROJECT : BLBD


Size	Document Number	Rev
	System 5V/3V (RT8210BGQW)	1A
Date:	Monday, November 22, 2010	Sheet 34 of 42



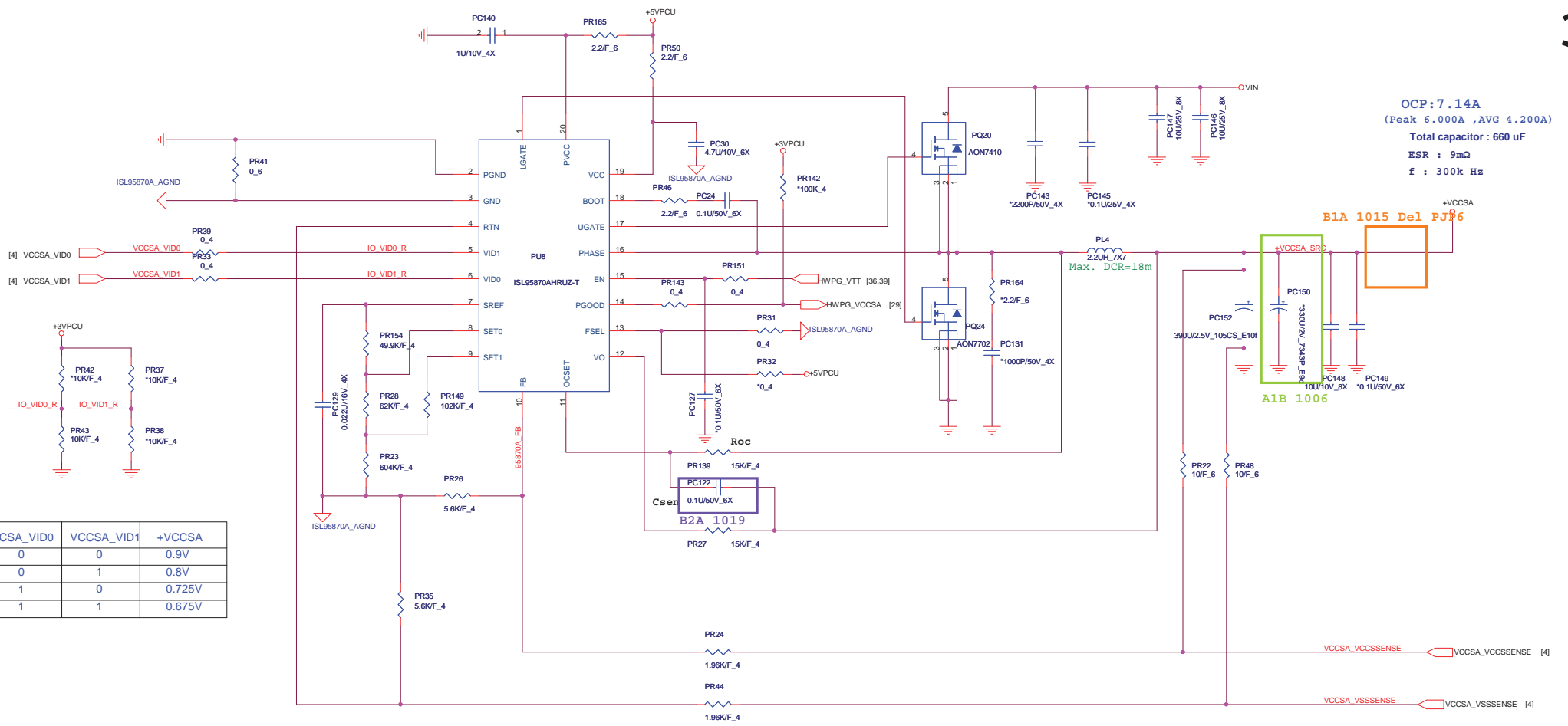


Total capacitor : 660uF
 F: 320k Hz
 (Peak 14.26A , AVG 10A)
 OCP:15.48A

B1A 1014



Quanta Computer Inc.
 PROJECT : BLBD

Size	Document Number	Rev
	+VTT /+1.05V(UP1522RQDD)	1A
Date:	Monday, November 22, 2010	Sheet 36 of 42

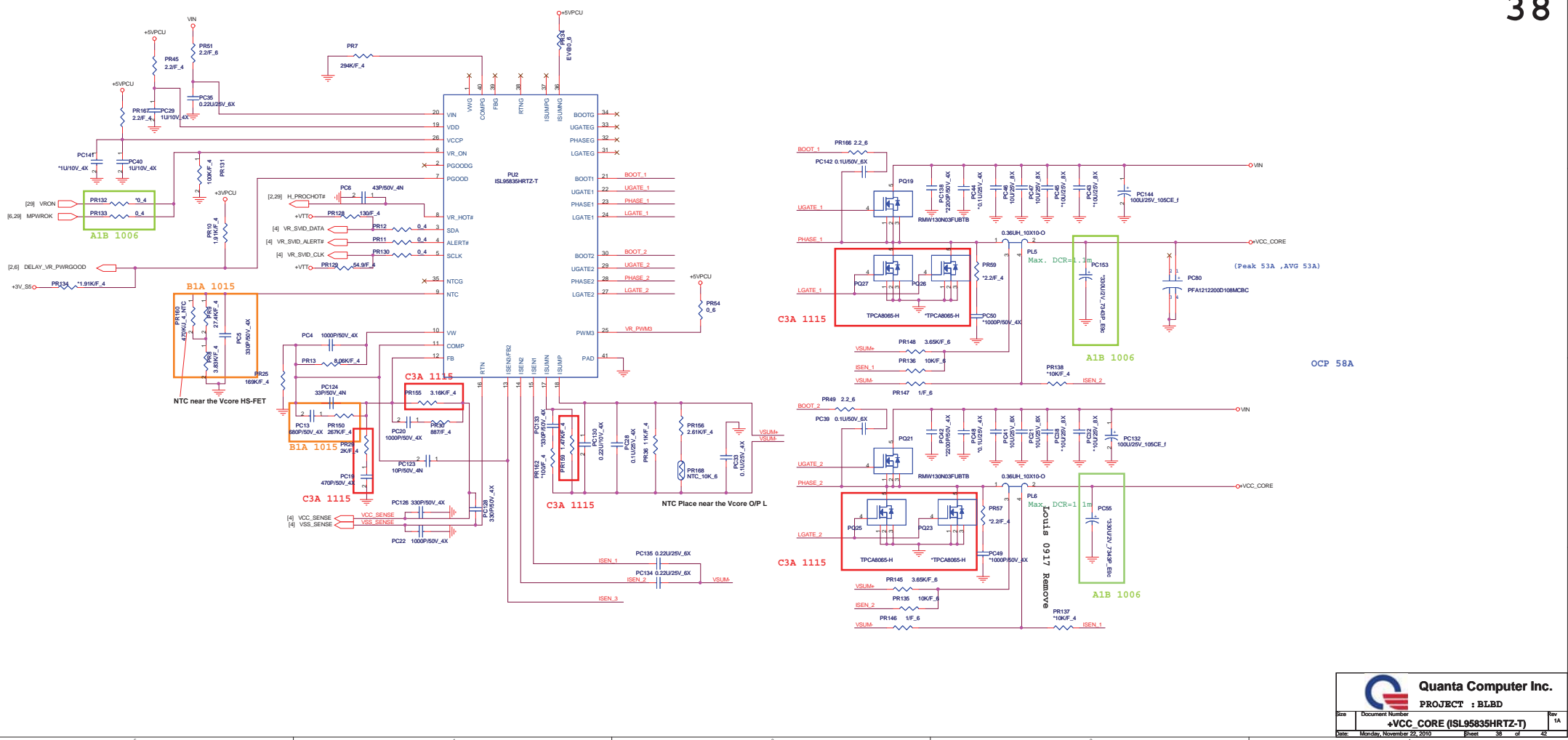



OCP: 7.14A
(Peak 6.000A, AVG 4.200A)
Total capacitor : 660 uF
ESR : 9mΩ
f : 300k Hz

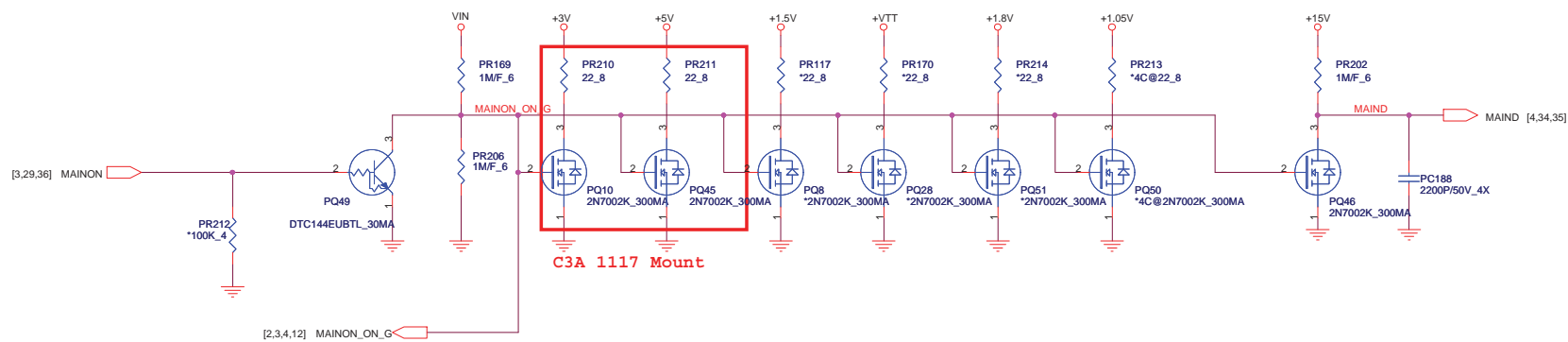
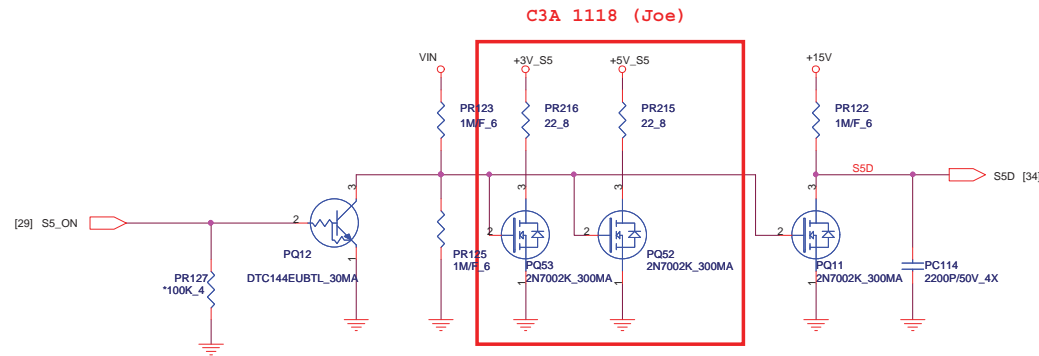
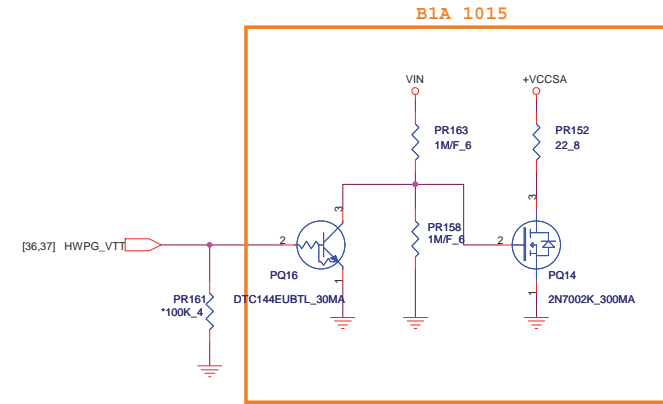
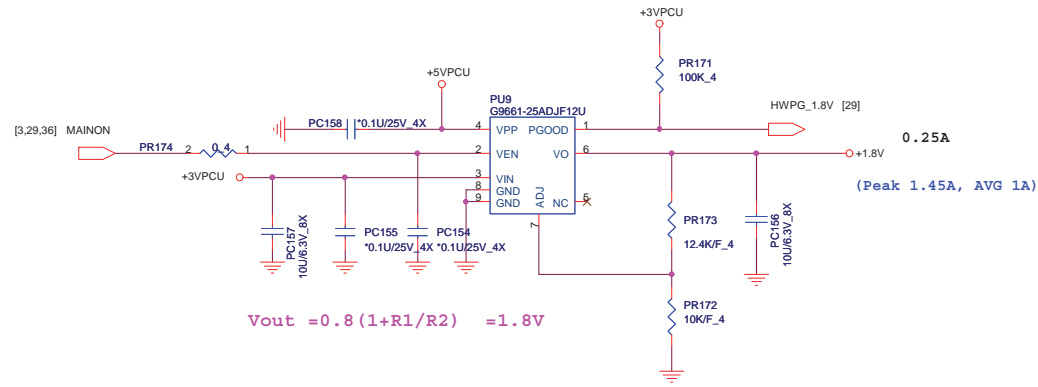
VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

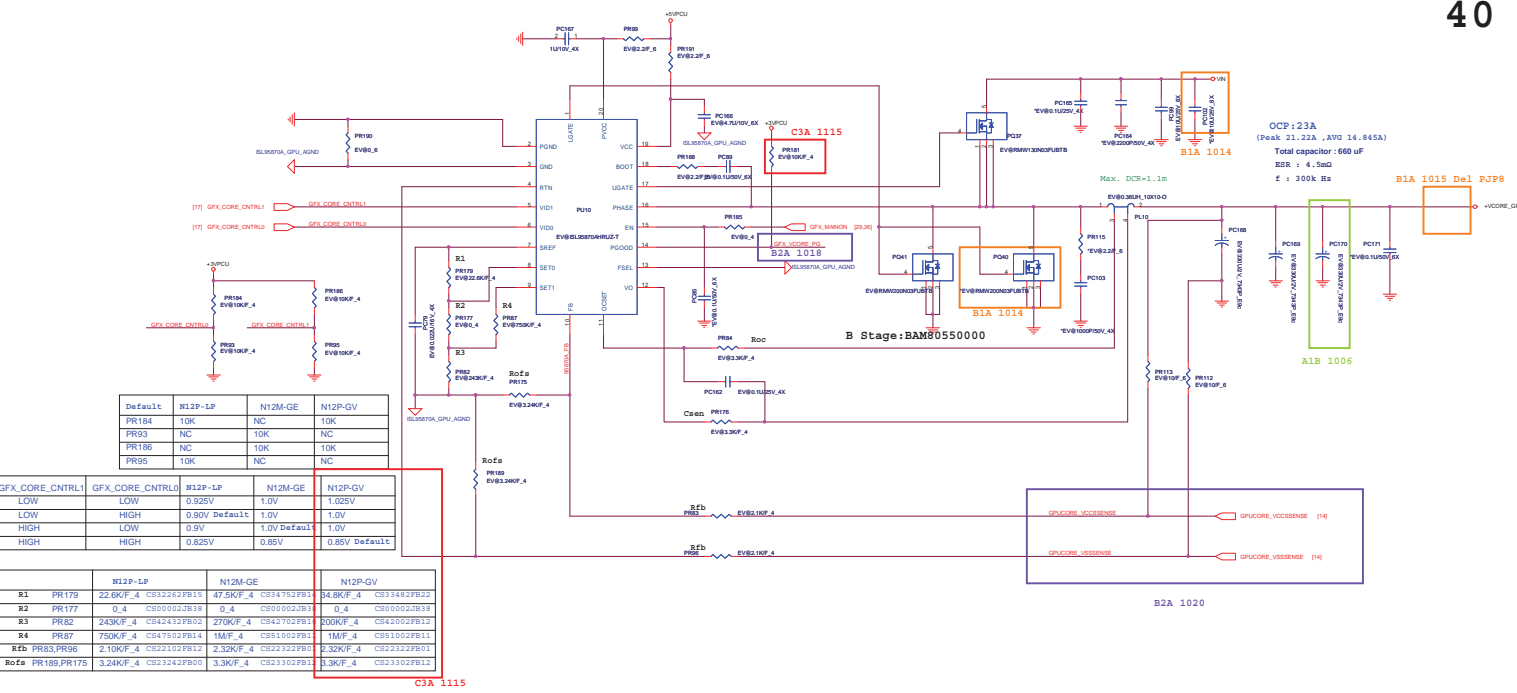
 **Quanta Computer Inc.**
PROJECT : BLBD

Size	Document Number	Rev
	+VCCSA ISL95870A)	1A
Date:	Monday, November 22, 2010	Sheet 37 of 42



 Quanta Computer Inc.		
PROJECT : BLBD		
Rev	Document Number	Rev
	+VCC_CORE (ISL95835HRTZ-T)	1A
Date	Monday, November 23, 2010	Sheet 38 of 42





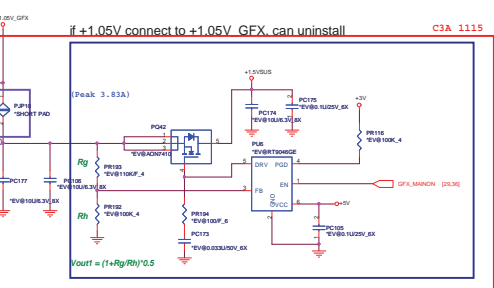
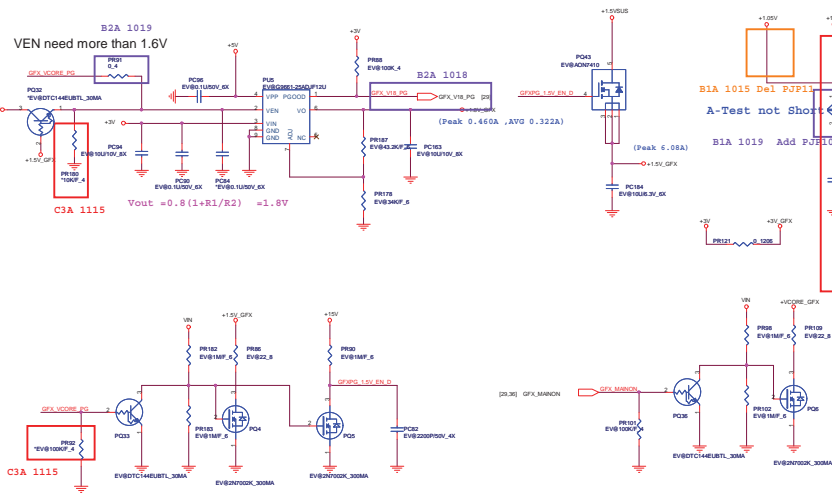
OCP: 23A
 (Peak 21.22A, ATO 14.845A)
 Total capacitor: 660 uF
 ESR: 4.5mΩ
 f: 300K Hz

Default	N12P-LP	N12M-GE	N12P-QV
PR184	10K	NC	10K
PR83	NC	10K	NC
PR186	NC	10K	10K
PR85	10K	NC	NC

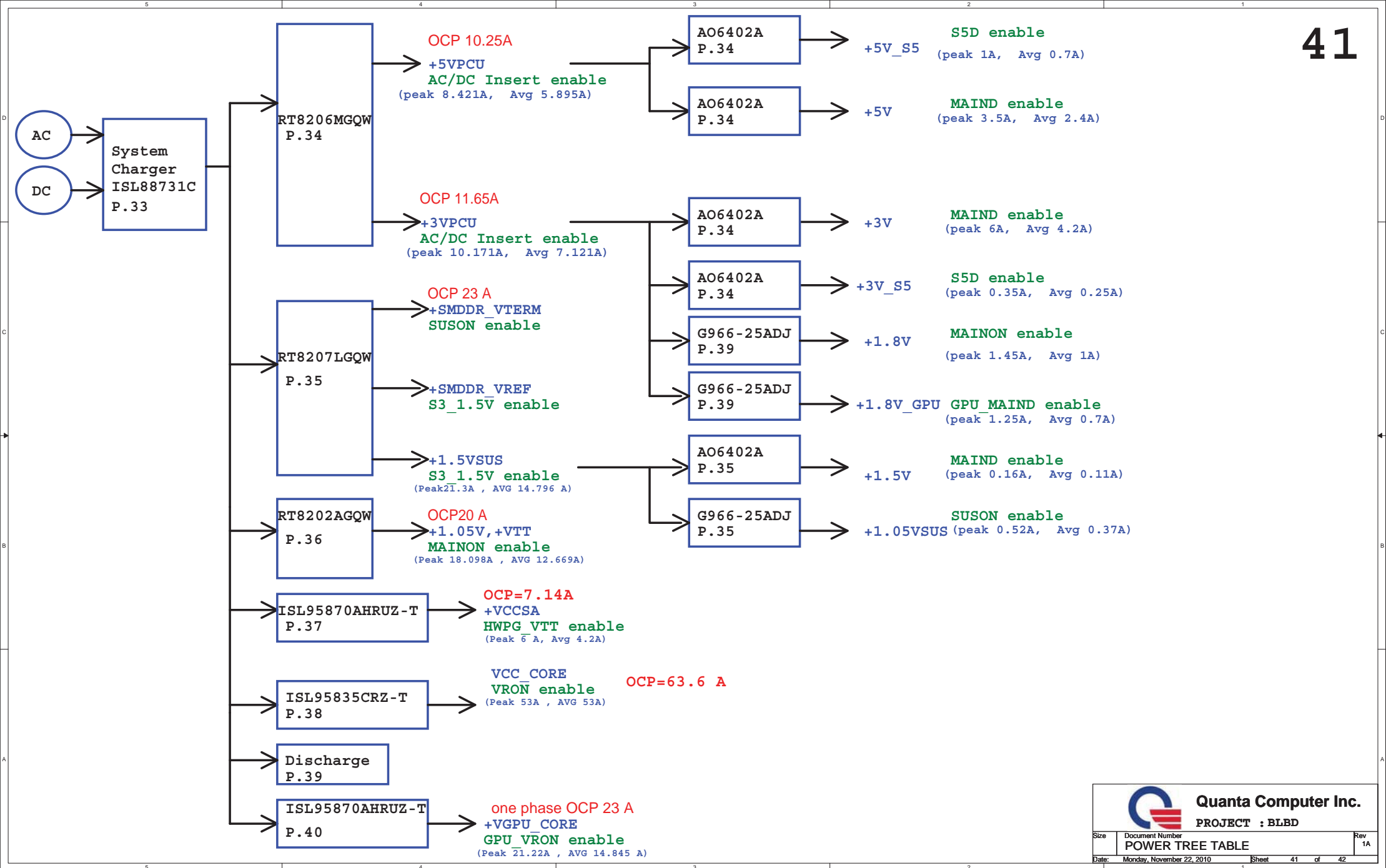
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	N12P-LP	N12M-GE	N12P-QV
LOW	LOW	0.925V	1.0V	1.025V
HIGH	HIGH	0.90V Default	1.0V	1.0V
HIGH	LOW	0.9V	1.0V Default	1.0V
HIGH	HIGH	0.825V	0.85V	0.85V Default


R1	PR179	N12P-LP	N12M-GE	N12P-QV
R1	PR179	22.6K_F_4	C832262PB15	47.5K_F_4
R2	PR177	0.4	C800002JB38	0.4
R3	PR82	243K_F_4	C842432PB02	270K_F_4
R4	PR87	750K_F_4	C847502PB14	1M_F_4
R1d	PR83, PR96	2.10K_F_4	C822102PB12	2.32K_F_4
R1e	PR189, PR175	3.24K_F_4	C823242PB00	3.3K_F_4

C3A 1115




- +3VPCU change to +3V
 - +5VPCU change to +5V
- Power On Sequence
- +3V_GFX connect +3V
 - +1.05V_GFX connect +1.05V
 - GFX_Mainon Enable +VCore_GFX
 - GFX_VCore_PG Enable(Delay) +1.5V_GFX
 - +1.5V_GFX Enable +1.8V_GFX
 - GFX_V18_PG connect GFX_PG
- Power Off Sequence
- compare +VCC3_GFX with +V1.8_GFX



 Quanta Computer Inc. PROJECT : BLBD		Rev
		1A
Size	Document Number	
POWER TREE TABLE		
Date:	Monday, November 22, 2010	Sheet 41 of 42

Model	REV	CHANGE LIST	MODEL			BLBD		
			PAGE	FROM	To			
BLBD MB	1A	PAGE 2: Del R19 0 ohm	1	1A				
		PAGE 2: ADD R599 0 ohm, TP81,TP82,TP83,TP84,TP85,TP86,TP87	2	1A				
		PAGE 2: STUFF R385,R394,Q28,C601,R387. NC R386	3	1A				
		PAGE 4: DEL C430, R37, R23, Add C477,C478,C479,C480,C740,C741,C742,C743,C744,C745,C746,R602,R603,R598, Stuff R21	4	1A				
		PAGE 5: ADD TP89, TP1	5	1A				
		PAGE 6: DEL R293, R503, NC R52, ADDR294	6	1A				
		PAGE 8: ADD C750, C751, R601, STUFF R501, NC Q14, Q15	7	1A				
		PAGE 9: DEL R253; R534 CHANGE TO PD	8	1A				
		PAGE 9: CHANGE Board ID9 strap Function name	9	1A				
		PAGE 10: ADD R604	10	1A				
		PAGE 17: CHANGE GPU MULTI level strap select	11	1A				
		PAGE 17: MODIFY GPU STRAP 1 SETTING	12	1A				
		PAGE 22: CHANGE LVDS CN1 FOOTPRINT	13	1A				
		PAGE 23: MINI CARD NC R99, DEL R184	14	1A				
		PAGE 23: ADD Q94,R920 BUT NC, ADD R921 AND MOUNT	15	1A				
		PAGE 25: DEL R68, R49	16	1A				
		PAGE 25: MOUNT C502, C1, C2	17	1A				
		PAGE 26: DEL R368, R369	18	1A				
		PAGE 26: ADD C953 BUT NC	19	1A				
		PAGE 26: ADD C759,C732,C733,C734	20	1A				
		PAGE 27: CHANGE ADOGND TO GND	21	1A				
		PAGE 27: ADD R342 BUT NC	22	1A				
		PAGE 27: NC C735	23	1A				
		PAGE 28: DEL R579, ADD C758	24	1A				
		PAGE 28: ADD R579, R600 PULL 3ND_MBCLK,3ND_MBDATA, NC R197	25	1A				
		PAGE 28: ADD SKU_STRAP1,SKU_STRAP2,SKU_STRAP3	26	1A				
		PAGE 28: CHANGE NET NAME FOR GFX_VCORE_PG TO GFX_V18_PG	27	1A				
		PAGE 31: LED1,LED4,LED5,LED6 change symbol and Foot-print	28	1A				
		PAGE 33: MOUNT PR5,PC2,PC51, ADD PU12 BUT NC	29	1A				
		PAGE 34: CHANGE PU4 TO PM6886	30	1A				
		PAGE 34: NC PR100,PR114,PR208,PR77,PR78, DEL PJP7	31	1A				
		PAGE 35: NC PR159, DEL PJP1,PJP2	32	1A				
		PAGE 36: CHANGE +VTT/+1.05V SCHEMATIC, CHANGE PU11 TO RT8240	33	1A				
		PAGE 37: DEL PJP6	34	1A				
		PAGE 40: DEL PJP8,PJP11, ADD PR91, NC PQ40	35	1A				
		PAGE 28: ADD Q3502	36	1A				
		PAGE 3: Add S3 Power reduction componet R489	37	2A				
		PAGE 31: Delete Card Reader LED componet Q16	38	2A				
		PAGE 31: Add Card Reader LED componet Q3052	39	2A				
		PAGE 8: Add USB_BUS_SW2/3 0 ohm R596,R597	40	2A				
		PAGE 10: Add +VCCAFDI_VRM PD Cap C381	41	2A				
		PAGE 17: Add 15K strap3/4 for GPU R3518,R3534	42	2A				
		PAGE 24: Add common choke for USB EMI solution L73	43	2A				
		PAGE 24: Reserve resistor for USB EMI solution RP24	44	2A				
		PAGE 25: Add ODD Zero power diischarge R614	45	2A				
		PAGE 25: Reserve ODD Zero power diischarge C577	46	2A				
		PAGE 26: Change Value for LAN 51@ to 52@, C95,C96,C100,C102,RN3,RN4	47	2A				
		PAGE 27: Change Card Reader controller U22 source	48	2A				
		PAGE 29: Change MS Strap Power name +3V_PCU to +3VPCU	49	2A				
		PAGE 36: 1.Add PR233 0 ohm PD form Pin7, NC PR230,PR232	50	2A				
PAGE 38: Change PR155 3.09K to 3.16K, PR159 1.37K to 1.47K, mount PR29,PC19								
PAGE 38: Change PQ26,PQ27,PQ23,PQ25 RMW200N03FUBTB to TPCA8065-H								
PAGE 40: Change PR181 to 10K								
PAGE 40: Change PR181 to 10K,Reserve PR92 100K ,Reserve +1.05 part all material, Reserve PR180 10K								
PAGE 40: Voltage Setting for N12P-GV								
PAGE 2: Add R118 R413, reserve R104,R105,Q5 for cost down Q5								

DOC NO. 204	PROJECT MODEL :	BLBD	APPROVED BY:	Angelo Su	DATE:	2010/10/01	 Quanta Computer Inc. PROJECT : BLBD
	PART NUMBER:		DRAWING BY:	Angelo Su	REVISION:	1A	

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