Application Note

Maximizing DAC Performance for Every Budget

Abstract

This application note discusses several factors that affect the audio performance of the Sabre digital audio converters. This article shows examples of possible tradeoffs for bill of materials cost vs. performance. The differences between topologies, PCB layouts, and components used are discussed with emphasis on BOM cost vs. performance.

Introduction

Design engineers face the challenge extracting the best possible performance from the least expensive circuit possible. The combination of digital logic with very low noise analog signals in a confined space presents a significant challenge to the PCB layout engineer. Designing a circuit that has a BOM under budget and meets performance requirements presents a compromise to the design engineer. This may be the ultimate performance, cost is no object, best in the world audiophile design, or a lowest cost, high performance solution, that out performs the competition.

Choosing the DAC

The ES9008 Reference DAC and the lower cost Premier ES9006 DAC are currently the available options when choosing an ESS Technology Inc. Sabre DAC. The Sabre Product Brief on ESS Technology Inc. website provides an overview of the features and performance expectations of both choices.

Choosing an output stage topology

ESS Technology has designed a few different output stages for use with the Sabre DAC's. If desired, the DAC output channels can be combined to increase the signal to noise performance of the DAC. The output impedance of the DAC is decreased by the number of paralleled outputs; therefore the output stage gain must also be decreased accordingly.

The typical performance numbers as measured on the Sabre evaluation boards are provided in Table 1.

	Differential Output		Single Ended Output	
Op Amp Part Number	**THD (dB)**	**DNR (dB)**	**THD (dB)**	**DNR (dB)**
ESS Reference Evaluation Board ES9008 2CH +/-12V Figure 1 and Figure 2, 4 DAC channels in parallel, R1 and R4 = 680 ohms				
AD797	-116	-132	-116	-128
LME49710	-114	-126	-114	-124
ESS Reference Evaluation Board ES9008 8CH +/-12V Figure 1 and Figure 2				
AD797	-114	-128	-114	-126
LME49710	-114	-126	-114	-124
NE5534	-112	-125	-110	-124
NE5534 for audio and AD797 for AVCC Regulator	-111	-126	-110	-124
OPA2134 for audio and AD797 for AVCC Regulator	-112	-120	-111	-120
ESS Evaluation Board ES9008 8CH LC SS +12V Figure 3				
LME49720	N/A	N/A	-112	-118
ESS Evaluation Board ES9006 8CH +/-12V Figure 1 and Figure 2				
AD797	-104	-124	-104	-123
NE5534	-104	-118	-104	-117
ESS Evaluation Board ES9006 8CH LC SS +12V Figure 3				
LME49720	N/A	N/A	-106	-118
ROHM 4560	N/A	N/A	-105	-114

Table 1 EVB Performance

The highest performance circuit is provided on the Sabre Reference Evaluation Board. This circuit is shown in Figure 1.

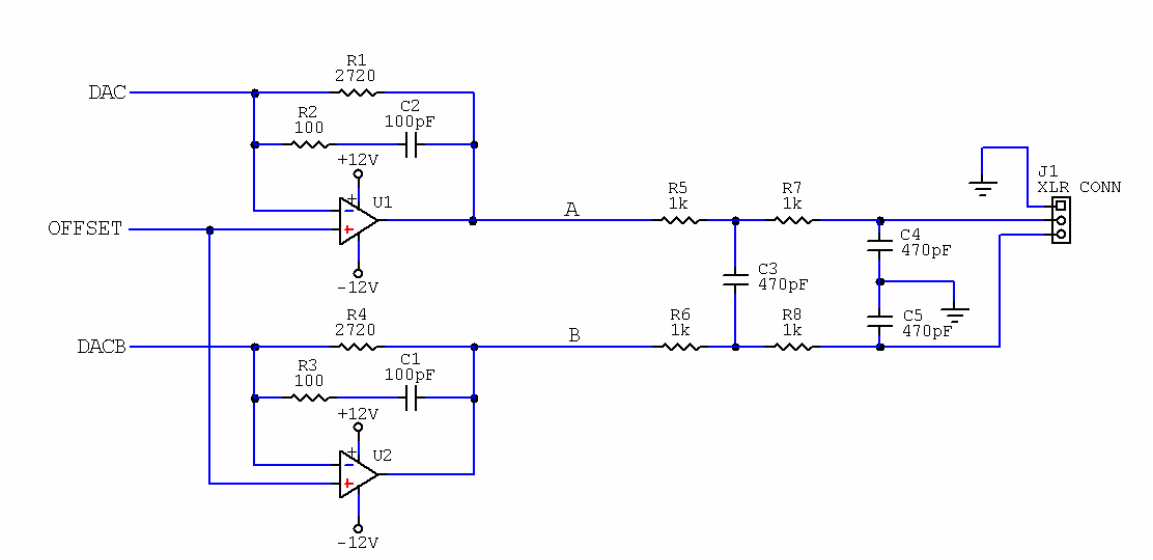

Figure 1: Sabre Reference Evaluation Board Differential Output

The Sabre Reference Evaluation Board also provides single ended outputs, this circuit is shown in Figure 2.

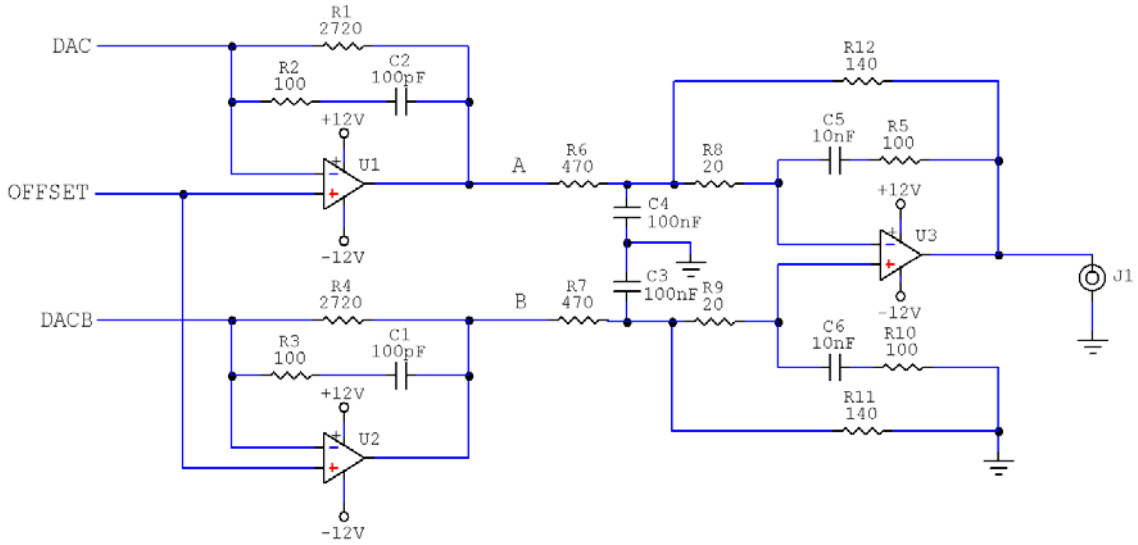

Figure 2: Sabre Reference Evaluation Board Single Ended Output

Note: The first half of the circuits in Figures 1 and 2 are identical, Point A and Point B are the same points in both the circuits.

For the lowest cost solution the circuit in Figure 3 provides excellent performance in both THD and SNR with the fewest possible components.

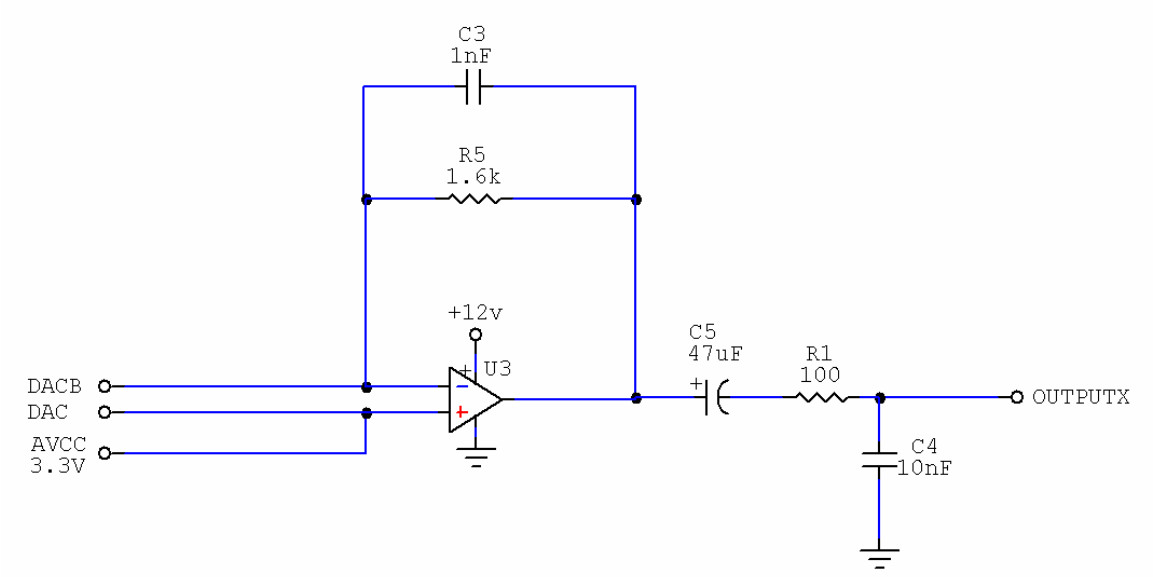

Figure 3: Sabre Premier Evaluation Board Single Ended Output

Component Selection

In order to extract the highest performance from the DAC, the following components in all the above topologies are critical:

Capacitors

All surface mount chip capacitors that are in the audio path must be COG dielectric. Dielectrics such as X7R and X5R cause nonlinearities this causes the total harmonic distortion to drastically degrade.

Resistors

For optimum THD and SNR the surface mount resistors within the audio path must be thin film resistors. Thick film surface mount resistors should be avoided as they have a Voltage Coefficient of Resistance approximately 100 times higher than thin film resistors. Metal film resistors also have a very low VCR but are typically higher cost.

Operation Amplifiers

Operational amplifiers typically are the most expensive component in the circuit. The choice of opamp varies for each design and budget. The power supply circuit shown in Figure 4 is necessary to provide a clean 3.3V to the analog section of the Sabre DAC. The opamp used for this circuit is the most critical for optimizing the THD and SNR performance. Use of a poorly designed opamp will degrade both the THD and SNR. This opamp may oscillate at a high frequency when driving the highly capacitive load of the AVCC decoupling capacitors. C2 can be reduced from 47uF to 10uF if a high performance opamp is used. The Rohm 4560 tends to oscillate at high frequency when driving a moderately capacitive load, but stop oscillating when that capacitive load is larger than ~30uF. C1 may be reduced to 1uF without observable consequences when using either the AD797 or LME opamps listed below.

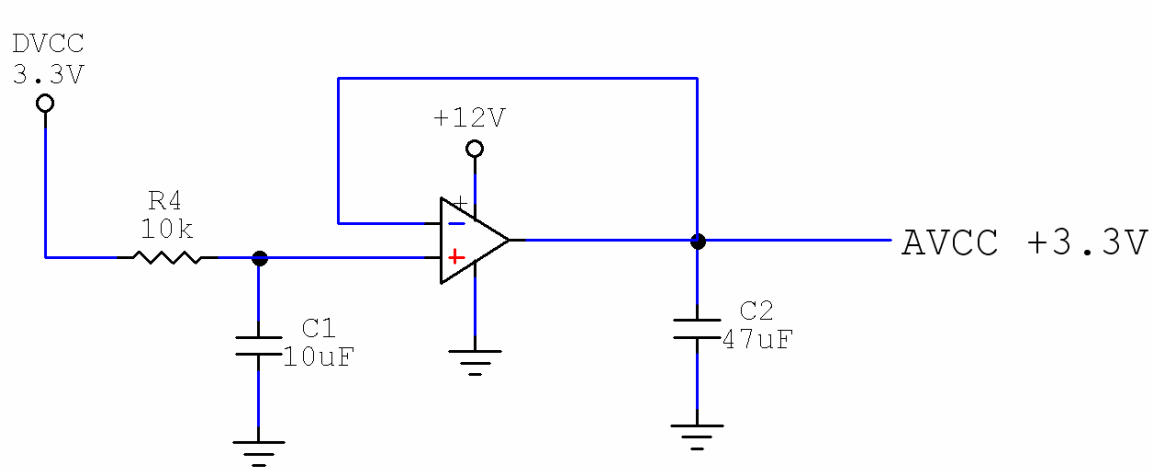

Figure 4: AVCC +3.3V Filter and Regulator

ESS recommends the opamps listed below. They are sorted from highest to lowest performance.

Manufacturer	**Part Number**
Analog Devices	AD797
National Semiconductor	LME49710, LME49720, LME49740, LM4562
Texas Instruments	NE5534, NE5532
Rohm	4560

Master Clock

As detailed in the datasheet, the MCLK must be at least 386*Fs for SPDIF inputs and 192*Fs for Serial/DSD inputs. For optimum jitter tolerance the MCLK should be at least 10% higher than this theoretical MCLK minimum, this ensures audio clarity free from input clock jitter.

If operating with a synchronous MCLK, it is recommended to use an inverted MCLK. The inverted synchronous MCLK ensures that the Sabre noise is as low as possible.

Printed Circuit Board Design

Proper PCB layout for the Sabre DAC is vital to the circuit's performance. Time spent achieving optimum component placement provides a good foundation to make the routing task provide the best performing circuit within the real estate provided. Every design will have different requirements, PCB stackup, via size, PCB size, component sizes, etc. ESS has experimented with DAC evaluation PCBs ground planes to determine any benefit of split plane grounds for analog and digital ground. It is our finding and recommendation to use only one ground plane for both digital and analog grounds as it simplifies layout and provides no performance degradation. The most important for DAC performance is the ground plane, it should be as solid as possible with as few traces routed through the ground plane as possible. Any traces that are routed through the ground plane and block the "line of sight" from the DAC output to the opamp output stage significantly degrades the output THD. ESS recommends using the evaluation board designs as a guide for your own PCB layout. Critical PCB layout items:

1.) Make the ground plane as solid as possible. Try to keep all ground connections as short as possible. Every ground connection should have its own via, do not share vias if possible.
2.) Keep opamp feedback paths as close as possible to the opamp.
3.) Ensure every opamp and DAC has decoupling capacitance on its power supply right next to the power supply pins.
4.) The audio path between the DAC and the opamp stage should be kept as short and clean as possible.
5.) The audio path after the opamps is not as critical.
6.) Try to keep the digital circuitry away from the analog circuitry.

Figure 5 shows the Sabre DAC Reference 64LQFP Evaluation Board. Each section of the circuit board is described in detail below.

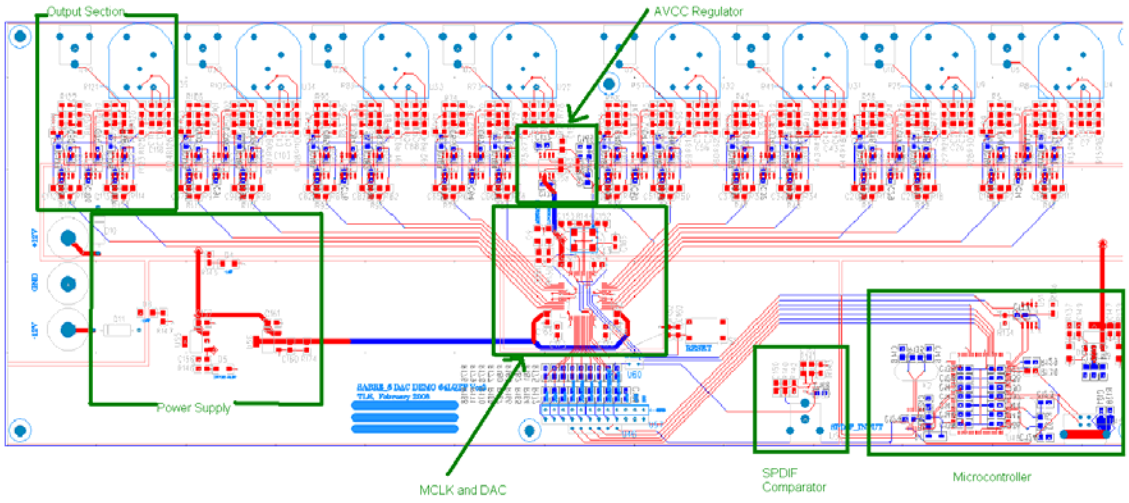

Figure 5: Sabre DAC Reference 64LQFP Evaluation Board

Output Section

The output section expanded in Figure 6 shows the opamps, filters, and XLR and RCA connectors. Figure 6 shows one of the eight identical output stages on the evaluation board. The top copper layer of the PCB is shown in red, the bottom is shown in dark blue and notes for the purpose of this document are in green. The +12V and -12V split planes are shown separated by the coral colored lines. The +12V and -12V split planes provides solid connections (circled in green) to the power supply for the outputs. Ensure that the connection to the rest of the plane is solid and not cut off on an island due to other traces being routed on the top layer.

The feedback resistors and capacitors are placed close to there respective amplifier. Decoupling capacitors for the +12V and -12V power supplies are placed close to the power supply pins of the opamps.

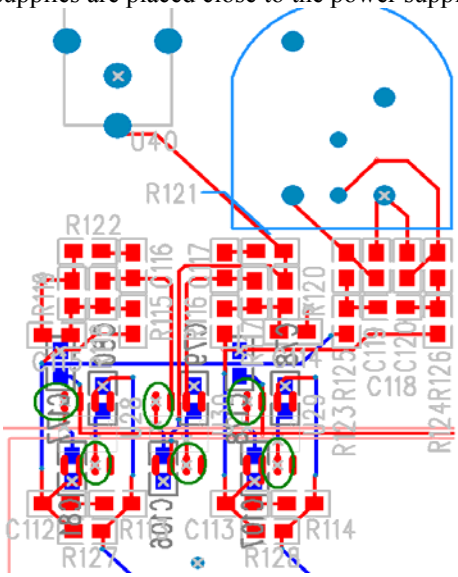

Figure 6: Output amplifier stage

Power Supply

Figure 7 shows the 3.3V DVCC and 1.2V VDD power linear power supplies. Linear power supplies are used to ensure a low noise design. U55 provides regulation from +12V to +3.3V for DVCC and also supplies U56. U56 regulates the +3.3V to +1.2V for VDD. All traces are kept large to ensure minimal trace resistance. Decoupling capacitance is kept close to the linear regulator. Ground connections are kept short with a via placed close to the pin. Try not to share vias, each ground connection should have its own via. D10 and D11 are provided on the evaluation board to prevent damage in the case of the user reversing the power supplies.

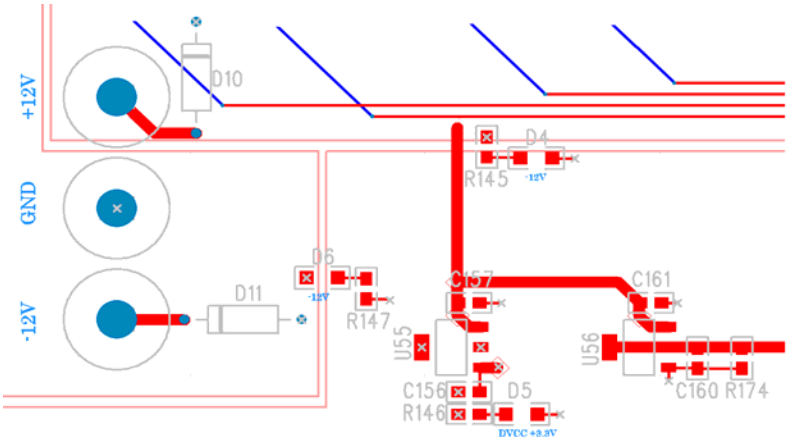

Figure 7: Power Supply

AVCC Regulator

The +3.3V required for the analog section of the DAC needs to be as quiet and well regulated as possible. The design uses the +3.3V DVCC as a reference and filters this signal with a RC filter. The opamp is configured in a buffer stage to supply the +3.3V for AVCC. As shown in Figure 8, the decoupling capacitors should be kept close to the supply pins and the filter should be close to the opamp input. The output trace with should be large and provide a very low impedance path to the DAC AVCC pins.

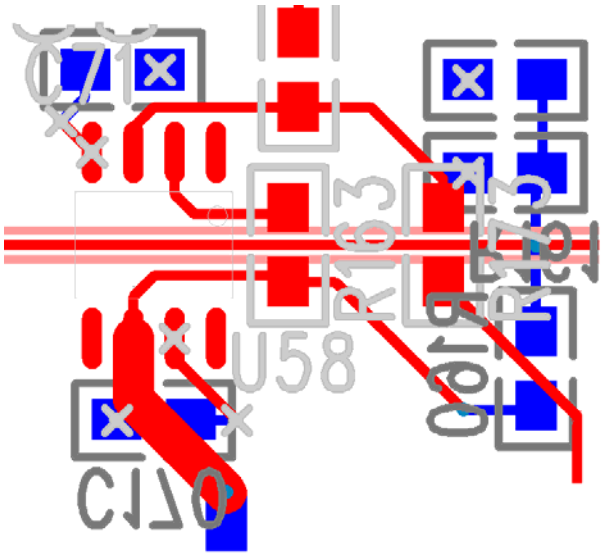

Figure 8: AVCC Regulator

DAC and MCLK

Figure 9 shows the DAC and MCLK section of the evaluation board. The ground plane should be unobstructed from the DAC outputs to the output amplifier stage. The crystal oscillator should be kept close to the DAC. Digital lines are routed away from the audio lines at the bottom of the figure. All power supply connections have decoupling capacitors place close to DAC pins.

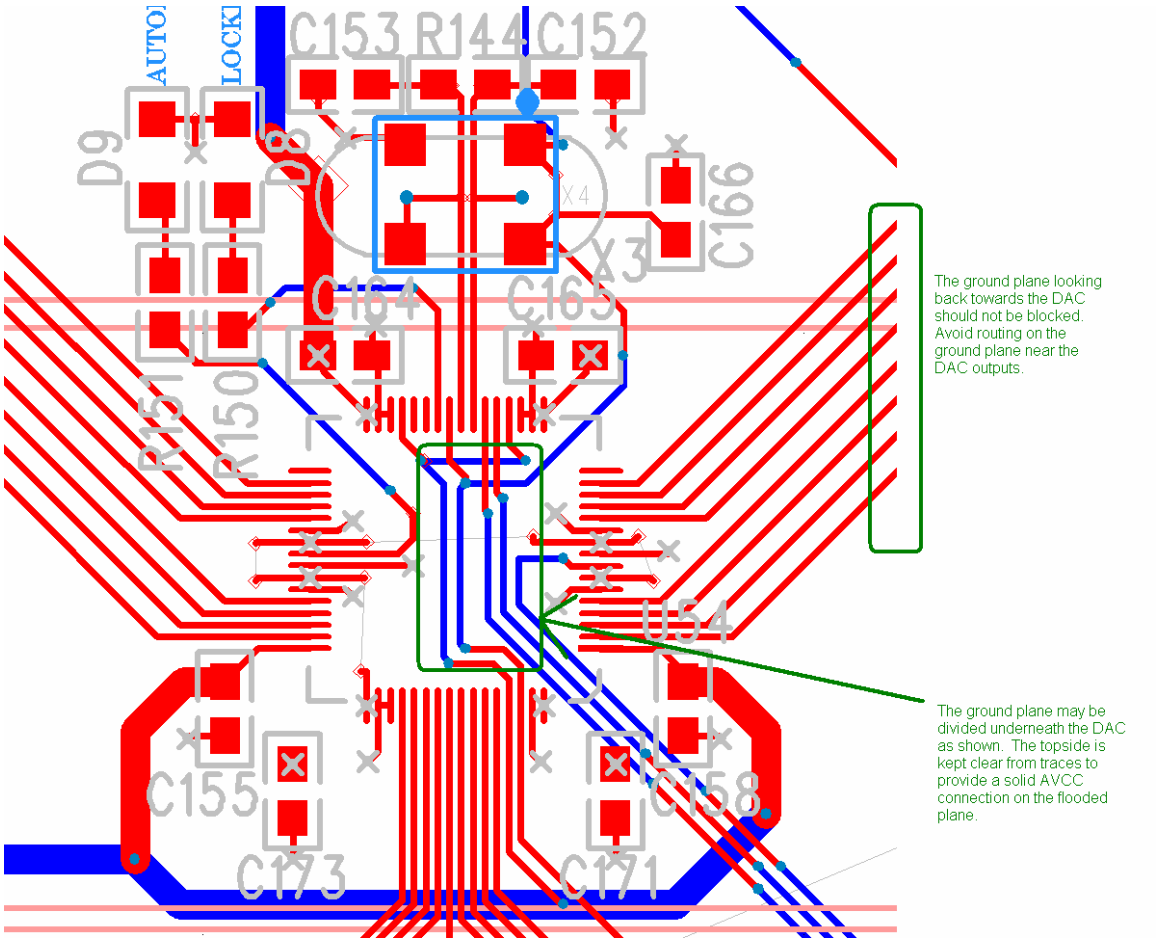

Figure 9: DAC and Oscillator

SPDIF

The SPDIF interface uses a comparator to clean up the input signal. The SPDIF input signal sees a 75 ohm impedance to ground.

Note: Some early evaluation board designs had the 75 ohm resistor in series with the input and thus did not provide a proper 75 ohm termination impedance.

Microcontroller

To minimize the risk of digital noise affecting the performance of the DAC, a separate +3.3V supply powers the microcontroller. Decoupling capacitors are kept close to the power pins. The USB ground is isolated from the common ground plane.