3-2 Interface Connections

- LCD connector (CN3): JAE FI-E30S or equivalent
- LVDS Transmitter: SN75LVDS83(Texas Instruments) or equivalent

Pin No	Symbol	Description	note
1	Reserved	Open or High	Auo internal test pin
2	Reserved	Open or High	Auo internal test pin
3	Reserved	Open or High	Auo internal test pin
4	GND	Ground and Signal Return	
5	RXIN0-	LVDS Channel 0 negative	
6	RXIN0+	LVDS Channel 0 positive	
7	GND	Ground and Signal Return for LVDS	
8	RXIN1-	LVDS Channel 1 negative	
9	RXIN1+	LVDS Channel 1 positive	
10	GND	Ground and Signal Return for LVDS	
11	RXIN2-	LVDS Channel 2 negative	
12	RXIN2+	LVDS Channel 2 positive	
13	GND	Ground and Signal Return for LVDS	
14	RXCLKIN-	LVDS Clock negative	
15	RXCLKIN+	LVDS Clock positive	
16	GND	Ground and Signal Return for LVDS	
17	RXIN3-	LVDS Channel 3 negative	
18	RXIN3+	LVDS Channel 3 positive	
19	GND	Ground and Signal Return	
20	Reserved	Open or High	Auo internal test pin
21	LVDS Option	Low for JEIDA, High/Open for NS	
22	Reserved	Open or Low	Auo internal test pin
23	GND	Ground and Signal Return	
24	GND	Ground and Signal Return	
25	GND	Ground and Signal Return	
26	Vcc	5V, DC, Regulated	
27	Vcc	5V, DC, Regulated	
28	Vcc	5V, DC, Regulated	
29	Vcc	5V, DC, Regulated	
30	Vcc	5V, DC, Regulated	

Note:

1. All GND (ground) pins should be connected together and should also be connected to the LCD's metal frame. All Vcc (power input) pins should be connected together.