OVERVIEW

SiRFatlasIII™ AT640 series navigation processor is another addition to the SiRFatlasIII family of GPS applications processors. In addition to being compatible with the SiRFatlasII™ platform, SiRFatlasIII enhances the navigation experience along dimensions of system speed, GPS performance, and platform flexibility. System performance enhancements are achieved through a 396MHz ARM 926EJ-S coupled with a 264MHz DSP. This allows over 600MIPS for computing intensive applications like high resolution multimedia. Like all the previous Atlas processors, GPS baseband is integrated in the processor.

SiRFatlasIII's added hardware acceleration and software enhancements provide up to 30 channels for GPS with increased accuracy and faster time to fix. Platform flexibility of SiRFatlasIII comes from two main areas. The SiRFatlasIII processor is pin compatible with the SiRFatlasII processor, enabling a significant decrease in development time for existing SiRFatlasII platforms. SiRFatlasIII also comes with DDR200 support for those applications that demand additional memory throughput.

CORE EXECUTION FEATURES

- Up to 396MHz 32-bit RISC (ARM926EJ)
  - 16KB I-Cache
  - 16KB D-Cache
  - Jazelle™ Java Acceleration
  - ETM9 Embedded Trace Module
- 264MHz 16-bit DSP enhanced with hardware acceleration
  - 5Kx24bit Program Memory
  - 10Kx16bit Data Memory
- SDRAM Interface
  - Up to 162MHz 3.3V SDRAM/mobile SDRAM
  - Up to 132MHz 2.5V mobile SDRAM
  - Up to 99MHz 2.5V DDR1 SDRAM
- Enhanced 30 Channel GPS Baseband
- Hardware GPS Accelerators
- I^2C interface
- RGB to YUV Hardware Conversion
- 189 Programmable GPIO
- ROM Interface with DMA
- 2 CANBus Ports
- 2D Acceleration Hardware
- PWM interface
- 6 OS Timers
- 3 Display Layers
- Advanced Power Management
  - Normal Mode
  - Idle Mode
  - Sleep Mode
- 130nm Process Technology
- 332-ball 14x14mm TFBGA package
- AC97/SPI/I2S
- 8/16-bit NAND Flash Interface
- CMOS/CCD sensor Interface
- USB OTG 2.0 Full-speed Interface
- ATA-4 Interface
- SD/MMC/SDIO Interface
- PCMCIA/CF Card Interface
- 5 Universal Serial Ports and 3 UARTs
- Color-TFT and CSTN Panel Interface

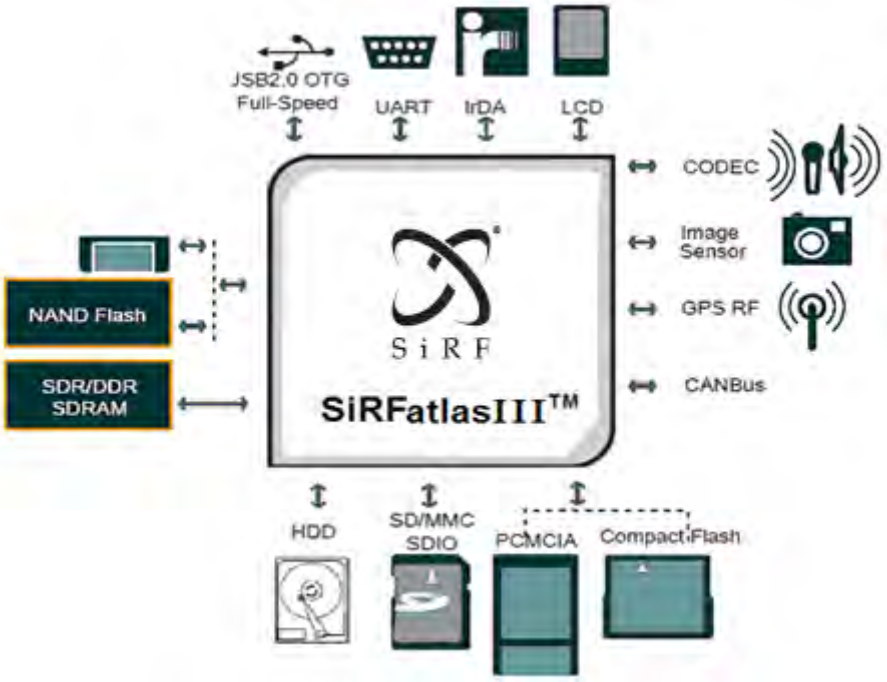


Figure 1: Application of SiRFatlasIII in Infotainment and Navigation System

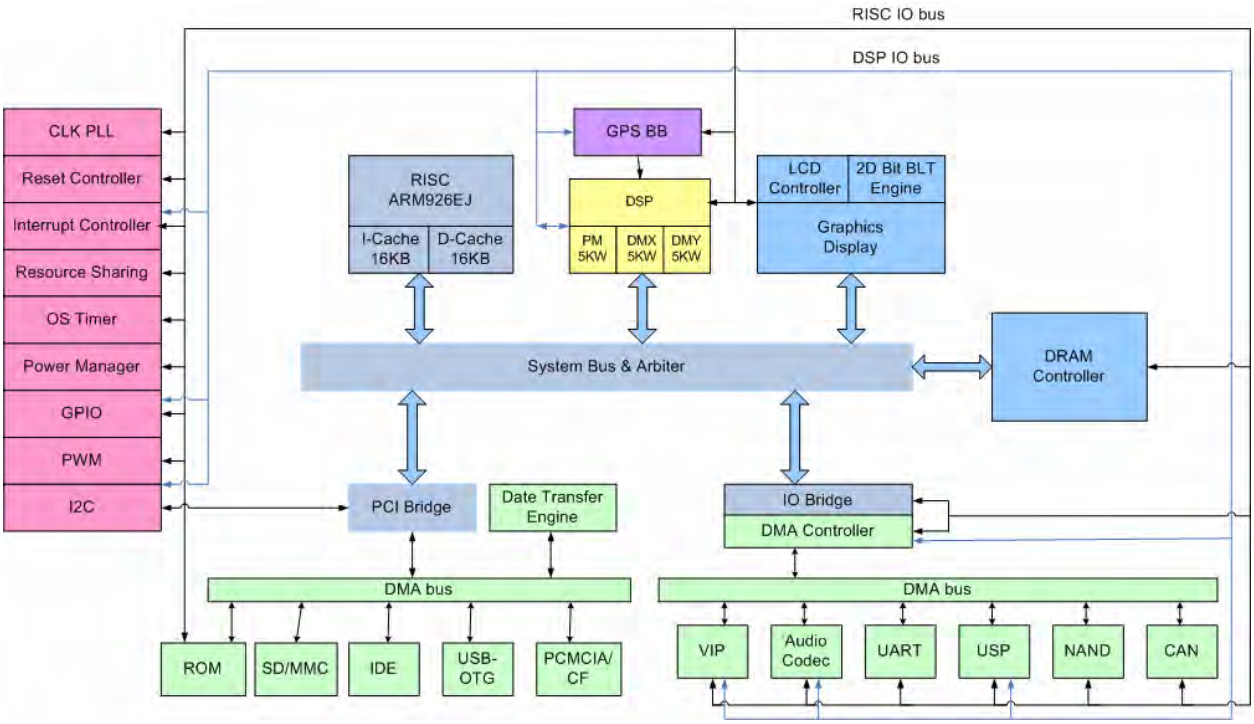


Figure 2: SiRFatlasIII Block Diagram

ELECTRICAL AND TIMING CHARACTERISTICS

Absolute Maximum Ratings

Characteristic	Symbol	Min.	Max.	Unit
Supply voltage-I/O buffers	VDDIO	-0.3	4	V
Supply voltage-I/O buffers	XVDDIO	-0.3	4	V
Supply voltage-mem bus (DDR SDRAM)	VDD_MEM (VSSTL)	-0.3	3	V
Supply voltage-mem bus (SDR SDRAM)	VDD_MEM (SDR SDRAM)	-0.3	4	V
Supply voltage-PLL	VDD_PHA	-0.3	4	V
Supply voltage-PLL	VDD_PLA	-0.3	1.44	V
Supply voltage-PLL	VDD_PLD	-0.3	1.44	V
Supply voltage-core	VREF	-0.3	1.44	V
Supply voltage-core	VDDPRE	-0.3	1.44	V
Supply voltage-inter model	VDDPDN	-0.3	1.44	V
Input voltage overshoot	Vinos	—	0.5	V
Input voltage undershoot	Vinus	—	0.5	V

Table 1: Absolute Maximum Ratings

NOTE: Absolute maximum ratings are stress ratings only, functional operations tested to the maximum stress capacity are not guaranteed. Stresses beyond those listed in the table above may affect device reliability or cause permanent damages.

Recommended Operating Conditions

Characteristic	Symbol	Min.	Type	Max.	Unit
Supply voltage - I/O buffers	VDDIO	3.13	3.3	3.5	V
Supply voltage - I/O buffers	XVDDIO	3.13	3.3	3.5	V
Supply voltage - mem bus (DDR DRAM)	VDD_MEM (VSSTL)	2.37	2.5	2.63	V
Supply voltage - mem bus (SDR DRAM)	VDD_MEM (SDR SDRAM)	3.13	3.3	3.5	V
Supply voltage - mem bus (2.5v SDR SDRAM)	VDD_MEM (2.5v SDR SDRAM)	2.37	2.5	2.63	V
Supply voltage - PLL	VDD_PHA	3.13	3.3	3.5	V
Supply voltage - PLL	VDD_PLA	1.14	1.2	1.26	V
Supply voltage - PLL	VDD_PLD	1.14	1.2	1.26	V
Supply voltage - core	VREF	1.225	1.25	1.275	V
Supply voltage - core	VDDPRE	1.22	1.3	1.38	V
Supply voltage - inter model	VDDPDN	1.22	1.3	1.38	V
Input voltage - standard I/O	Vin	0	VDDIO	VDDIO	V
Input voltage - memory I/O buffers (SDRAM)	V_{in_sdr}	0	—	VDD_MEM (SDRAM)	V

Table 2: Recommended Operating Conditions

NOTE: The conditions in the table above are tested and recommended. Any device operation not listed in this table is not guaranteed.

DC Electrical Specifications

Characteristic	Condition	Symbol	Min.	Max.	Unit
Input high voltage	Input type = CMOS	VIH	1.8	—	V
Input high voltage	Input type = TTL VDD_IO/VDD_MEM_IOSDR	VIH	2.0	—	V
Input high voltage	Input type = SSTL VDD_MEM_IODDR	VIH	1.5	—	V
Input high voltage	Input type = SCHMITT VDD_IO	VIH	2.0	—	V
Input high voltage	X_XIN, X_XINW	VIH	2.0	—	V
Input low voltage	Input type = CMOS	VIL	—	1.1	V
Input low voltage	Input type = TTL VDD_IO/VDD_MEM_IOSDR	VIL	—	0.8	V
Input low voltage	Input type = TTL VDD_MEM_IODDR	VIL	—	0.8	V
Input low voltage	Input type = SCHMITT VDD_IO	VIL	—	0.8	V
Input low voltage	X_XIN, X_XINW	VIL	—	0.8	V
Input leakage current	Vin = 0 or VDD_IO	I_{IN}	—	±10	uA
Input current, pull-up resistor	Vin = 0	I_{INpu}	40	110	uA
Input current, pull-down resistor	Vin = VDD_IO	I_{INpd}	40	110	uA
Output high voltage	IOH is driver dependent VDD_IO=3.0, DRV4	VOH	2.4	—	V
Output high voltage	IOH is driver dependent VDD_IO=3.0,DRV8	VOH	2.4	—	V
Output high voltage	IOH is driver dependent VDD_MEM=2.3, DRV8_MEM	VOHDDR	1.8	—	V
Output low voltage	IOL is driver dependent VDD_IO=3.0, DRV4	VOL	—	0.4	V
Output low voltage	IOL is driver dependent VDD_IO=3.0,DRV8V	VOL	—	0.4	V

Table 3: DC Characteristics

The following table shows the typical drive capability of a signal pin based on the type of output driver.

Driver Type	Supply Voltage	IOH	IOL	Unit
DRV4	VDDIO = 3.0V	4	4	mA
DRV8_MEM	VDDIO = 2.3V	8	8	mA
DRV8	VDDIO = 3.0V	8	8	mA

Table 4: Drive Capability of SiRFatlasIII Output Pins

Electrostatic Discharge

CAUTION: This device contains a circuitry that prevents damage from high-static voltage or electrical fields. Take normal precaution measures to avoid over-voltage. Tie up the unused inputs to an appropriate logic voltage level (either GND or VCC) to improve the operation reliability.

The following table lists the ESDl characteristics of this device.

Symbol	Rating	Min.	Max.	Unit
VHBM	Human Body Model (HBM) - JEDEC JESD22-A114-B	2000	—	V
VCDM	Charge Device Model (CDM) - JEDEC JESD22-C101	500	—	V
ILAT	Latch-up Current at TA = 23±5°C positive negative	—	±100	mA

Table 5: ESD Characteristics

Power Consumption

Power dissipation of the SiRFatlasIII is caused by 4 different components:

- Core power domains: Non-power-down domain

  This part is supplied by VDDPRE. It can not be shut down in sleep mode.

- Power-down domain

  This part is supplied by VDDPDN. It can be shut down by external power management.

- PLL power domains

  This part is supplied by VDD_PHA and VDD_PLA and VDD_PLD

- IO power domains

  This part is supplied by VDD_MEM and VDD_IO

Table 6 and Table 7 show the typical measured core and PLL power consumption for a range of operating modes.

TYPICAL	CPU/DSP/SYS/IO: 396/198/198/99	Unit
Pcore (VDDPRE)	3 ~ 30	mW
PLL	6	mW
IO(VDDIO)	10 ~ 50	mW
IO (VSSTL, A3 memory pad power consumption, not including memory chips power)	30 ~ 75	mW
Pcore (VDDPDN)	20 ~ 470	mW
Total	70 ~ 630	mW

Table 6: Normal Mode Power Consumption

NOTE: The small number is about reset status's power consumption, the big number is under operation system running condition with GPS running, graphic test bench, music playback and data transfer between peripherals. This table is just for reference, because SoC's power consumption is based on application conditions.

	Pio+Pmem	Ppll	Ppre	Pcore	Unit
Typical Power	<3 (based on leakage on board and GPIO setting)	0	1.3	0	mW
Total	<4				mW

Table 7: Sleep Mode Power Consumption

Thermal Performance

Rating			Value	Unit	Note
Junction to ambient natural convection	Four layer board (2s2p)	R_{JA}	38.5	°C/W	14x14 package
Junction to ambient (@1 m/s)	Four layer board (2s2p)	R_{JA}	34.7	°C/W	14x14 package

Table 8: Thermal Resistance Data

NOTE: Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

AC Specifications

AC Test Timing Conditions

Unless otherwise specified, the test conditions are:

- TA = -20 to 70 °C
- VDD_CORE = 1.3 V
- VDD_IO = 3.13 to 3.5 V

Output loading: All output is about 50 pF.

AC Operation Frequency Data

The following table provides the operating frequencies of SiRFatlasIII.

		Max. for 372MHz	Max. for 396MHz	Unit
1	ARM Clock	372	396	MHz
2	DSP Clock	248	264	MHz
3	SYS Clock	186	198	MHz
4	SDR SDRAM Clock	162	162	MHz
4	DDR SDRAM Clock	93	99	MHz
5	IO Clock	100	100	MHz

Table 9: Clock Frequencies

Crystal

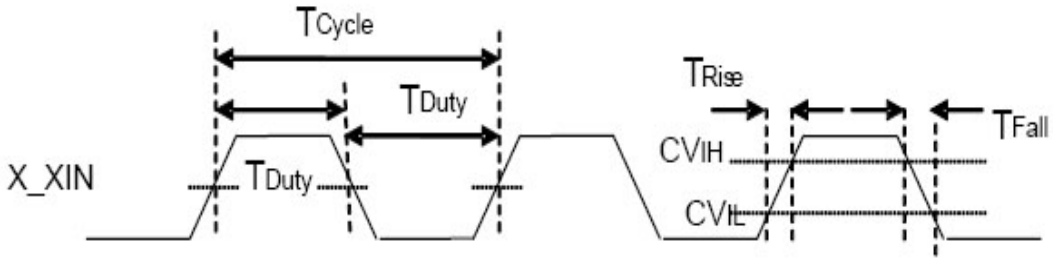


Figure 3: X_XIN Crystal Timing

Symbol	SpecID Description	Min.	Type	Max.	Unit
T_{Cycle}	X_XIN cycle time.	—	83.3	—	ns
T_{Rise}	X_XIN rise time.	—	—	5.0	ns
T_{Fall}	X_XIN fall time.	—	—	5.0	ns
T_{Duty}	X_XIN duty cycle	40.0	—	60.0	%
CV$_{IH}$	X_XIN input voltage high	2.0	—	—	V
CV$_{IL}$	X_XIN input voltage low	—	—	0.8	V

Table 10: X_XIN Timing

Reset

Following is the power-on sequence for 3.3v SDR, 3.3v/2.5v mobile SDR and 2.5v DDR1.

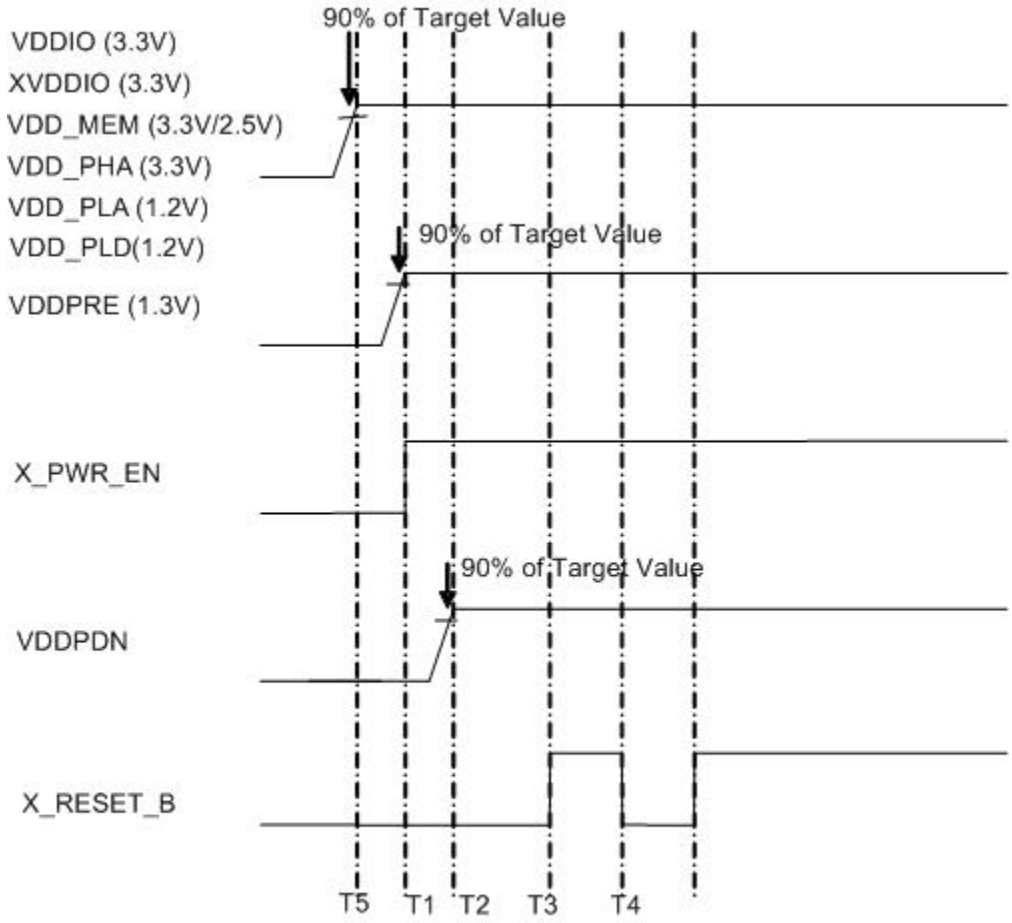
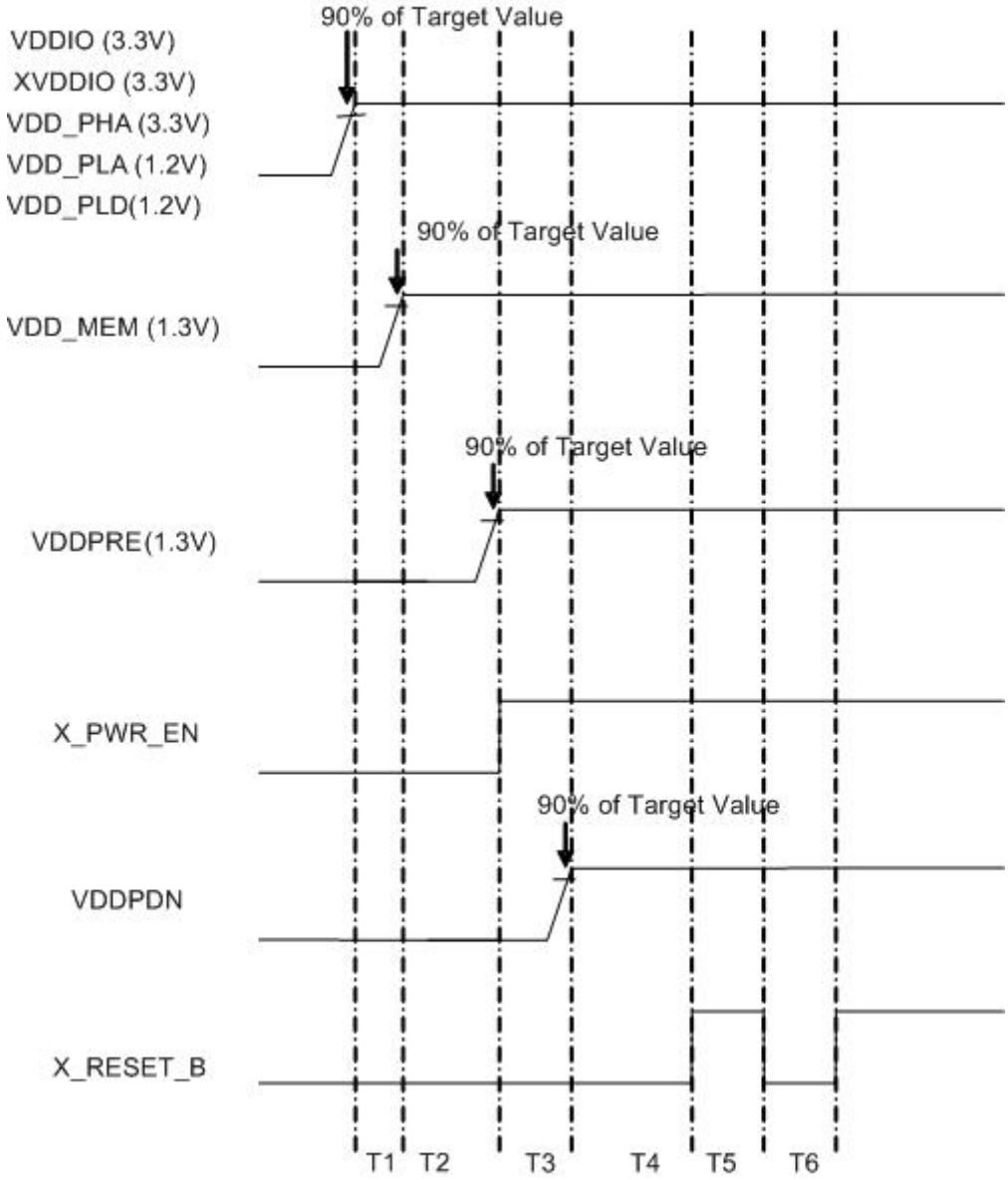


Figure 4: Power-On and Reset Sequence for SDR



T1>=0ms, T2>1ms, T3>=0ms, T4>1ms, 5ms>T5>1ms, T6>1ms

12Mhz clock must be stable before T5

Figure 5: Power-On and Reset Sequence for DDR

External Interrupts

The SiRFatlasIII provides 32 external interrupts: GPIO group 0 [31:0]. Each pin has two methods interrupt: edge and level.

Due to synchronization, prioritization, and mapping of external interrupt sources, the propagation of external interrupts to the core processor is delayed by several IO_clk clock cycles. The following table specifies the interrupt latencies in IO_clk cycles. The IO_clk frequency is programmable in the Clock Distribution Module.

Name	Min Pulse Width	Max Pulse Width	Reference Clock
All external interrupts	> 3 clock cycles	—	IO_clk

Table 11: Minimum Pulse Width for External Interrupts to Recognize

SDR SDRAM

x_mem_clk, Address, Control, and Data output are clocked by sys_clk. The path delay of x_mem_clk can be adjusted by Manager Delay Control Register PWR_DELAY_CTRL_0 (only x_mem_clk, others cannot be changed).

Data input is clocked by mck_i, which can be driven by internal mem_clk or pad loop back (x_mem_clk). The path delay of mck_i can be configured by PWR_DELAY_CTRL_1. Because the internal delay of x_mem_clk and mck_i are configurable, the values in Table 12 and Table 13 are relatively flexible.

SDR SDRAM Read Command

Symbol	Description	Min.	Max.	Unit
tmem_clk	MEM_CLK period	6	—	ns
tvalid	Control Signals, Address and MBA Valid after rising edge of MEM_CLK	—	4	ns
thold	Control Signals, Address and MBA Hold after rising edge of MEM_CLK	2	—	ns
DMvalid	DQM valid after rising edge of MEM_CLK	—	4.5	ns
DMhold	DQM hold after rising edge of MEM_CLK	3.0	—	ns
tdatasetup	MDQ setup to rising edge of MEM_CLK	-2.0	—	ns
tdatahold	MDQ hold after rising edge of MEM_CL	4	—	ns

Table 12: SDR SDRAM Memory Read Timing

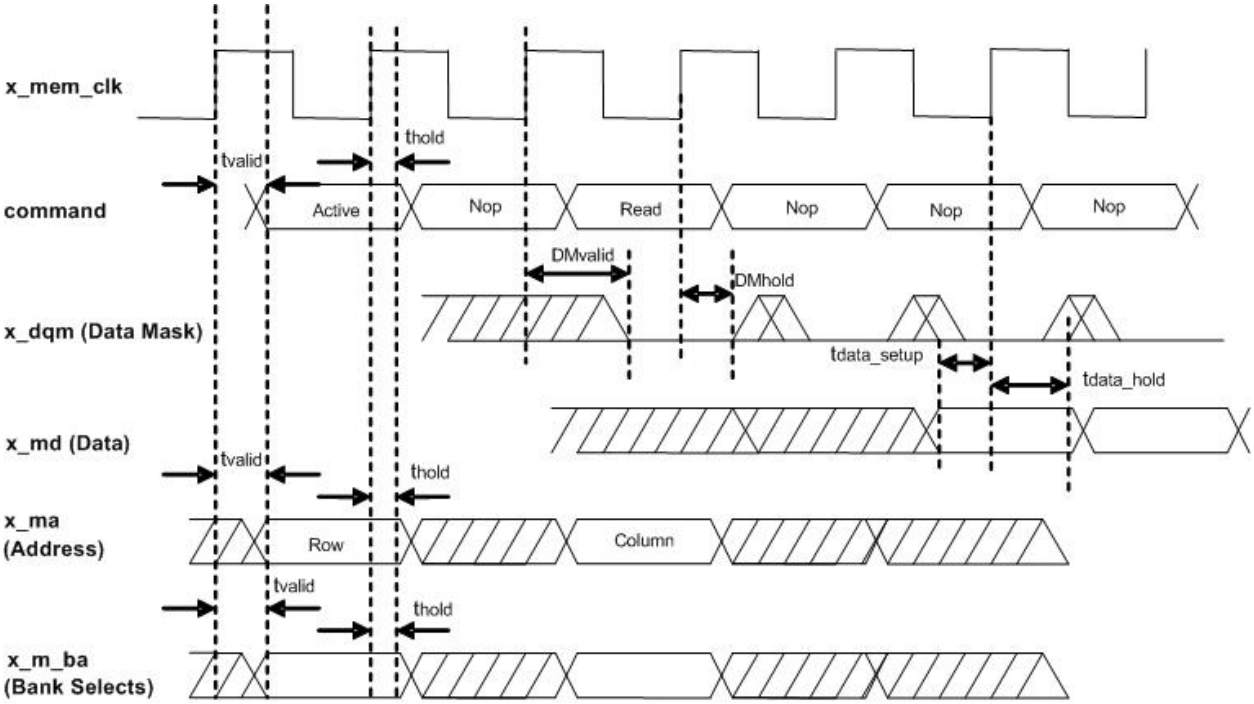


Figure 6: SDR SDRAM Memory Read Timing Diagram

NOTE: Command is composed of RAS, CAS, WE, CS and MCKE.

SDR SDRAM Write Command

Symbol	Description	Min.	Max.	Unit
tmem_clk	MEM_CLK period	7.5	—	ns
tvalid	Control Signals, Address and MBA Valid after rising edge of MEM_CLK	—	6	ns
Thold	Control Signals, Address and MBA Hold after rising edge of MEM_CLK	2	—	ns
DMvalid	DQM valid after rising edge of MEM_CLK	—	4.5	ns
DMhold	DQM hold after rising edge of MEM_CLK	3.0	—	ns
tdatavalid	MDQ setup to rising edge of MEM_CLK	—	7	ns
tdatahold	MDQ hold after rising edge of MEM_CL	5	—	ns

Table 13: SDR SDRAM Write Timing

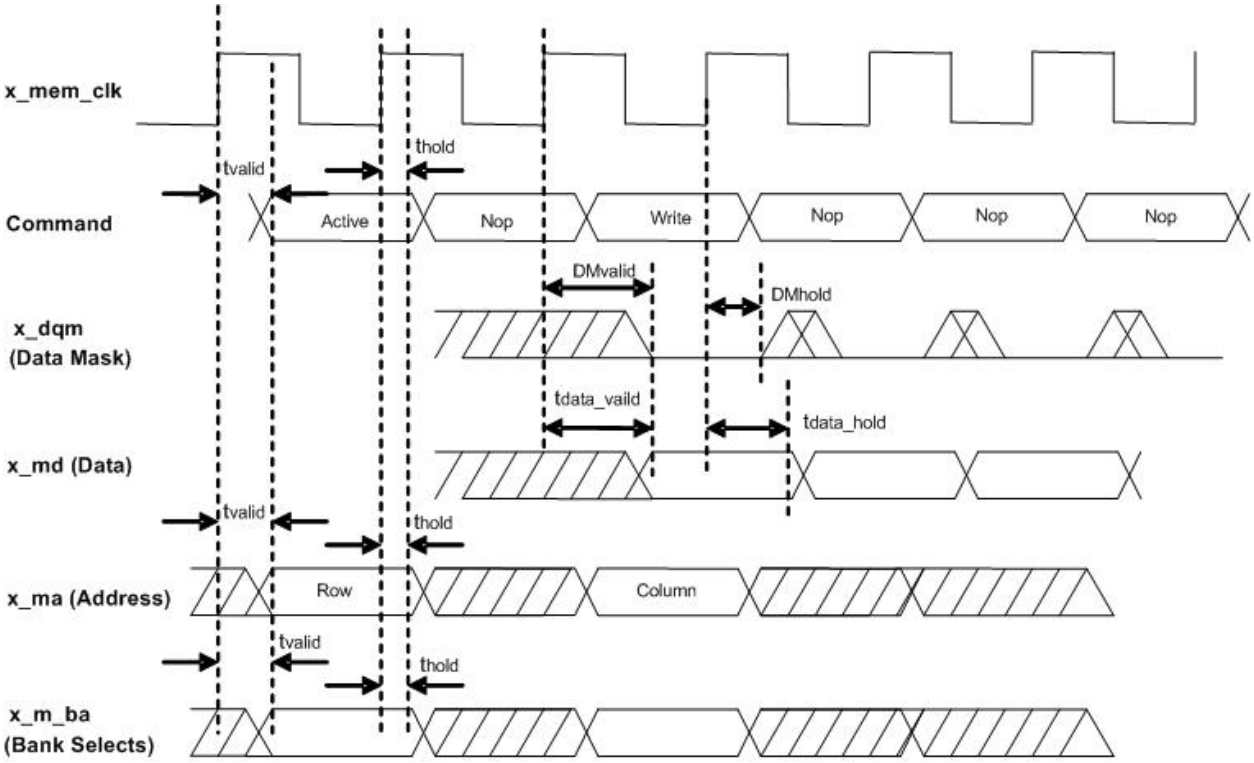


Figure 7: SDR SDRAM Memory Write Timing Diagram

NOTE: Command is composed of RAS, CAS, WE, CS and MCKE.

DDR SDRAM

Address and control output is clocked by sys_clk. Data, DQS, and DM output is clocked by mck2x_o which should match the delay between mck2x_o and mck_clk.
Data inputs are clocked by delayed DQS.

DDR SDRAM Read Command

Symbol	Description	Min.	Max.	Unit
tmem_clk	MEM_CLK period	10	—	ns
tvalid	Control Signals, Address and MBA Valid after rising edge of MEM_CLK	—	5	ns
Thold	Control Signals, Address and MBA Hold after rising edge of MEM_CLK	4	—	ns
tdatasetup	MDQ setup to rising edge of x_mdqs	4.5	—	ns
tdatahold	MDQ hold after rising edge of x_mdqs	-3.0	—	ns

Table 14: DDR SDRAM Memory Read Timing

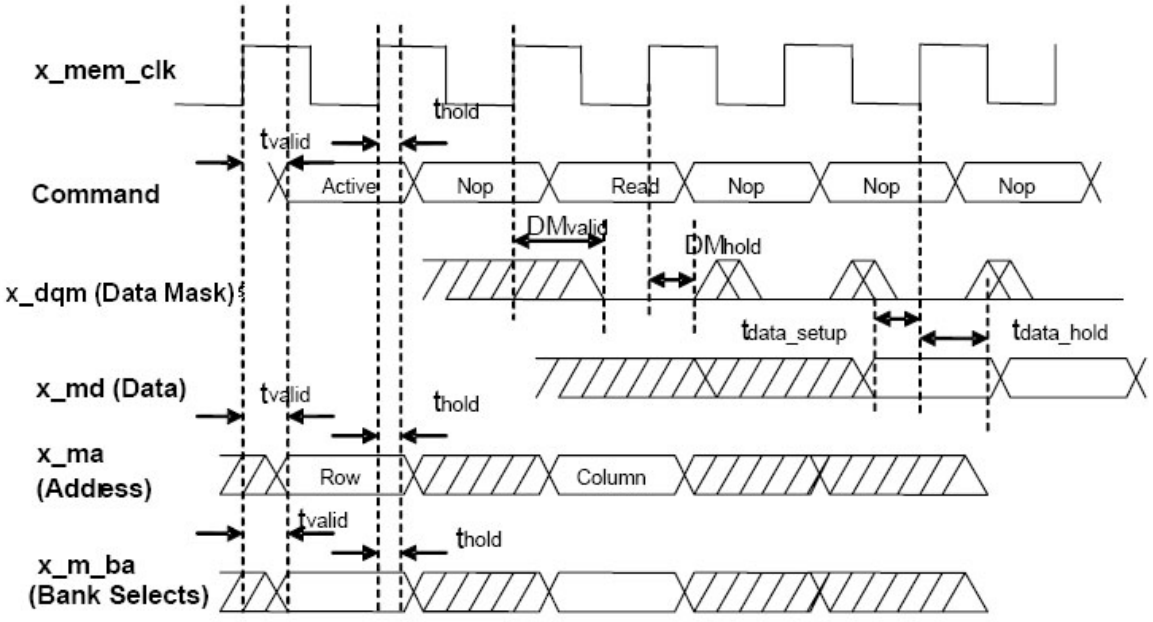


Figure 8: DDR SDRAM Memory Read Timing

NOTE: Command is composed of RAS, CAS, WE, CS, and MCKE.

DDR SDRAM Write Command

Symbol	Description	Min.	Max.	Unit
T_{mem_clk}	MEM_CLK period	10	—	ns
t_{dqss}	Delay from write command to first rising edge of MDQS	T_{mem_clk} + 0.2	T_{mem_clk} + 1.5	ns

Table 15: DDR SDRAM Write Timing

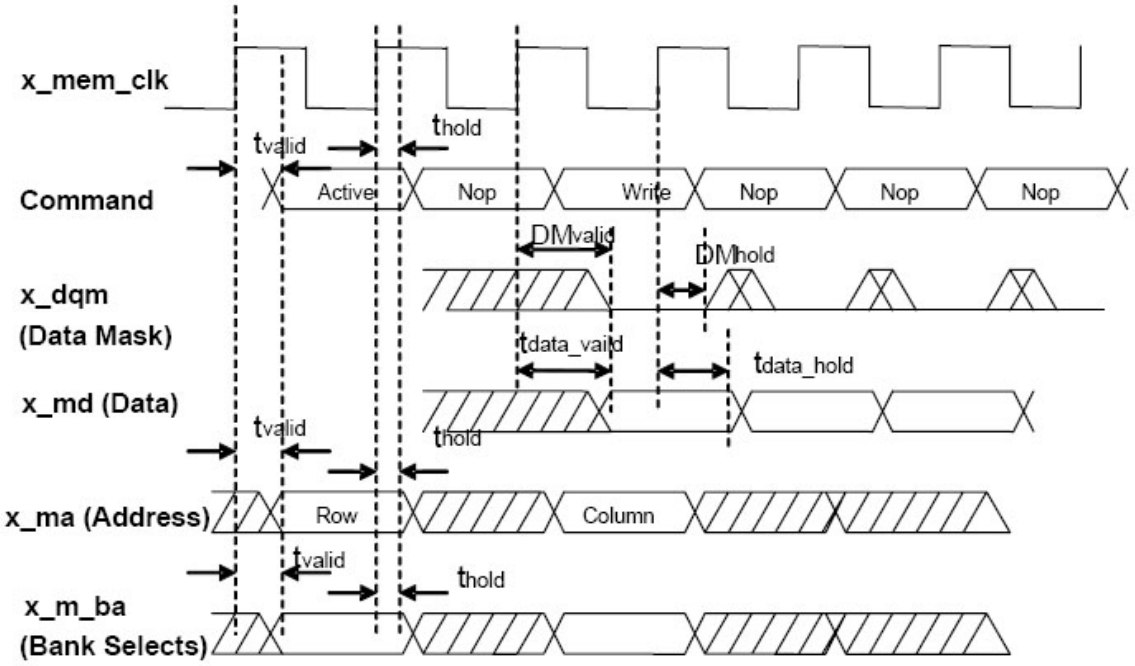


Figure 9: DDR SDRAM Memory Write Timing

NOTE: Command is composed of RAS, CAS, WE, CS, and MCKE.

Video Input Port

Symbol	Description	Min.	Max.	Unit
t_{vvaild}	Vsync output valid time	—	1.5	ns
t_{vhd}	Vsync hold time	0.2	—	ns
t_{hvaild}	Hsync output valid time	—	1.8	ns
t_{hd}	Hsync output hold time	0.5	—	ns
t_{st}	Input setup time	0.8	—	ns
t_{hd}	Input hold time	1.0	—	ns

Table 16: Video Input Port Timing

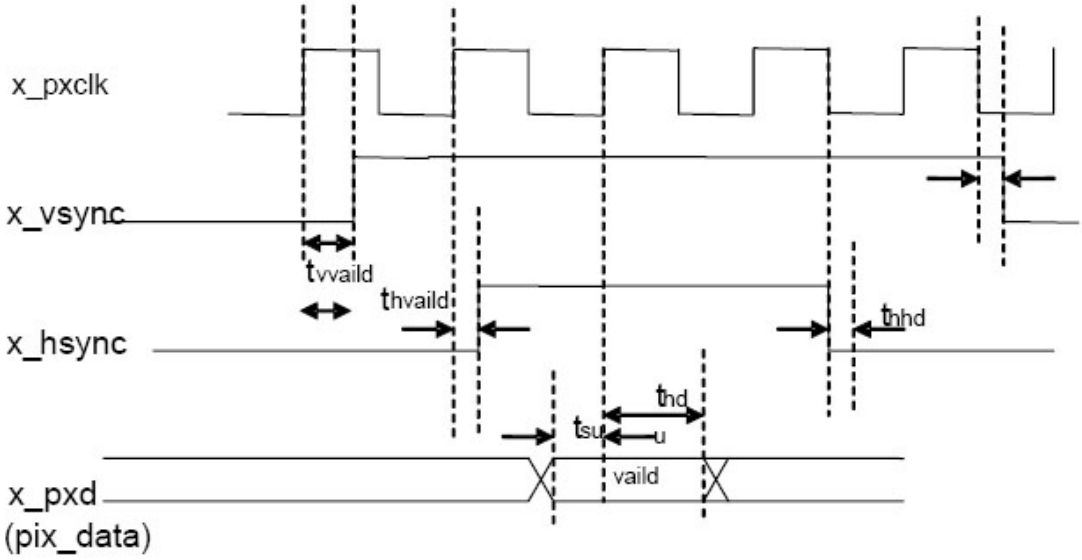


Figure 10: Video Input Port Timing

NOTE: When Video Input Port works in master mode, x_pixclk, x_vsync, and x_hsync are output while x_pxd (pixel_data) is input.

LCD Interface

Symbol	Description	Min.	Max.	Unit
t_{fvaild}	Frame output valid time	—	-0.6.	ns
t_{fhd}	Frame hold time	-0.2	—	ns
t_{lvaild}	Line output valid time	—	-0.7	ns
t_{lhd}	Line output hold time	-0.3	—	ns
t_{bvaild}	Bias output valid time	—	1.4	ns
t_{bhd}	bias output hold time	0.4	—	ns
t_{dvaild}	Pix_data output valid time	—	5.8	ns
t_{dhd}	Pix_data output hold time	0.6	—	ns

Table 17: LCD Interface Timing

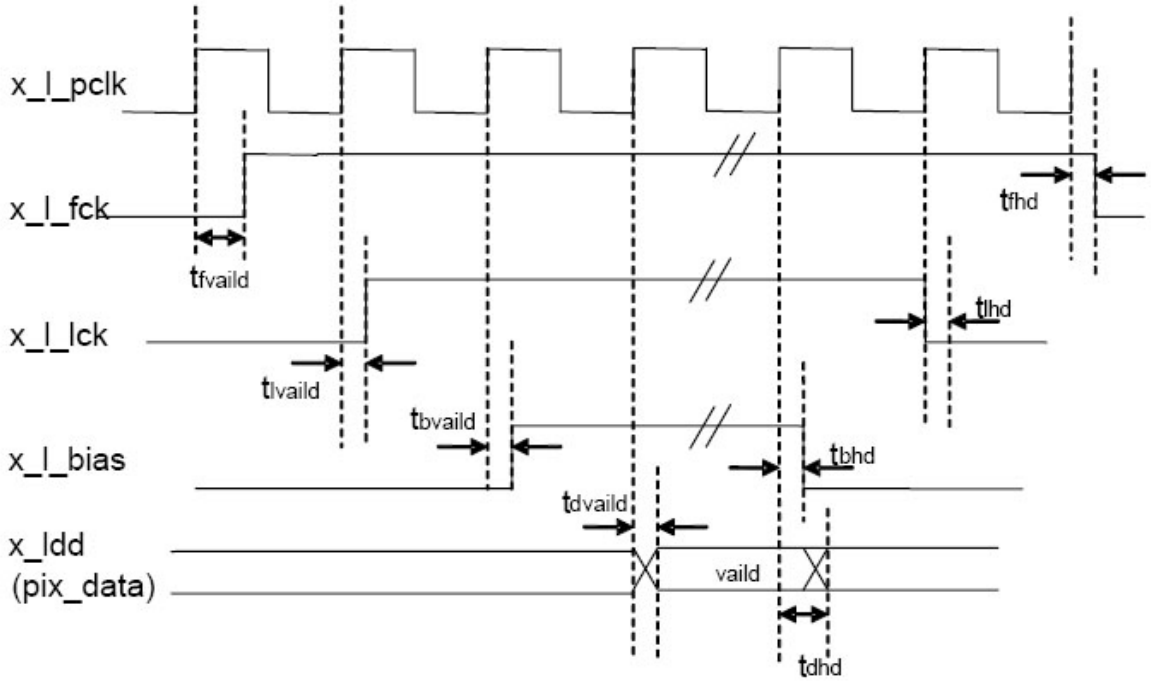


Figure 11: LCD Interface Timing

NOTE: When LCD interface works in master mode, x_pclk, x_l_fck, and x_l_lck are output.

ROM/SRAM Interface[1]

Symbol	Description	Min.	Max.	Unit
t_{oesu1}	oe high to ce active switching time delay1	—	30	ns
t_{oehd1}	cs active to oe active delay1	—	20	ns
T_{oesu2}	oe high to ce active switching time delay2	—	20	ns
T_{oehd2}	cs active to oe active delay2	—	50	ns
T_{dsu}	Valid data setup time	10	—	ns
T_{dhd}	Valid data hold up time	-8	—	ns

Table 18: ROM Read Data Timing

***** **t**oesu, **t**oehd are copied from SiRFatlasI™, they can be adjusted through internal registers.

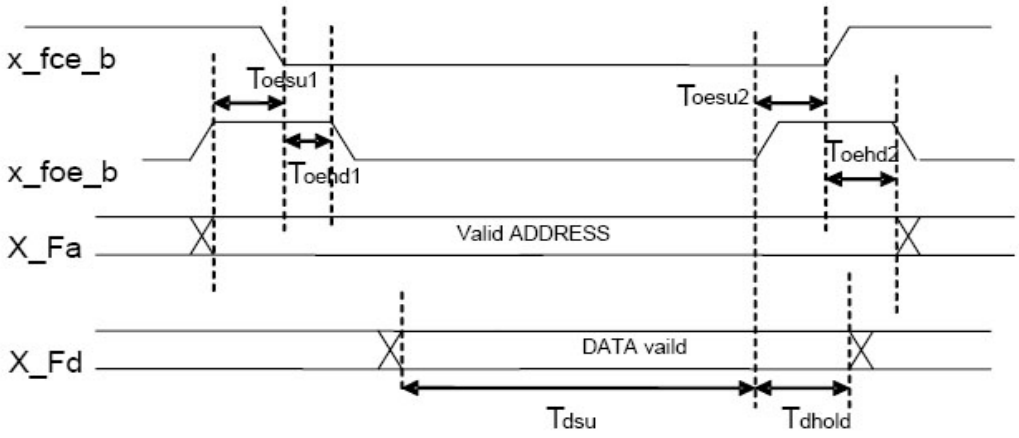


Figure 12: ROM Read Timing

Symbol	Description	Min.	Max.	Unit
t_{oesu1}	oe high to ce active switching time delay1	—	30	ns
t_{oehd1}	cs active to oe active delay1	—	20	ns
T_{oesu2}	oe high to ce active switching time delay2	—	20	ns
T_{oehd2}	cs active to oe active delay2	—	50	ns
T_{dvaild}	Data valid time	—	15	ns
T_{dhd}	Data hold time	3	—	ns

Table 19: ROM Write Timing

[1] When multiplexed with ROM interface.

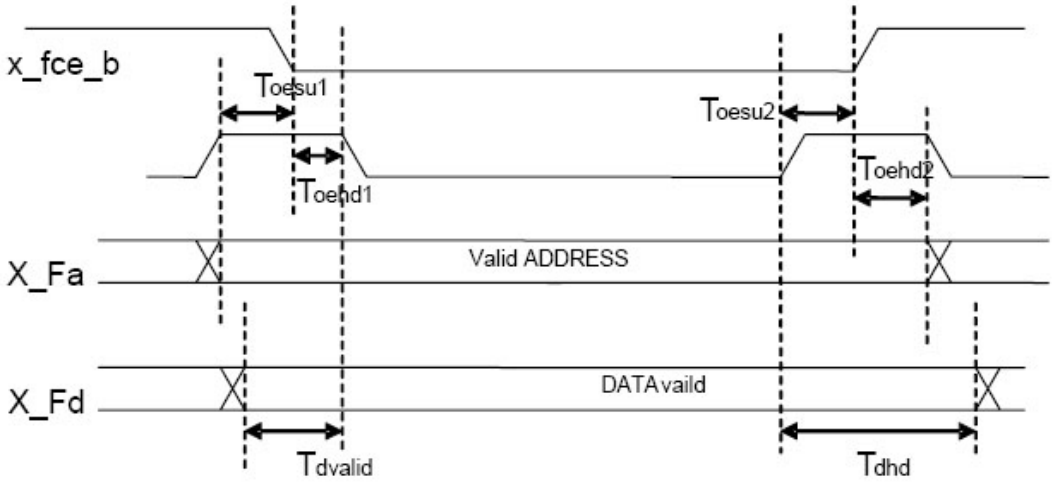


Figure 13: ROM Write Timing

NAND Flash Interface

Symbol	Description	Min.	Max.	Unit
Tcss	Chip select setup time	(2*io_clk)-1	—	ns
Tcsh	Chip select hold time	(3*io_clk)-1	—	ns
Trp	Read active time	(0x1~0xF) *io_clk		ns
Treh	For next read hold high time	(1~2)*io_clk		ns
Trea	Valid data setup time	10	—	ns
Trhz	Valid data hold time	0	—	ns
Trr	Valid read setup time	6*io_clk	—	ns

Table 20: NAND Flash Multiplexed with VIP Port Read Data Timing

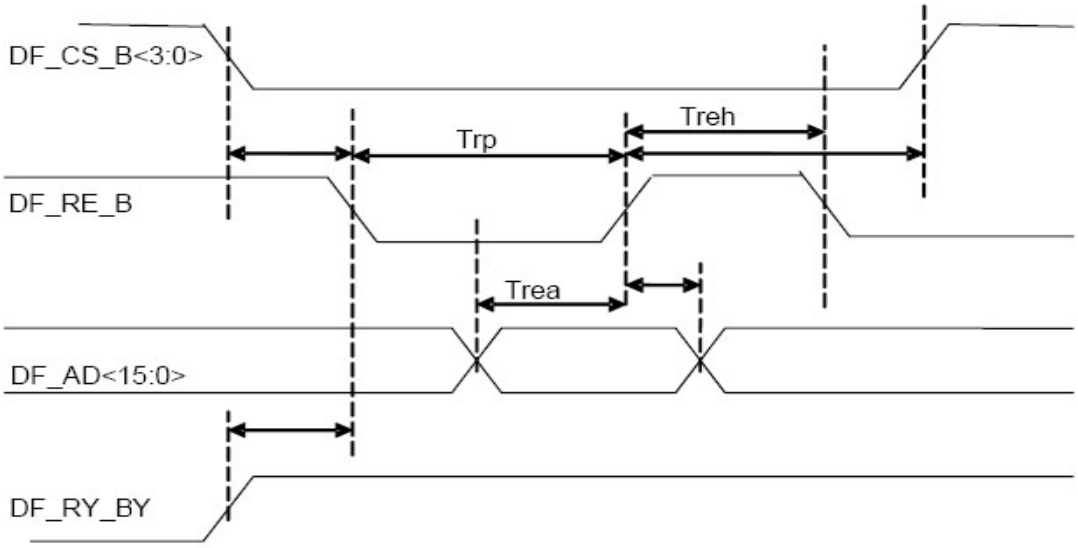


Figure 14: NAND Flash Multiplexed with VIP Port Read Data Timing

Symbol	Description	Min.	Max.	Unit
Tcss	Chip select setup time	(2*io_clk)-1	—	ns
Tcsh	Chip select hold time	io_clk-1	—	ns
Tcls	Address and command select setup time	0	—	ns
Tclh	Address and command select hold time	io_clk	—	ns
Twp	Write valid time	(0x1~0xF) *io_clk		ns
Twh	Next write hold high time	(1~2)*io_clk		ns
Tds	Data setup time		-4	ns
Tdh	Data hold time	io_clk+2	—	ns

Table 21: NAND Flash Multiplexed with VIP Port Write Data Timing

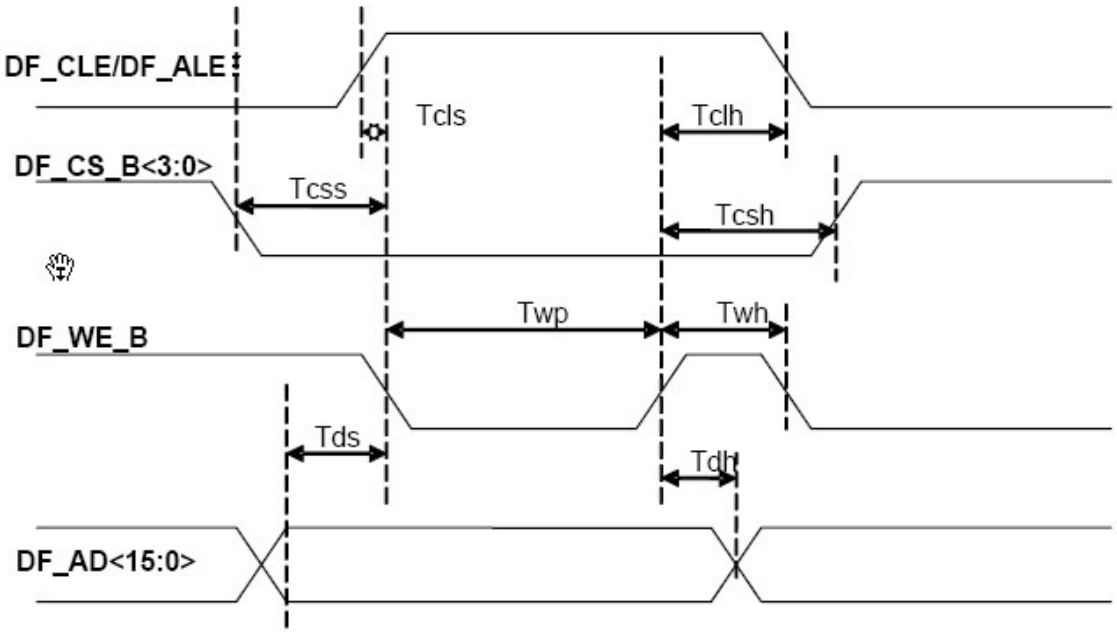


Figure 15: NAND Flash Multiplexed with VIP Port Write Data Timing

IDE Specifications (Reference IDE Specifications)

- IDE Register Read/Write Timing

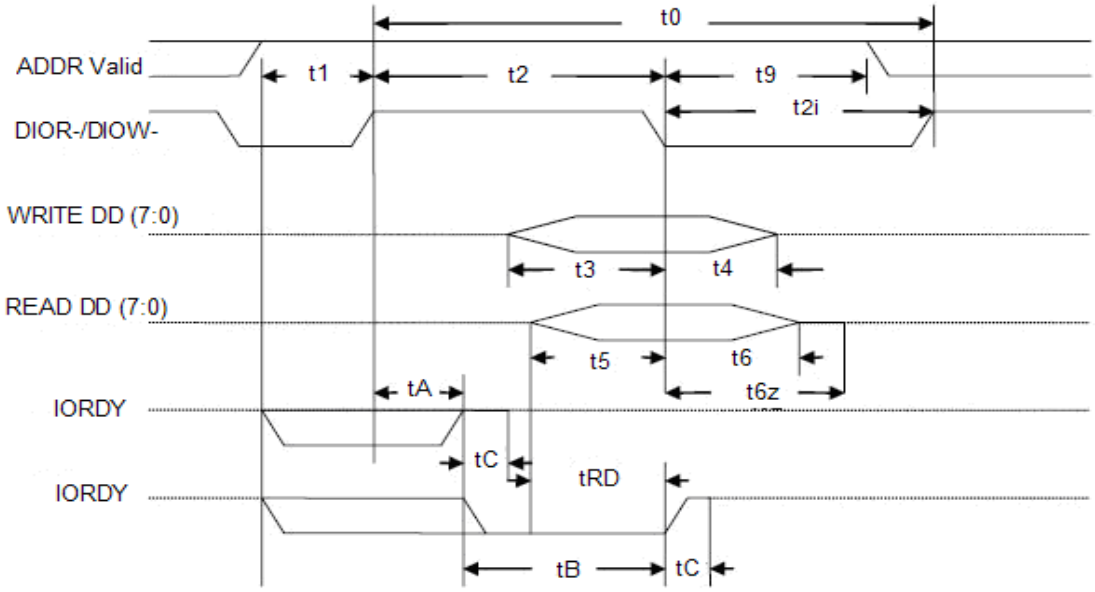


Figure 16: IDE Register Transfer Timing

Register Transfer Timing Parameters		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t0	Cycle time (min.)	600	383	330	180	120
t1	Address valid to DIOR-/DIOW- setup (min.)	70	50	30	30	25
t2	DIOR-/DIOW- pulse width 8-bit (min.)	290	290	290	80	70
t2i	DIOR-/DIOW- recover time (min.)	—	—	—	70	25
t3	DIOW- data setup (min.)	60	45	30	30	20
t4	DIOW- data hold (min.)	30	20	15	10	10
t5	DIOR- data setup (min.)	50	35	20	20	20
t6	DIOR- data hold (min.)	5	5	5	5	5
t6z	DIOR- data tristate (max.)	30	30	30	30	30
t9	DIOR-/DIOW- to address valid hold (min.)	20	15	10	10	10
tRD	Read data valid to IORDY active (min.)	0	0	0	0	0
tA	IORDY setup time	35	35	35	35	35
tB	IORDY pulse width (max.)	1250	1250	1250	1250	1250
tC	IORDY assertion to release	5	5	5	5	5

Table 22: IDE Register Transfer Required Timing

- IDE PIO Read/Write Timing

PIO Transfer Timing Parameters		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t0	Cycle time (min.)	600	383	330	180	120
t1	Address valid to DIOR-/DIOW- setup (min.)	70	50	30	30	25
t2	DIOR-/DIOW- pulse width (min.)	165	125	100	80	70
t2i	DIOR-/DIOW- recover time (min.)	—	—	—	70	25
t3	DIOW- data setup (min.)	60	45	30	30	20
t4	DIOW- data hold (min.)	30	20	15	10	10
t5	DIOR- data setup (min.)	50	35	20	20	20
t6	DIOR- data hold (min.)	5	5	5	5	5
t6z	DIOR- data tristate (max.)	30	30	30	30	30
t9	DIOR-/DIOW- to address valid hold (min.)	20	15	10	10	10
tRD	Read data valid to IORDY active (min.)	0	0	0	0	0
tA	IORDY setup time	35	35	35	35	35
tB	IORDY pulse width (max.)	1250	1250	1250	1250	1250
tC	IORDY assertion to release	5	5	5	5	5

Table 23: IDE PIO Transfer Required Timing

- IDE Multi-Word DMA Timing

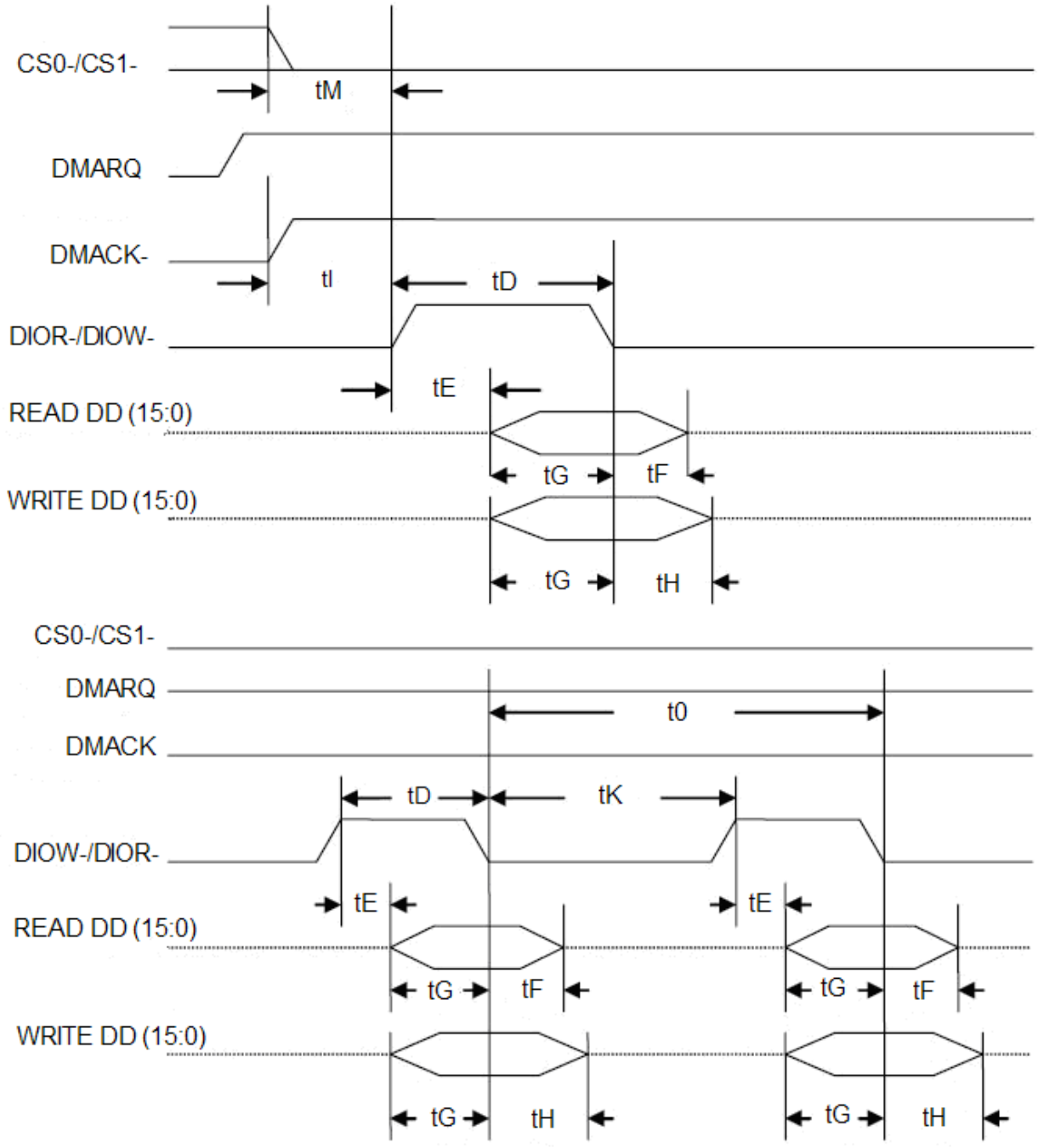


Figure 17: IDE Multi-Word DMA Timing

Multi-word DMA Timing Parameters		Mode 0	Mode 1	Mode 2
t0	Cycle time (min.)	480	150	120
tD	DIOR-/DIOW- asserted pulse width (min.)	215	80	70
tE	DIOR- data access (max.)	150	60	50
tF	DIOR- data hold (min.)	5	5	5
tG	DIOR-/DIOW- data setup (min.)	100	30	20
tH	DIOW- data hold (min.)	20	15	10
tI	DMACK to DIOR-/DIOW- setup (min.)	0	0	0
tJ	DIOR-/DIOW- to DMACK hold (min.)	20	5	5
tKR	DIOR- negated pulse width (min.)	50	50	25
tKW	DIOW- negated pulse width (min.)	215	50	25
tLR	DIOR- to DMARQ delay (max.)	120	40	35
tLW	DIOW- to DMARQ delay (max.)	40	40	35
tM	CS (1:0) valid to DIOR-/DIOW-	50	30	25
tN	CS (1:0) hold	15	10	10
tZ	DMACK- to read data released (max.)	20	25	25

Table 24: IDE Multi-Word DMA Required Timing

Serial Port

Pin Name	Symbol	Parameter	Min.	Max.	Unit
X_TXD	Tvaild	Txd valid time	—	30	ns
	Tdhd	Txd data hold time	0.3	—	ns
X_TFS	Tvalid	TFS valid time	—	30	ns
	Tdhd	TFS data hold time	0.4	—	ns
X_RXD	Tsu	RXD setup time	-10	—	ns
	Thd	RXD hold time	-11	—	ns
X_RFS	Tsu	RFS setup time	-10	—	ns
	Thd	RFS hold time	-11	—	ns

Table 25: Serial Port Timing

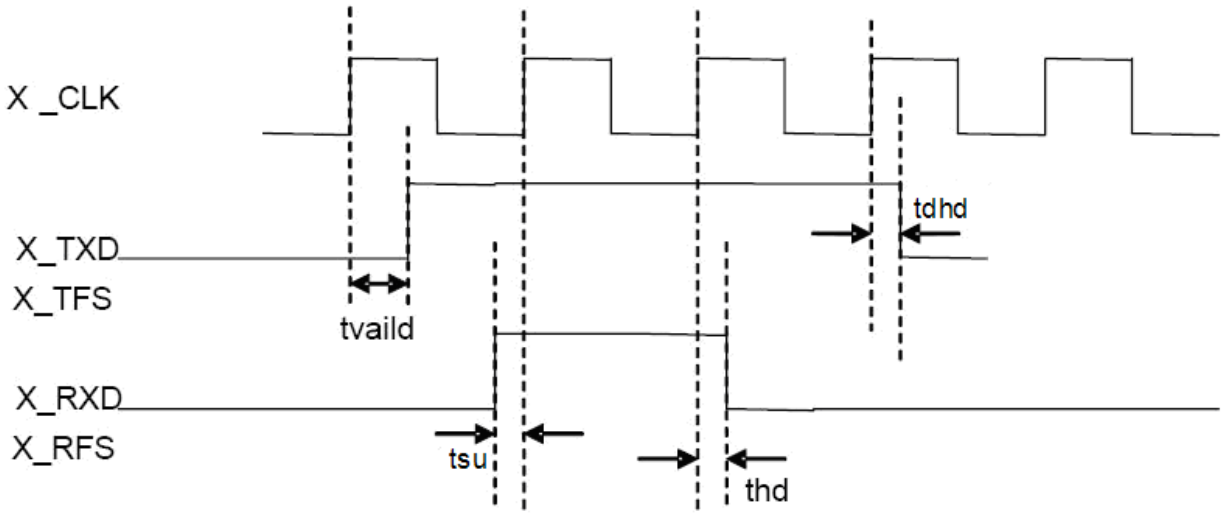


Figure 18: Serial Port Timing

CANBUS AC Specifications

Symbol	Spec ID Description	Min.	Type	Max.	Unit
tbit	Minimum bit time	1	—	100	us
tonRXD	Delay TXD to receiver active	—	50	90	ns
toffRXD	Delay TXD to receiver inactive	—	50	90	ns

Table 26: Serial Port AC Timing

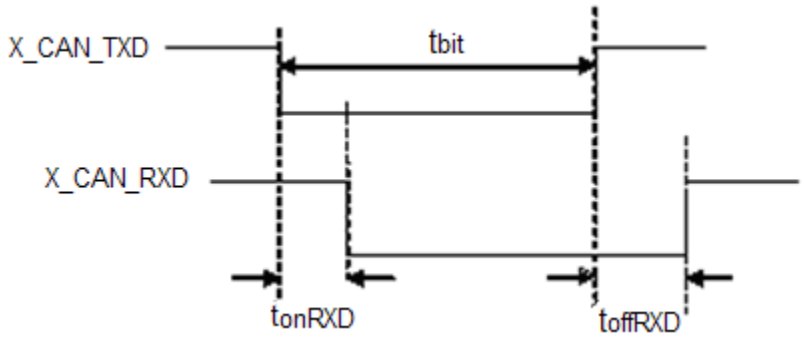


Figure 19: CANBUS Port AC Timing

PCMCIA AC Specifications

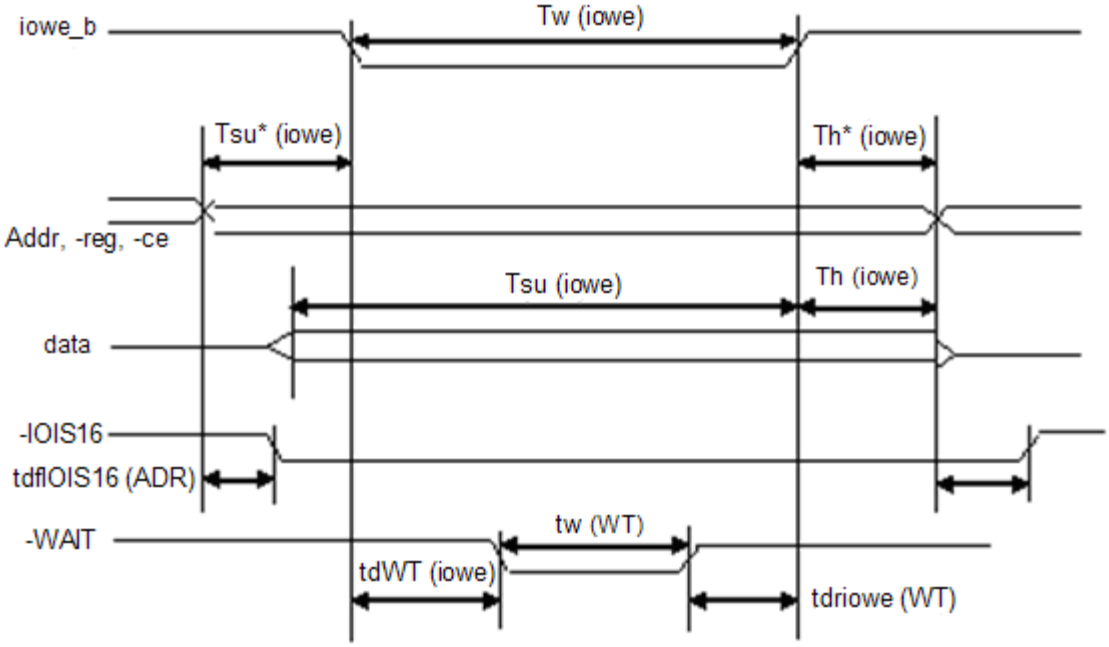


Figure 20: I/O Write Timing

Item	Symbol	Min.	Max.	Unit
Cycle time mode	—	255	—	ns
Data setup before iowe_b (min.)	tsu (iowe)	(2 * setup timing register + 2 * command timing register + 4) * Tclk_pci		ns
Data hold following iowe_b (min.)	th (iowe)	(2 * recovery timing register + 4) * Tclk_pci		ns
Iowe_b width time (min.)	tw (iowe)	2 * (command timing register + 1)* Tpci_clk + tw(WT)		ns
Address setup before iowe_b (min.)	tsuA (iowe)	(2 * setup timing register + 4) * Tclk_pci		ns
Address hold following iowe_b (min.)	thA (iowe)	(2 * recovery timing register + 4) * Tclk_pci		ns
CE setup before iowe_b (min.)	tsuCE (iowe)	(2 * setup timing register + 2) * Tclk_pci		ns
CE hold following iowe_b (min.)	thCE (iowe)	(2 * recovery timing register + 2) * Tclk_pci		ns
REG setup before iowe_b (min.)	tsuREG (iowe)	(2 * setup timing register + 2) * Tclk_pci		ns
REG hold following iowe_b (min.)	thREG (iowe)	(2 * recovery timing register + 4) * Tclk_pci		ns
IOIS16 delay falling from address (max.)	tdfIOIS16 (ADR)	—	35	ns
IOIS16 delay rising from address (max.)	tdrIOIS16 (ADR)	—	35	ns
WAIT delay falling from iowe_b (max.)	tdWT (iowe)	—	35	ns
iowe high from wait high (min.)	tdriowe (WT)	0	—	ns
WAIT width time (max.)	tw (WT)	—	350 (3000 for F+)	—

Table 27: I/O Write Timing

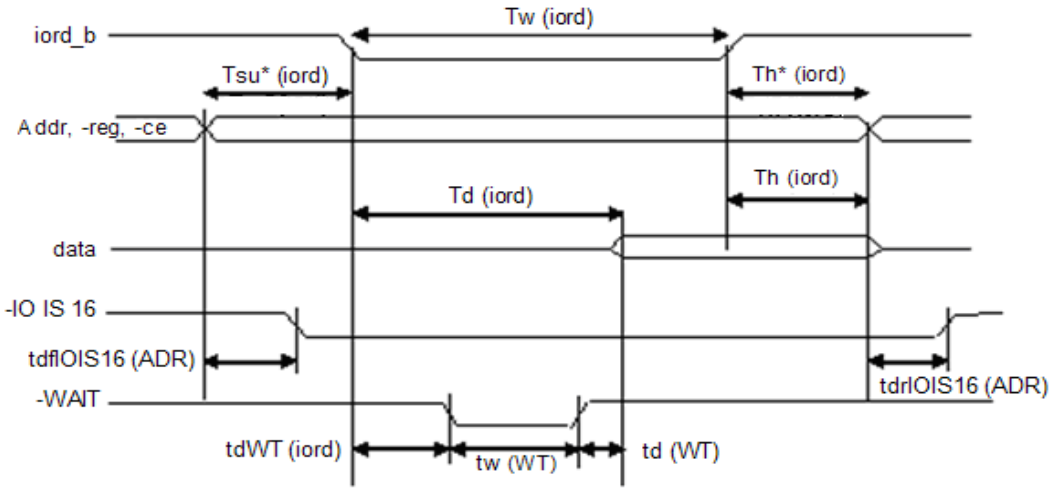


Figure 21: I/O Read Timing

Item	Symbol	Min.	Max.	Unit
Cycle time mode	—	250	—	ns
Data delay after iord_b (max.)	Td (iord)	2 * command timing register * Tpci_clk + tw(WT)		ns
Data hold following iord_b (min.)	Th (iord)	0		ns
Iord_b width time (min.)	Tw (iord)	2 * (command timing register + 1)* Tpci_clk + tw(WT)		ns
Address setup before iord_b (min.)	TsuA (iord)	(2 * setup timing register +4) * Tclk_pci		ns
Address hold following iord (min.)	ThA (iord)	(2 * recovery timing register +4) * Tclk_pci		ns
CE setup before iord (min.)	TsuCE (iord)	(2 * setup timing register +2) * Tclk_pci		ns
CE hold following iord (min.)	ThCE (iord)	(2 * recovery timing register +2) * Tclk_pci		ns
REG setup before iord (min.)	TsuREG (iord)	(2 * setup timing register +2) * Tclk_pci		ns
REG hold following iord (min.)	ThREG (iord)	(2 * recovery timing register +4) * Tclk_pci		ns
IOIS16 delay falling from address (max.)	tdfIOIS16 (ADR)	—	35	ns
IOIS16 delay rising from address (max.)	tdrIOIS16 (ADR)	—	35	ns
WAIT delay falling from iord (max.)	tdWT (iord)	—	35	ns
Data delay from wait rising (max.)	td (WT)	—	0	ns
WAIT width time (max.)	tw (WT)	—	350 (3000 for CF+)	—

Table 28: I/O Read Timing

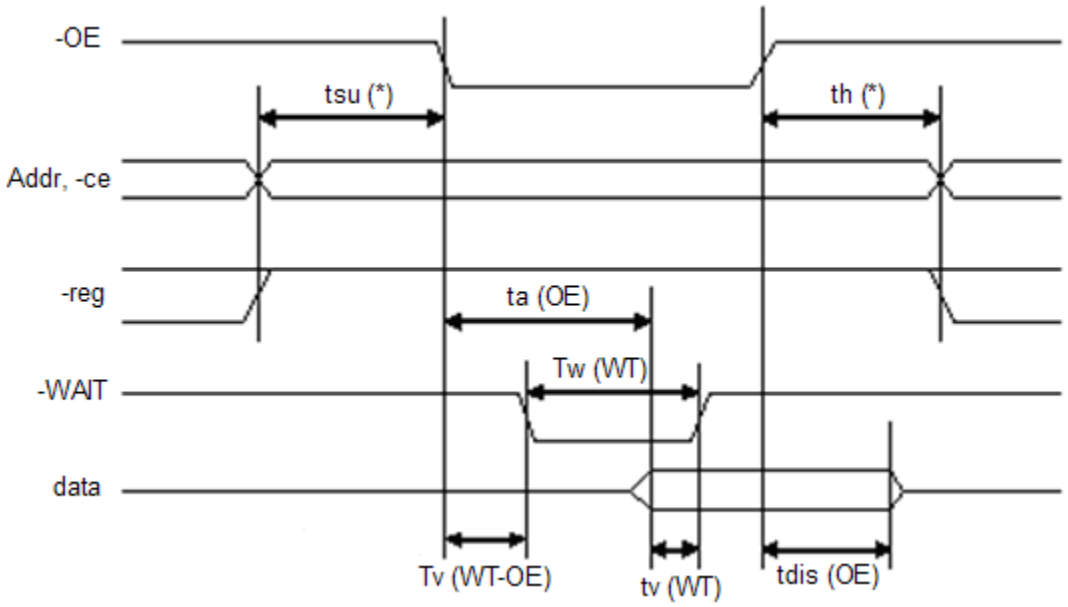


Figure 22: Common Memory Read Timing

Item	Symbol	Min.	Max.	Unit
Cycle time mode	—	250	—	ns
Output enable access time (max.)	ta (OE)	2 * command timing register * Tpci_clk + tw (WT)		ns
Output disable time from OE (max.)	tdis (OE)	(2 * recovery timing register + 2) * Tclk_pci		ns
Address setup time (min.)	tsu (A)	(2 * setup timing register + 4) * Tclk_pci		ns
Address hold time (min.)	th (A)	(2 * recovery timing register + 4) * Tclk_pci		ns
CE setup before OE (min.)	tsu (CE)	(2 * setup timing register + 2) * Tclk_pci		ns
CE hold following OE (min.)	th (CE)	(2 * recovery timing register + 2) * Tclk_pci		ns
Wait delay falling from OE (max.)	tv (WT-OE)	—	35	ns
Data setup for wait release (max.)	tv (WT)	—	0	ns
Wait width time (max.)	tw (WT)	—	350 (3000 for CF+)-	ns

Table 29: Common Memory Read Timing

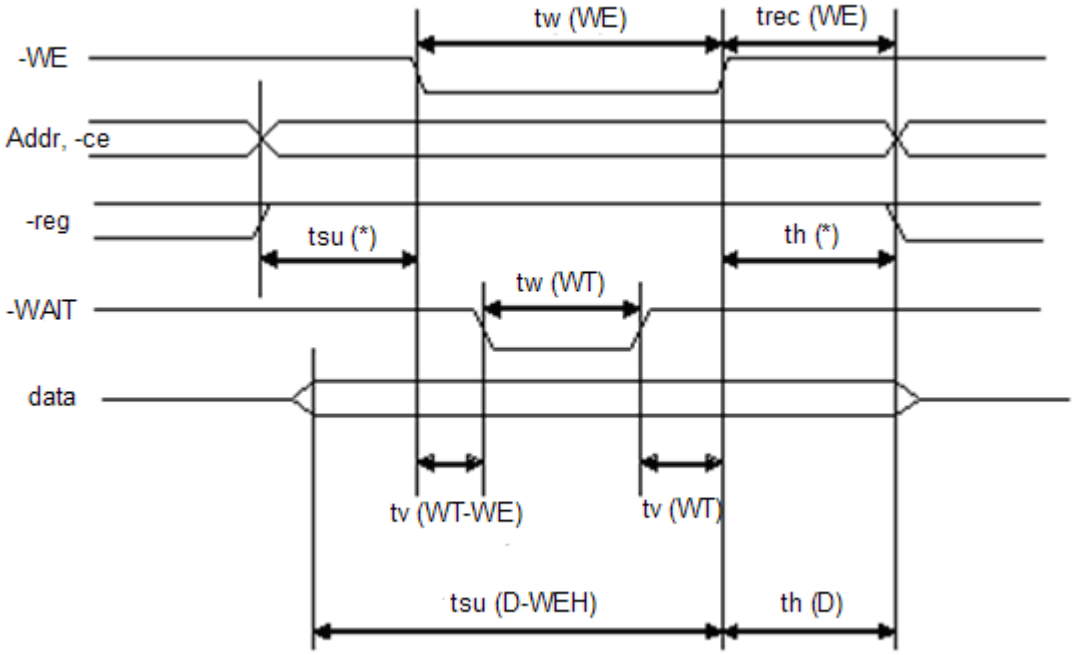


Figure 23: Common Memory Write Timing

Item	Symbol	Min.	Max.	Unit
Cycle time mode	—	250	—	ns
Data setup before WE (min.)	tsu (D-WEH)	(2 x setup timing register + 2 x command timing register +4) * Tclk_pci		ns
Data hold following WE (min.)	th (D)	(2 x recovery timing register +4) * Tclk_pci		ns
WE pulse width (min.)	tw (WE)	2 x (command timing register + 1)* Tpci_clk + tw(WT)		ns
Address setup time (min.)	tsu (A)	(2 x setup timing register +4) * Tclk_pci		ns
CE setup before WE (min.)	tsu (CE)	(2 x setup timing register +2) * Tclk_pci		ns
Write recovery time (min.)	trec (WE)	(2 x recovery timing register +2) * Tclk_pci		ns
Address hold time (min.)	th (A)	(2 x recovery timing register +4) * Tclk_pci		ns
CE hold following WE (min.)	th (CE)	(2 x recovery timing register +2) * Tclk_pci		ns
Wait delay falling from WE (max.)	tv (WT-WE)	—	35	ns
WE high from wait release (min.)	tv (WT)	0	—	ns
Wait width time (max.)	—	—	350 (3000 for CF+)-	ns

Table 30: Common Memory Write Timing

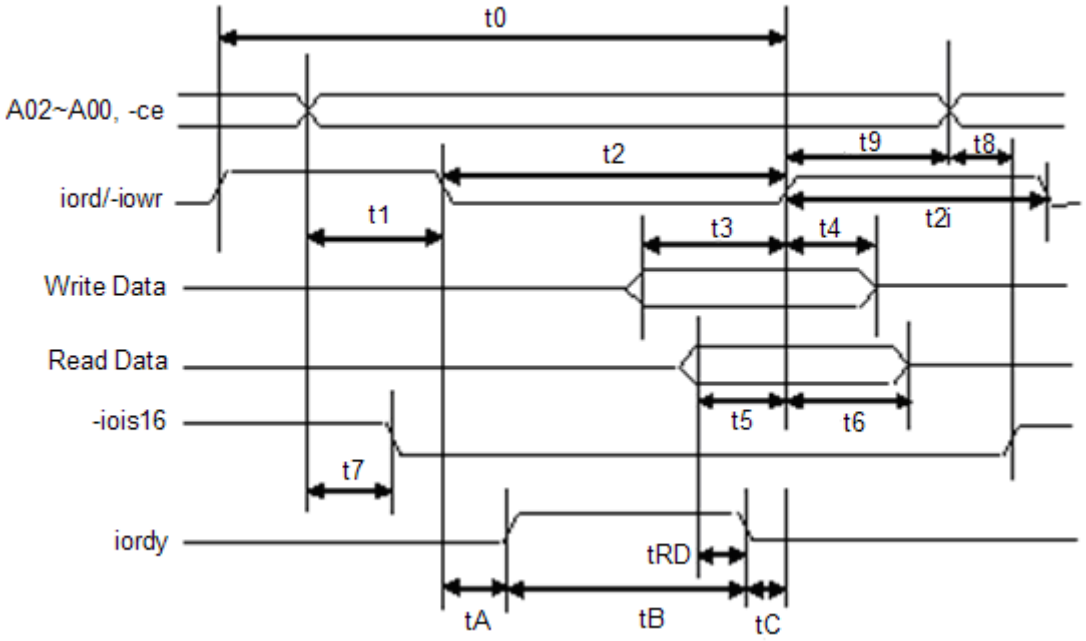


Figure 24: True IDE PIO Mode Timing

		Min.	Max.	Unit
Cycle Time Mode		Mode 0		
Symbol	Item			
t0	Cycle time (min.)	(2 * setup timing register + 2 * command timing register+ 2 * recovery timing register + 10) * Tpci_clk + tB		ns
t1	Address valid to –IORD/-IOWR setup (min.)	(2 * setup timing register +4) * Tclk_pci		ns
t2	-IORD/-IOWR (min.)	2 * (command timing register + 1) * Tpci_clk + tB		ns
t2i	-IORD/-IOWR recovery time (min.)	(2 * recovery timing register +2) * Tclk_pci		ns
t3	-IOWR data setup (min.)	(2 * setup timing register + 2 * command timing register +4) * Tclk_pci		ns
t4	-IOWR data hold (min.)	(2 * recovery timing register +4) * Tclk_pci		ns
t5	-IORD data setup (min.)	2 * Tpci_clk		ns
t6	-IORD data hold (min.)	0	—	ns
t7	Address valid to –IOIS16 assertion (max.)	—	90	ns
t8	Address valid to –IOIS16 released (max.)	—	60	ns
t9	-IORD/-IOWR to address valid hold	(2 * recovery timing register +4) * Tclk_pci		ns
tRD	Read data valid to IORDY active (min.) if IORDY initially low after tA	0	—	ns
tA	IORDY setup time	—	35-	ns
tB	IORDY pulse width (max.)	—	1250	ns
tC	IORDY assertion to release (max.)	—	5	ns

Table 31: True IDE PIO Mode Timing

USB-OTG Interface

Symbol	Spec ID Description	Min.	Max.	Unit
1	USB bit width[1]	83.3	667	ns
2	Signal falling time	4	20	ns
3	Signal rising time	4	20	ns

Table 32: USB Interface Timing

NOTE: Output timing is specified at a nominal 50 pF load.

[1] The USB bit width is defined in the USB config register (12 Mbit/s or 1.5 Mbit/s modes).

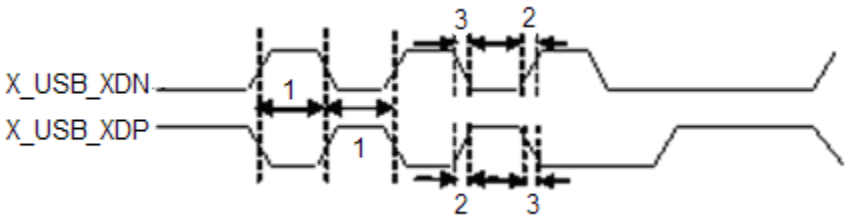


Figure 25: USB Interface Timing

SDIO AC Specifications

Parameter	Symbol	Min.	Max.	Unit
Clock frequency data transfer mode	Fpp	0	24	MHz
SD card input set-up time	Tisu	13	—	ns
SD card input hold time	Tihd	-12	—	ns
SD card output delay time during data transfer mode	Todly	-1	1	ns

Table 33: SD Card Bus Timing

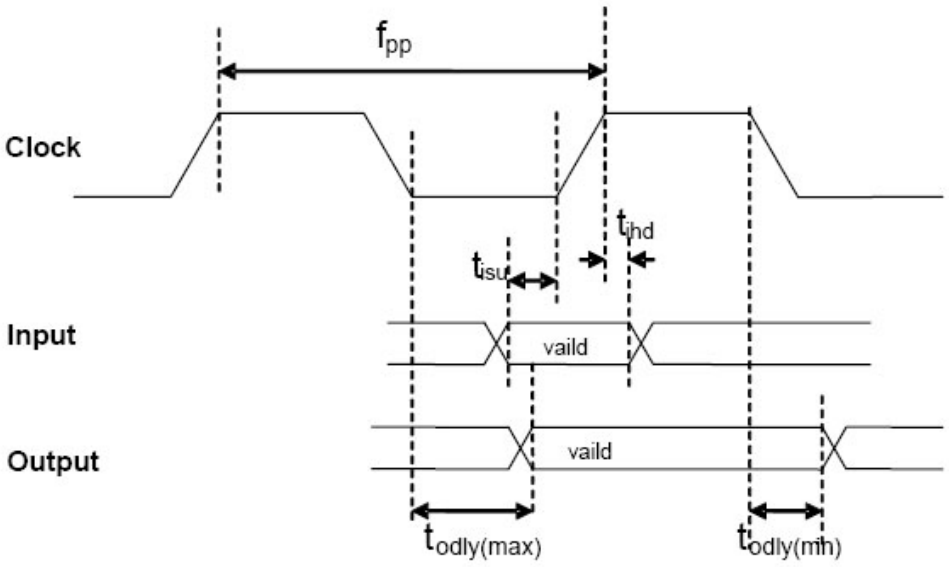


Figure 26: SD Bus Line Timing

NOTES:

- The clock delay register is set to 0x20. If it is changed, the timing will be different.
- The clock DELAY reg is set to 0x20, the result will be different.

Audio CODEC

Description	Symbol	Min.	Max.	Unit
SYNC signal output valid delay	Tsyn_od	—	14	ns
SYNC signal output hold time	Tsyn_hold	4	—	ns
AD_DATA signal set-up time	Tad_su	1.5	—	ns
AD_DATA signal hold time	Tad_hd	3.5	—	ns
DA_DATA output vaild delay	Tda_od	—	12	ns
DA_DATA output hold delay	Tda_hold	5	—	ns

Table 34: AC97 Bus Timing

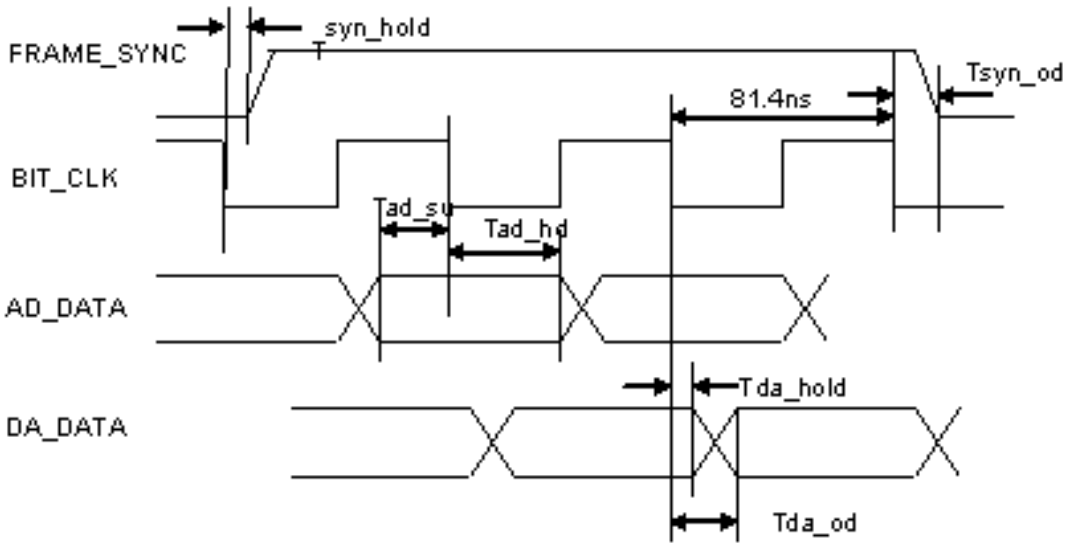


Figure 27: CODEC Interface Timing

JTAG Interface

Symbol	Spec ID Description	Min.	Max.	Unit
1	JTAG clock frequency	—	5	MHz
2	TRST/TMS/TDI data setup time	4	—	ns
3	TRST/TMS/TDI data holdup time	4	—	ns
4	TDO data output delay	—	15	ns

Table 35: JTAG Timing

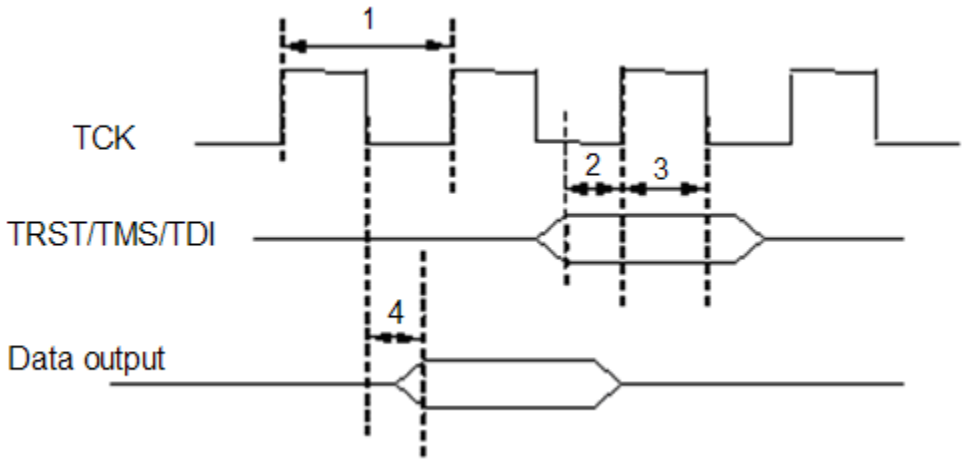


Figure 28: JTAG Interface Timing

Reliability Test Specifications

The reliability test specifications for SiRFatlasIII follow the JEDEC testing standards as part of the product qualification plan. The detailed testing items and conditions are listed in Table 36.

Test Item	Test Method	Test Condition	Sample Size (1 lot)	Criteria
HTOL	JEDEC 22-A108	125°C /1.1Vcc/1000hrs, read point: 168hrs, 500hrs, 1000hrs.	77	LTPD=3% (Acc/Rej=0/1)
ESD	JEDEC 22-A114/115	HBM(Human Body Mode): R=1.5kΩ/C=100pF MM (Machine Mode): R=0kΩ/C=200pF CDM (Charge Device Mode): +/-500V, 1000V	18 18 6	HBM≧+/-2KV MM≧+/-200V CDM≧+/-500V
Latch up	JEDEC 78	+(Inom+100mA)/-100mA /1.5X max. Vsupply	9	1.4X Inom
Pre-condition	JEDEC 22-A113	1. SAT, -65/150°C 5 cycle, bake@30°C /60%RH/192 hrs, IR*3, visual/ func./ SAT. 2. Reflow Peak@260 +0/-5°C	77	0/1
TCT	JEDEC 22-A104	-65°C ~+150°C /1000cycles/Pre-condition	77	LTPD=3% (Acc/Rej=0/1)

Table 36: Reliability Qualification Summary

IR Reflow Profile

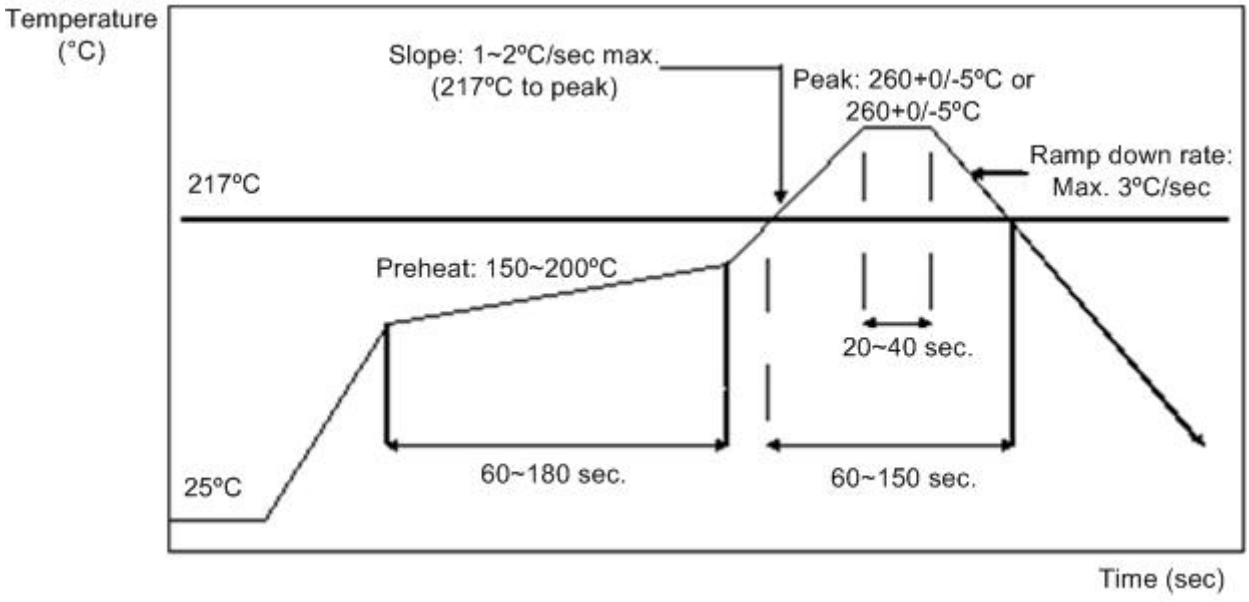


Figure 29: IR-Reflow Profile

PACKAGE AND PIN SPECIFICATION

AT640 Series Marking Code

AT640 Series Marking Code

Top Marking:

- Marking Type: Ink
- Marking Font: Arial
- Line 1 Logo: SiRF
- Line 2 Product Family: SiRFatlas
- Line 3 Part Number: AT64x
- Line 4 Control Code: XAC
- Line 5 Lot No.+ LF: xxxxxxx-xx-xLF
  LF stands for Lead Free.
- Line 6 Date Code: YYWW (Work order date) COO (Country of origin)
  Example: YY (Year 2007) → 07
  WW (Week 12) → 12
  → 0712

NOTES:

- AT642: 372MHz
- AT643: 396MHz

Mechanical Drawing of Package

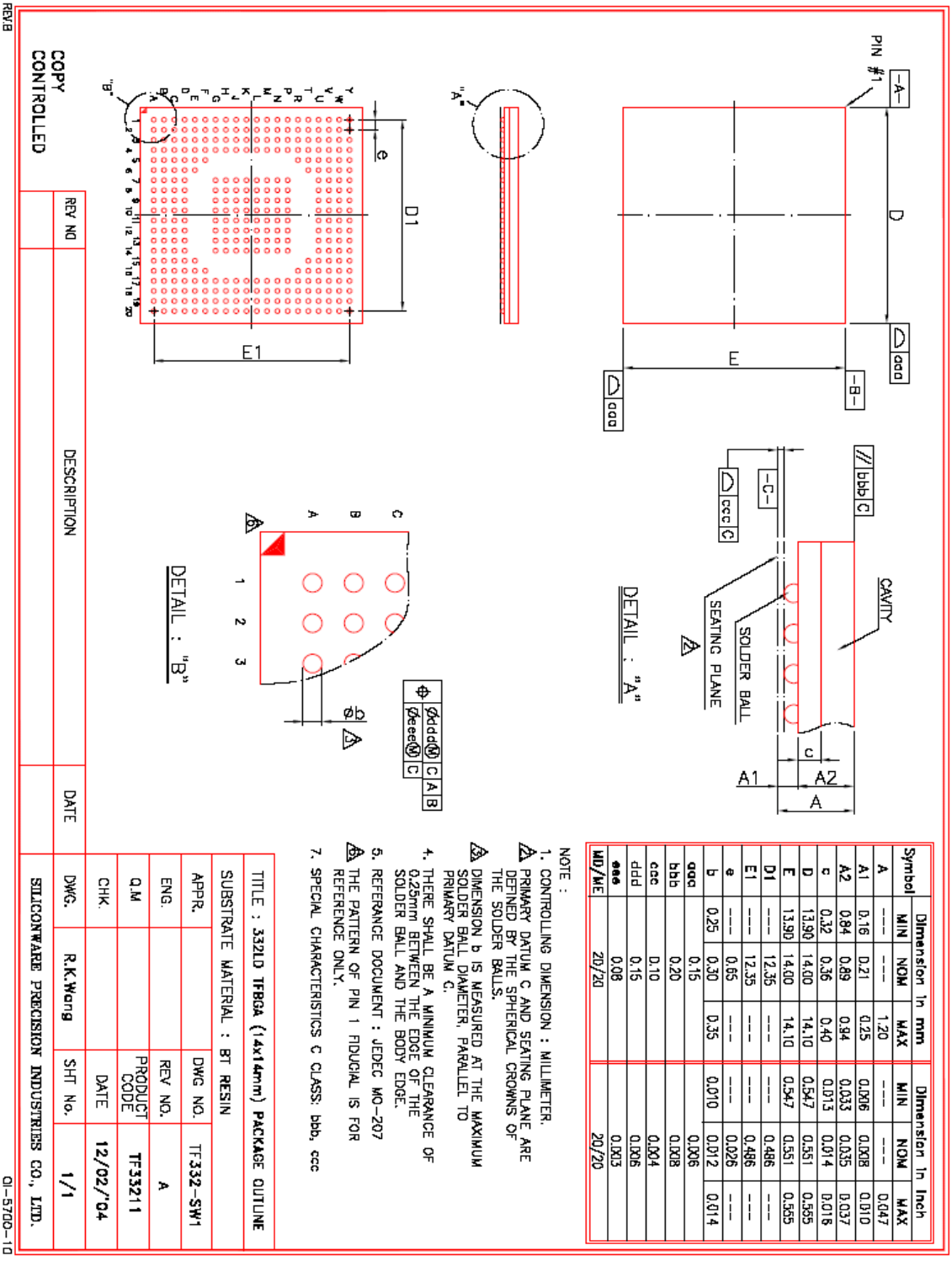


Figure 30: 14x14mm Package Mechanical Drawing

Symbol	Dimension in mm			Dimension in Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	0.047
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	16.90	17.00	17.10	0.665	0.669	0.673
E	16.90	17.00	17.10	0.665	0.669	0.673
D1	---	14.95	---	---	0.589	---
E1	---	14.95	---	---	0.589	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.10			0.004		
bbb	0.20			0.008		
ccc	0.12			0.005		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	24/24			24/24		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERANCE DOCUMENT : JEDEC MO-216.
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
7. SPECIAL CHARACTERISTICS C CLASS: bbb, ccc

Figure 31: TFBGA-477 Package (B)

Pin Definitions

This chapter describes the mechanical data and package information of SiRFatlasIII:

- A 14x14mm 332-ball TFBGA package with 0.65mm pitch.

Pinout

The following table lists the 14x14mm package pinout:

Pin Name	Pin #	Pin Type	Pin Description
x_pxd<15>	C15	PCOMB21X	Video input port data (DF_AD<13>)
x_pxd<14>	D15	PCOMB21X	Video input port data (DF_AD<12>)
x_pxd<13>	D16	PCOMB21X	Video input port data (DF_AD<11>)
x_pxd<12>	C16	PCOMB21X	Video input port data (DF_AD<10>)
x_pxd<11>	E15	PCOMB21X	Video input port data (DF_AD<9>)
x_pxd<10>	G14	PCOMB21X	Video input port data (DF_AD<8>)
x_pxd<9>	G13	PCOMB21X	Video input port data (DF_CLE)
x_pxd<8>	G12	PCOMB21X	Video input port data (DF_ALE)
x_pxd<7>	E6	PCOMB21X	Video input port data (DF_AD<7>)
x_pxd<6>	C6	PCOMB21X	Video input port data (DF_AD<6>)
x_pxd<5>	A5	PCOMB21X	Video input port data (DF_AD<5>)
x_pxd<4>	B4	PCOMB21X	Video Input Port Data Input (DF_AD<4>)
x_pxd<3>	A4	PCOMB21X	Video Input Port Data Input (DF_AD<3>)
x_pxd<2>	C3	PCOMB21X	Video Input Port Data Input (DF_AD<2>)
x_pxd<1>	B3	PCOMB21X	Video Input Port Data Input (DF_AD<1>)
x_pxd<0>	A3	PCOMB21X	Video Input Port Data Input (DF_AD<0>)
x_vsync	A2	PCOMB21X	Video Input Port Vertical Sync (DF_WE_B)
x_pxclk	B5	PCOMB21X	Video Input Port Pixel Clock (DF_RY_BY)
x_hsync	C4	PCOMB21X	Video Input Port Horizontal Sync (DF_RE_B)
x_fce_b<3>	C2	PDUW08DGZ	ROM/SRAM Chip Select (DF_CS_B<3>)
x_fce_b<2>	D2	PDUW08DGZ	ROM/SRAM Chip Select (DF_CS_B<2>)
x_fce_b<1>	E2	PDUW08DGZ	ROM/SRAM Chip Select (DF_CS_B<1>)
x_fce_b<0>	B2	PDUW08DGZ	ROM/SRAM Chip Select (DF_CS_B<0>)
x_pad_rq	A1	PDUW08DGZ	Companion Chip Pad Request
x_pad_gnt	D3	PDUW08DGZ	Companion Chip Pad Grant
x_sda	C1	PDUW04DGZ	I2C Data
x_scl	B1	PDUW04DGZ	I2C Clock
x_l_pclk	D1	PDU04SDGZ	LCD Pixel Clock

x_l_lck	E1	PDUW04DGZ	LCD Line Clock
x_l_fck	F2	PDUW04DGZ	LCD Frame Clock
x_l_bias	F1	PDUW04DGZ	LCD AC Bias
x_ldd<0>	E3	PDUW04DGZ	LCD Data Output
x_ldd<1>	C5	PDUW04DGZ	LCD Data Output
x_ldd<2>	D4	PDUW04DGZ	LCD Data Output
x_ldd<3>	F3	PDUW04DGZ	LCD Data Output
x_ldd<4>	G1	PDUW04DGZ	LCD Data Output
x_ldd<5>	G2	PDUW04DGZ	LCD Data Output
x_ldd<6>	E4	PDUW04DGZ	LCD Data Output
x_ldd<7>	H1	PDUW04DGZ	LCD Data Output
x_gpio<8>	D5	PDUW04DGZ	GPIO (LDD<8>) (General Purpose IO)
x_gpio<9>	D6	PDUW04DGZ	GPIO (LDD<9>)
x_gpio<10>	H2	PDUW04DGZ	GPIO (LDD<10>)
x_gpio<11>	J1	PDUW04DGZ	GPIO (LDD<1>)
x_gpio<12>	G3	PDUW04DGZ	GPIO (LDD<12>)
x_gpio<13>	F4	PDUW04DGZ	GPIO (LDD<13>)
x_gpio<14>	G4	PDUW04DGZ	GPIO (LDD<14>)
x_gpio<15>	E5	PDUW04DGZ	GPIO (LDD<15>)
x_rf_datain<1>	J2	PDUW04DGZ	GPS RF Data Input (SGN)
x_rf_datain<0>	H3	PDUW04DGZ	GPS RF Data Input (MAG)
x_sample_clk	G9	PDUW04DGZ	GPS Sample Clock
x_rf_clk	F5	PDU04SDGZ	GPS RF Clock
x_usb_xdp	K1	PUSBF11OTG	USB Pad (Positive)
x_usb_xdn	L1	PUSBF11OTG	USB Pad (Negative)
x_usb_vdda	G8	PUSBF11OTG	USB Analog Power (3.3V)
x_usb_vbus	K2	PUSBF11OTG	USB VBUS
x_usb_vssa	J3	PUSBF11OTG	USB Analog Ground
x_usb_pddm	H4	PUSBF11OTG	USB DM Pull-down
x_usb_pudp	J4	PUSBF11OTG	USB DP Pull-up
x_usb_pddp	M1	PUSBF11OTG	USB DP Pull-down
x_usb_vddl	L2	PUSBF11OTG	USB Digital Power (1.2V)
x_usb_vsdl	K3	PUSBF11OTG	USB Digital Ground
x_usb_id	K4	PUSBF11OTG	USB ID
x_usb_drvvbusc	L3	PUSBF11OTG	USB Drive VBUS Control
x_gpio<23>	M2	PDUW04DGZ	GPIO (RTS0/DBGACK)

x_gpio<22>	N1	PDUW04DGZ	GPIO (CTS0/DBGRQ)
x_gpio<21>	G7	PDUW04DGZ	GPIO (RI0/RTCK)
x_txd<0>	H7	PDUW04DGZ	UART0 Transmit Data
x_rxd<0>	M3	PDUW04DGZ	UART0 Receive Data
x_sclk<1>	N2	PDU04SDGZ	USP1 Clock (BIT_CLK)
x_txd<1>	L4	PDUW04DGZ	USP1 Transmit Data (DA_DATA)
x_rxd<1>	M4	PDUW04DGZ	USP1 Receive Data (AD_DATA)
x_tfs<1>	P1	PDUW04DGZ	USP1 Transmit Frame Sync (FRAME_SYNC)
x_rfs<1>	N3	PDUW04DGZ	USP1 Receive Frame Sync
x_scan_en	P2	PDDDGZ	ATPG Shift Enable
x_sclk<2>	J7	PDU04SDGZ	USP2 Clock (TRACECLK)
x_txd<2>	R1	PDUW04DGZ	USP2 Transmit Data (TRACESYNC)
x_rxd<2>	P3	PDUW04DGZ	USP2 Receive Data (PIPESTAT<2>)
x_tfs<2>	R2	PDUW04DGZ	USP2 Transmit Frame Sync (PIPESTAT<1>/TXD<6>)
x_rfs<2>	M7	PDUW04DGZ	USP2 Receive Frame Sync (PIPESTAT<0>/RXD<6>)
x_sclk<3>	N4	PDU04SDGZ	USP3 Clock
x_txd<3>	T1	PDUW04DGZ	USP3 Transmit Data
x_rxd<3>	T2	PDUW04DGZ	USP3 Receive Data
x_tfs<3>	P4	PDUW04DGZ	USP3 Transmit Frame Sync (TXD<7>)
x_rfs<3>	R3	PDUW04DGZ	USP3 Receive Frame Sync (RXD<7>)
x_gpio<20>	T3	PDUW04DGZ	GPIO (TCK)
x_gpio<19>	R4	PDUW04DGZ	GPIO (nTRST)
x_gpio<18>	T5	PDUW04DGZ	GPIO (TMS/DCD0)
x_gpio<17>	T4	PDUW04DGZ	GPIO (TDO/DTR0)
x_gpio<16>	U4	PDUW04DGZ	GPIO (TDI/DSR0)
x_can_txd<0>	N7	PDUW04DGZ	CAN Bus Port 0 Transmit Data
x_can_rxd<0>	U5	PDUW04DGZ	CAN Bus Port 0 Receive Data
x_can_txd<1>	R5	PDUW04DGZ	CAN Bus Port 1 Transmit Data
x_can_rxd<1>	V4	PDUW04DGZ	CAN Bus Port 1 Receive Data
AVDDIO	U3	-	PLL IO Power (3.3V) (VDD_PHA)
AHVDD	U1	-	PLL1 Analog Power (3.3V) (VDD_PHA)
AHVDDG	U2	-	PLL1 Analog Power (3.3V) (VDD_PHA)
AVSSIO	V3	-	PLL1 IO Ground
AHVSS	V1	-	PLL1 Analog Ground
AHVSSG	V2	-	PLL1 Analog Ground

DVDD1	W2	-	PLL1 Digital Power (1.2V) (VDD_PLD)
DVDD2	Y2	-	PLL2 Digital Power (1.2V) (VDD_PLD)
DVSS1	W3	-	PLL1 Digital Ground
DVSS2	Y3	-	PLL2 Digital Ground
AVDD	W1	-	PLL2 Analog Power (1.2V) (VDD_PLA)
AVSS	Y1	-	PLl2 Analog Ground
XVSSIO	W5	-	Oscillator IO Ground
x_xinw	W4	PDXO01M	32.769 KHz Oscillator Input
x_xoutw	Y4	PDXO01M	32.769 KHz Oscillator Output
XVDDIO	Y5	-	Oscillator IO Power (3.3V)
x_vdd_fault	V5	PDD04DGZ	VDD Fault
x_batt_fault	P12	PDD04DGZ	Battery Fault
x_pwr_en	V6	PDO04CDG	Power Enable
x_reset_b	P7	PDUSDGZ	Reset Input
x_xin	W6	PDXOE3DG	Main Oscillator Input
x_xout	Y6	PDXOE3DG	Main Oscillator Output
x_pc_ce_b<1>	U6	PDUW08DGZ	PCMCIA Card Enable 1
x_pc_ce_b<0>	P8	PDUW08DGZ	PCMCIA Card Enable 0
x_pc_wait_b	T6	PDUW08DGZ	PCMCIA Wait
x_pc_iois16_b	P13	PDUW08DGZ	PCMCIA IO IS16-bit
x_fa<20>	W7	PDUW08DGZ	ROM/SRAM Address (DF_ALE/JTAG_MODE<0>)
x_fa<21>	Y7	PDUW08DGZ	ROM/SRAM Address (DF_CLE/JTAG_MODE<1>)
x_fa<22>	V7	PDUW08DGZ	ROM/SRAM Address (PC_IORD_B/IDE_IOR_B)
x_fa<23>	U7	PDUW08DGZ	ROM/SRAM Address(PC_IOWE_B/IDE_IOW_B)
x_fa<24>	P9	PDUW08DGZ	ROM/SRAM Address (PC_WE_B)
x_fa<25>	Y8	PDUW08DGZ	ROM/SRAM Address (PC_OE_B)
x_cko_0	W8	PDO08CDG	Clock Output
x_foe_b	V8	PDUW08DGZ	ROM/SRAM Read Enable (DF_RD_B)
x_fwe_b	U8	PDUW08DGZ	ROM/SRAM Write Enable (DF_WE_B)
x_fbe<3>	V9	PDUW08DGZ	ROM/SRAM Byte Enable
x_fbe<2>	Y9	PDUW08DGZ	ROM/SRAM Byte Enable
x_fbe<1>	W9	PDUW08DGZ	ROM/SRAM Byte Enable
x_fbe<0>	U9	PDUW08DGZ	ROM/SRAM Byte Enable
x_frdy_b	U10	PDUW08DGZ	ROM/SRAM Ready/Busy (IDE_IORDY_B)

x_fd<0>	V10	PDUW08DGZ	ROM/SRAM Data (PD<0>/DF_AD<0>/IDE_D<0>)
x_fd<1>	W10	PDUW08DGZ	ROM/SRAM Data (PD<1>/DF_AD<1>/IDE_D<1>)
x_fd<2>	Y10	PDUW08DGZ	ROM/SRAM Data (PD<2>/DF_AD<2>/IDE_D<2>)
x_fd<3>	V11	PDUW08DGZ	ROM/SRAM Data (PD<3>/DF_AD<3>/IDE_D<3>)
x_fd<4>	U11	PDUW08DGZ	ROM/SRAM Data (PD<4>/DF_AD<4>/IDE_D<4>)
x_fd<5>	N14	PDUW08DGZ	ROM/SRAM Data (PD<5>/DF_AD<5>/IDE_D<5>)
x_fd<6>	W11	PDUW08DGZ	ROM/SRAM Data (PD<6>/DF_AD<6>/IDE_D<6>)
x_fd<7>	V12	PDUW08DGZ	ROM/SRAM Data (PD<7>/DF_AD<7>/IDE_D<7>)
x_fd<8>	Y11	PDUW08DGZ	ROM/SRAM Data (PD<8>/ DF_AD<8>/IDE_D<8>)
x_fd<9>	W12	PDUW08DGZ	ROM/SRAM Data (PD<9>/ DF_AD<9>/IDE_D<9>)
x_fd<10>	V13	PDUW08DGZ	ROM/SRAM Data (PD<10>/DF_AD<10>/IDE_D<10>)
x_fd<11>	P14	PDUW08DGZ	ROM/SRAM Data (PD<11>/DF_AD<11>/IDE_D<11>)
x_fd<12>	U14	PDUW08DGZ	ROM/SRAM Data (PD<12>/DF_AD<12>/IDE_D<12>)
x_fd<13>	U12	PDUW08DGZ	ROM/SRAM Data (PD<13>/DF_AD<13>/IDE_D<13>)
x_fd<14>	V14	PDUW08DGZ	ROM/SRAM Data (PD<14>/DF_AD<14>/IDE_D<14>)
x_fd<15>	Y12	PDUW08DGZ	ROM/SRAM Data (PD<15>/DF_AD<15>/IDE_D<15>)
x_fd<16>	W13	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<0>)
x_fd<17>	U15	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<1>)
x_fd<18>	R17	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<2>)
x_fd<19>	T17	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<3>)
x_fd<20>	Y13	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<4>)
x_fd<21>	U13	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<5>)
x_fd<22>	W14	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<6>)
x_fd<23>	V15	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<7>)
x_fd<24>	U16	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<8>)
x_fd<25>	Y14	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<9>)
x_fd<26>	T18	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<10>)
x_fd<27>	M14	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<11>)

x_fd<28>	U17	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<12>)
x_fd<29>	Y15	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<13>)
x_fd<30>	V16	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<14>)
x_fd<31>	W15	PDUW08DGZ	ROM/SRAM Data (TRACEPKT<15>)
x_fa<0>	Y16	PDUW08DGZ	ROM/SRAM Address (PA<0>/IDE_A<0>)
x_fa<1>	T15	PDUW08DGZ	ROM/SRAM Address (PA<1>/IDE_A<1>)
x_fa<2>	T19	PDUW08DGZ	ROM/SRAM address (PA<2>/ IDE_A<2>)
x_fa<3>	J14	PDUW08DGZ	ROM/SRAM address (PA<3>)
x_fa<4>	U18	PDUW08DGZ	ROM/SRAM address (PA<4>)
x_fa<5>	Y17	PDUW08DGZ	ROM/SRAM address (PA<5>)
x_fa<6>	W16	PDUW08DGZ	ROM/SRAM address (PA<6>)
x_fa<7>	Y18	PDUW08DGZ	ROM/SRAM address (PA<7>)
x_fa<8>	V17	PDUW08DGZ	ROM/SRAM address (PA<8>)
x_fa<9>	H14	PDUW08DGZ	ROM/SRAM address (PA<9>)
x_fa<10>	Y20	PDUW08DGZ	ROM/SRAM address (PA<10>)
x_fa<11>	Y19	PDUW08DGZ	ROM/SRAM address (PA<11>)
x_fa<12>	U19	PDUW08DGZ	ROM/SRAM address (PA<12>)
x_fa<13>	T20	PDUW08DGZ	ROM/SRAM address (PA<13>/ PAD_MODE<0>)
x_fa<14>	W18	PDUW08DGZ	ROM/SRAM address (PA<14>/ PAD_MODE<1>)
x_fa<15>	W17	PDUW08DGZ	ROM/SRAM Address (PA<15>/ NAND_MODE)
x_fa<16>	V18	PDUW08DGZ	ROM/SRAM address (PA<16>/ NAND_BOOT)
x_fa<17>	W19	PDUW08DGZ	ROM/SRAM address (PA<17>/BOOT_IS16)
x_fa<18>	W20	PDUW08DGZ	ROM/SRAM address (PA<18>/TEST_MODE<0>)
x_fa<19>	T16	PDUW08DGZ	ROM/SRAM address (PA<19>/TEST_MODE<1>)
x_pc_ireq_b	V20	PDUW08DGZ	PCMCIA interrupt request
x_pc_inpack_b	R18	PDUW08DGZ	PCMCIA input acknowledge
x_scan_test	V19	PDDDGZ	ATPG mode
x_pc_vs<2>	R16	PDUW08DGZ	PCMCIA voltage sense
x_cko_1	U20	PDO08CDG	Clock output
x_pc_vs<1>	R20	PDUW08DGZ	PCMCIA voltage sense
x_pc_cd_b<1>	R19	PDUW08DGZ	PCMCIA card detect
x_pc_cd_b<0>	P17	PDUW08DGZ	PCMCIA card detect
x_pc_stschg	N17	PDUW08DGZ	PCMCIA status change

x_pc_spkr_b	P20	PDUW08DGZ	PCMCIA speaker
x_pc_reset	P18	PDUW08DGZ	PCMCIA reset
x_pc_reg_b	M17	PDUW08DGZ	PCMCIA register enable
x_sclk<4>	P19	PDU04SDGZ	USP4 clock (SD_DAT<3>/PA<23>)
x_txd<4>	N18	PDUW04DGZ	USP4 transmit data
x_rxd<4>	N20	PDUW04DGZ	USP4 receive data
x_tfs<4>	L17	PDUW04DGZ	USP4 transmit frame sync (SD_DAT<2>/PA<22>)
x_rfs<4>	M18	PDUW04DGZ	USP4 receive frame sync (SD_DAT<1>/PA<21>)
x_sclk<5>	K17	PDU04SDGZ	USP5 clock (SD_CLK/PA<25>)
x_txd<5>	N19	PDUW04DGZ	USP5 transmit data
x_rxd<5>	M20	PDUW04DGZ	USP5 receive data
x_tfs<5>	L18	PDUW04DGZ	USP5 transmit frame sync (SD_CMD/PA<24>)
x_rfs<5>	J17	PDUW04DGZ	USP5 receive frame sync (SD_DAT<0>/PA<20>)
x_df_ry_by	L20	PDUW08DGZ	NAND flash read/busy (NAND_SEL)
x_ide_cs_b<1>	F16	PDUW08DGZ	IDE chip select
x_ide_cs_b<0>	M19	PDUW08DGZ	IDE chip select
x_ide_dreq	K18	PDUW08DGZ	IDE data request
x_ide_dack	H17	PDUW08DGZ	IDE data acknowledge
x_ide_irq	K20	PDUW08DGZ	IDE interrupt request
x_gpio<7>	G17	PDUW04DGZ	GPIO (PWM<3>)
x_gpio<6>	L19	PDUW04DGZ	GPIO (PWM<2>)
x_gpio<5>	J18	PDUW04DGZ	GPIO (PWM<1>)
x_gpio<4>	E16	PDUW04DGZ	GPIO (PWM<0>)
x_gpio<3>	J20	PDUW04DGZ	GPIO
x_gpio<2>	H18	PDUW04DGZ	GPIO
x_gpio<1>	K19	PDUW04DGZ	GPIO
x_gpio<0>	F17	PDUW04DGZ	GPIO
x_gpio<24>	J19	PDUW04DGZ	GPIO (LDD<16>)
x_gpio<25>	E17	PDUW04DGZ	GPIO (LDD<17>)
x_gpio<26>	G18	PCOMB21X	GPIO (DF_AD<15>)
x_gpio<27>	H20	PCOMB21X	GPIO (DF_AD<14>)
x_mcke	G20	PCOMB21X	Memory clock enable
x_mcs_b<1>	F20	PCOMB21X	Memory chip select
x_mcs_b<0>	H19	PCOMB21X	Memory chip select
x_mdqm<3>	A17	PCOMB21X	Memory data mask
x_mdqm<2>	B17	PCOMB21X	Memory data mask

x_mdqm<1>	C17	PCOMB21X	Memory data mask
x_mdqm<0>	D17	PCOMB21X	Memory data mask
x_ma<12>	F18	PCOMB21X	Memory address
x_ma<11>	E20	PCOMB21X	Memory address
x_ma<10>	G19	PCOMB21X	Memory address
x_ma<9>	E18	PCOMB21X	Memory address
x_ma<8>	D20	PCOMB21X	Memory address
x_ma<7>	C20	PCOMB21X	Memory address
x_ma<6>	B20	PCOMB21X	Memory address
x_ma<5>	F19	PCOMB21X	Memory address
x_ma<4>	A20	PCOMB21X	Memory address
x_ma<3>	E19	PCOMB21X	Memory address
x_ma<2>	D19	PCOMB21X	Memory address
x_ma<1>	C19	PCOMB21X	Memory address
x_ma<0>	B19	PCOMB21X	Memory address
x_m_ba<1>	A18	PCOMB21X	Memory bank address
x_m_ba<0>	A19	PCOMB21X	Memory bank address
x_mwe_b	B18	PCOMB21X	Memory write enable
x_mras_b	D18	PCOMB21X	Memory row address strobe
x_mcas_b	C18	PCOMB21X	Memory column address strobe
x_mclk_o	A11	PDIFF21X	Memory clock output (+)
x_mclkb_o	B11	PDIFF21X	Memory clock output (-)
x_mdqs<3>	A16	PCOMB21X	Memory data strobe
x_mdqs<2>	B16	PCOMB21X	Memory data strobe
x_mdqs<1>	B10	PCOMB21X	Memory data strobe
x_mdqs<0>	A10	PCOMB21X	Memory data strobe
x_md<31>	B15	PCOMB21X	Memory data
x_md<30>	A15	PCOMB21X	Memory data
x_md<29>	B14	PCOMB21X	Memory data
x_md<28>	A14	PCOMB21X	Memory data
x_md<27>	B13	PCOMB21X	Memory data
x_md<26>	A13	PCOMB21X	Memory data
x_md<25>	B12	PCOMB21X	Memory data
x_md<24>	A12	PCOMB21X	Memory data
x_md<23>	C11	PCOMB21X	Memory data
x_md<22>	D11	PCOMB21X	Memory data

x_md<21>	C12	PCOMB21X	Memory data
x_md<20>	D12	PCOMB21X	Memory data
x_md<19>	C13	PCOMB21X	Memory data
x_md<18>	D13	PCOMB21X	Memory data
x_md<17>	C14	PCOMB21X	Memory data
x_md<16>	D14	PCOMB21X	Memory data
x_md<15>	D7	PCOMB21X	Memory data
x_md<14>	C7	PCOMB21X	Memory data
x_md<13>	D8	PCOMB21X	Memory data
x_md<12>	C8	PCOMB21X	Memory data
x_md<11>	D9	PCOMB21X	Memory data
x_md<10>	C9	PCOMB21X	Memory data
x_md<9>	D10	PCOMB21X	Memory data
x_md<8>	C10	PCOMB21X	Memory data
x_md<7>	A9	PCOMB21X	Memory data
x_md<6>	B9	PCOMB21X	Memory data
x_md<5>	A8	PCOMB21X	Memory data
x_md<4>	B8	PCOMB21X	Memory data
x_md<3>	A7	PCOMB21X	Memory data
x_md<2>	B7	PCOMB21X	Memory data
x_md<1>	A6	PCOMB21X	Memory data
x_md<0>	B6	PCOMB21X	Memory data
VDDIO	J8, N8, N11, N12, P10		Digital IO power
VDDPDN	K9, K13, L9, L13, M9, M13		Digital core power
VDDPRE	K7, K14, L7, L14, M8, N9		Digital core power
VDHPSSTL	J10, J11, J12, K10, K11, K12		SSTL IO power(VDD_MEM)
VREFSSTL	H8, J9		SSTL reference voltage(Vref)
VSS	L10, L11, L12, M10, M11, M12		Digital core ground
VSSIO	K8, L8, N10, N13, P11		Digital IO ground
VSSPSSTL	G10, G11, H9, H12, H13, J13		SSTL IO ground
VSSRSSTL	H10, H11		SSTL IO ground

Table 37: SiRFatlasIII 14x14mm Package Pinout

Pin Type Description

Refer to the following table for the pin type descriptions.

Pin Type	Description
PCOMB21X	3-state output 1.8/2.5/3.3V LVTTL and SSTL2 buffer pad
PDIFF21X	3-state differential output 1.8/2.5/3.3V LVTTL and SSTL2 buffer pad
PDDDGZ	Input pad with pull-down, 5V-tolerance
PDO04CDG	CMOS output pad. 4mA driving strength
PDO08CDG	CMOS output pad. 8mA driving strength
PDUSDGZ	Schmitt triggered input with pull-up. 5V-tolerance
PDD04DGZ	CMOS 3-state output pad with input and pull-down, 5V-tolerance, 4mA driving strength
PDU04SDGZ	CMOS 3-state output pad with Schmitt trigger input and pull-up, 5V-tolerance, 4 mA driving strength
PDUW04DGZ	3-state output pad with input and enable controlled pull-up, 5V-tolerance, 4 mA driving strength
PDUW08DGZ	3-state output pad with input and enable controlled pull-up, 5V-tolerance, 8 mA driving strength
PDXOE3DG	High-frequency oscillator pad
PDXO01M	Low-frequency oscillator pad
PUSBF11OTG	Full-speed USB OTG transceiver pad

Table 38: Pin Type Description

ADDITIONAL INFORMATION

Additional technical information including Application Notes are available through the Customer Zone on the SiRF web site at http://www.sirf.com

ORDERING INFORMATION

Part Number	Package	Frequency	Dimension (mm)	Packing
AT642D-XAC	TFBGA-332LD	372MHz	14×14	Tray
AT643D-XAC	TFBGA-332LD	396MHz	14×14	Tray

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