1. Description

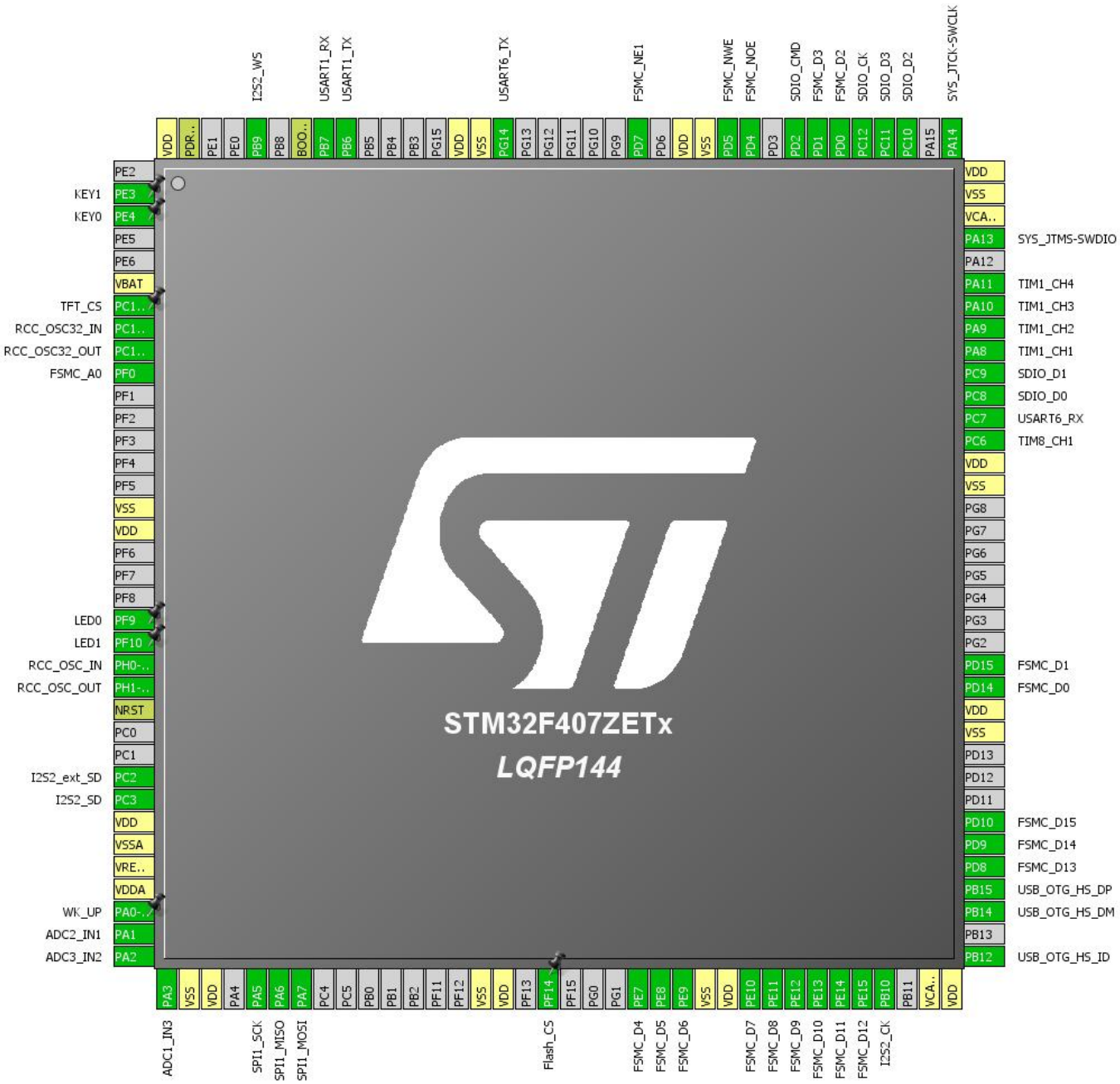
1.1. Project

Project Name	F407zetSD_DMA
Board Name	F407zetSD_DMA
Generated with:	STM32CubeMX 4.22.0
Date	05/17/2018

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407ZETx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

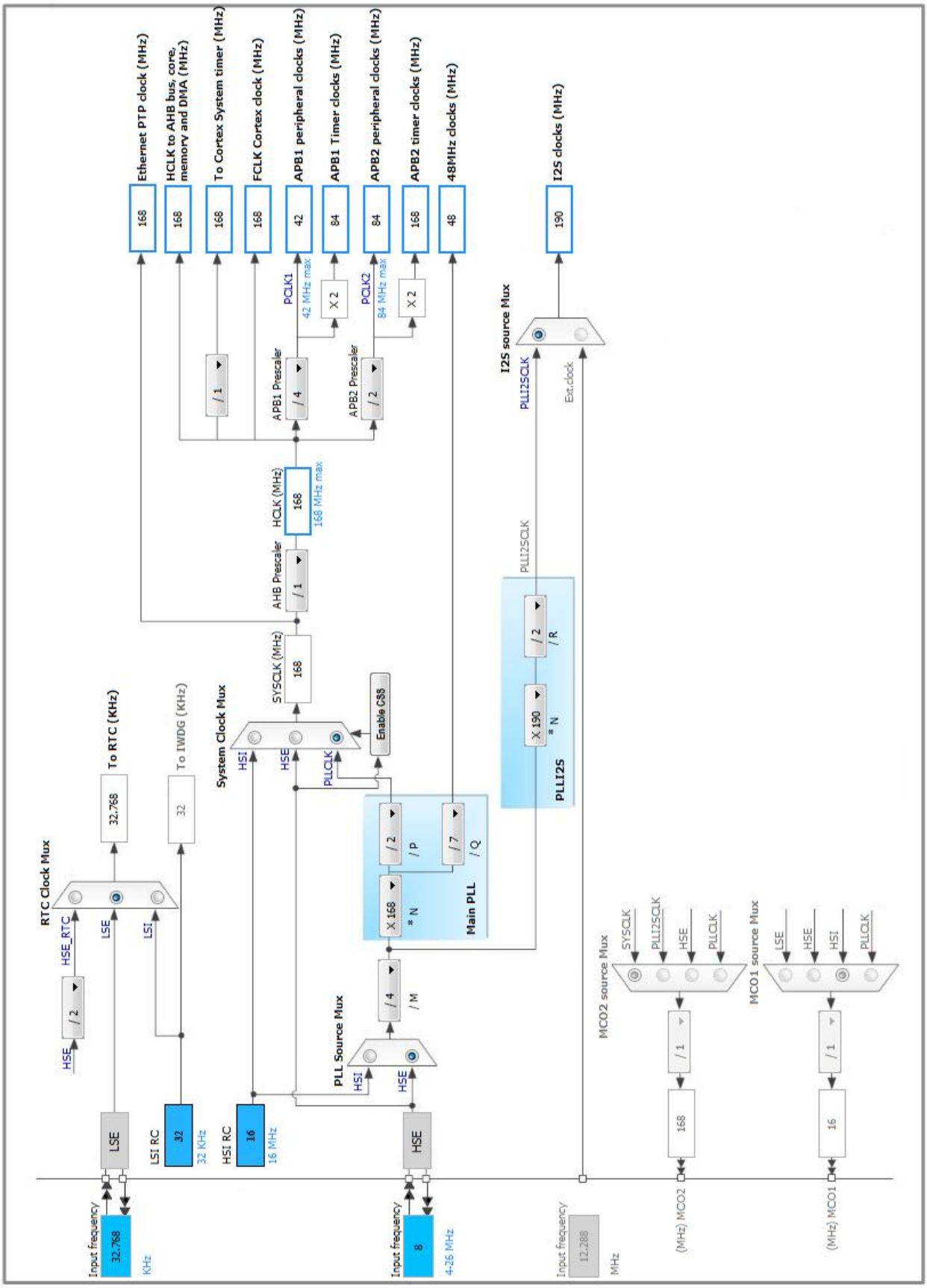
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
2	PE3 *	I/O	GPIO_Input	KEY1
3	PE4 *	I/O	GPIO_Input	KEY0
6	VBAT	Power		
7	PC13-ANTI_TAMP *	I/O	GPIO_Output	TFT_CS
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	PF0	I/O	FSMC_A0	
16	VSS	Power		
17	VDD	Power		
21	PF9 *	I/O	GPIO_Output	LED0
22	PF10 *	I/O	GPIO_Output	LED1
23	PH0-OSC_IN	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
28	PC2	I/O	I2S2_ext_SD	
29	PC3	I/O	I2S2_SD	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0-WKUP *	I/O	GPIO_Input	WK_UP
35	PA1	I/O	ADC2_IN1	
36	PA2	I/O	ADC3_IN2	
37	PA3	I/O	ADC1_IN3	
38	VSS	Power		
39	VDD	Power		
41	PA5	I/O	SPI1_SCK	
42	PA6	I/O	SPI1_MISO	
43	PA7	I/O	SPI1_MOSI	
51	VSS	Power		
52	VDD	Power		
54	PF14 *	I/O	GPIO_Output	Flash_CS
58	PE7	I/O	FSMC_D4	
59	PE8	I/O	FSMC_D5	
60	PE9	I/O	FSMC_D6	
61	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
62	VDD	Power		
63	PE10	I/O	FSMC_D7	
64	PE11	I/O	FSMC_D8	
65	PE12	I/O	FSMC_D9	
66	PE13	I/O	FSMC_D10	
67	PE14	I/O	FSMC_D11	
68	PE15	I/O	FSMC_D12	
69	PB10	I/O	I2S2_CK	
71	VCAP_1	Power		
72	VDD	Power		
73	PB12	I/O	USB_OTG_HS_ID	
75	PB14	I/O	USB_OTG_HS_DM	
76	PB15	I/O	USB_OTG_HS_DP	
77	PD8	I/O	FSMC_D13	
78	PD9	I/O	FSMC_D14	
79	PD10	I/O	FSMC_D15	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FSMC_D0	
86	PD15	I/O	FSMC_D1	
94	VSS	Power		
95	VDD	Power		
96	PC6	I/O	TIM8_CH1	
97	PC7	I/O	USART6_RX	
98	PC8	I/O	SDIO_D0	
99	PC9	I/O	SDIO_D1	
100	PA8	I/O	TIM1_CH1	
101	PA9	I/O	TIM1_CH2	
102	PA10	I/O	TIM1_CH3	
103	PA11	I/O	TIM1_CH4	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
111	PC10	I/O	SDIO_D2	
112	PC11	I/O	SDIO_D3	
113	PC12	I/O	SDIO_CK	
114	PD0	I/O	FSMC_D2	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
115	PD1	I/O	FSMC_D3	
116	PD2	I/O	SDIO_CMD	
118	PD4	I/O	FSMC_NOE	
119	PD5	I/O	FSMC_NWE	
120	VSS	Power		
121	VDD	Power		
123	PD7	I/O	FSMC_NE1	
129	PG14	I/O	USART6_TX	
130	VSS	Power		
131	VDD	Power		
136	PB6	I/O	USART1_TX	
137	PB7	I/O	USART1_RX	
138	BOOT0	Boot		
140	PB9	I/O	I2S2_WS	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN3

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 3
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN1

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. ADC3

mode: IN2

5.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 2
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.4. FSMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: LCD Interface

LCD Register Select: A0

Data: 16 bits

5.4.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	LCD Interface
Bank	Bank 1 NOR/PSRAM 1
Write operation	Enabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	15
Data setup time in HCLK clock cycles	255
Bus turn around time in HCLK clock cycles	15

5.5. I2S2

Mode: Full-Duplex Master

5.5.1. Parameter Settings:

Generic Parameters:

Transmission Mode	Mode Master Transmit
Communication Standard	I2S Philips
Data and Frame Format	16 Bits Data on 16 Bits Frame
Selected Audio Frequency	**48 KHz ***
Real Audio Frequency	**47.883 KHz ***
Error between Selected and Real	**-0.24 % ***

Clock Parameters:

Clock Source	I2S PLL Clock
Clock Polarity	Low

5.6. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.7. RTC

mode: Activate Clock Source

mode: Activate Calendar

Alarm A: Internal Alarm

Alarm B: Internal Alarm

5.7.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

Alarm A:

Hours	0
Minutes	0
Seconds	0
Sub Seconds	0
Alarm Mask Date Week day	Disable
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	Date
Alarm Date	1

Alarm B:

Hours	0
Minutes	0
Seconds	0
Sub Seconds	0
Alarm Mask Date Week day	Disable
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	Date
Alarm Date	1

5.8. SDIO

Mode: SD 4 bits Wide bus

5.8.1. Parameter Settings:

SDIO parameters:	
SDIOCLK clock divide factor	0

5.9. SPI1

Mode: Full-Duplex Master

5.9.1. Parameter Settings:

Basic Parameters:	
Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First
Clock Parameters:	
Prescaler (for Baud Rate)	2
Baud Rate	**42.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge
Advanced Parameters:	
CRC Calculation	Disabled
NSS Signal Type	Software

5.10. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.11. TIM1

Clock Source : Internal Clock
Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: Output Compare CH4

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0

Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 4:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

5.12. TIM2

Clock Source : Internal Clock

mode: One Pulse Mode

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.13. TIM6

mode: Activated

5.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.14. TIM8

Clock Source : Internal Clock

Channel1: Input Capture direct mode

5.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.15. TIM14

mode: Activated

5.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

5.16. USART1

Mode: Asynchronous

5.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.17. USART6

Mode: Asynchronous

5.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.18. USB_OTG_HS

Internal FS Phy: OTG/Dual_Role_Device

5.19. FATFS

mode: SD Card

5.19.1. Set Defines:

Version:

FATFS version	R0.11

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Multilingual Latin 1 (OEM)
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
NORTC_YEAR (Year for timestamp)	2015
NORTC_MON (Month for timestamp)	6
NORTC_MDAY (Day for timestamp)	4
WORD_ACCESS (Platform dependent access option)	Byte access
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	2

5.19.2. IPs instances:

SDIO/SDMMC:

SDIO instance	SDIO

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA1	ADC2_IN1	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PA2	ADC3_IN2	Analog mode	No pull-up and no pull-down	n/a	
FSMC	PF0	FSMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FSMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FSMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FSMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FSMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FSMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FSMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FSMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FSMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FSMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FSMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FSMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FSMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FSMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FSMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FSMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FSMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD4	FSMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD5	FSMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD7	FSMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2S2	PC2	I2S2_ext_SD	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	
	PC3	I2S2_SD	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	
	PB10	I2S2_CK	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	
	PB9	I2S2_WS	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDIO_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDIO_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDIO_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB6	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PB7	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART6	PC7	USART6_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PG14	USART6_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
USB_OTG_HS	PB12	USB_OTG_HS_ID	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB14	USB_OTG_HS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB15	USB_OTG_HS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PE3	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE4	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY0
	PC13-ANTI_TAMP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TFT_CS
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED0
	PF10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PA0-WKUP	GPIO_Input	Input mode	**Pull-down ***	n/a	WK_UP
	PF14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Flash_CS

6.2. DMA configuration

DMA request	Stream	Direction	Priority
I2S2_EXT_RX	DMA1_Stream3	Peripheral To Memory	Low
SDIO_RX	DMA2_Stream6	Peripheral To Memory	**High ***
SDIO_TX	DMA2_Stream3	Memory To Peripheral	Low
USART1_RX	DMA2_Stream5	Peripheral To Memory	Low
USART1_TX	DMA2_Stream7	Memory To Peripheral	Low
USART6_RX	DMA2_Stream1	Peripheral To Memory	Low
ADC1	DMA2_Stream4	Peripheral To Memory	Low
ADC2	DMA2_Stream2	Peripheral To Memory	Low
ADC3	DMA2_Stream0	Peripheral To Memory	Low
TIM6_UP	DMA1_Stream1	Peripheral To Memory	Low

I2S2_EXT_RX: DMA1_Stream3 DMA request Settings:

Mode:	**Circular ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Half Word ***
Memory Data Width:	**Half Word ***
Peripheral Burst Size:	Single
Memory Burst Size:	Single

SDIO_RX: DMA2_Stream6 DMA request Settings:

Mode:	**Peripheral Flow Control ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	Word
Peripheral Burst Size:	**4 Increment ***
Memory Burst Size:	4 Increment

SDIO_TX: DMA2_Stream3 DMA request Settings:

Mode:	**Peripheral Flow Control ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	Word
Peripheral Burst Size:	**4 Increment ***
Memory Burst Size:	4 Increment

USART1_RX: DMA2_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA2_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART6_RX: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Half Word ***

Memory Data Width:	**Half Word ***
Peripheral Burst Size:	Single
Memory Burst Size:	Single

ADC1: DMA2_Stream4 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC2: DMA2_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC3: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

TIM6_UP: DMA1_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word

Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream1 global interrupt	true	0	0
DMA1 stream3 global interrupt	true	0	0
ADC1, ADC2 and ADC3 global interrupts	true	0	0
TIM1 break interrupt and TIM9 global interrupt	true	0	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
SPI1 global interrupt	true	0	0
USART1 global interrupt	true	0	0
TIM8 break interrupt and TIM12 global interrupt	true	0	0
TIM8 update interrupt and TIM13 global interrupt	true	0	0
SDIO global interrupt	true	0	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream1 global interrupt	true	0	0
DMA2 stream2 global interrupt	true	0	0
DMA2 stream3 global interrupt	true	0	0
DMA2 stream4 global interrupt	true	0	0
DMA2 stream5 global interrupt	true	0	0
DMA2 stream6 global interrupt	true	0	0
DMA2 stream7 global interrupt	true	0	0
USART6 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
SPI2 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
RTC alarms A and B interrupt through EXTI line 17	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407ZETx
Datasheet	022152_Rev8

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	F407zetSD_DMA
Project Folder	F:\!!zet\STM32F407zetSD_DMA\F407zetSD_DMA
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.16.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No