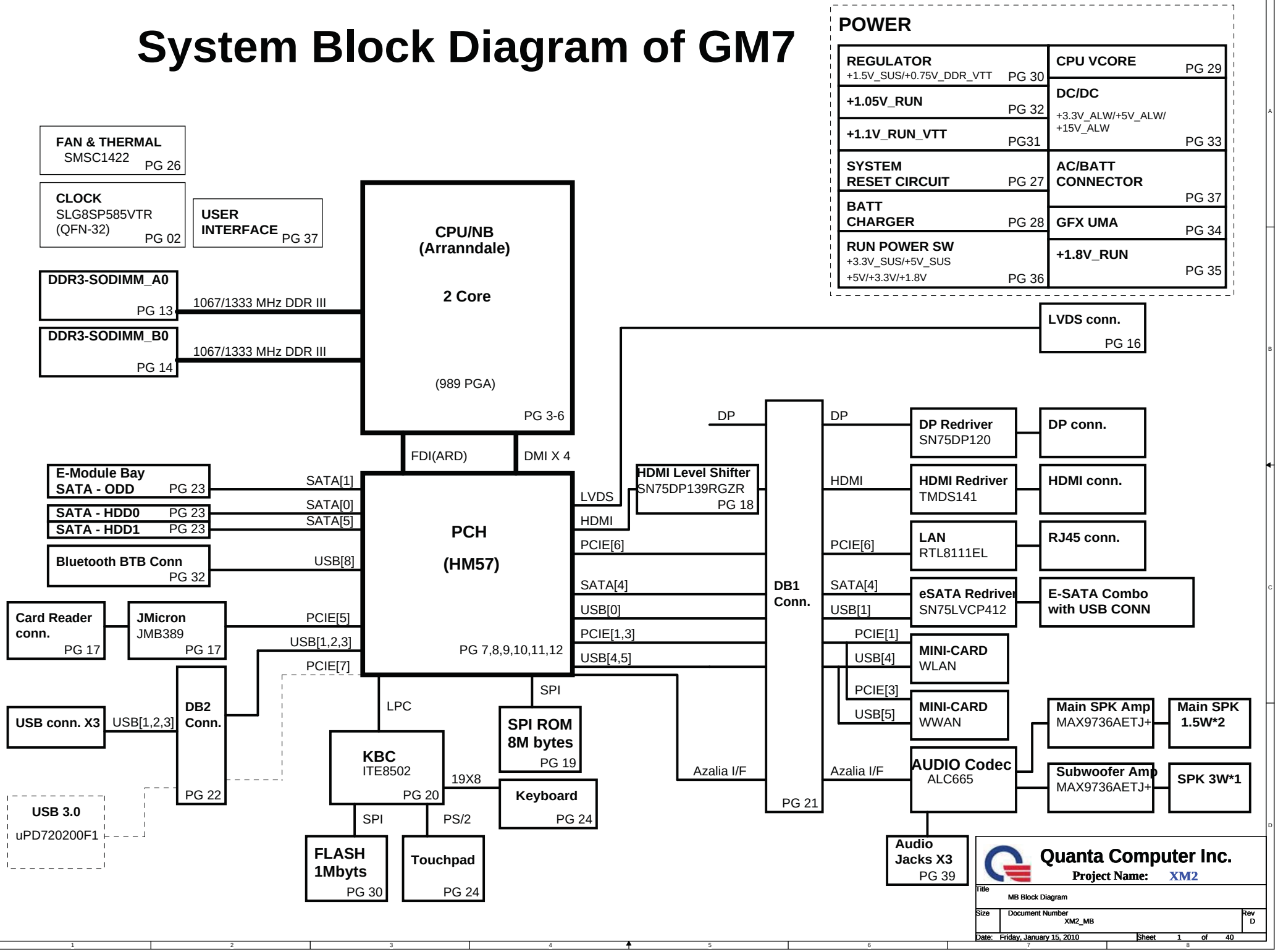
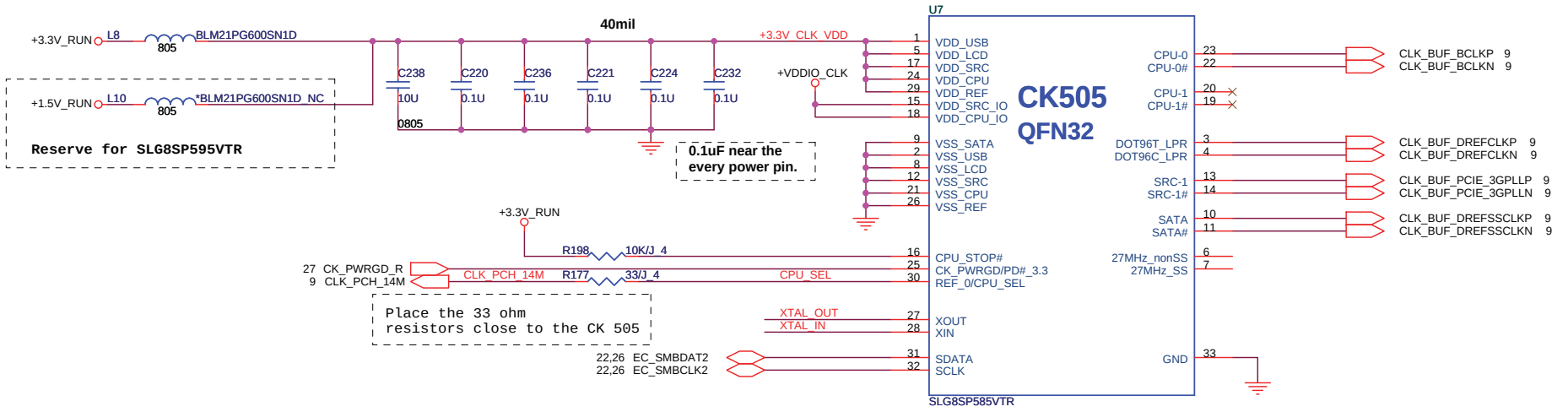
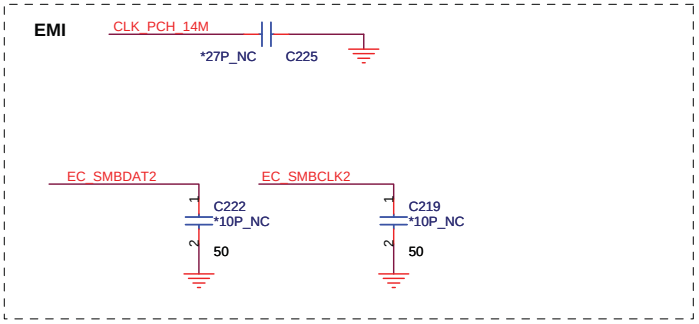
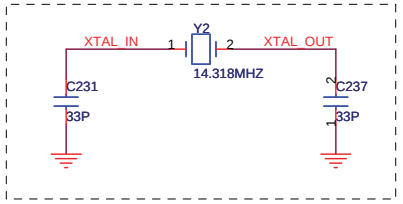
System Block Diagram of GM7

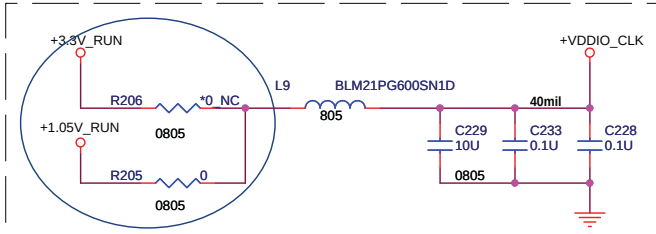








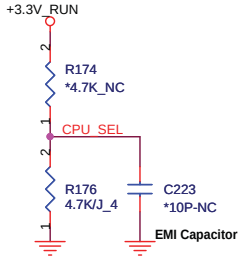
Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs



SLG,IDT: +1.05V
Realtek: +3.3V

Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.



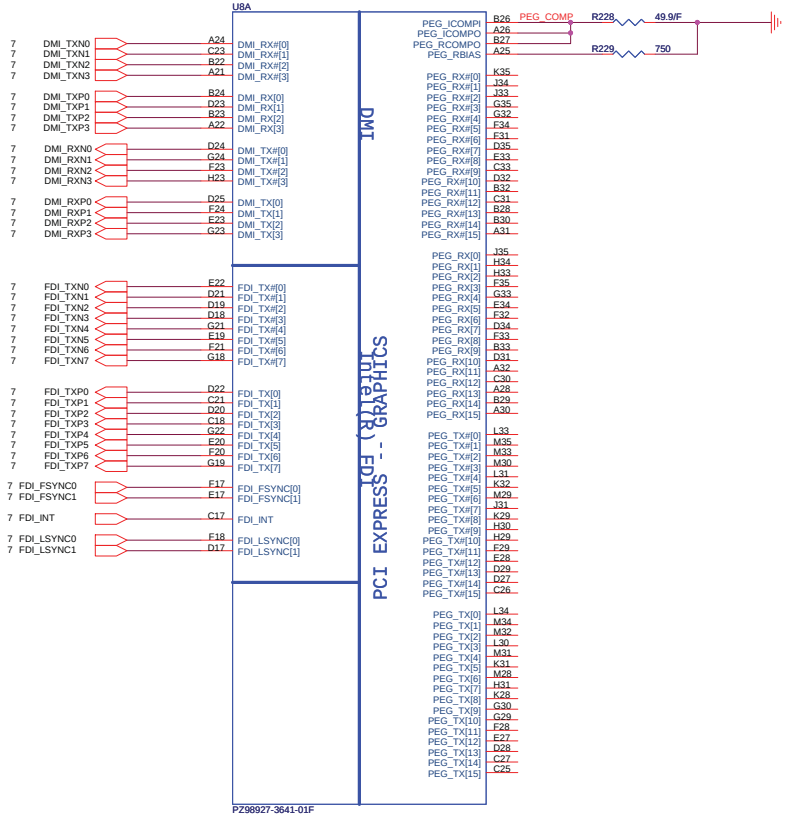
PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

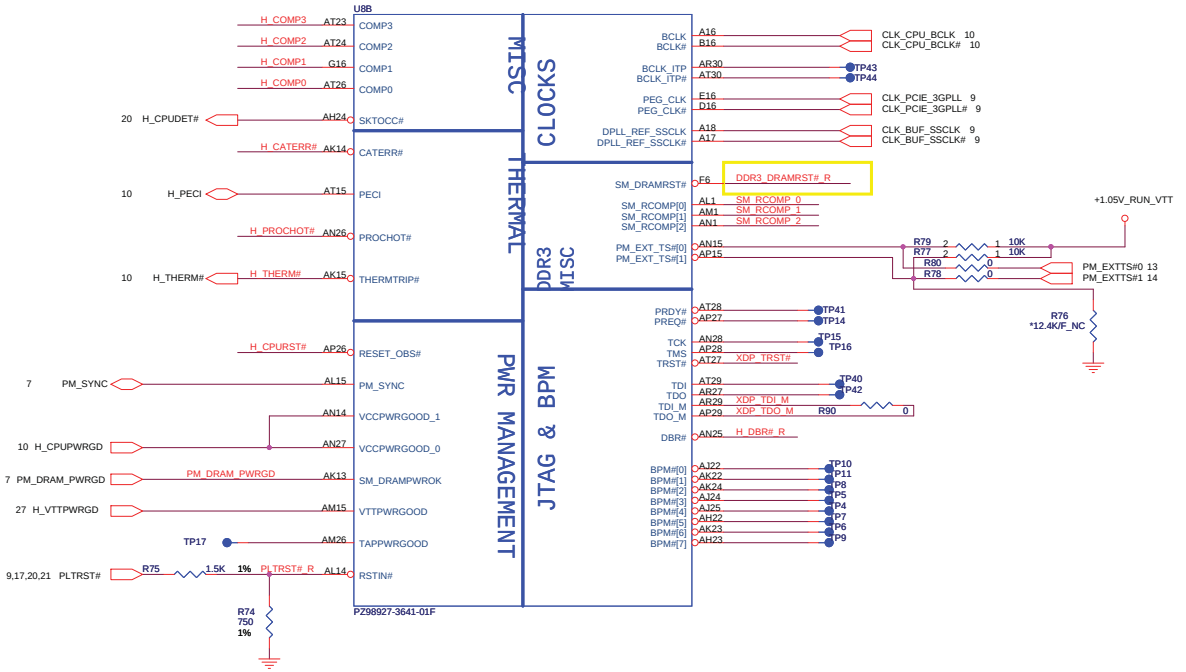
Quanta Computer Inc.
Project Name: GM7B

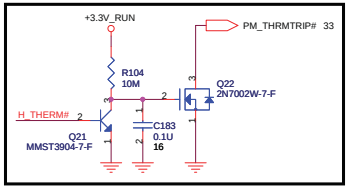
Title: Clock Gen		
Size	Document Number: GM7B	Rev: D
Date: Friday, January 15, 2010	Sheet 2 of 40	

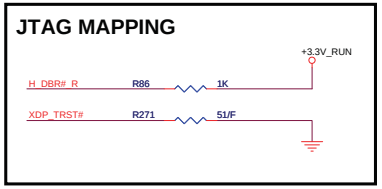
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

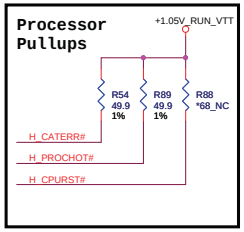


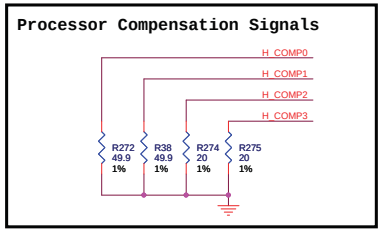
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

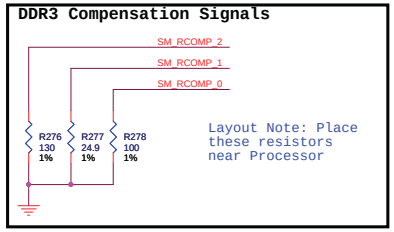


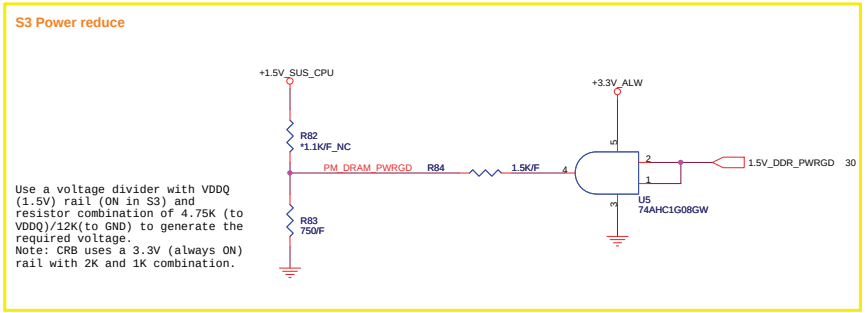


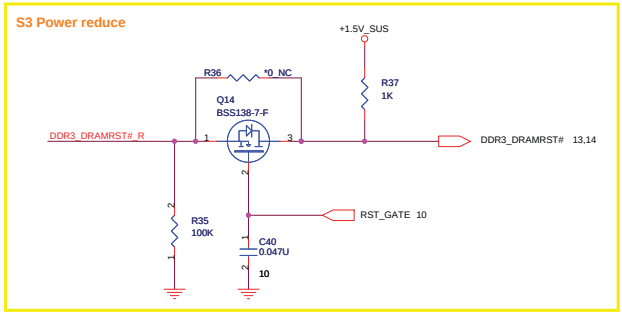










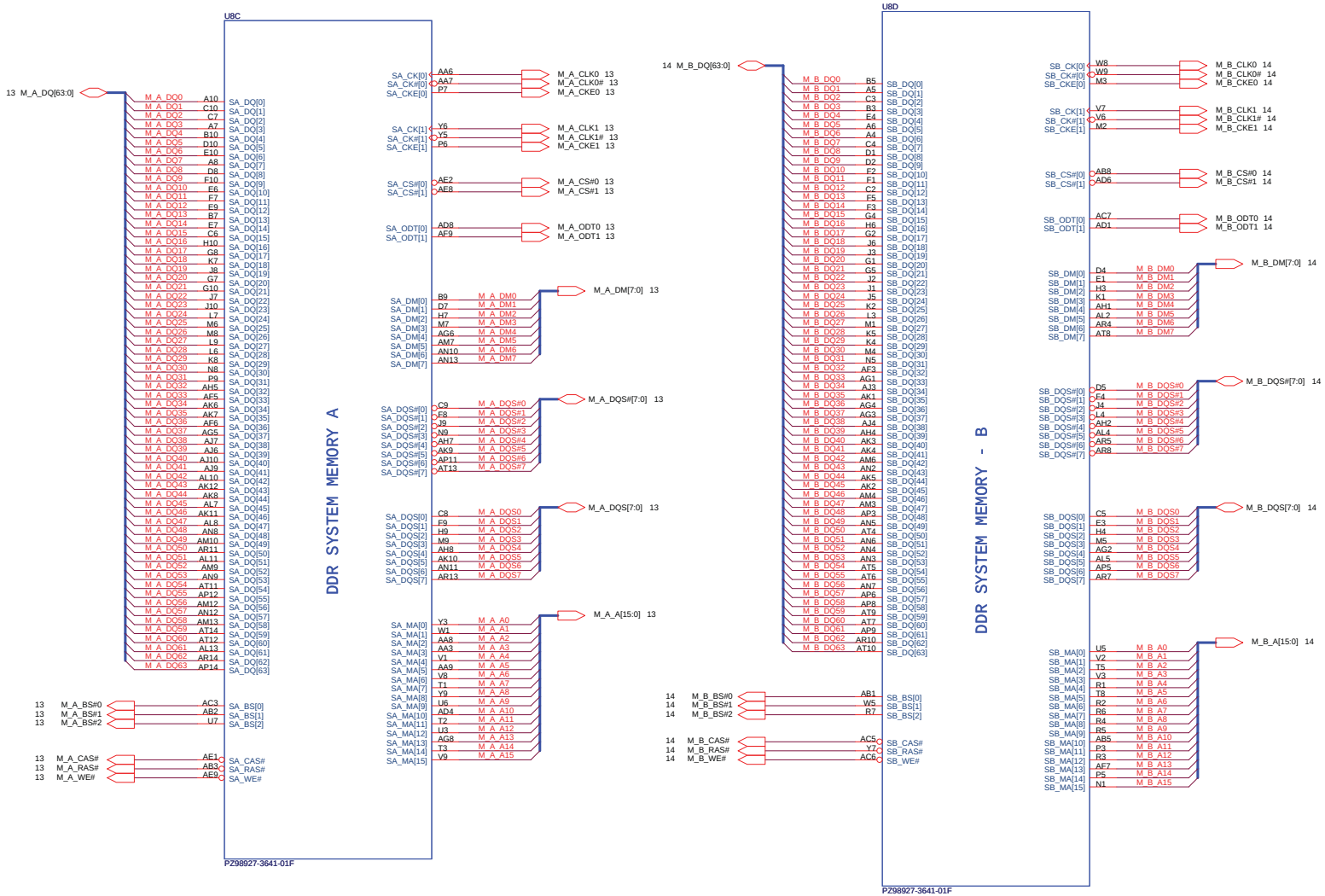


Quanta Computer Inc.

Project Name: XM2

Title	CPU 1/4(PEG_DMI)	
Size	Document Number XM2_MB	Rev D
Date: Friday, January 15, 2010	Sheet 3 of 40	

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

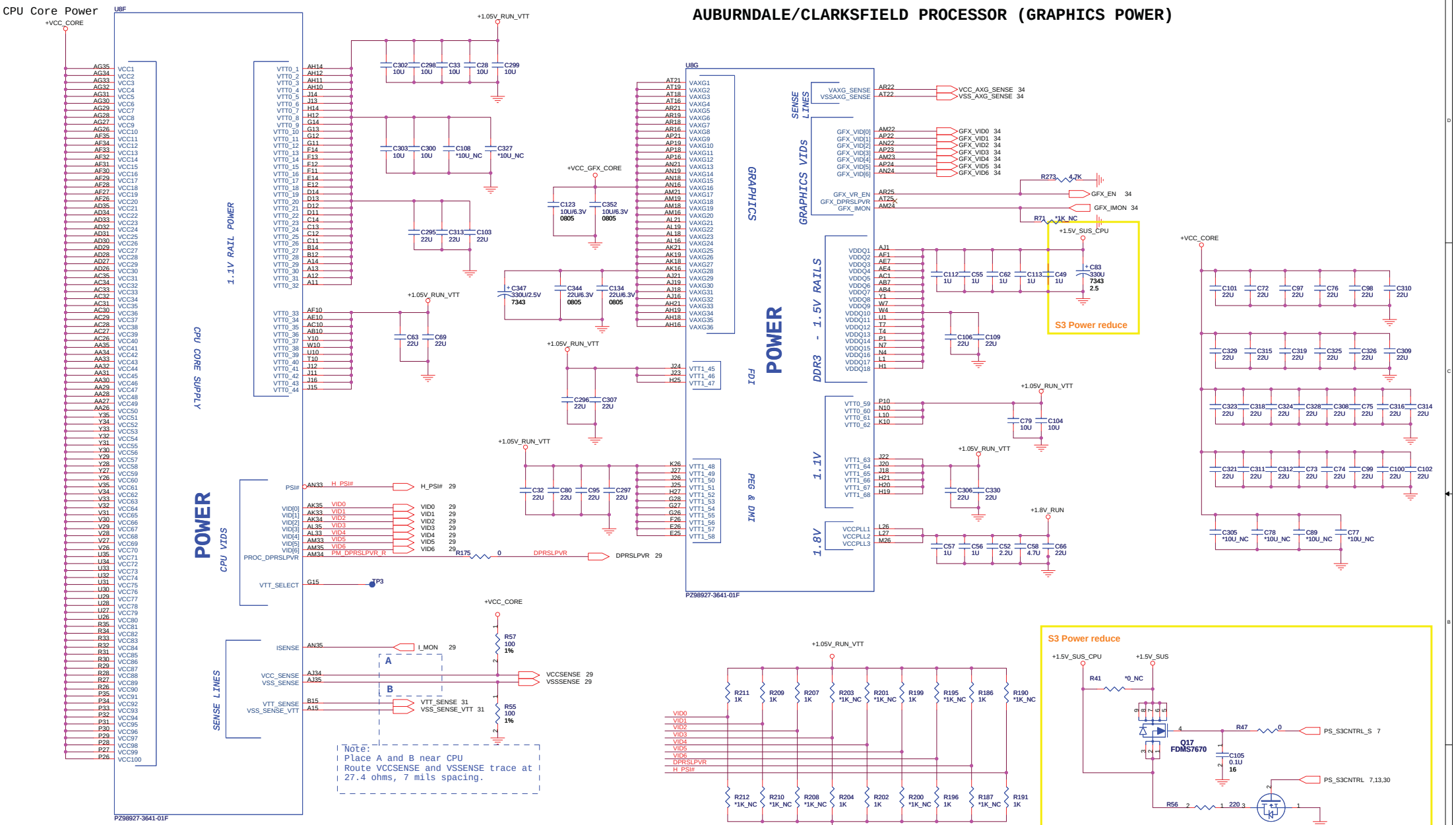


Quanta Computer Inc.

Project Name: XM2

Title: CPU 2/4(DDR)		
Size	Document Number: XM2_MB	Rev: D
Date: Friday, January 15, 2010	Sheet 4 of 40	

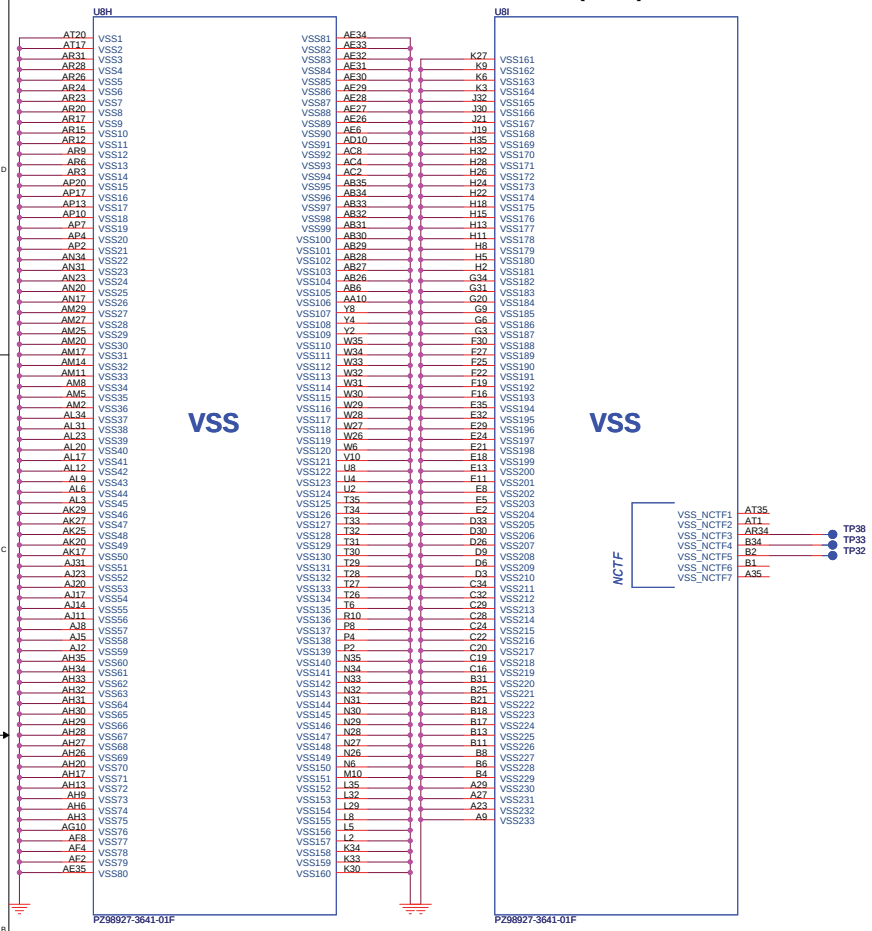
AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



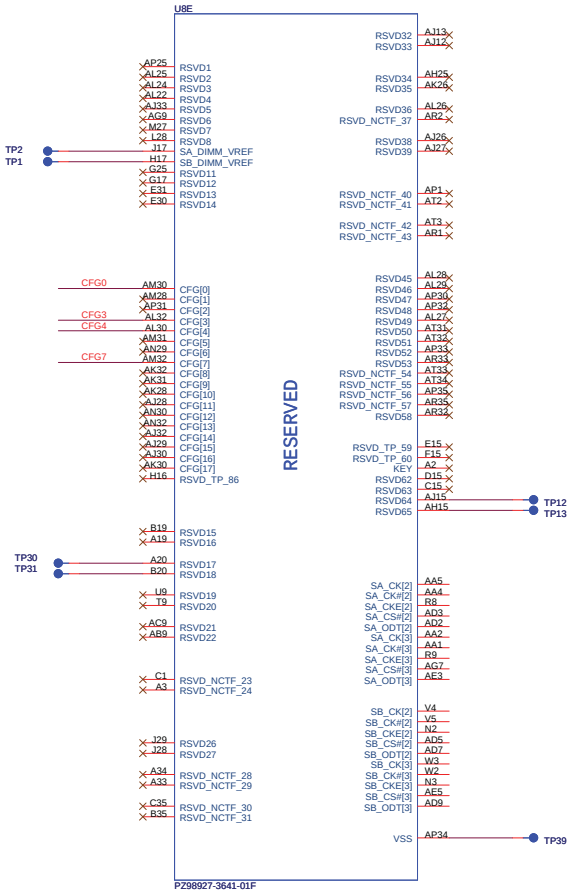
AUBURNDALE PROCESSOR (POWER)

Quanta Computer Inc.	
Project Name: XM2	
Title: CPU 3/4(POWER)	
Size:	Document Number: XM2_MB — Rev: D
Date: Friday, January 15, 2010	Sheet 5 of 40

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



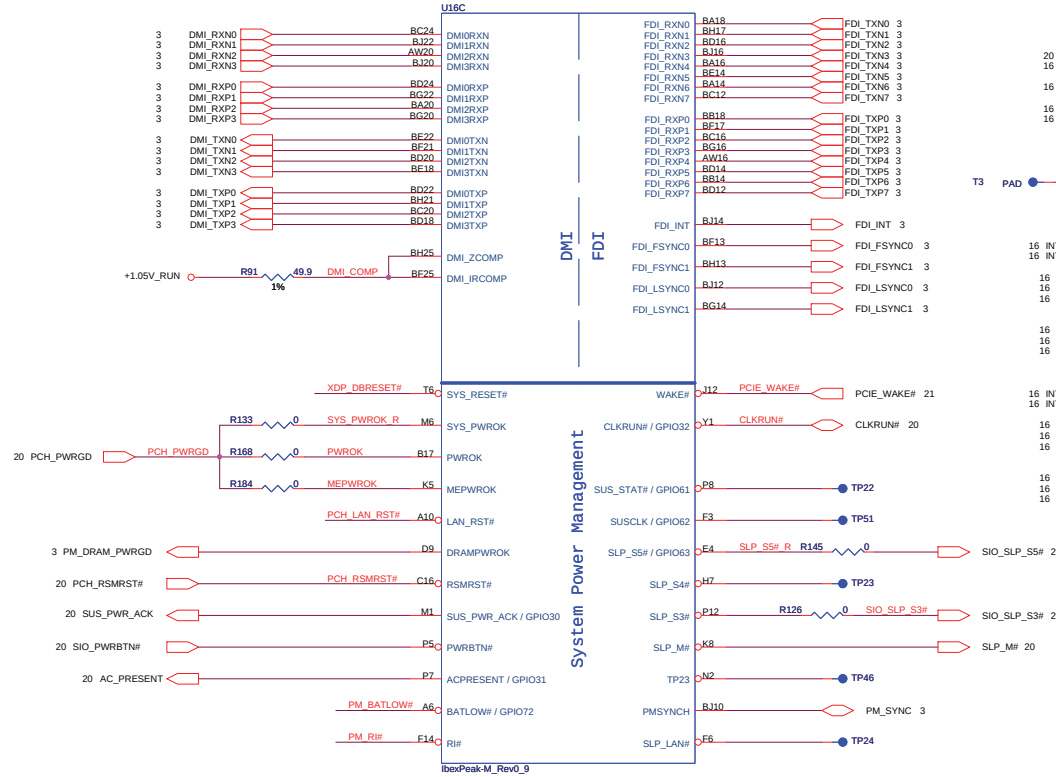
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed
CFG7 Clarksfield (only for early samples pre-ES1)	Common motherboard design	For early samples pre-ES1 CFD

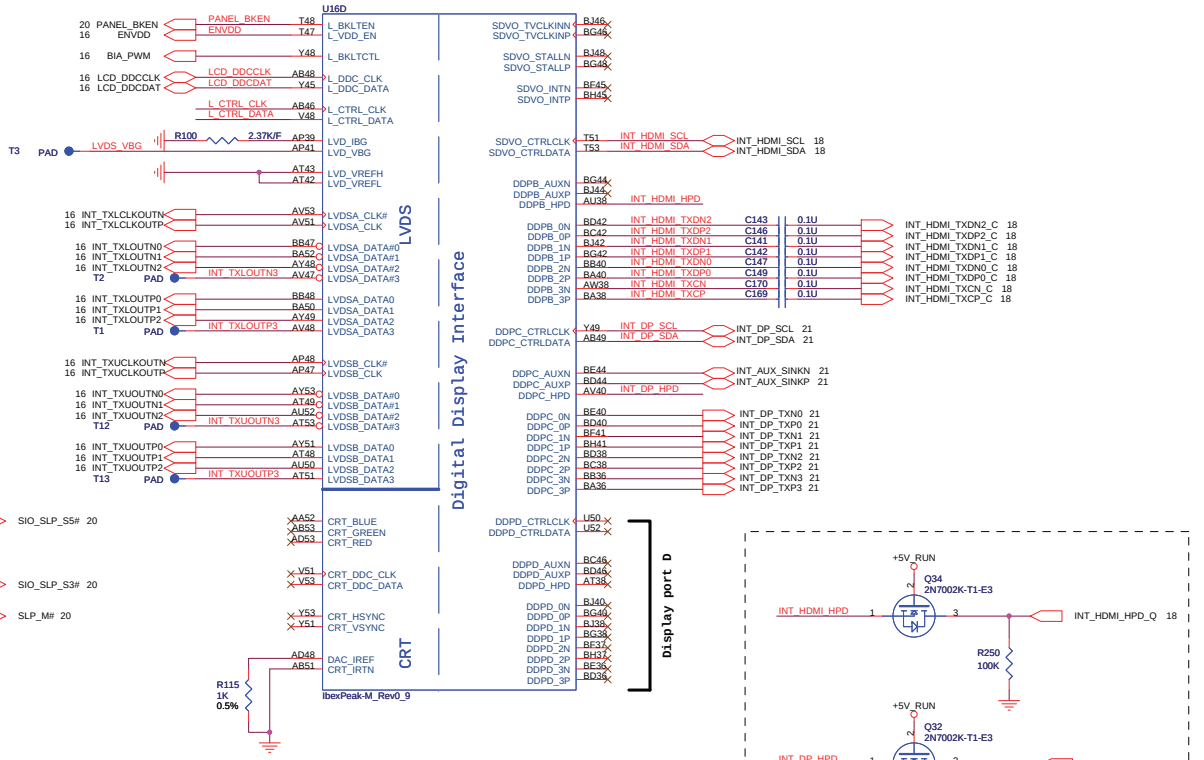
Quanta Computer Inc.
Project Name: XM2

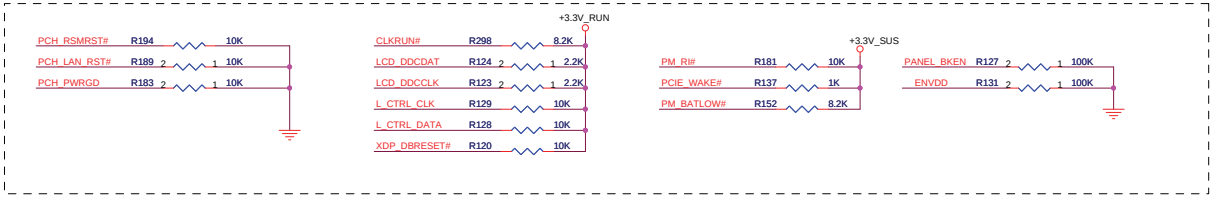
Title	CPU 4/4(GND_RESV)	
Size	Document Number XM2_MB	Rev D
Date: Friday, January 15, 2010	Sheet 6 of 40	

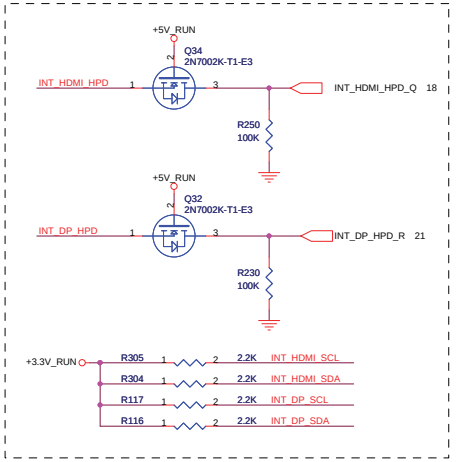
IBEX PEAK-M (DMI,FDI,GPIO)

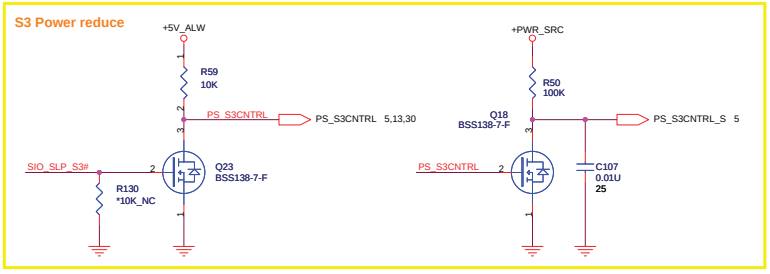


IBEX PEAK-M (LVDS,DDI)



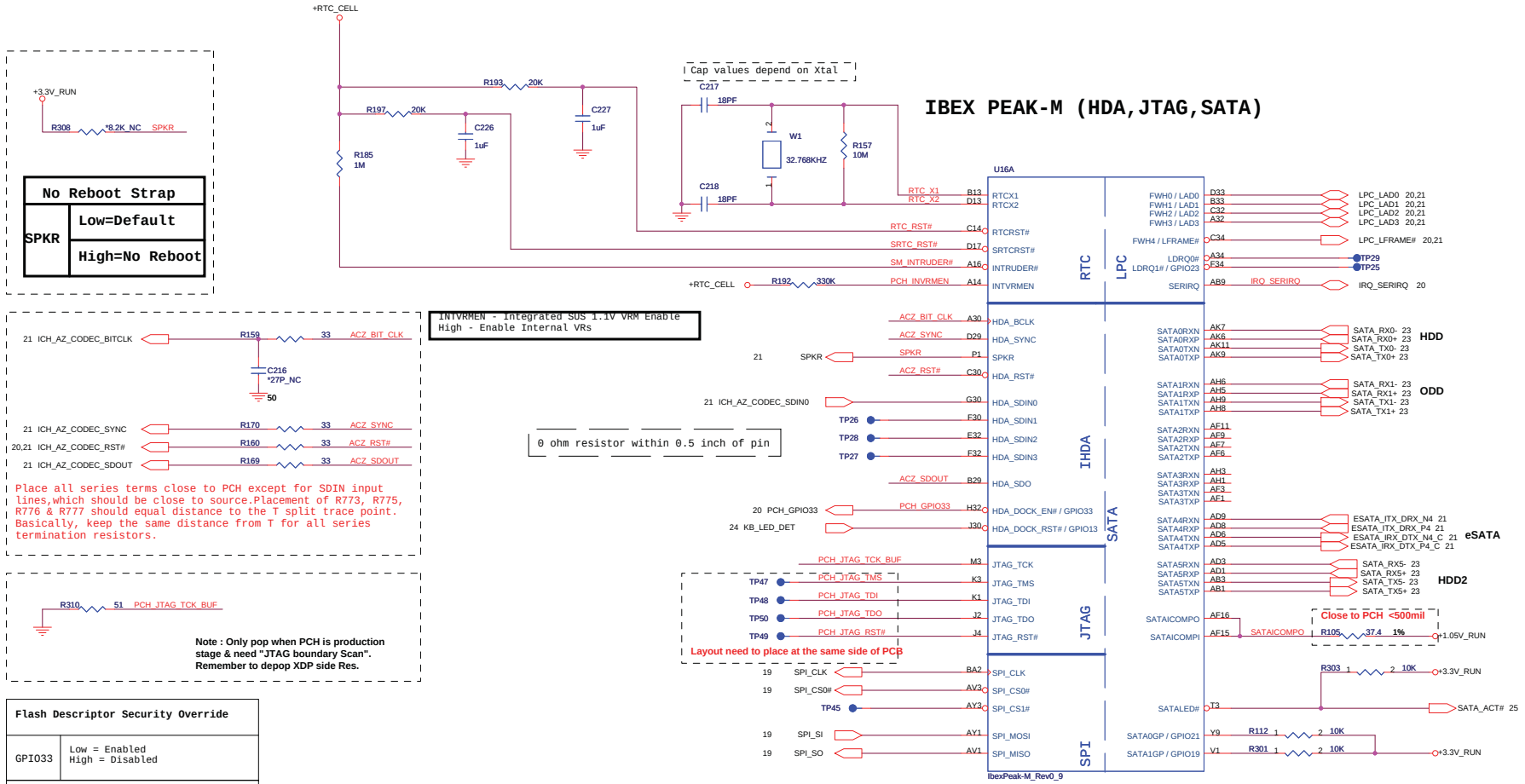






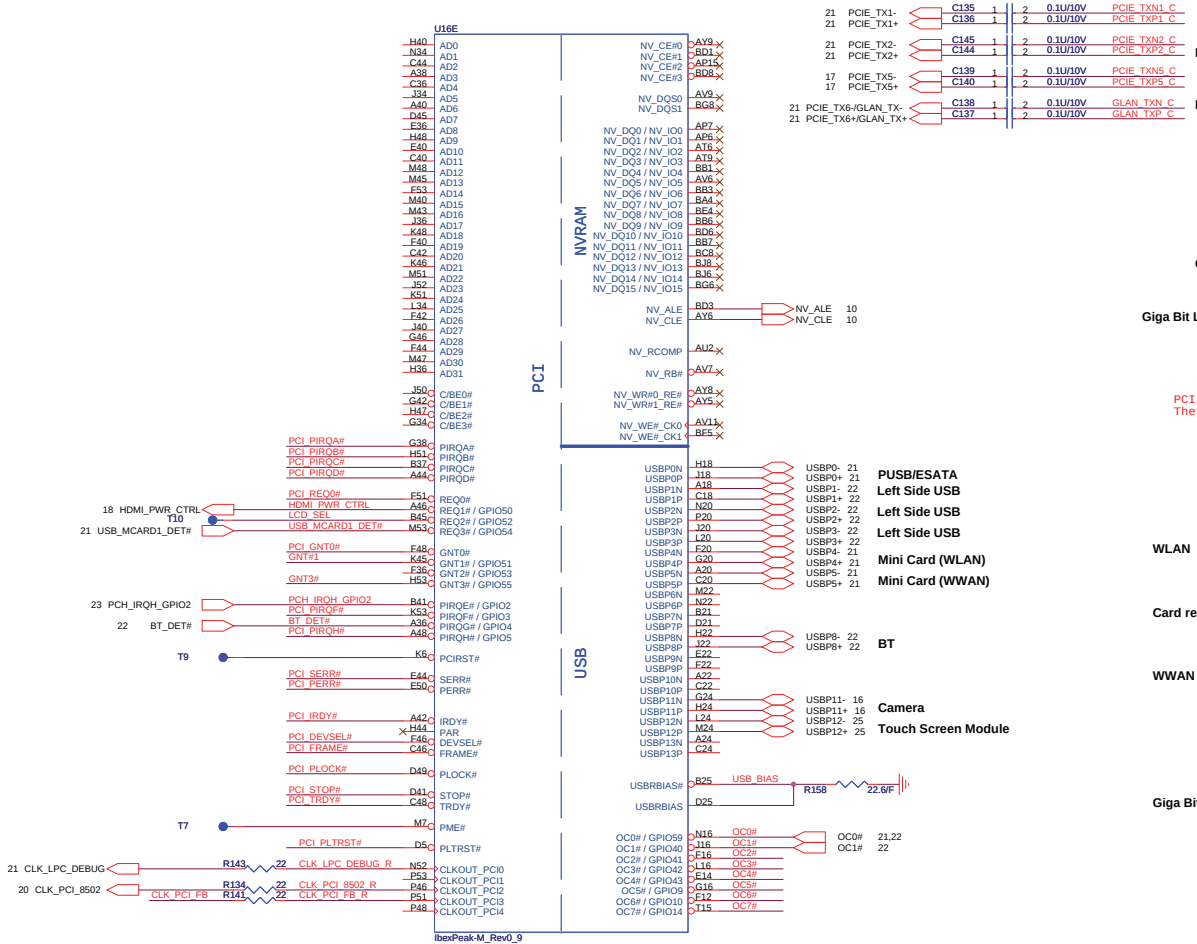
Quanta Computer Inc.			
Project Name: XM2			
Title: PCH 1/6 (DMI_VIDEO)			
Size	Document Number: XM2_MB		Rev: D
Date: Friday, January 15, 2010	Sheet 7 of 40		

IBEX PEAK-M (HDA,JTAG,SATA)

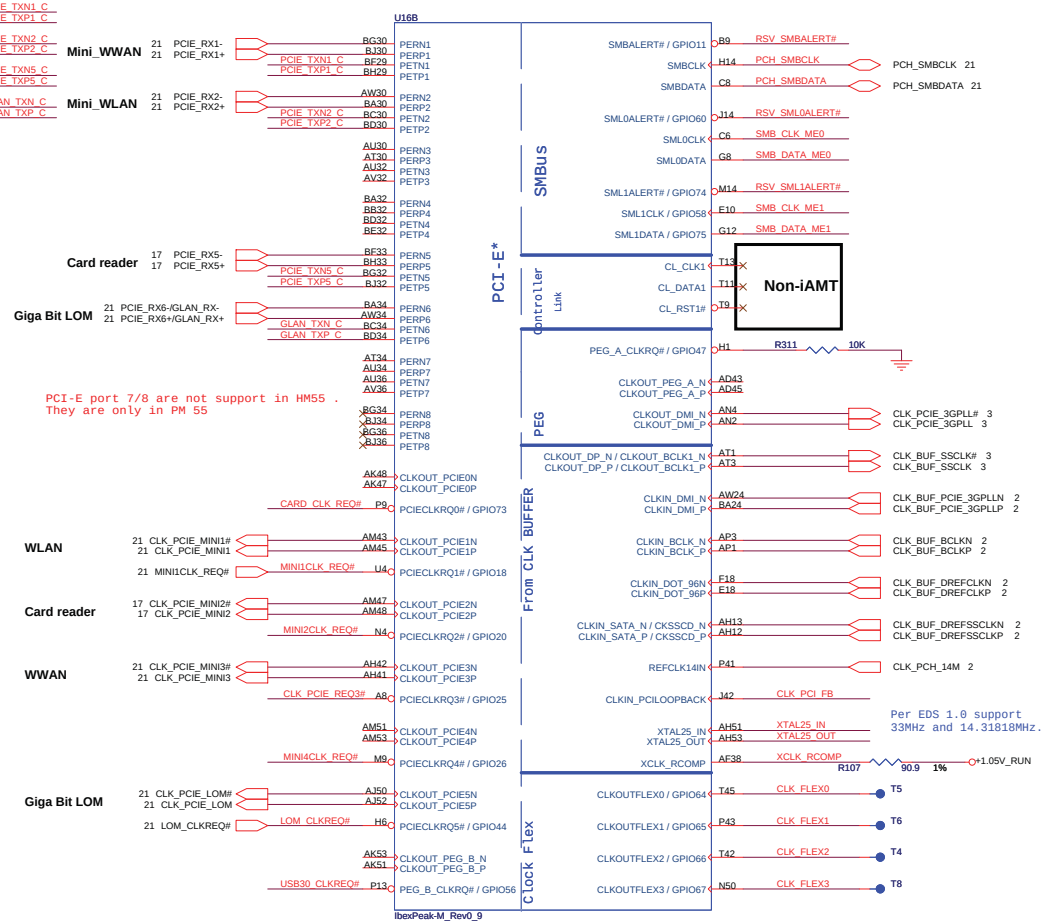


Quanta Computer Inc.	Project Name: XM2		
Title: PCH 2/6 (SATA_SPI)			
Size	Document Number: XM2_MB		Rev: D
Date: Friday, January 15, 2010	Sheet 8	of 40	

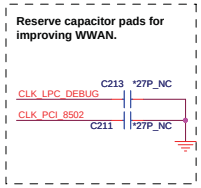
IBEX PEAK-M (PCI,USB,NVRAM)

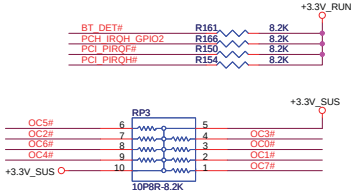


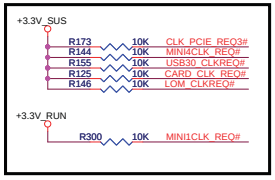
IBEX PEAK-M (PCI-E,SMBUS,CLK)

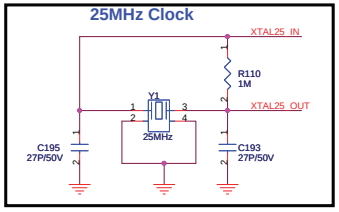


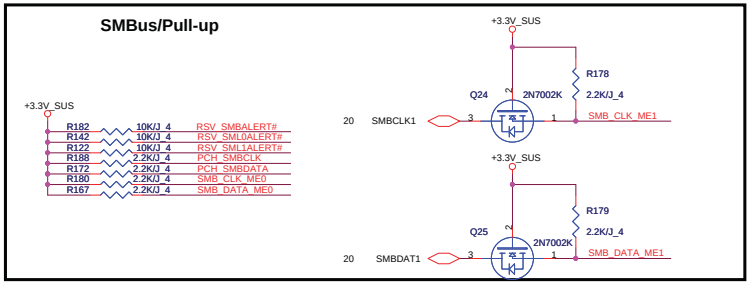
Reserve capacitor pads for improving WWAN.





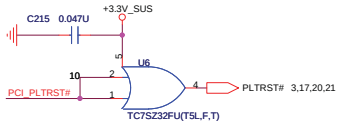


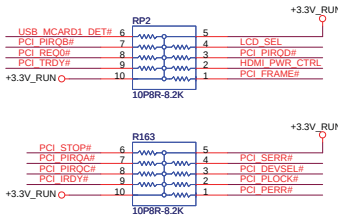


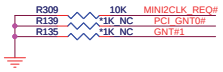


Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

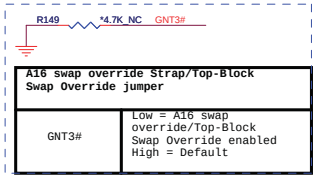






Boot BIOS Strap

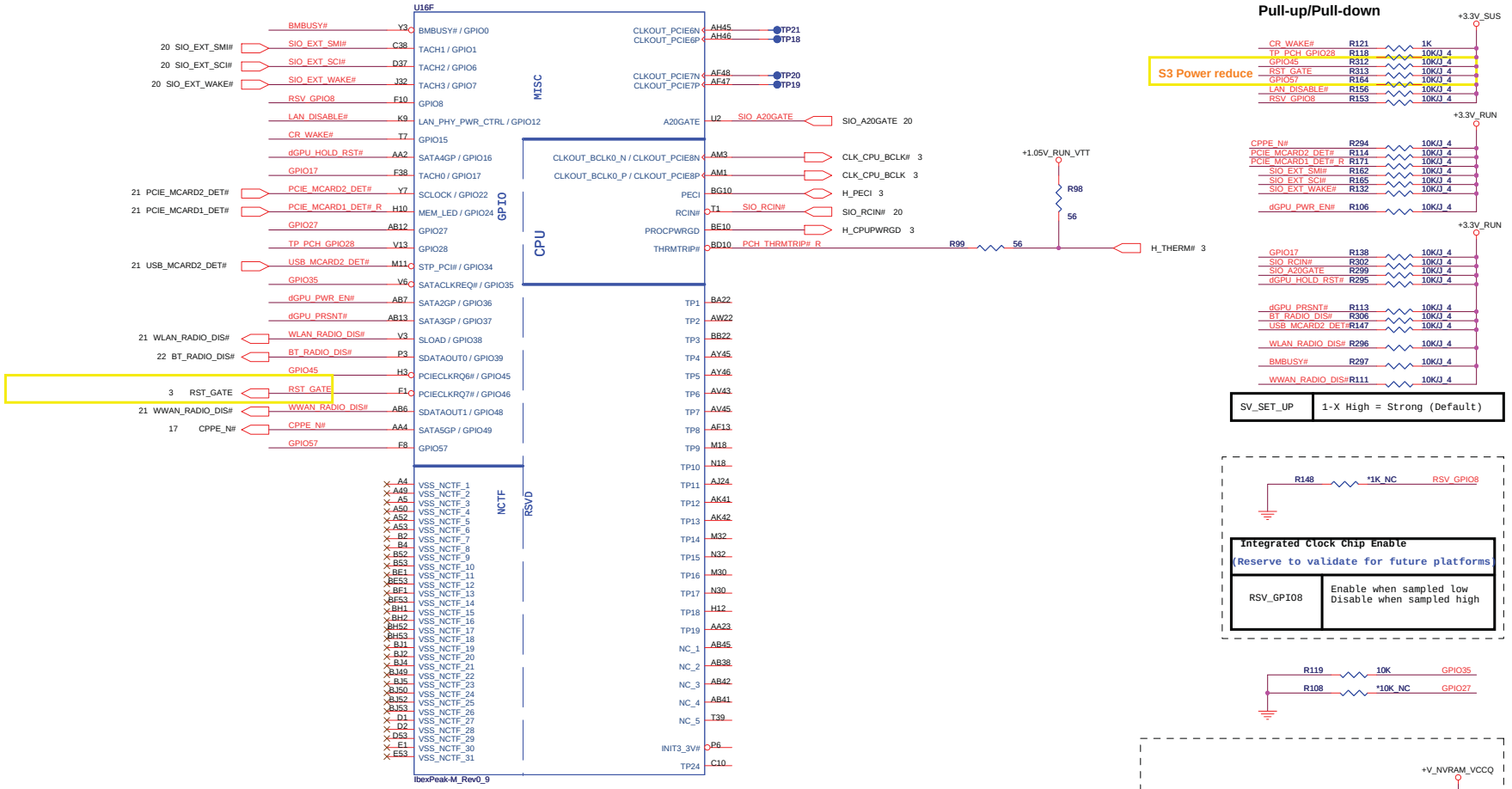
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



Quanta Computer Inc.
Project Name: XM2

Title	PCH 3/6 (PCI_SMBUS_CLK)	
Size	Document Number XM2_MB	Rev D
Date: Friday, January 15, 2010	Sheet 9 of 40	

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down

S3 Power reduce

+3.3V_SUS

CR_WAKE#	R121	1K	
TP_PCH_GPIO28	R118	10K/J_4	
GPIO45	R312	10K/J_4	
RST_GATE	R313	10K/J_4	
GPIO57	R164	10K/J_4	
LAN_DISABLE#	R156	10K/J_4	
RSV_GPIO8	R153	10K/J_4	

+3.3V_RUN

CPPE_N#	R294	10K/J_4
PCIE_MCARD2_DET#	R114	10K/J_4
PCIE_MCARD1_DET# R	R171	10K/J_4
SIO_EXT_SMI#	R162	10K/J_4
SIO_EXT_SCI#	R165	10K/J_4
SIO_EXT_WAKE#	R132	10K/J_4
dGPU_PWR_EN#	R106	10K/J_4

+3.3V_RUN

GPIO17	R138	10K/J_4
SIO_RCIN#	R302	10K/J_4
SIO_A20GATE	R299	10K/J_4
dGPU_HOLD_RST#	R295	10K/J_4
dGPU_PRSNT#	R113	10K/J_4
BT_RADIO_DIS#	R306	10K/J_4
USB_MCARD2_DET#	R147	10K/J_4
WLAN_RADIO_DIS#	R296	10K/J_4
BMBUSY#	R297	10K/J_4
WWAN_RADIO_DIS#	R111	10K/J_4

SV_SET_UP	1-X High = Strong (Default)

R148 *1K_NC RSV_GPIO8

Integrated Clock Chip Enable
(Reserve to validate for future platforms)

RSV_GPIO8	Enable when sampled low Disable when sampled high

R119 10K GPIO35
R108 *10K_NC GPIO27

+V_NVRAM_VCCQ

9 NV_ALE R92 *8.2K_NC
9 NV_CLE R93 *8.2K_NC

DMI Termination Voltage

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled

NV_ALE	High = Enable(Default) Low = Disable

Quanta Computer Inc.
Project Name: XM2

Title: PCH 4/6 (GPIO)
Size: Document Number: XM2_MB
Rev: D
Date: Friday, January 15, 2010
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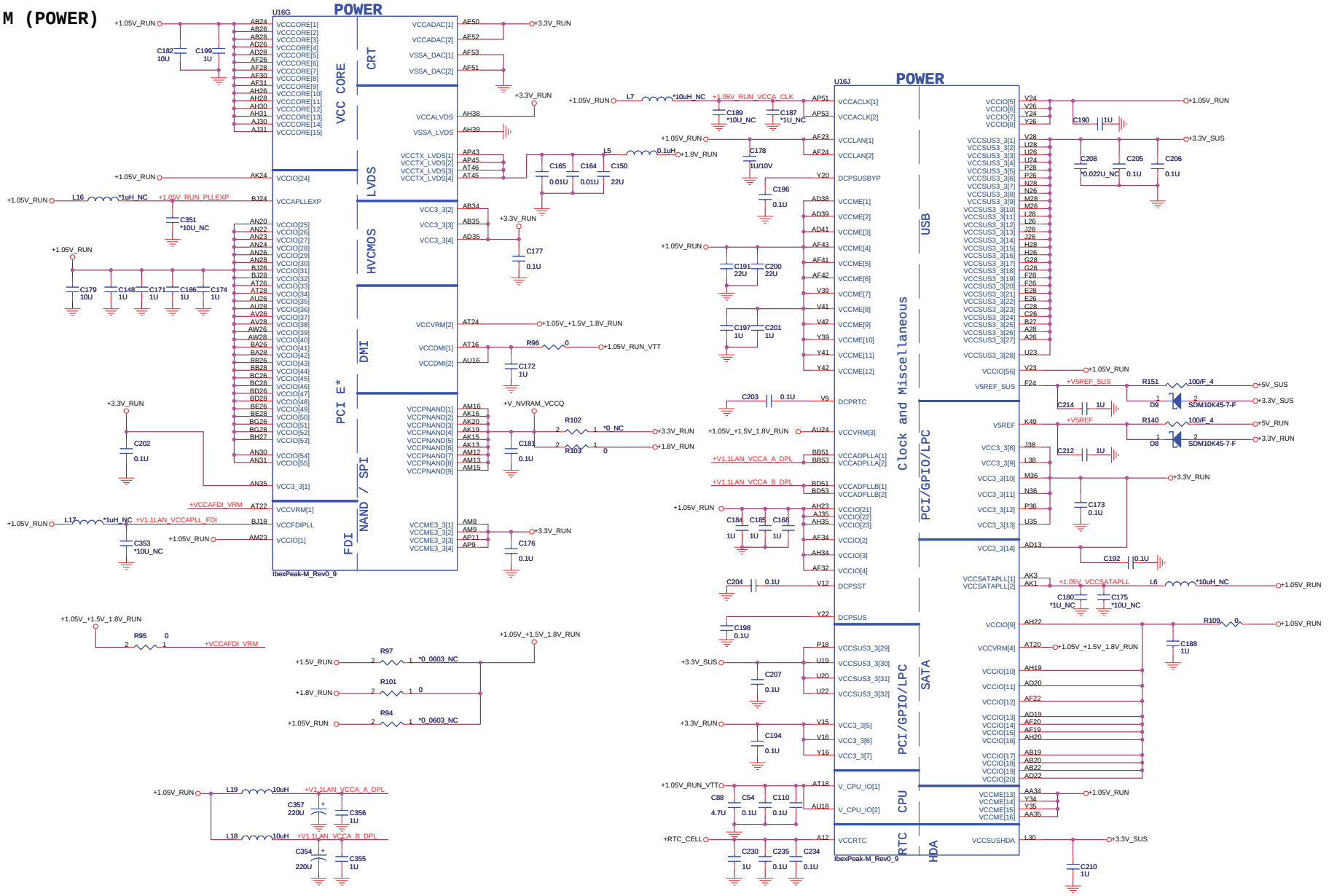
IBEX PEAK-M (POWER)

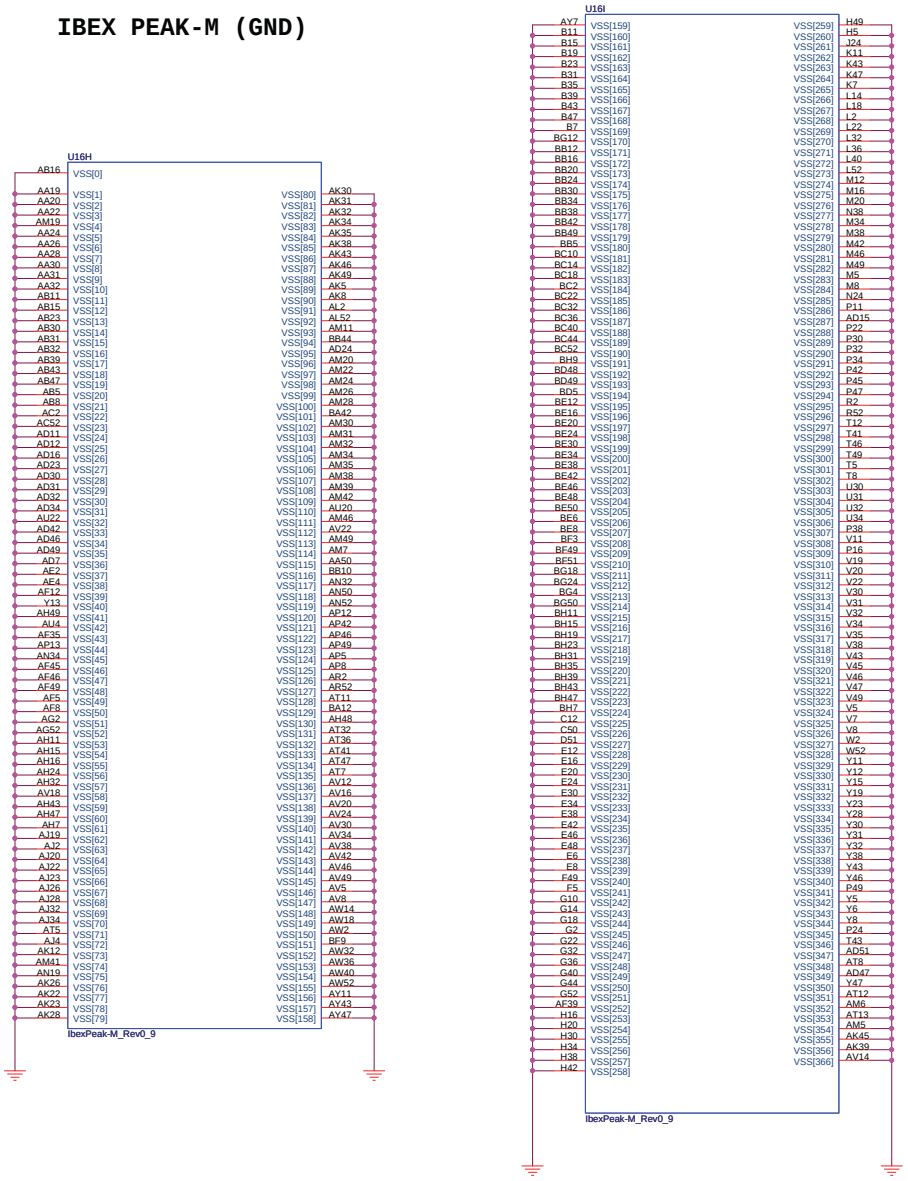


Quanta Computer Inc.

Project Name: XM2

Title: PCH 5/6 (POWER)		
Size	Document Number: XM2_MB	Rev: D
Date: Friday, January 15, 2010	Sheet 11 of 40	

IBEX PEAK-M (GND)

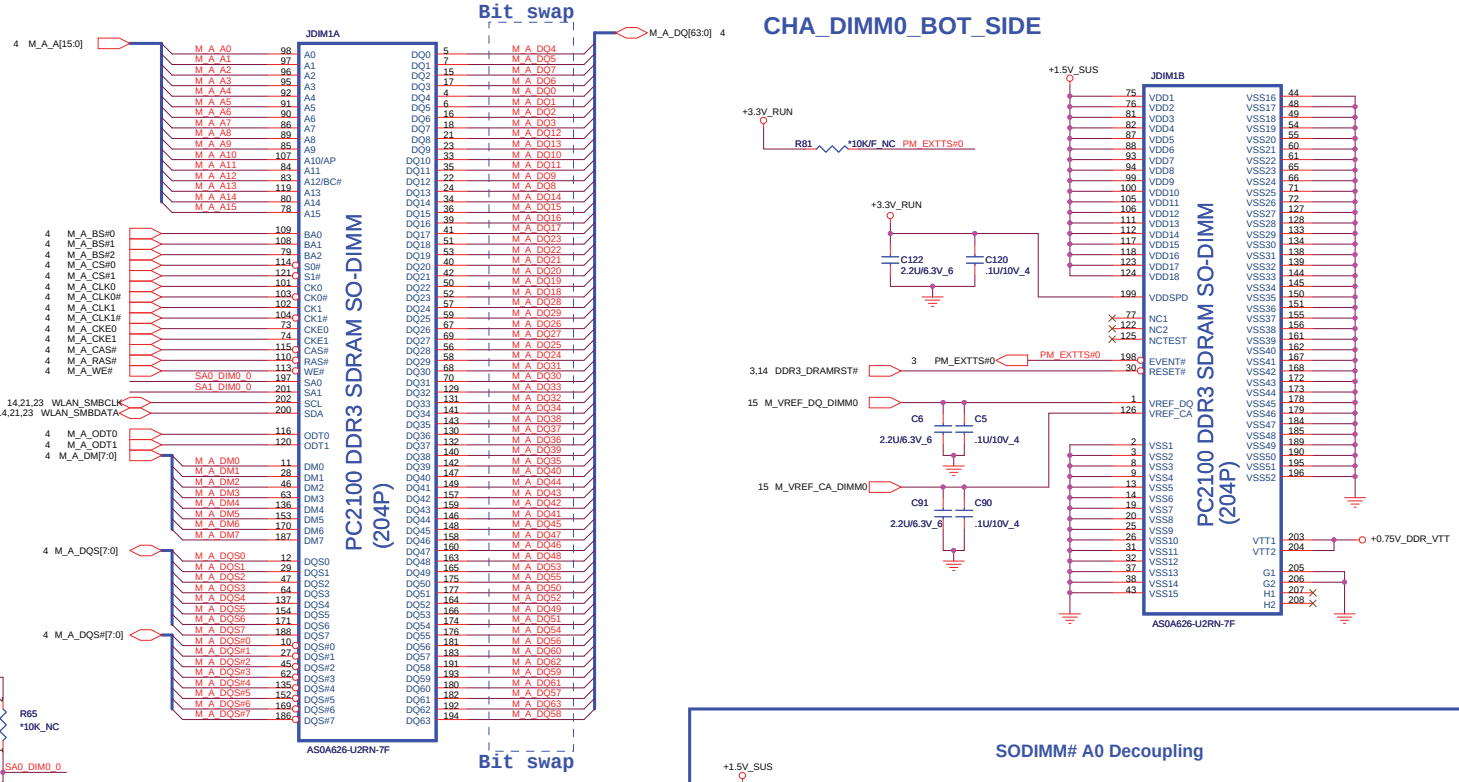


Quanta Computer Inc.

Project Name: XM2

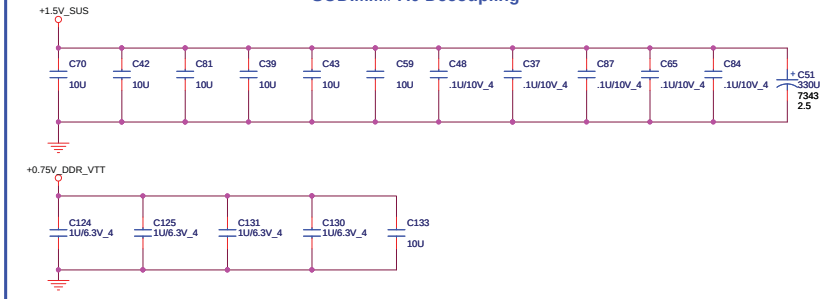
Title	PCH 6/6 (GND)	
Size	Document Number XM2_MB	Rev D
Date: Friday, January 15, 2010	Sheet 12 of 40	

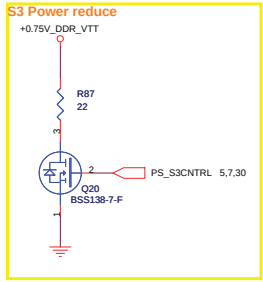
CHA_DIMM0_BOT_SIDE



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

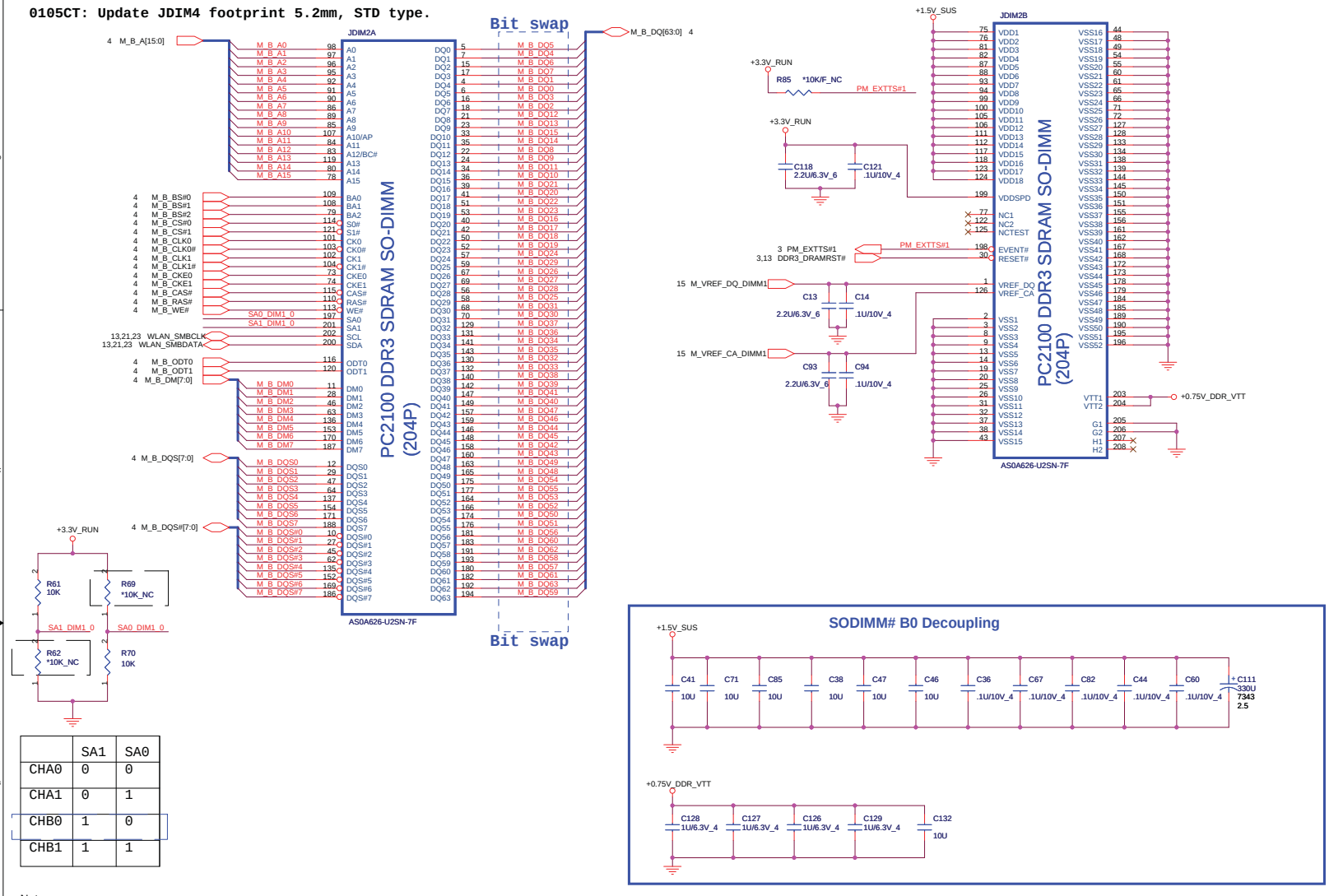
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32





Quanta Computer Inc.	
Project Name: XM2	
Title: DDR3 DIMM-A0	
Size	Document Number: XM2_MB — Rev: D
Date: Friday, January 15, 2010	Sheet 13 of 40

0105CT: Update JDIM4 footprint 5.2mm, STD type.



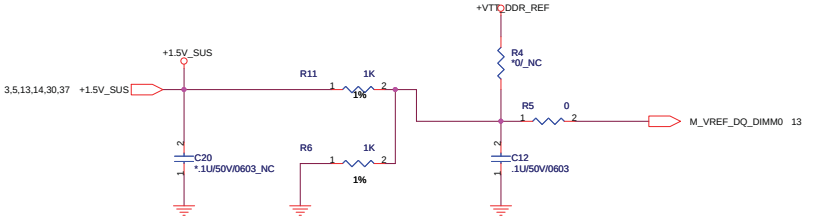
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

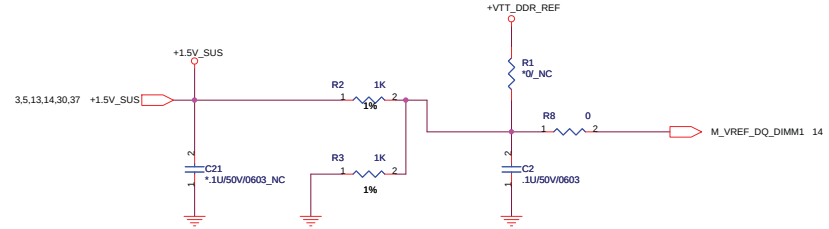
Note:
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

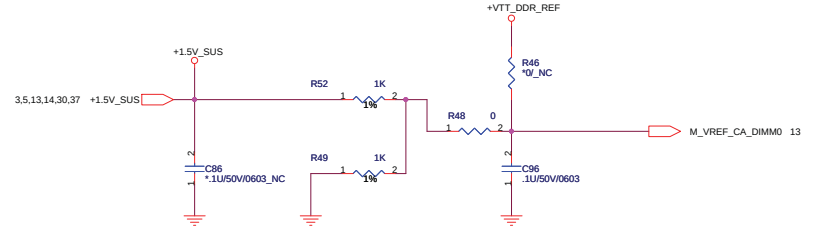
Quanta Computer Inc.
Project Name: XM2

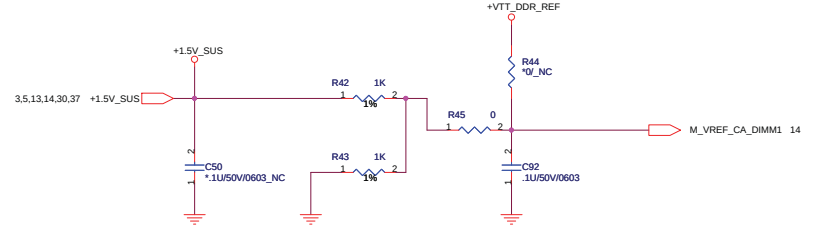
Title	DDR3 DIMM-B0	
Size	Document Number XM2_MB	Rev D
Date: Friday, January 15, 2010	Sheet 14 of 40	

Fixed SO-DIMM VREF_DQ (M1): Default





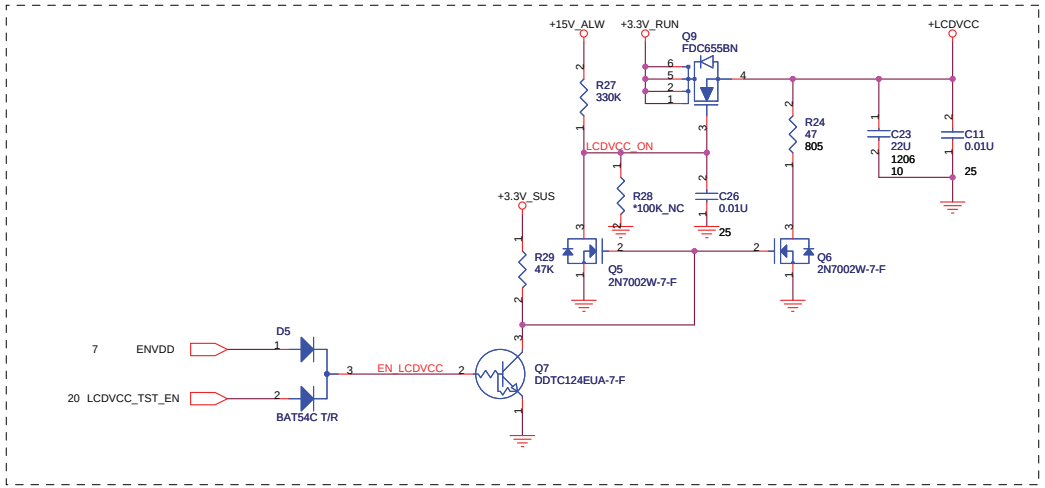


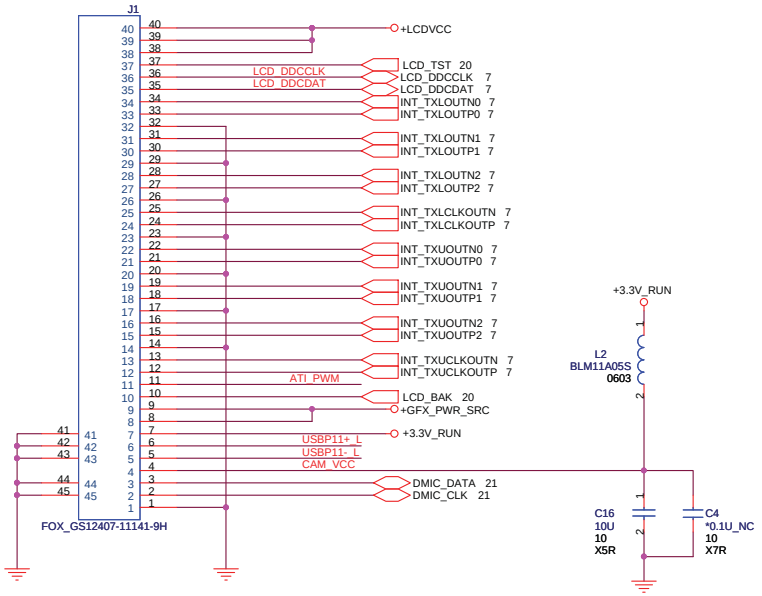


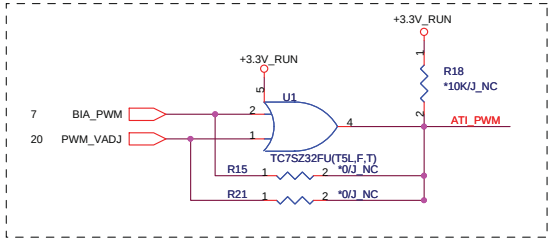
Quanta Computer Inc.
Project Name: XM2

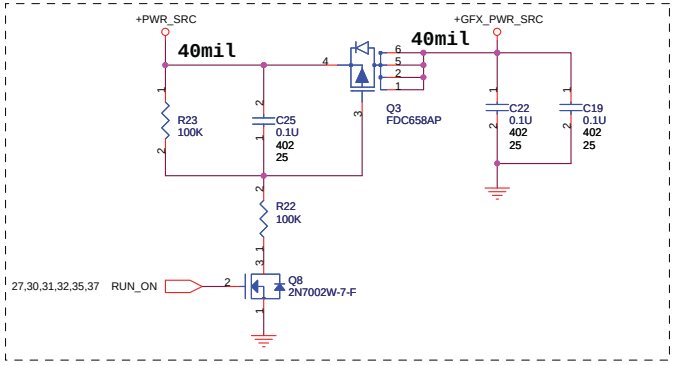
Title: DDR3 VREF		
Size	Document Number: XM2_MB	Rev: D
Date: Friday, January 15, 2010	Sheet 15 of 40	

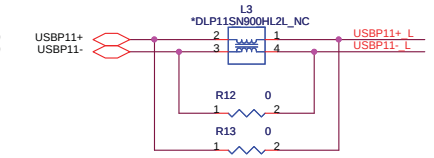
40Pin LVDS & Array Microphone & Camera Connector

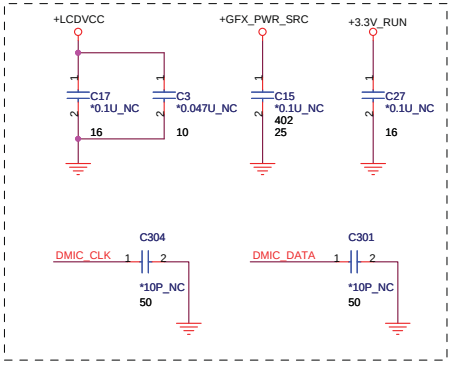












Quanta Computer Inc.

PROJECT : Calpella UMA

Size	Document Number	Rev
	LVDS CONN	1A

Date: Friday, January 15, 2010 Sheet 16 of 40

Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MDIO00	SD/MMC/MS/xD	SD_D0	MS_D0	XD_D0
MDIO01		SD_D1	MS_D1	XD_D1
MDIO02		SD_D2	MS_D2	XD_D2
MDIO03		SD_D3	MS_D3	XD_D3
MDIO04		SD_CMD	MS_BS	XD_WE#
MDIO05		SD_CLK	MS_CLK	XD_CE#
MDIO06		SD_WP		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_D4	MS_D4	XD_D4
MDIO09		MMC_D5	MS_D5	XD_D5
MDIO10		MMC_D6	MS_D6	XD_D6
MDIO11		MMC_D7	MS_D7	XD_D7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE
CR1_LEDN		SD_LED#	MS_LED#	XD_LED#
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD1			MS_CD#	
CR1_CD2				XD_CD#

+DVDD18 +APVDD R323 0 0603 (>40mil)

+3.3V_RUN +VDD33 R321 0 0603 (>40mil)

(>20mil) +CR_PWR R322 0 0603 +3.3V_CARD C368 22U/6.3V_8 C284 0.1U

+DVDD18 C372 0.1U C375 0.1U

+VDD33 C373 0.1U C369 0.1U

2.2uF cap is no more than 250mils away from the power pin and a have a min trace width of 40mils.

+3.3V_CARD C283 2.2U/6.3V CC0603

C7577 need close to pin7

CON3

SD_MS_XD-D2 SD_MS_XD-D3 SD_MS_XD-D4 SD-CMD_MS-BS_XD-WE# SD_MS_XD-D5 SD-CLK_MS-CLK_XD-CE# SD_MS_XD-D3 MS_CD# SD_MS_XD-D2 SD_MS_XD-D0 SD_MS_XD-D1 SD-CMD_MS-BS_XD-WE# SD-CLK_MS-CLK_XD-CE# SD_MS_XD-D6 SD_MS_XD-D7 SD_MS_XD-D0 SD_MS_XD-D1

SD-9(D2) SD-1(D3) MMC-10(D4) SD-2(SD_CMD) MMC-11(D5) SD-3(VSS) SD-4(VDD) MS-10(VSS) MS-9(VCC) MS-8(SCLK) MS-7(D3) MS-6(INS) MS-5(D2) MS-4(D0) MS-3(D1) MS-2(BS) MS-1(VSS) SD-5(CLK) MMC-12(D6) SD-6(GND) MMC-13(D7) SD-7(D0) SD-8(D1)

SD(SW.COM) SD(SW.CD) XD-1(GND) XD-0(CDSW) XD-2(R/-B) XD-3(RE) XD-4(CE) XD-5(CLE) XD-6(ALE) XD-7(WE) XD-8(-WP) XD-9(GND) XD-10(D0) XD-11(D1) XD-12(D2) XD-13(D3) XD-14(D4) XD-15(D5) XD-16(D6) XD-17(D7) XD-18(VCC) SD(SW.WP)

TAS_5-250907001000-9
5in1-5-250907001000-9-45p

C281 270P/25V C279 *10P_NC C282 *10P_NC

+3.3V_CARD **C85 need close to pin44** C278 2.2U 6.3 X5R

SD_CD# XD_CD# XD-R/B# XD-RE# SD-CLK_MS-CLK_XD-CE# XD-CLE XD-ALE SD-CMD_MS-BS_XD-WE# SD-WP_XD-WP# SD_MS_XD-D0 SD_MS_XD-D1 SD_MS_XD-D2 SD_MS_XD-D3 SD_MS_XD-D4 SD_MS_XD-D5 SD_MS_XD-D6 SD_MS_XD-D7 SD-WP_XD-WP#

C271 *270P/25V_NC

XD_CD# C285 *270P/25V_NC

SD_MS_XD-D1 R224 *0_NC C280 *10P_NC

+3.3V_CARD R327 10K SD-WP_XD-WP# R328 1K XD-R/B#

+3.3V_RUN R326 10K XD-CLE R325 200K XD-ALE

+VDD33 SD_MS_XD-D4 SD_MS_XD-D5 SD_MS_XD-D6 SD_MS_XD-D7 XD-RE#

U17 JMB389

MIDO Single End = 50 ohm

+DVDD18 XD-CLE SD-CMD_MS-BS_XD-WE# SD-CLK_MS-CLK_XD-CE# R324 22 C374 22P/50V_4 C371 2.2U

+VDD33 SD_MS_XD-D3 SD_MS_XD-D2 SD_MS_XD-D1 SD_MS_XD-D0

DV18 GND TXIN MDIO7 MDIO4 MDIO5 SDDV33_18 DV33 MDIO3 MDIO2 MDIO1 MDIO0

MDIO6 MDIO13 MDIO14 CR1_LEDN DV33 DV33 DV18 CR1_PCTLN CR1_CD0N CR1_CD1N CR1_CD2N CPPE_N

SD-WP_XD-WP# XD-R/B# XD-ALE +VDD33 +CR_PWR SD_CD# MS_CD# XD_CD#

TAV33 SPI_SI SPI_SO SPI_CSN SPI_CLK GND SPI_SCK MDIO8 MDIO9 MDIO10 MDIO11 MDIO12

XRSTN XTEST APCLKN APCLKP APVDD APGND APREXT APRXP APRXN APV18 APTXN APTXP

+DVDD18 CPPE_N# C C370 10U Needs close to Pin18: 12mil/<250mil

+3.3V_SUS R319 *10K_NC CPPE_N# 10 Q47 *2N7002W-7-F_NC

MIDO[0..5] Single Skew
Should be smaller +/- 100 mil
for SDA3.Application

3,9,20,21 PLTRST# R320 0 C367 0.1U 10 X7R

9 CLK_PCIE_MINI2# 9 CLK_PCIE_MINI2

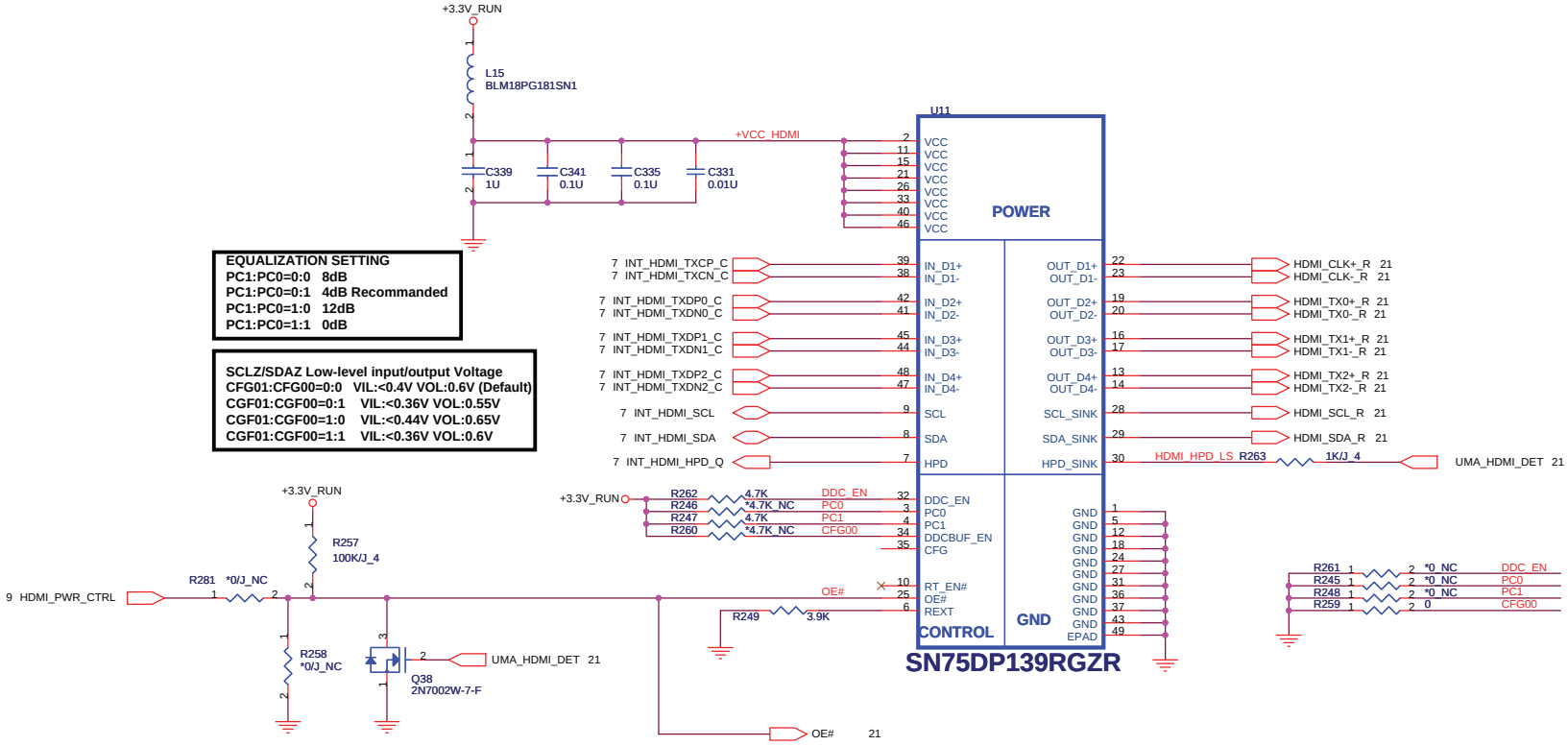
R318 12K +APV18 PCIE_RXN5_C PCIE_RXP5_C

+APVDD C360 10U C364 0.1U C362 1000P (20mil) +APV18 C363 0.1U C361 10U

C365 0.1U C366 0.1U

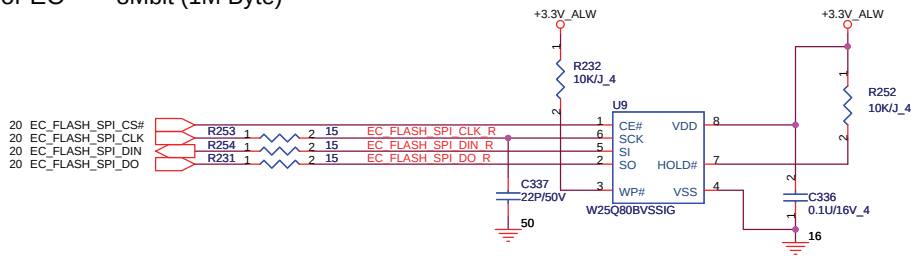
PCIE_TX5+ PCIE_TX5- PCIE_RX5- PCIE_RX5+

Quanta Computer Inc.			
PROJECT : Calpella UMA			
Size	Document Number		Rev
	Card Reader (JMB389A)		1A
Date: Friday, January 15, 2010		Sheet 17 of 40	

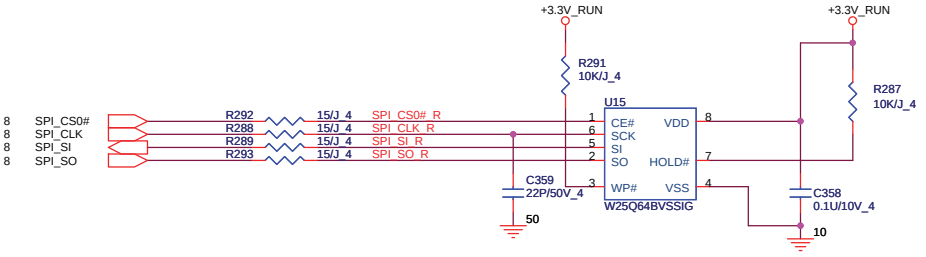


Quanta Computer Inc.		
PROJECT : Calpella UMA		
Size	Document Number: HDMI CONN	Rev: 1A
Date: Friday, January 15, 2010	Sheet 18 of 40	

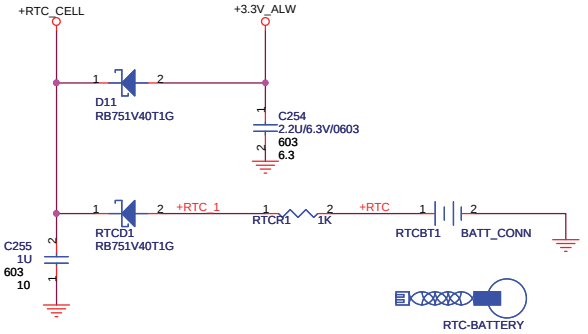
For EC 8Mbit (1M Byte)



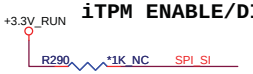
For PCH 64Mbit (8M Byte), SPI



RTC BATTERY



iTPM ENABLE/DISABLE

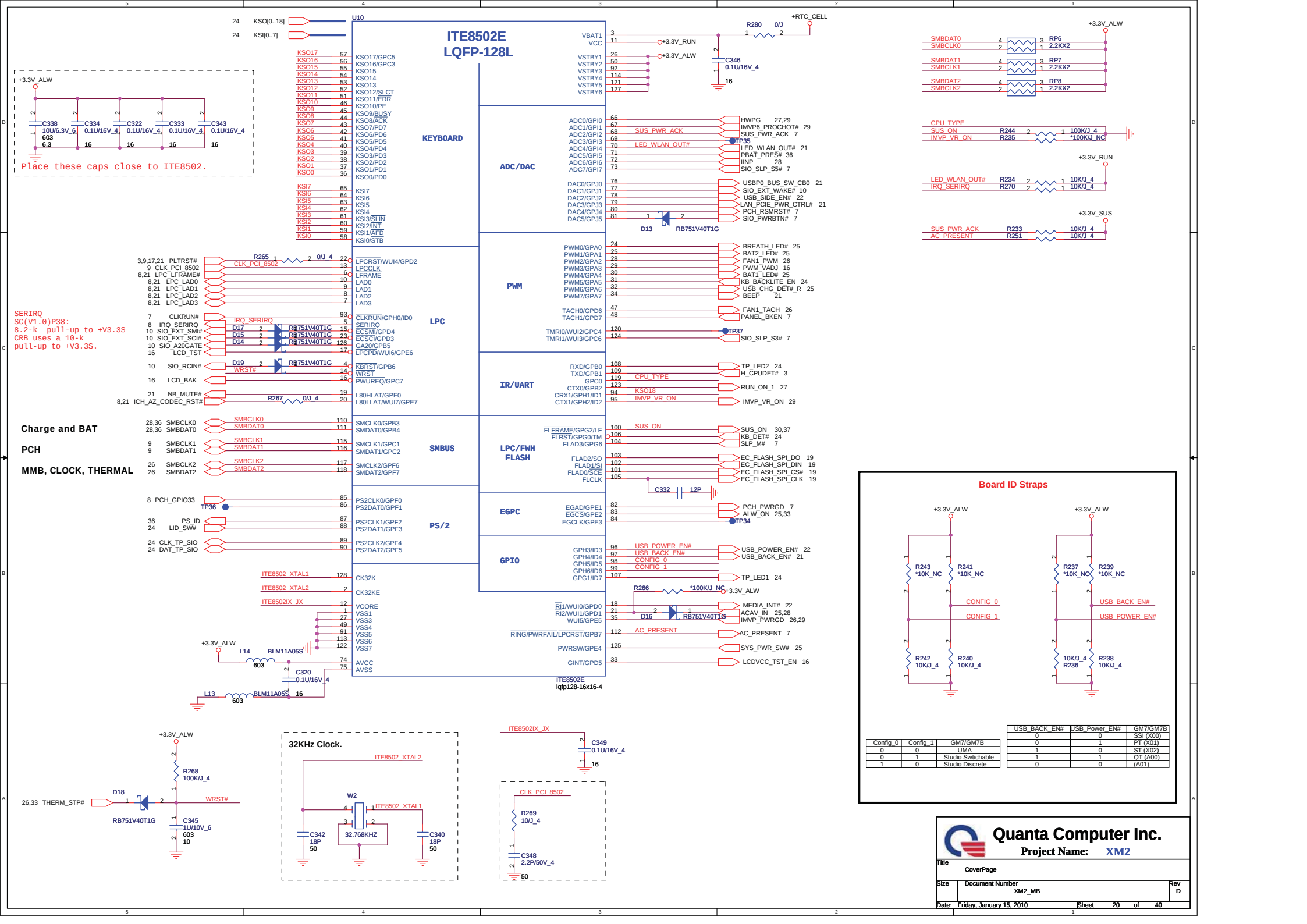


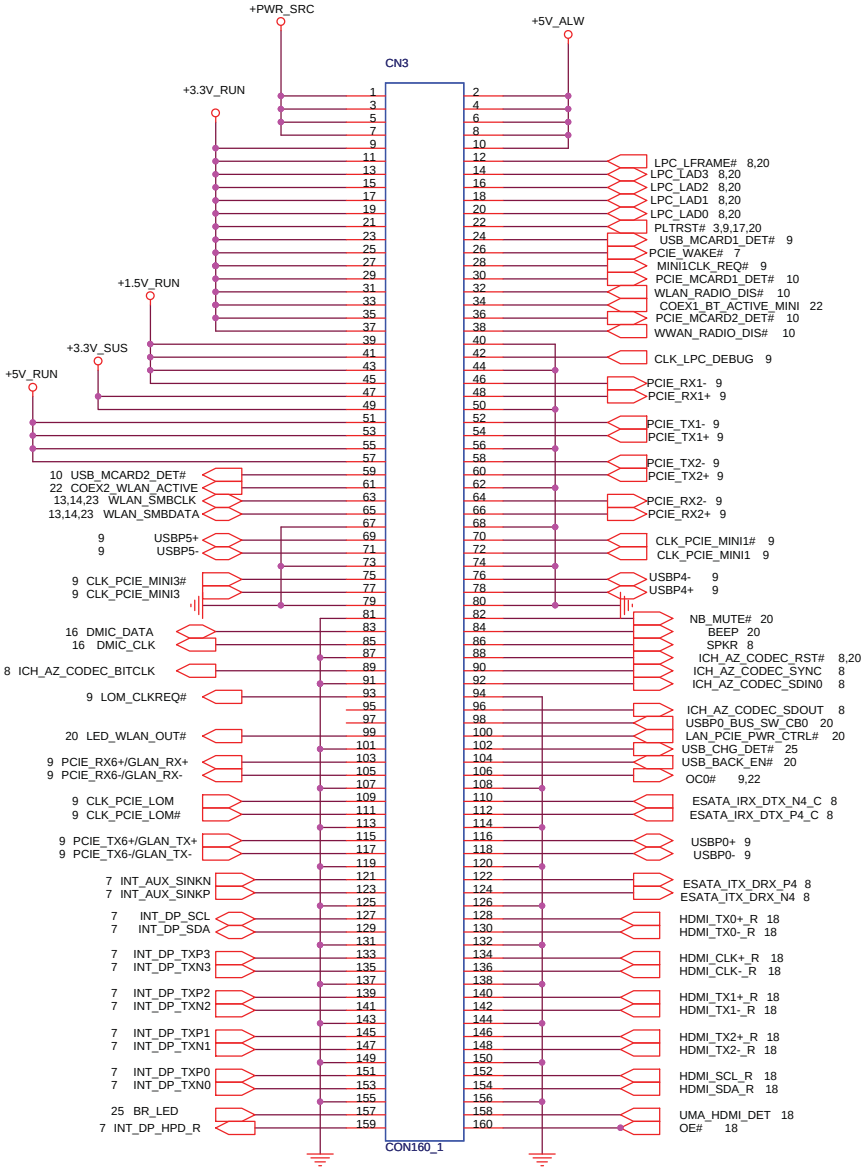
TPM Function	R712
Enable	Mount
Disable	NC (Default)

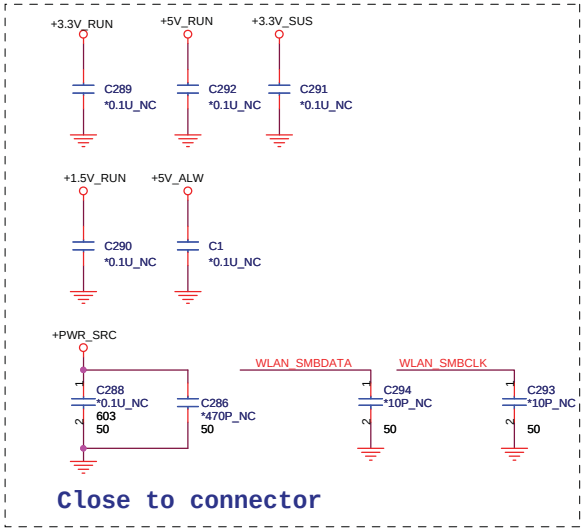
Quanta Computer Inc.

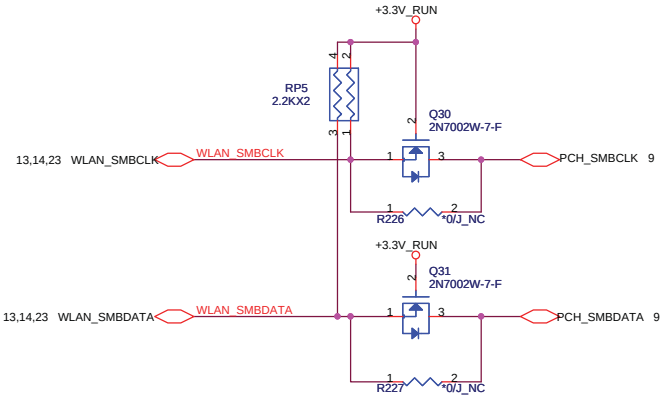
PROJECT : Calpella UMA

Size	Document Number	Rev
	FLASH / RTC	1A
Date: Friday, January 15, 2010	Sheet 19 of 40	


ITE8502E
LQFP-128L
U10
KEYBOARD
ADC/DAC
PWM
LPC
IR/UART
SMBUS
LPC/FWH FLASH
EGPC
PS/2
GPIO
Charge and BAT
PCH
MMB, CLOCK, THERMAL
Place these caps close to ITE8502.
SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k
pull-up to +V3.3S.
Board ID Straps
32KHz Clock.
Quanta Computer Inc.
Project Name: XM2
CoverPage
XM2_MB
Friday, January 15, 2010







Quanta Computer Inc.

PROJECT : Calpella UMA

Size	Document Number	Rev
	DBC01(WLAN/WPAN)	1A
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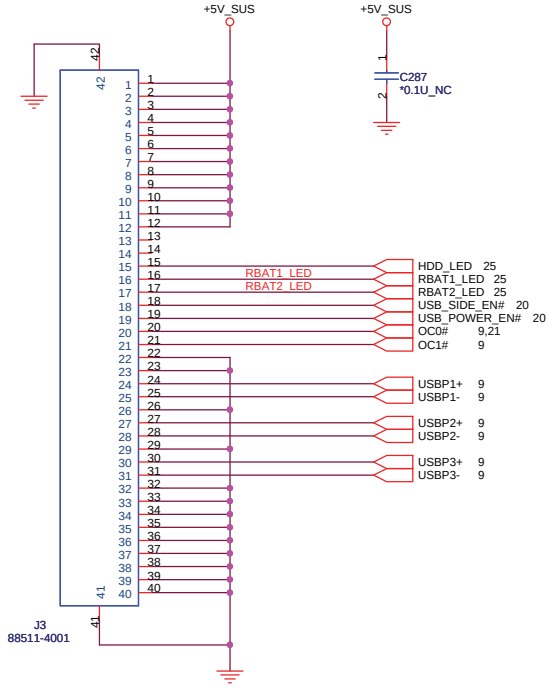
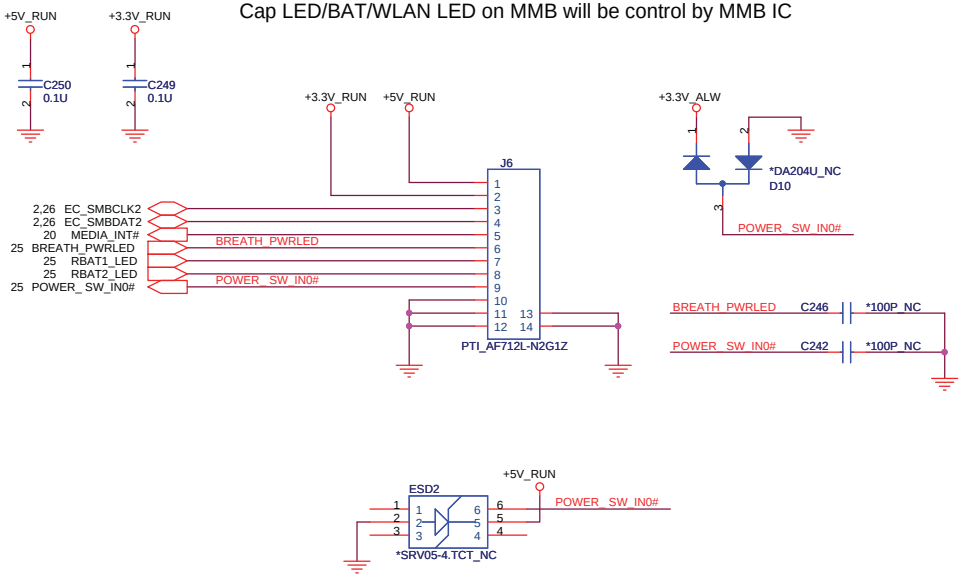
USB IO 40 pins

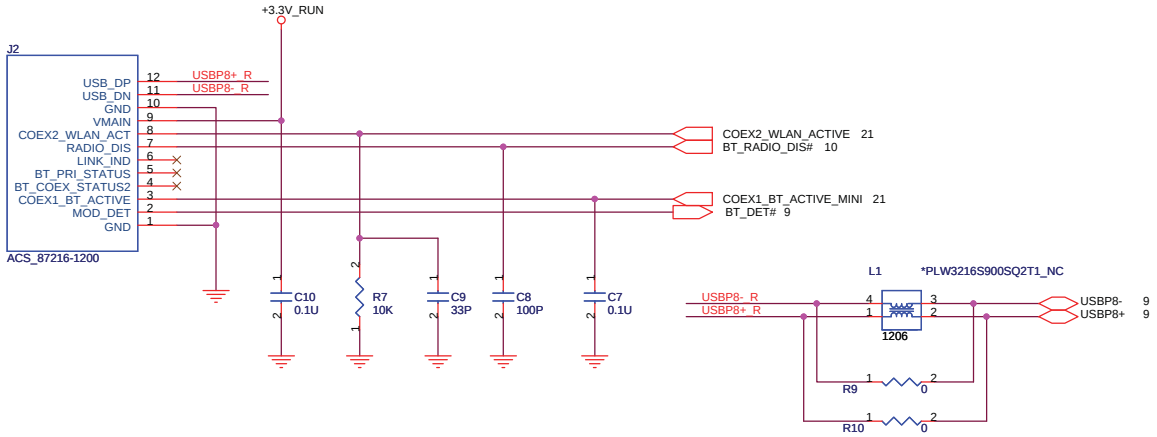


MMB & Power Board 12pins

Cap LED/BAT/WLAN LED on MMB will be control by MMB IC



Support Dell BT3xx series module
Bluetooth WTB Conn



Quanta Computer Inc.		
PROJECT : Calpella UMA		
Size	Document Number: Left USB / MMB CONN	Rev: 1A
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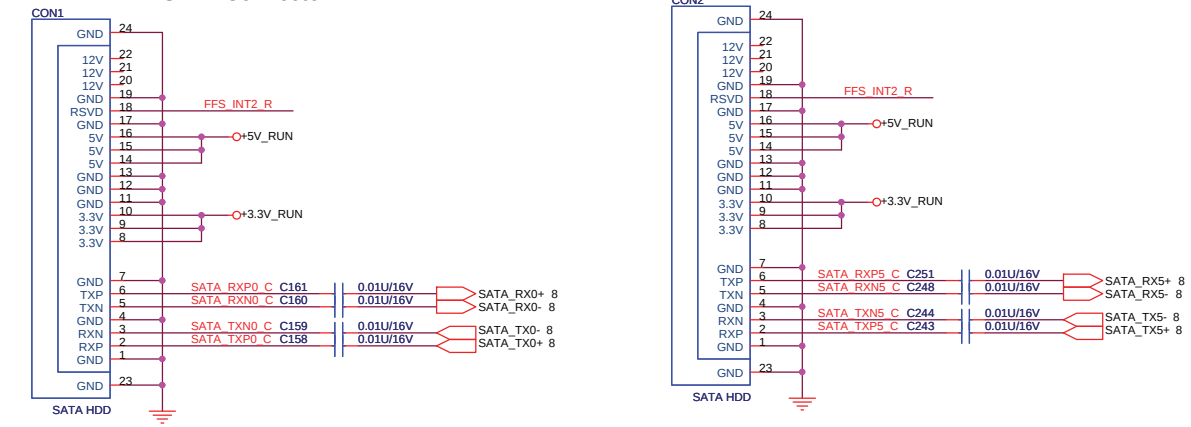
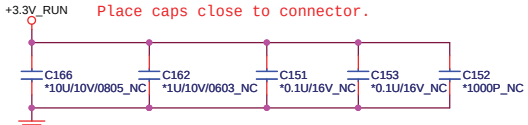
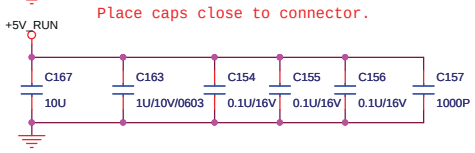
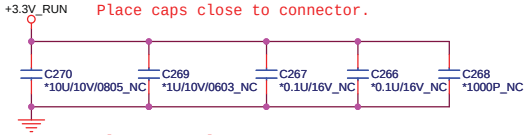
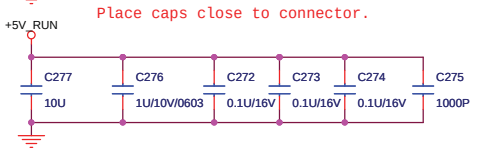
SATA Connector.



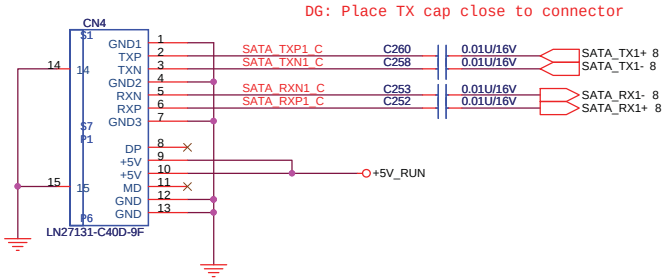


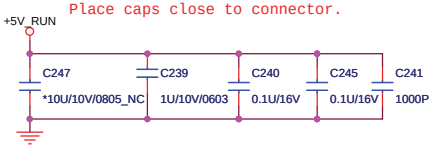




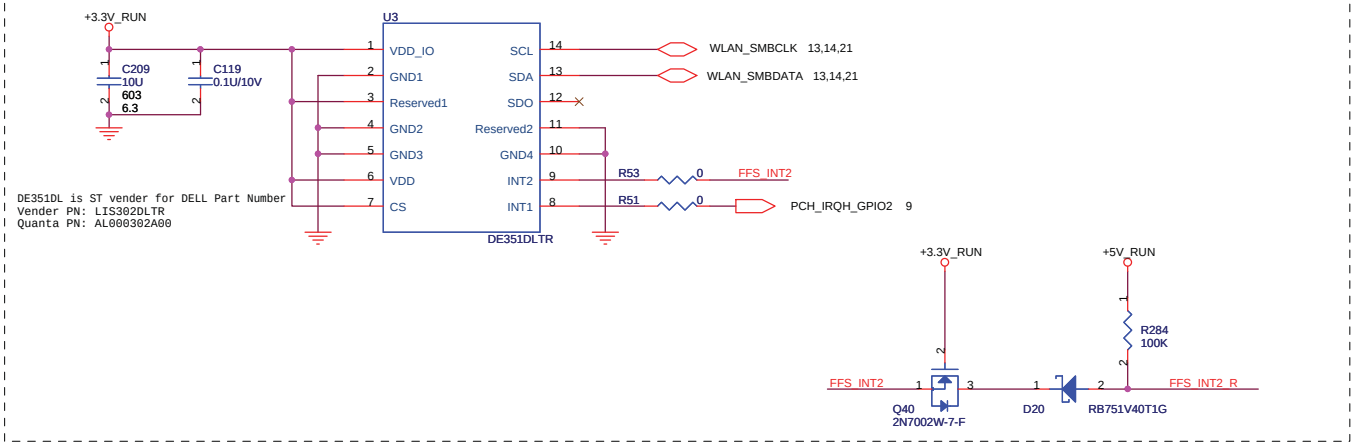


ODD Connector





3-axis Fall Sensor (HDD data protector)



Quanta Computer Inc.

PROJECT : Calpella UMA

Size	Document Number	Rev
	SATA (HDD&ODD)	1A
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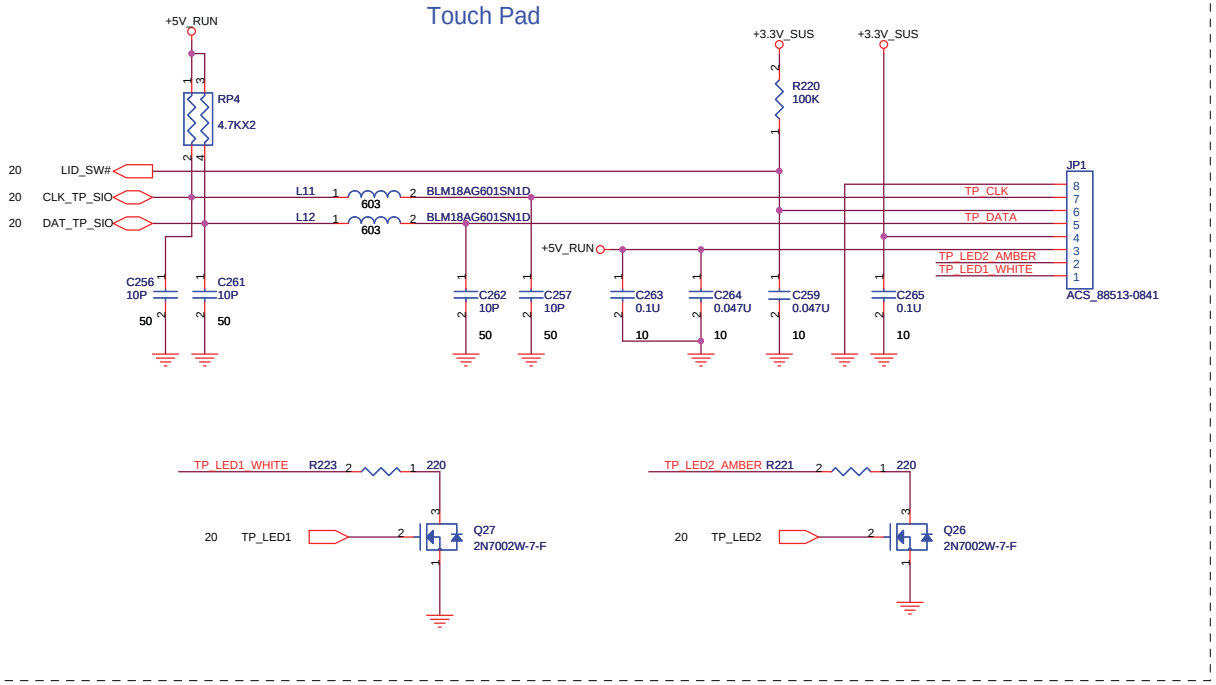
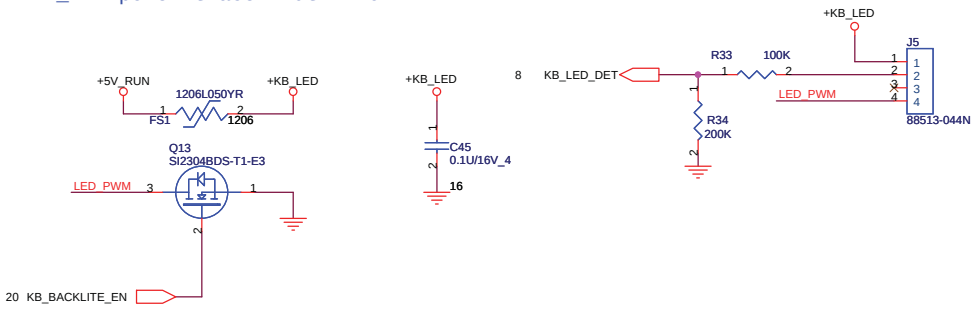
Touch Pad

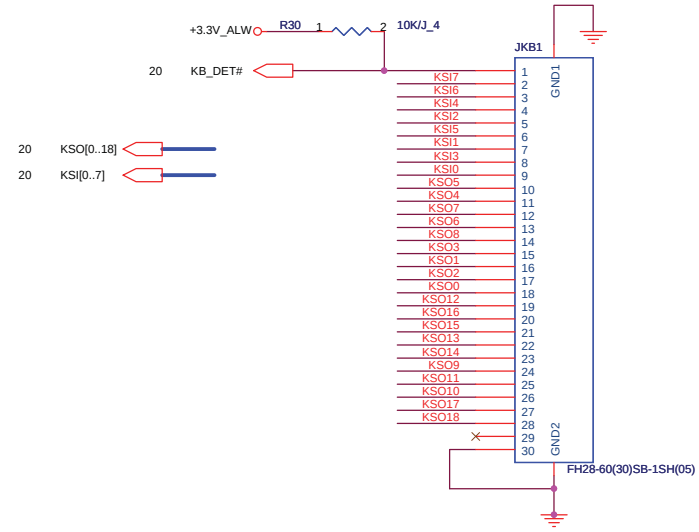


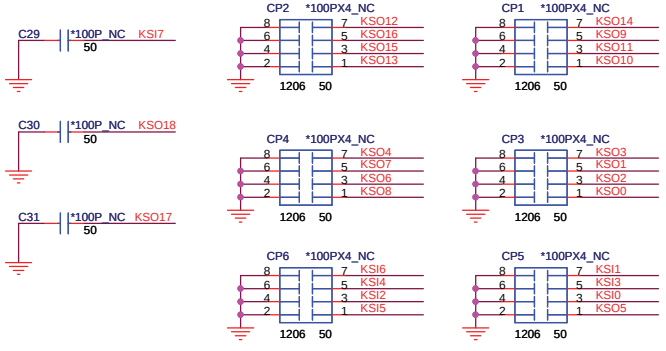
Key board illumination

+KB_LED power trace width >10 mil



KEYBOARD CONNECTOR





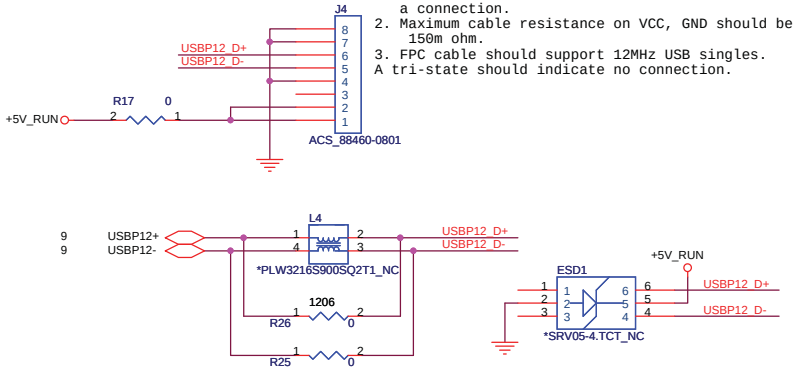
100P CAPS CLOSE TO JKB1

Quanta Computer Inc.
PROJECT : Calpella UMA

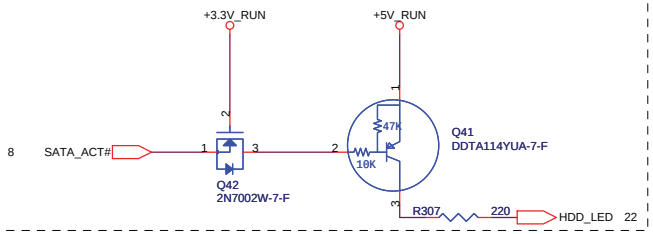
Size	Document Number	Rev
	TP / KB	1A
Date: Friday, January 15, 2010	Sheet 24 of 40	

Touch Screen Module

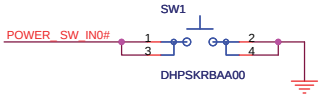
Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
2. Maximum cable resistance on VCC, GND should be 150m ohm.
3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



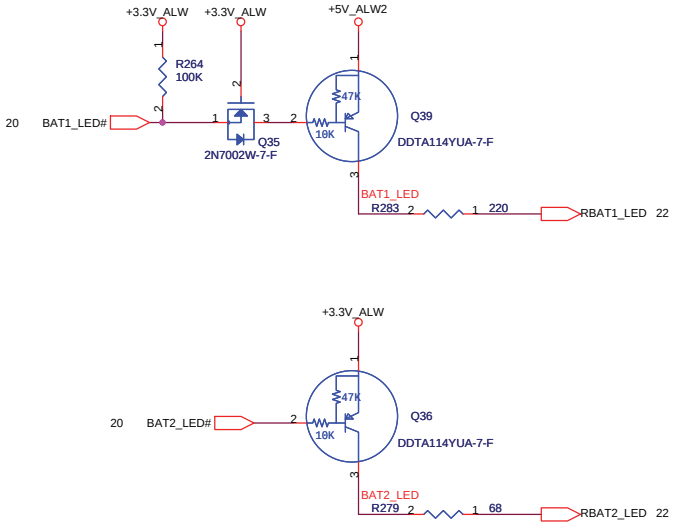
HDD activity LED.

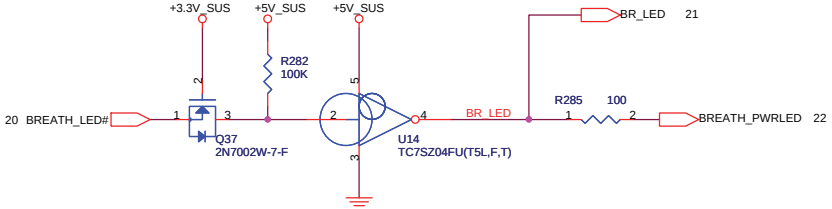


Power button for Engineer

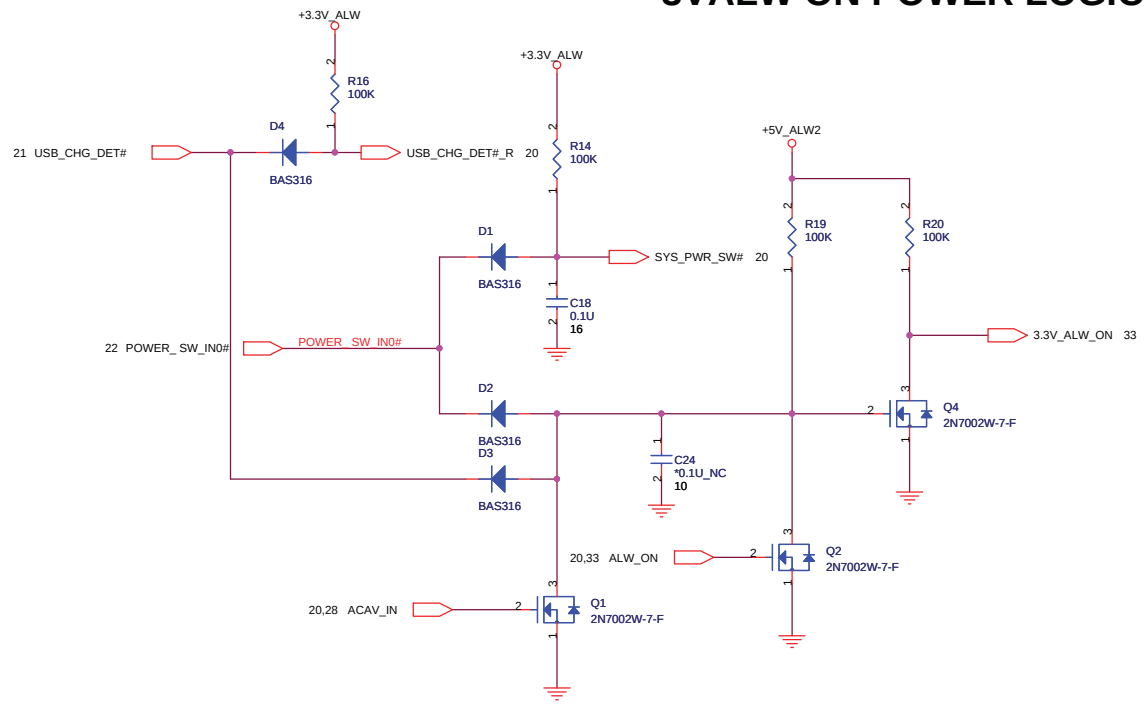


Battery status.





3VALW ON POWER LOGIC



Quanta Computer Inc.
PROJECT : Calpella UMA

Size	Document Number	Rev
	SWITCH / LED / T-Screen	1A
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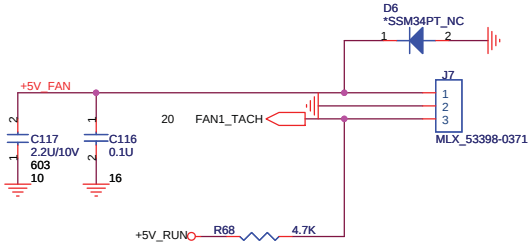
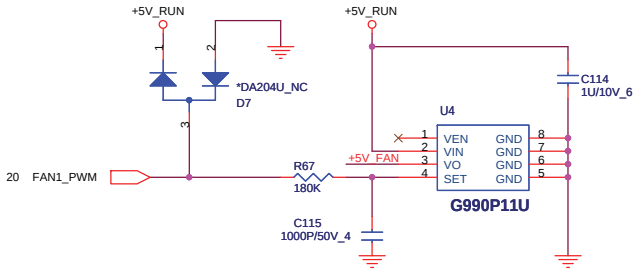
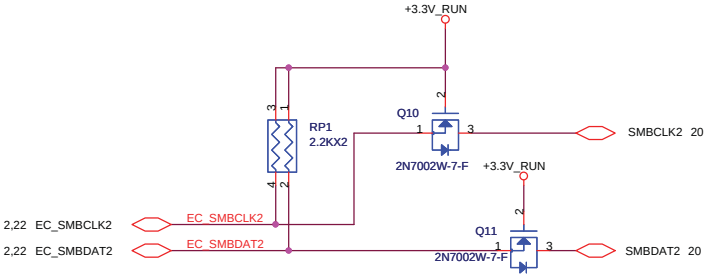
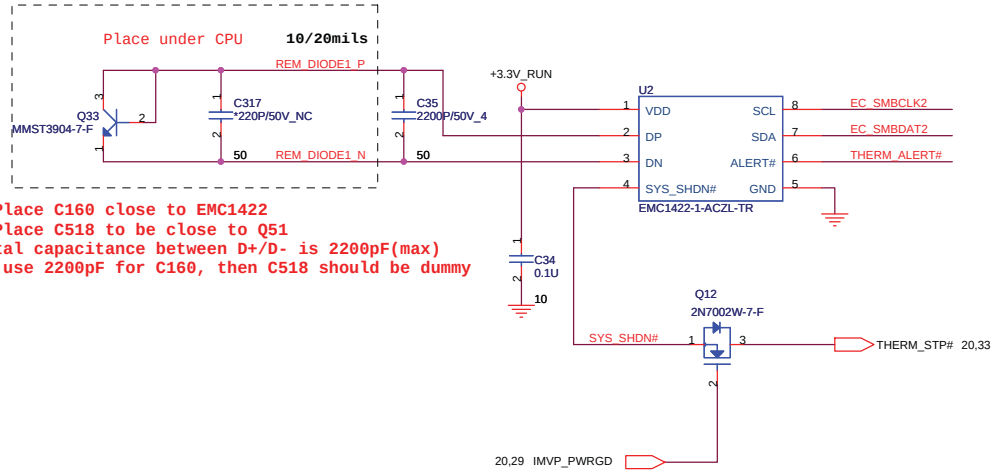


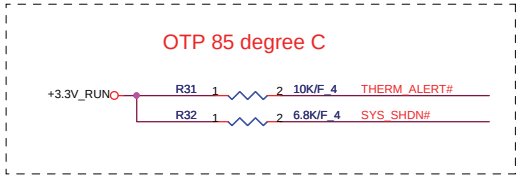




0907 Steg: Need to check C484 if needed



1.Place C160 close to EMC1422
2.Place C518 to be close to Q51
Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C160, then C518 should be dummy



Quanta Computer Inc.		
PROJECT : Calpella UMA		
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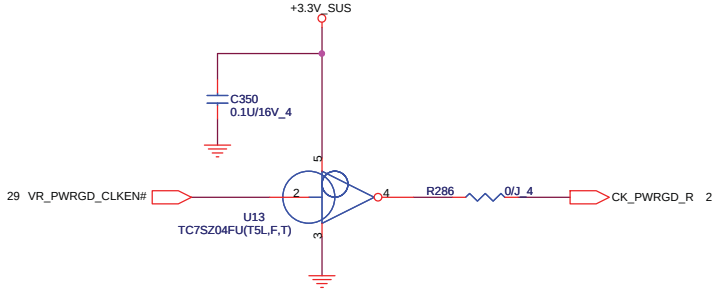

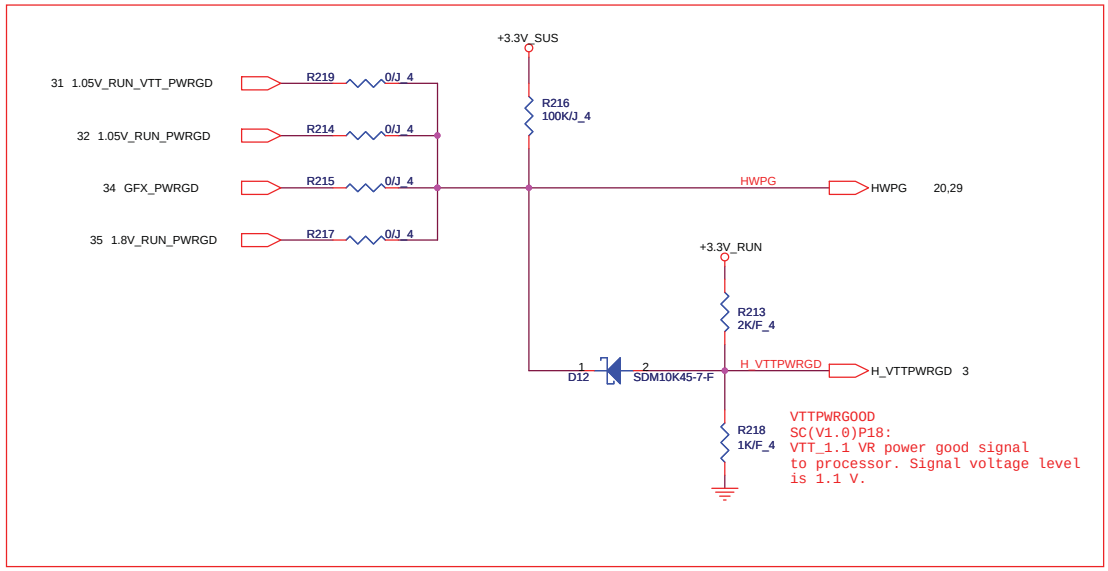

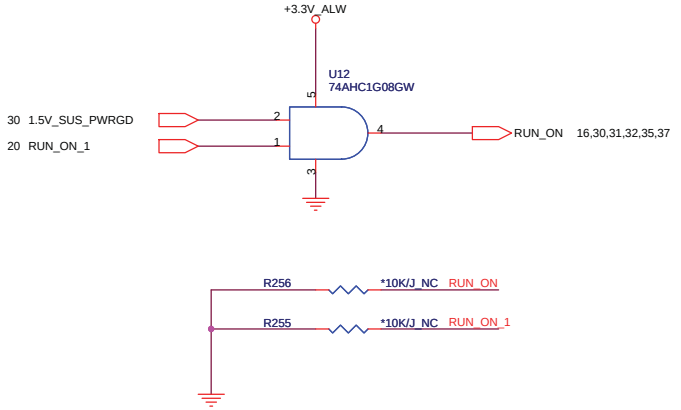

Quanta Computer Inc.		
PROJECT : Calpella UMA		
Size	Document Number: System Reset Circuit	Rev: 1A
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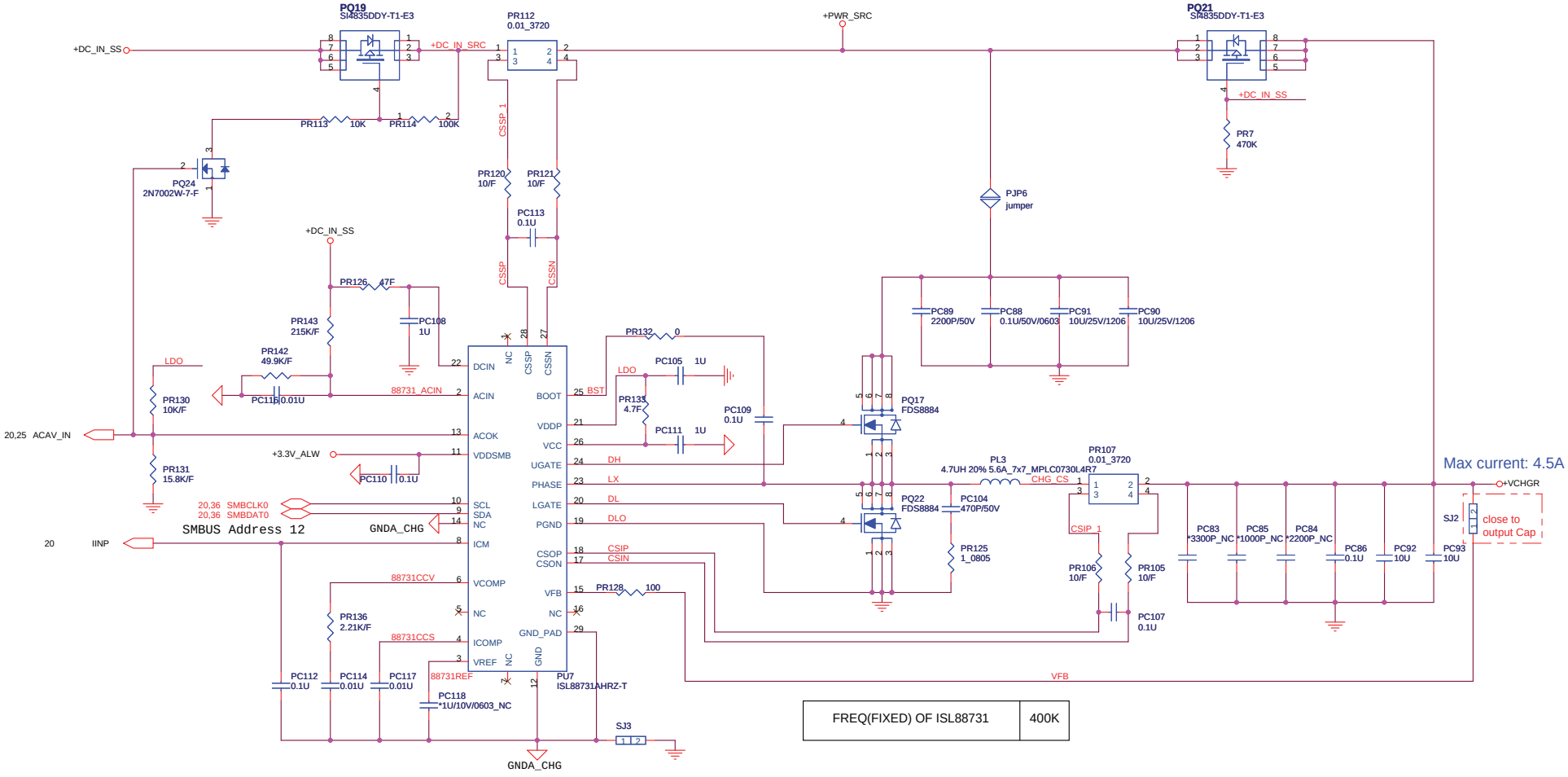

Quanta Computer Inc.	Project Name: XM2
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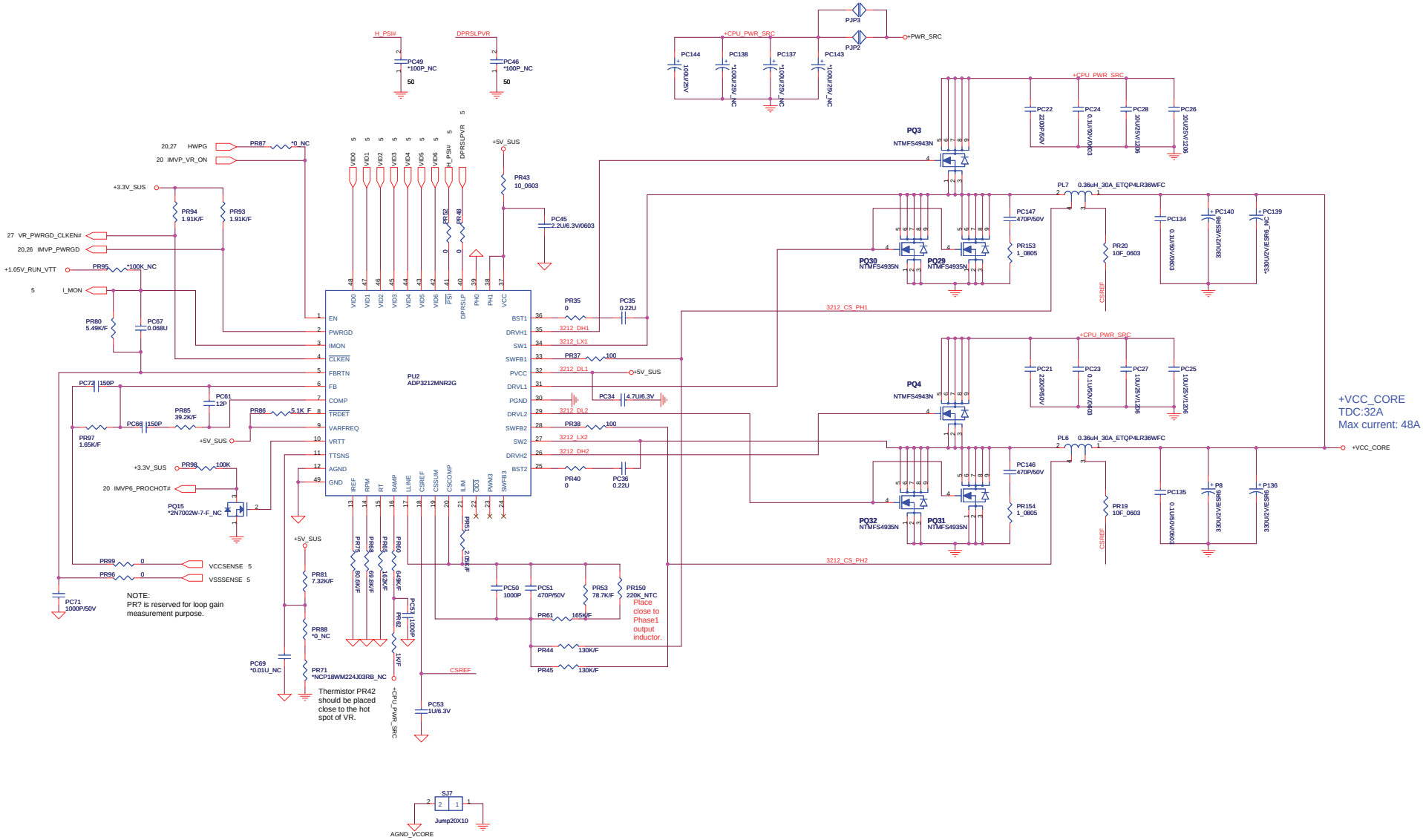

Quanta Computer Inc.			
Project Name: XM2			
Title: CoverPage			
Size	Document Number: XM2_MB		Rev: D
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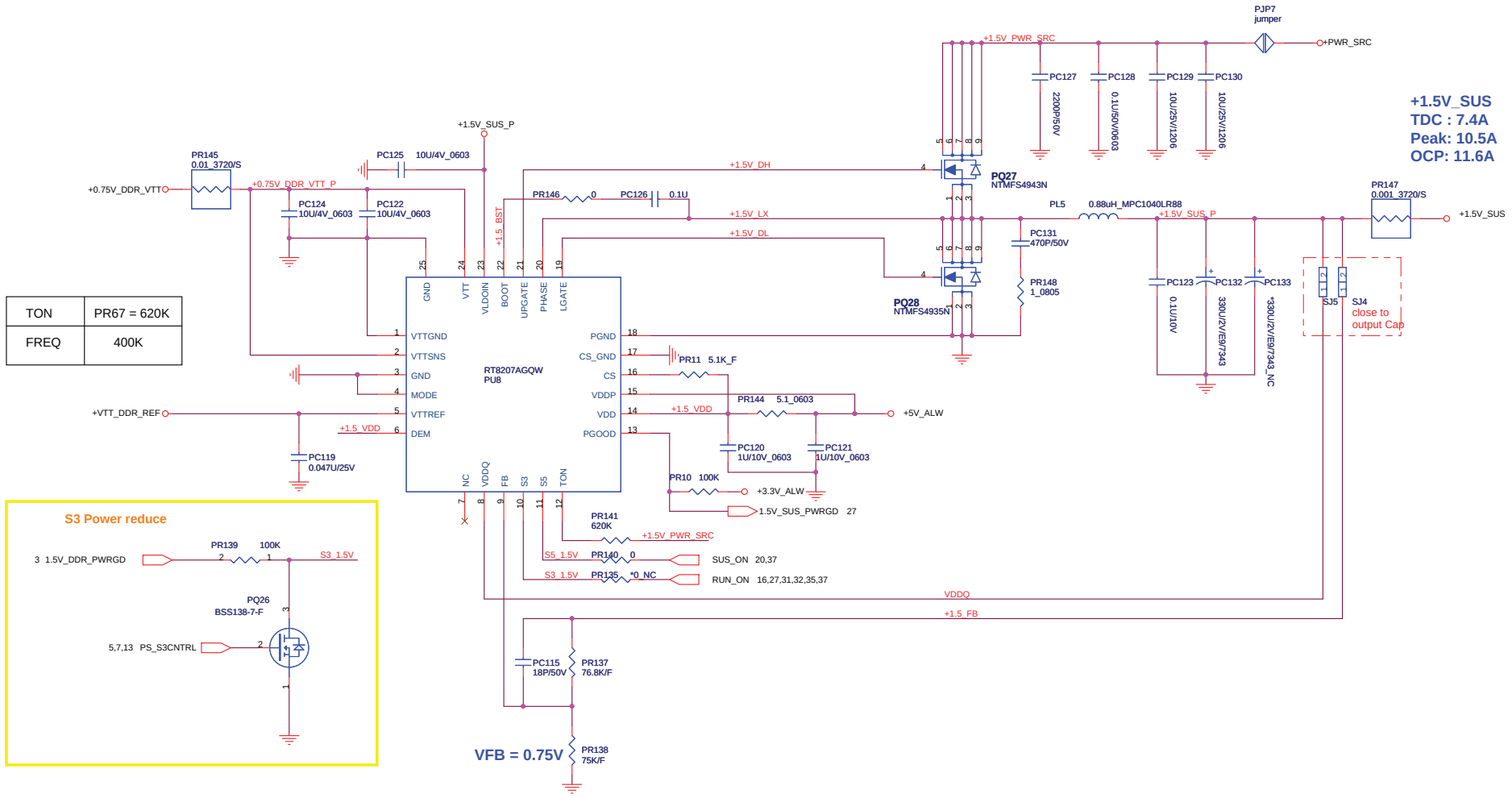

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
GND	Non-tracking discharge

VDDQ output voltage selection

FB	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	0.75V < VDDQ < 3.3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

Quanta Computer Inc.
Project Name: XM2

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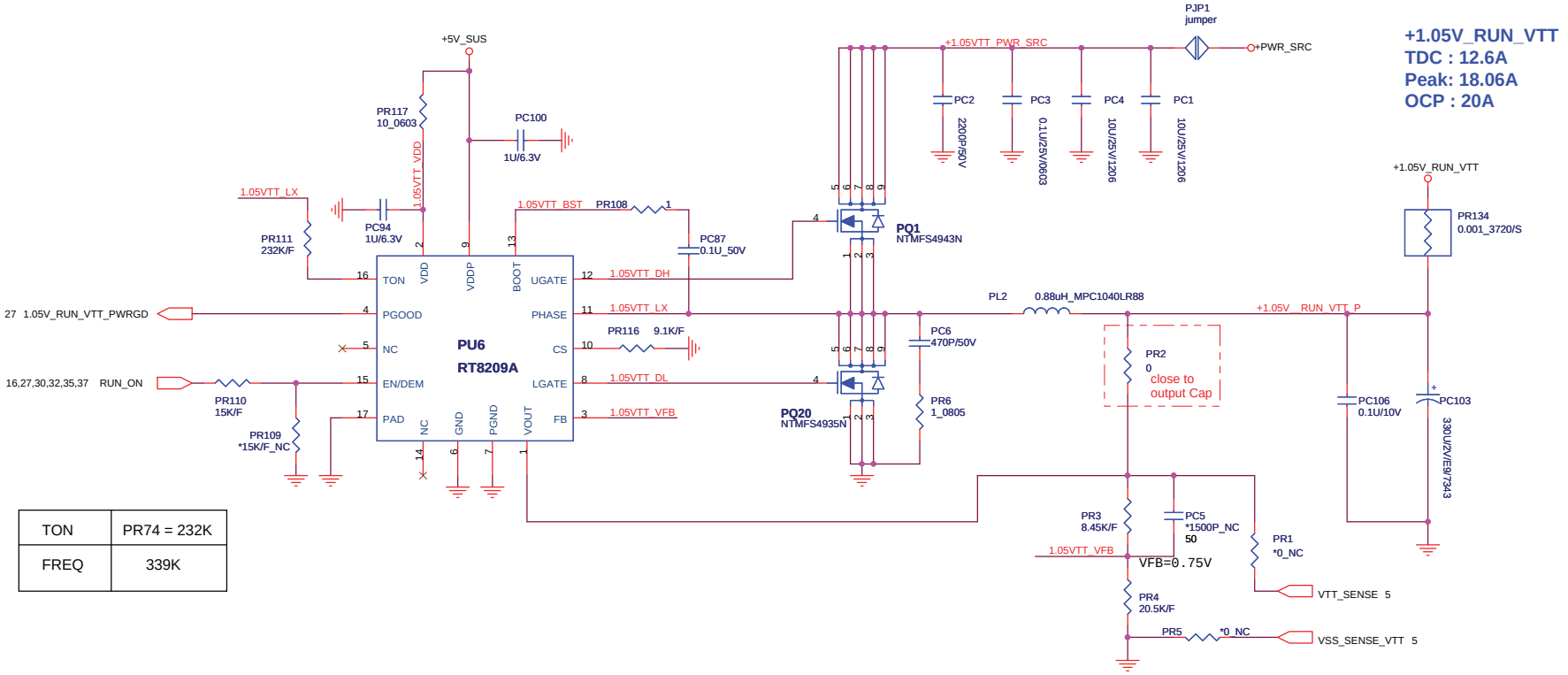

TON	PR74 = 232K
FREQ	339K

Quanta Computer Inc.

Project Name: XM2

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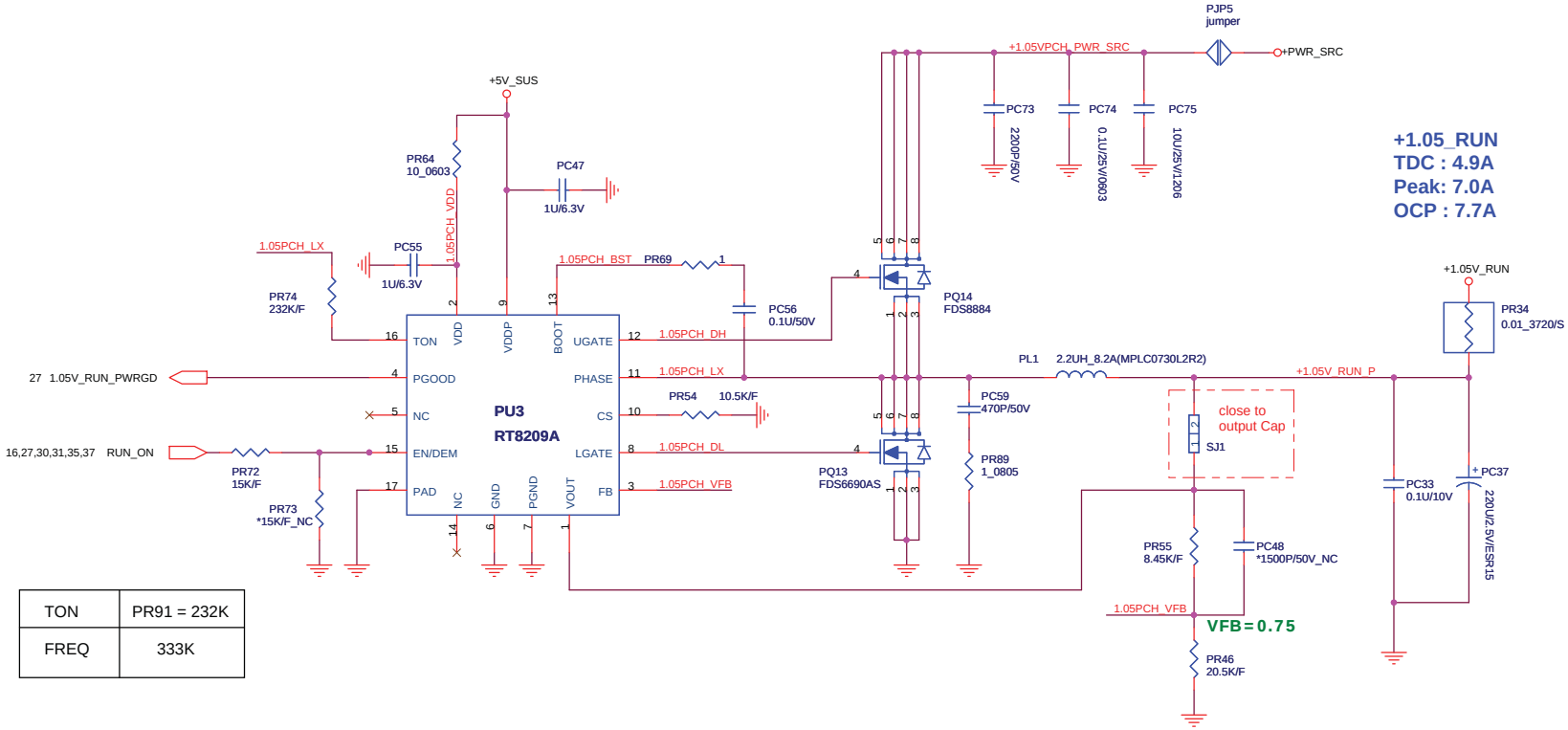

TON	PR91 = 232K
FREQ	333K

Quanta Computer Inc.

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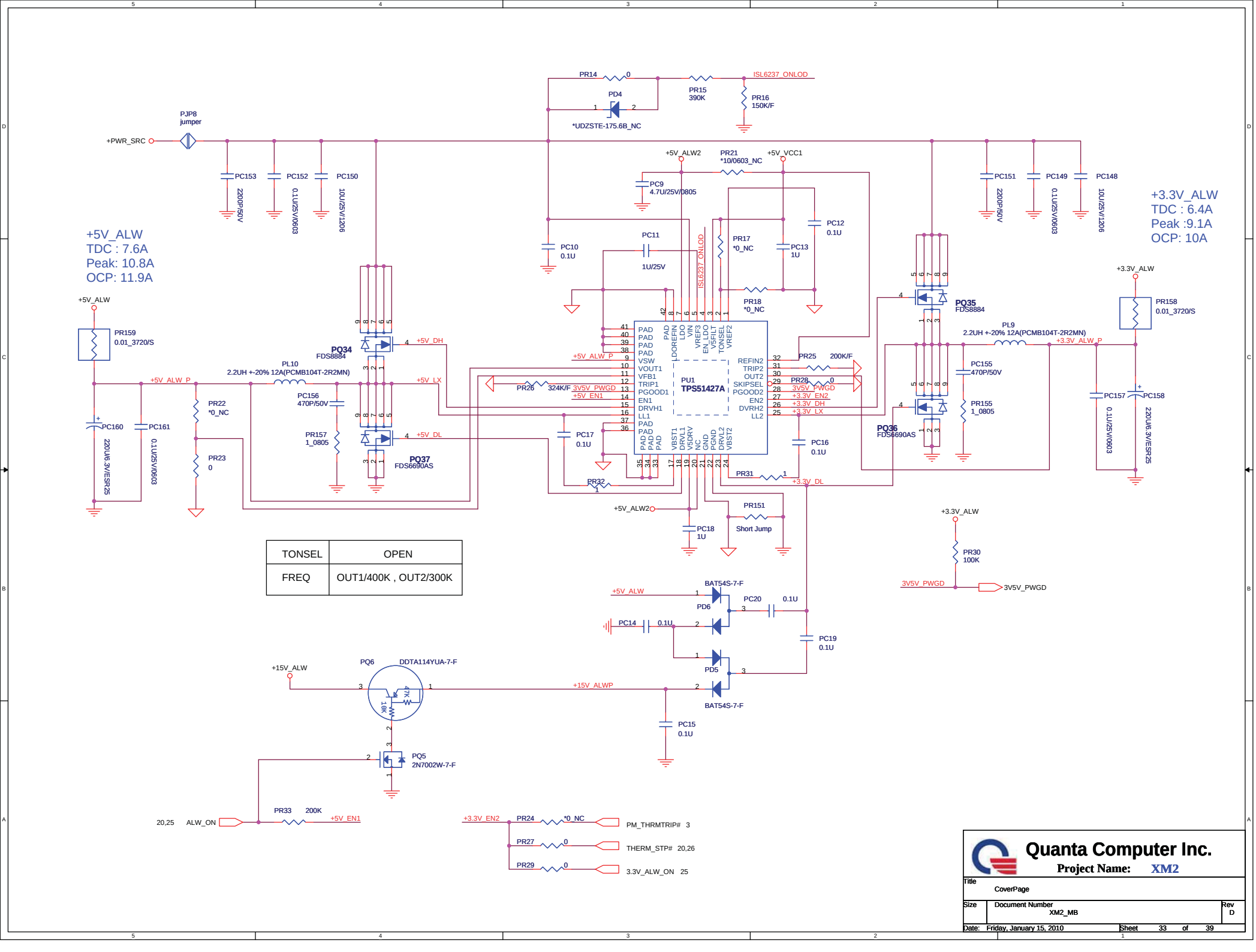

TONSEL	OPEN
FREQ	OUT1/400K , OUT2/300K

Quanta Computer Inc.

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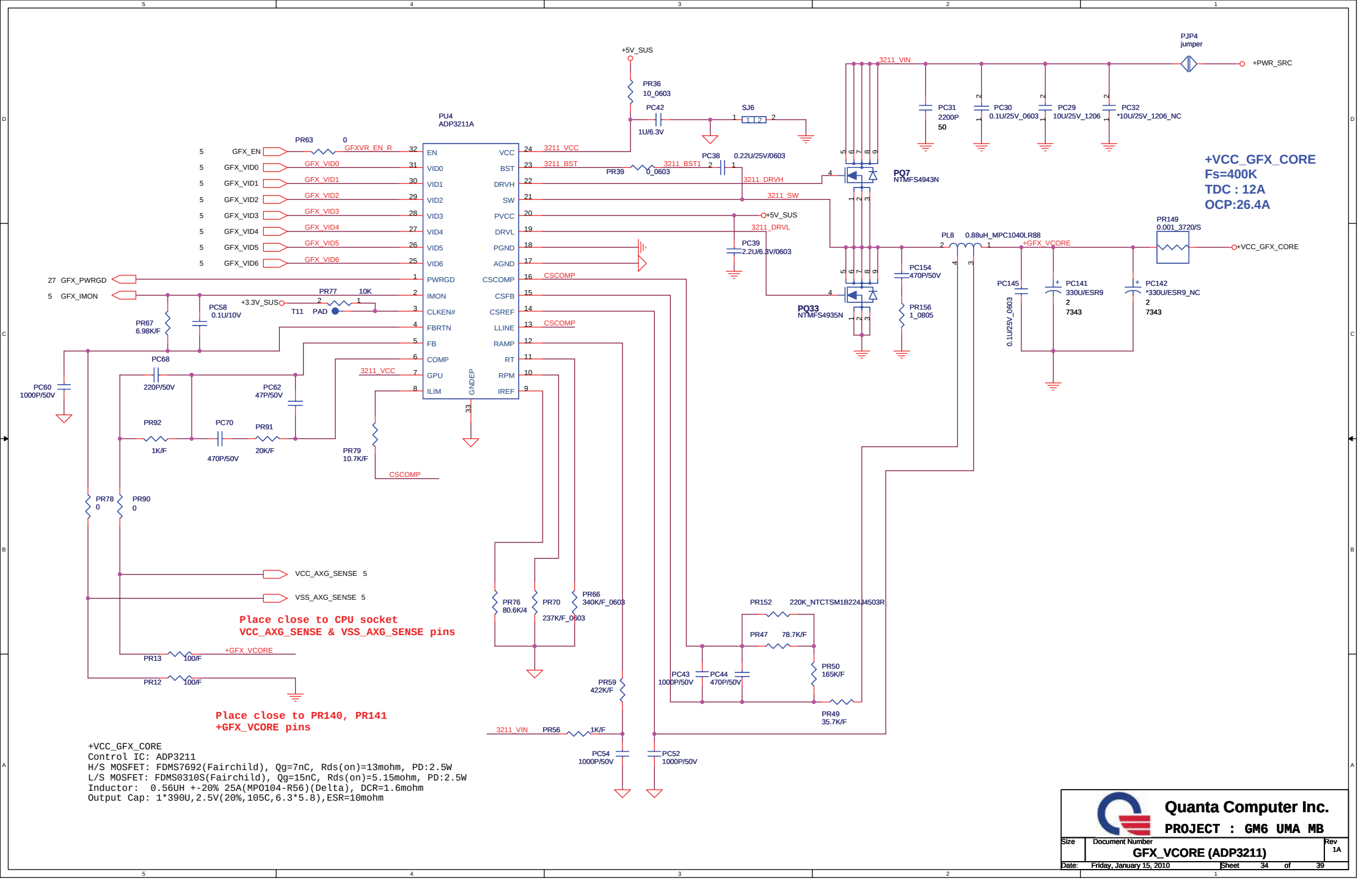
+VCC_GFX_CORE
Fs=400K
TDC : 12A
OCP:26.4A
PU4
ADP3211A
PQ7
NTMFS4943N
PQ33
NTMFS4935N
PJP4
jumper
+PWR_SRC
+VCC_GFX_CORE
PL8
0.88uH_MPC1040LR88
+GFX_VCORE
Place close to CPU socket
VCC_AXG_SENSE & VSS_AXG_SENSE pins
Place close to PR140, PR141
+GFX_VCORE pins
+VCC_GFX_CORE
Control IC: ADP3211
H/S MOSFET: FDMS7692(Fairchild), Qg=7nC, Rds(on)=13mohm, PD:2.5W
L/S MOSFET: FDMS0310S(Fairchild), Qg=15nC, Rds(on)=5.15mohm, PD:2.5W
Inductor: 0.56UH +-20% 25A(MPO104-R56)(Delta), DCR=1.6mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm
Quanta Computer Inc.
PROJECT : GM6 UMA MB
GFX_VCORE (ADP3211)
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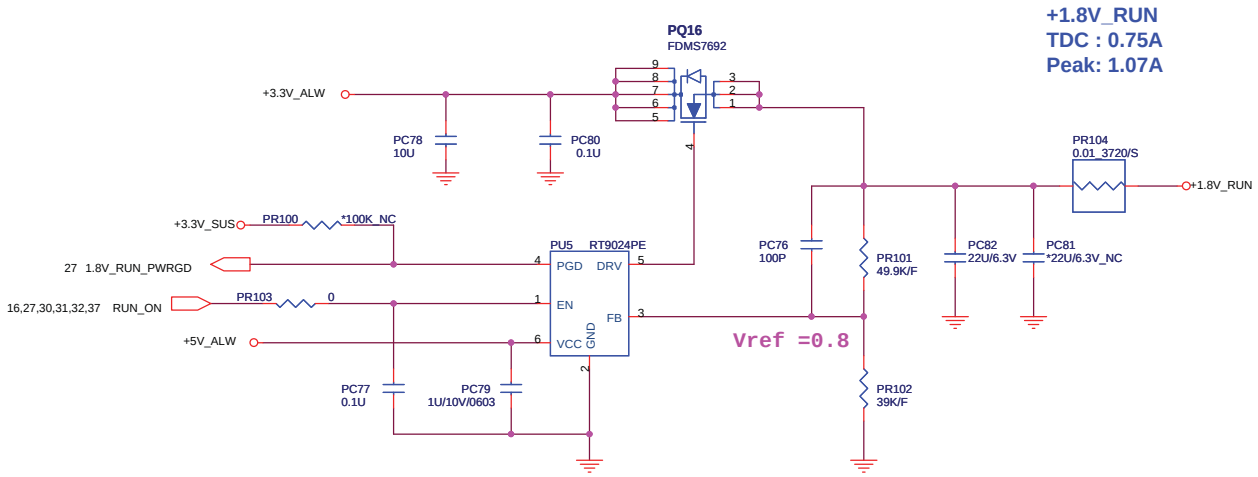

Quanta Computer Inc.		
Project Name: XM2		
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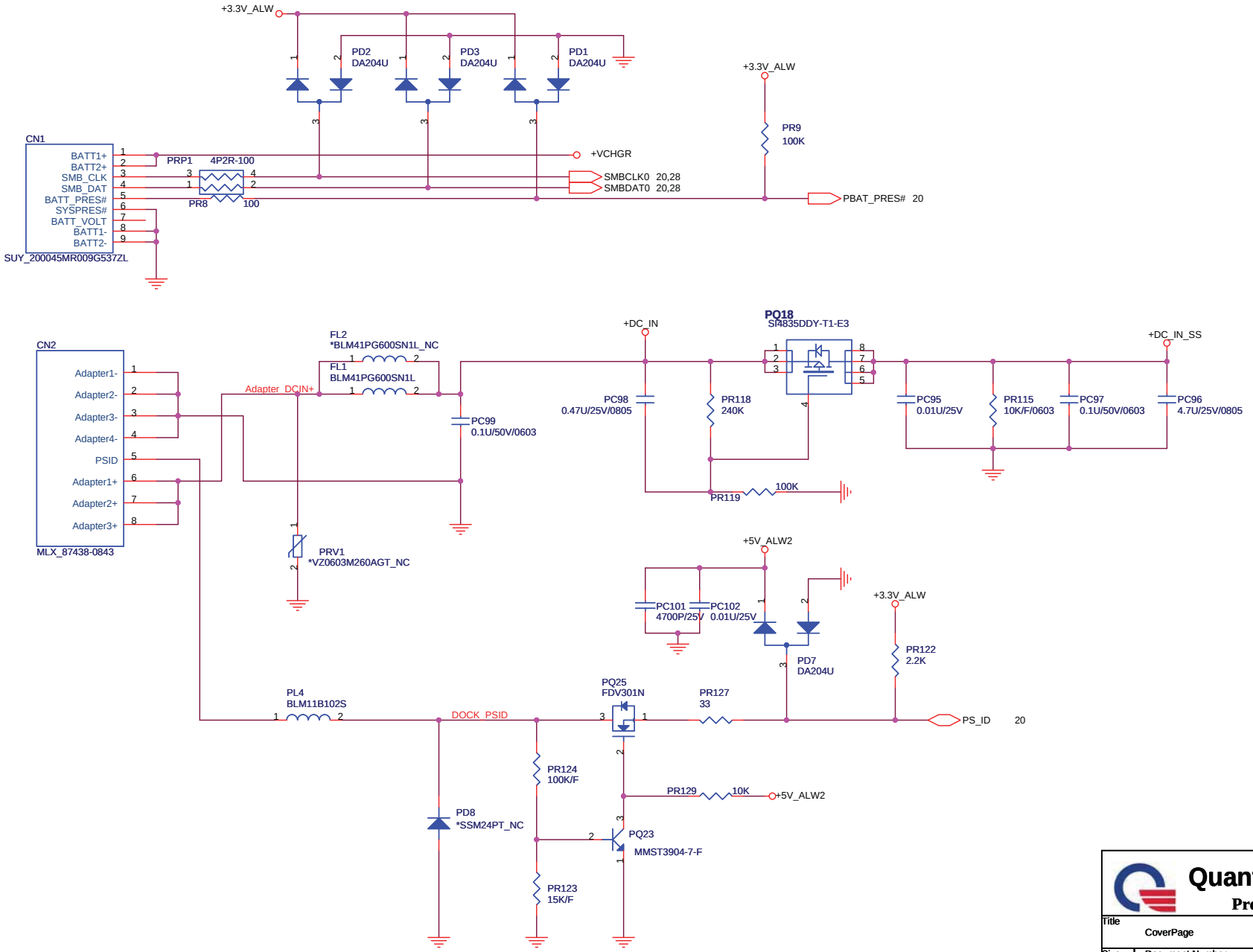

Quanta Computer Inc.

Project Name: XM2

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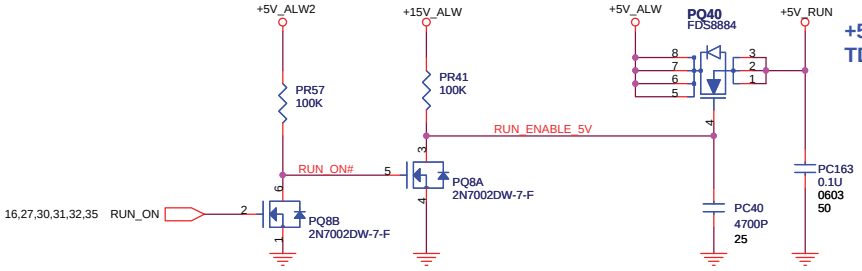
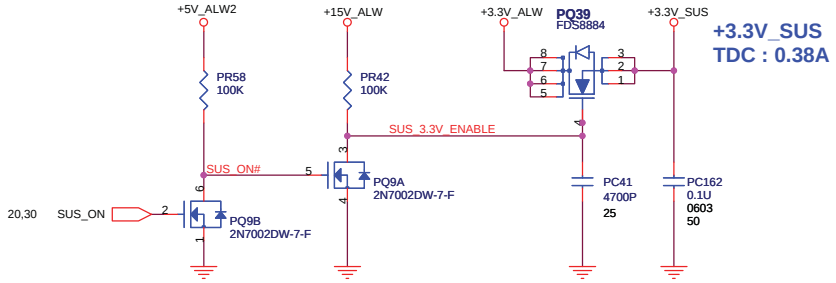
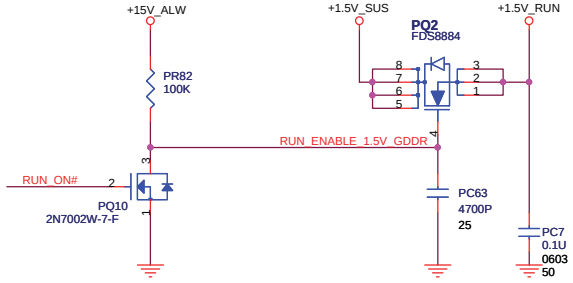


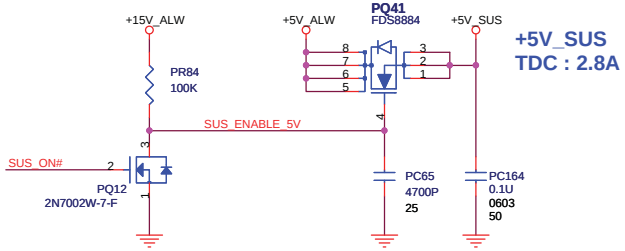
+5V_RUN
TDC : 3.38A



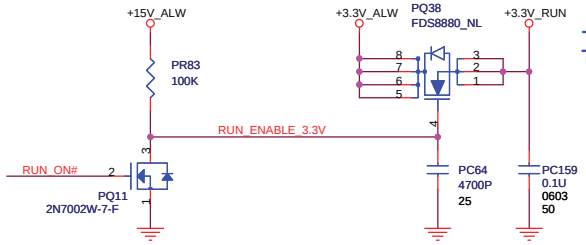
+3.3V_SUS
TDC : 0.38A



+1.5V_RUN
TDC : 0.35A

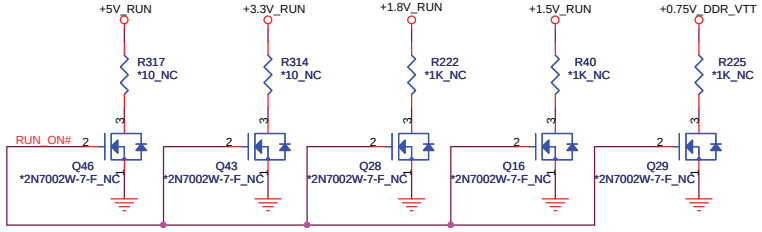


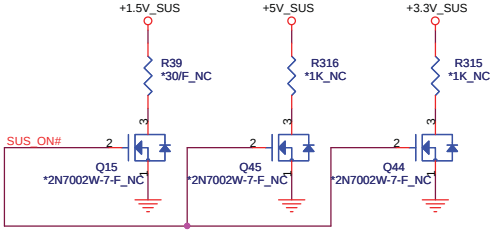
+5V_SUS
TDC : 2.8A



+3.3V_RUN
TDC : 5.4A

Reserve discharge path





Quanta Computer Inc.
Project Name: XM2

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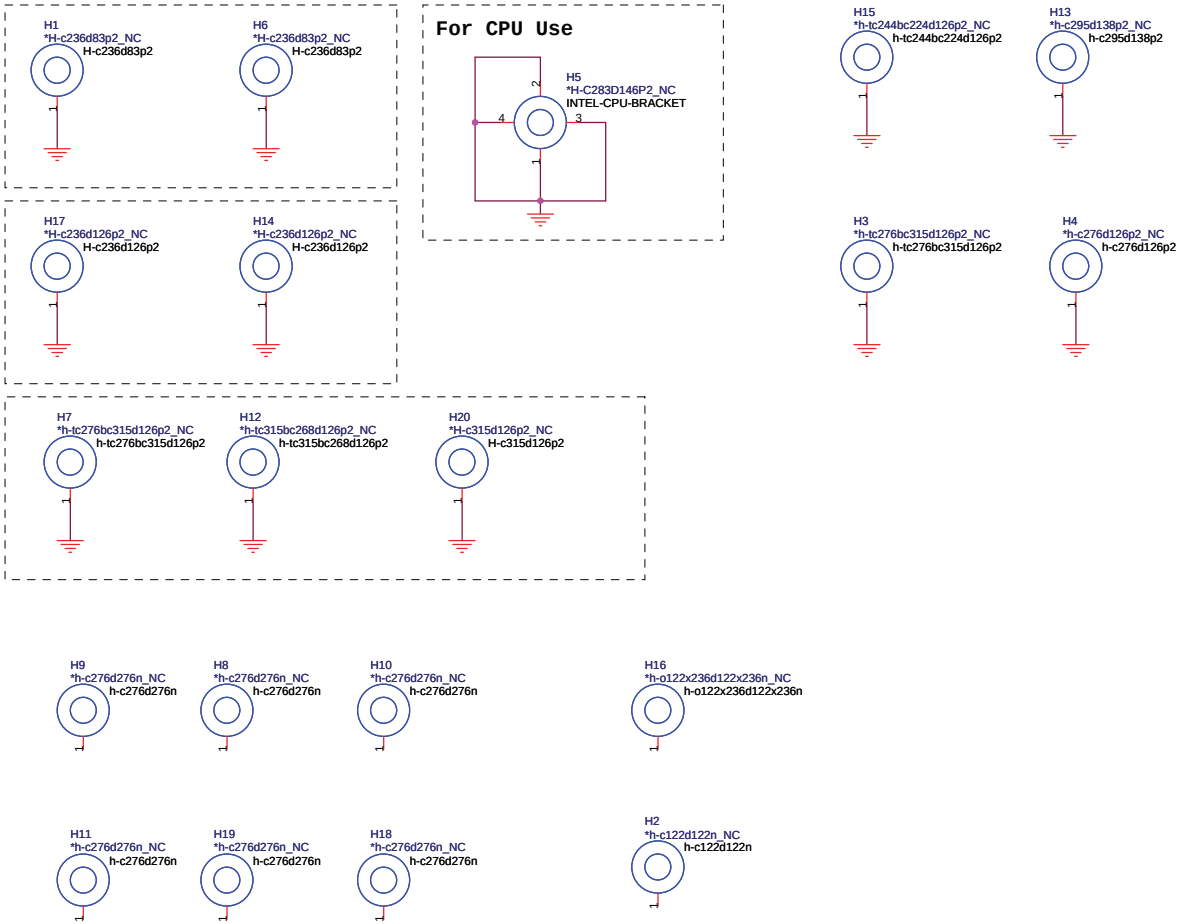

Quanta Computer Inc.

Project Name: GM7

Title	PAD & SCREW	
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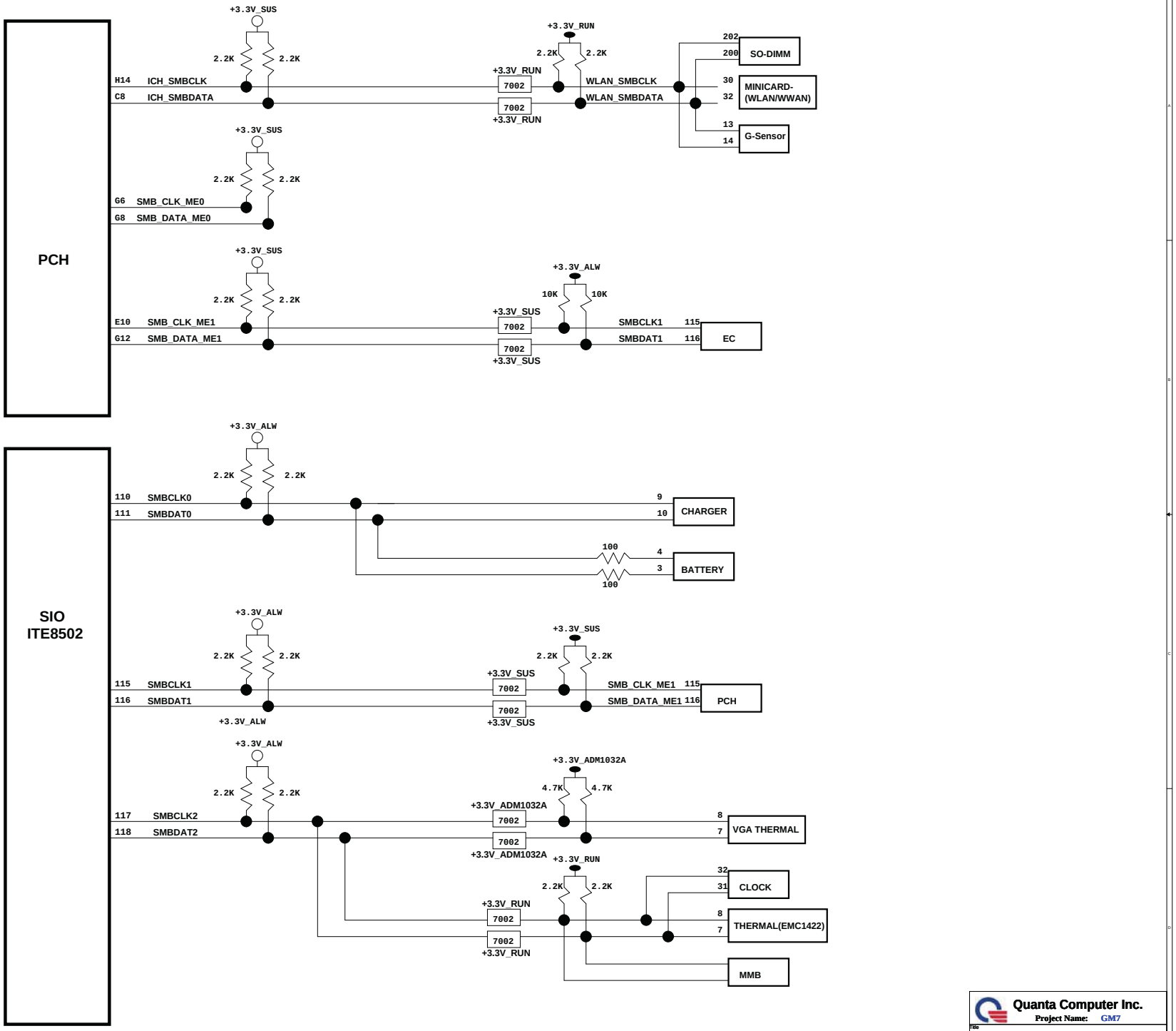

Quanta Computer Inc.
Project Name: GM7

Title	SMBus	
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