LTspice Tutorial: Part 6

Creating LTspice® MOSFET models
LTspice Tutorial 4 explained that there are 2 different types of SPICE model: those defined by the simple .MODEL statement and those defined by the more complex .SUBCKT statement. The .MODEL statement defines simple components such as diodes, transistors, MOSFETs etc with a list of predefined characteristics given to us by the writers of SPICE programs. The more esoteric components such as op amps, comparators etc were defined by a more general .SUBCKT model.

When SPICE (not LTspice) was first created, the programmers gave the user a specific number of characteristics to define certain components. In the case of the MOSFET, this included the gate source turn on voltage, the transconductance, the resistance of the gate, source and drain connections etc. These are known as Level 1 parameters and define the most important parameters of the MOSFET. In later years, the MOSFET manufacturers wanted to further characterise their MOSFETs and not be restricted by the fixed list of parameters given to them by the writers of SPICE. They therefore turned to the .SUBCKT definition to allow them to expand the list of parameters. These are known as Level 2 and Level 3 parameters and describe characteristics of the MOSFET not defined in the original SPICE definition of a MOSFET. However in making the model more complicated, they slowed down the simulation time of the MOSFET.

LTspice therefore uses the simpler .MODEL statement to define the characteristics of a MOSFET. If using a 3rd party MOSFET model results in very slow simulation performance, it is probably because the model is defined using the .SUBCKT model and includes many parameters that are not necessary in getting an idea of the circuit performance.

To create an LTspice model of a given MOSFET, you need the original datasheet and the pSPICE model of that MOSFET.

The parameters needed to define a MOSFET in LTspice are as follows:

Rg   Gate ohmic resistance
Rd   Drain ohmic resistance (this is NOT the RDSon, but the resistance of the bond wire)
Rs   Source ohmic resistance.
Vto   Zero-bias threshold voltage.
Kp –   Transconductance coefficient
Lambda Change in drain current with Vds
Cgdmax Maximum gate to drain capacitance.
Cgdmin   Minimum gate to drain capacitance.
Cgs   Gate to source capacitance.
Cjo   Parasitic diode capacitance.
Is   Parasitic diode saturation current.
Rb   Body diode resistance.

Rg, Rd and Rs are the resistances of the bond wires connecting the die to the package.

Vto is the turn on voltage of the MOSFET.

Kp is the transconductance of the MOSFET. This determines the drain current that flows for a given gate source voltage.

Lambda is the change in drain current with drain source voltage and is used with Kp to determine the RDSon.

Cgdmax and Cgdmin are the minimum and maximum values of the gate drain capacitance and are normally graphed in the MOSFET datasheet as Crss. The capacitance of a capacitor is inversely proportional to the distance between its plates. When the MOSFET is turned on, distance between the gate and the conducting channel of the drain is equal to the thickness of the insulating gate oxide layer (which is small) so the gate drain capacitance is high. When the MOSFET is turned off, the gate drain region is large, making the gate drain capacitance low. This can be seen on the plot of Crss.

Cgs is the gate source capacitance. Although it changes slightly with gate source voltage, LTspice assumes it is constant.

Is is the parasitic body diode saturation current.

Rb is the series resistance of the body diode.

The Fairchild FDS6680A MOSFET is defined in LTspice by the line

.model FDS6680A VDMOS(Rg=3 Rd=5m Rs=1m Vto=2.2 Kp=63 Cgdmax=2n Cgdmin=1n Cgs=1.9n Cjo=1n Is=2.3p Rb=6m mfg=Fairchild Vds=30 Ron=15m Qg=27n)

Note: the characteristics Vds, Ron and Qg are actually ignored by LTspice. These are only added to aid the user to compare MOSFETs.

Therefore an example template MOSFET model is

.model XXXX VDMOS(Rg= Rd=5 Rs=1 Vto= Kp= Cgdmax= Cgdmin= Cgs= Cjo= Is= Rb=)

We are now going to construct a MOSFET model for the SUM75N06 and SUM110N04 low ON resistance MOSFETs from Vishay

SUM75N06 datasheet   Original SUM75N06 Model

SUM110N04 datasheet   Original SUM110N04 Model

The SUM75N06 has a moderately low ON resistance and a moderately low Qg, so is suitable as the top FET in a synchronous buck converter. The SUM110N04 has a high Qg but lower ON resistance, so is suitable as the bottom FET in a synchronous buck converter (see Buck Converter Design).

SUM75N06:

Characteristic	Source	Value
Rg	another SPICE model	1.5 Ohms
Rd	SPICE model	0 Ohms

Rs	SPICE model	25m Ohms
Vto	Datasheet	2V
Kp	Datasheet	75 S
Lambda	SPICE default value	1
Cgdmax	Datasheet Crss curve	1200pF
Cgdmin	Datasheet Crss curve	150pF
Cgs	SPICE model	2000pF
Cjo	SPICE model	1200pF
Is	SPICE model	1pA
Rb	SPICE default value	0 Ohms

The final SPICE model can be downloaded here: SUM75N06 LTspice model

SUM110N04:

Characteristic	Source	Value
Rg	another SPICE model	1.5 Ohms
Rd	SPICE model	0 Ohms
Rs	SPICE model	0.86m Ohms
Vto	Datasheet	1.85V
Kp	Datasheet	180 S
Lambda	SPICE default value	1
Cgdmax	Datasheet Crss curve	3000pF
Cgdmin	Datasheet Crss curve	900pF
Cgs	SPICE model	14.5nF

Cjo	SPICE model	4.9nF
Is	SPICE model	33.4pA
Rb	SPICE default value	0 Ohms

The final SPICE model can be downloaded here: SUM110N04 LTspice model

The SPICE models can then be testing using these test jigs:

RDSon test jig
To test the RDSON of the MOSFET import the model into the LTspice test circuit. Check the datasheet to see how the RDSOn has been tested. It will be characterised with a certain gate-source voltage and a certain drain current.

Run the simulation. Probe the drain voltage. Probe the drain current. Edit the Drain current icon to read **V(drain)/Id(M1)**. This changes one of the axes to read ON resistance. You may have to change the parameter Kp slightly to match the datasheet performance.

Switching Time Test Jig
To test the switching time of the MOSFET import the model into the LTspice test circuit. Check the datasheet to see how the switching times have been tested. They will be characterised with a certain gate drive voltage, gate drive resistance and drain voltage and the response time will be characterised when the drain current ramps to a certain level.

Run the simulation. Probe the gate voltage. Probe the drain current. Zoom in on the rising edge of the gate/drain waveforms. Left click on the Drain current axis and rescale the axis to measure slightly over the current desired drain current. The timings can now be measured. Rise time is normally measured over 10% to 90% of the desired voltage swing. You may have to change the model capacitances slightly to meet datasheet performance.