### Life on the Edge

## A Universal Grammar of Class D Amplification

**Bruno Putzeys** 

Hypex Electronics, The Netherlands

On the occasion of the 124rd AES Convention, May, 2007

# Copyright notice

- This presentation ©2008 Bruno Putzeys, Hypex Electronics.
- Do not distribute this file, instead link to this file on the Hypex web site.

## Contents

- Definition
  - Basic principles
  - Class D as Power Converter
- Output stage distortion
- MOSFET switching behaviour
- Output filter errors
- Loop control
  - Topologies, equivalence
  - Effect of sampling
  - Effect on modulation linearity
- Self-oscillating loops
- EMI
  - Filter components
  - Board layout

### Definition

A class D amplifier is a power amplifier where all active devices in the power stage are operating in on/off mode.

- On=current, but no voltage
- Off=voltage, but no current

## Definition

#### "Digital amplifier" is an oxymoron

- Voltage, current and time are physical quantities (analogue).
- Digital is strings of numbers.
- Speakers don't understand numbers.
- Class D requires analogue design skills to make work.
- DSP control may help solve or exacerbate analogue issues.

### **PWM** basics



### **PWM** basics

#### Two-state clocked PWM



#### Some conventions



#### Spectrum of 2-state PWM



#### Full-Bridge amplifier in 2 state PWM



# Three-state PWM (class BD)



#### Spectrum of 3-state PWM



### 2-State vs 3-State

#### Three-state...

- doubles sampling rate
  - Better efficiency vs bandwidth
- halves open-loop error
  Output filter?
  - Single-core
    - no excitation current
    - crossover distortion results
  - Two-core
    - excitation current doubles for constant sampling rate



### Yet More Phases



### It can get worse...



### **Class D as Power Converter**

Half bridge



### **Class D as Power Converter**



## Inductor current



## Inductor current

Large modulation index

Current sense does not change





### Dead time effects

### Simplified MOSFET model



## Dead time effects

#### Small modulation index





## Dead time effects

#### Large modulation index





# **Open-Loop Distortion**



# Analyser Reading



# **MOSFET** parasitics



#### Parasitic capacitances



### Gate Waveform (hard switching, ideal diode)



### Gate Waveform (real diode)



## Gate Gotchas

Until and during recovery

- Dissipated power = Vcc\*Qrr
- Vds=Vcc
- Gate capacitance is low
- But we'd like to go slow

After recovery

- Vds<Vgs</li>
- Gate capacitance is high
- Dissipated power = Vds\*Id\*time
- We'd like to finish quickly

Current limiting gate driver works the wrong way round.

# Output filter

### **Desired** function

• Attenuate the carrier

### **Undesired functions**

- Restrict bandwidth
- Increase output impedance
- Modify the frequency response
- Add distortion

### Load response of 2nd order LPF



# **Output Filter**

## The optimisation problem

- Reduce  $Z_{out} \rightarrow$  Increase  $f_c \rightarrow$  Reduce attenuation
- Improve Bandwidth  $\rightarrow$  Increase  $f_c \rightarrow$  Reduce attenuation
- Improve Flatness  $\rightarrow$  Increase  $f_c \rightarrow$  Reduce attenuation
- Reduce distortion → Reduce L → Reduce attenuation

The root cause

- Controlled variable is an internal node
- Output voltage is uncontrolled

# Summary of (analogue!) nonidealities

## **Power Supply Rejection**

- PWM power stage is an AM modulator Switch Timing
- Dead time causes distortion Output Filter
  - Output impedance is infinity at fc
  - Inductor is non-linear

## Feedback

### Solves many problems at once

- Output impedance (post LPF only)
- Distortion
- Frequency response (post LPF only)
- Why many don't use it
  - Audio folk lore
    - "Feedback sounds bad"
    - "Class D is Digital"

## Why global feedback is even rarer

- LC phase shift considered "insurmountable"
- No "rules of thumb"

## Delay in the LC filter?



#### Some control theory basics


## ETF & STF





$$\mathsf{ETF}(s) = \frac{1}{1 - \mathsf{A}(s) \cdot \mathsf{B}(s)}$$

$$STF(s) = \frac{A(s)}{1 - A(s) \cdot B(s)}$$

#### Various permutations



#### Various permutations



### Loop needs

ETF must be stable and not have excessive gain

• Poles well left of imaginary axis

ETF must have very low gain in audio band

• Zeros close to or on imaginary axis

Loop function A<sub>L</sub>

- Loop poles=zeros of ETF
- Loop zeros must be freely settable

## Universal loop control function

If  $A_L \dots$ 

- has n poles and n-1 zeros
- has independently settable zeros
  ...then
- a stable loop is always possible

$$A_{L}(s) = k \cdot \frac{\prod_{i=1}^{n-1} (s - z_i)}{\prod_{i=1}^{n} (s - p_i)} = \frac{\sum_{i=0}^{n-1} a_i \cdot s^i}{\sum_{i=0}^{n} b_i \cdot s^i}$$

#### 1 pole, no zeros, pre-filter f/b only



#### 2 poles, 1 zero, pre-filter f/b only



#### 3 poles, 2 zeros, mixed feedback



#### 3 poles, 2 zeros, global feedback



...also known as...:

...PID!



# PI(I...)D control for global loops

Pro

- Very low output impedance
- Minimum 3rd order loop
  - Large loop gain
- Nonlinear distortion from inductor is reduced
- Known art

Contra

• Can't get away with bad PCB layout

No good excuses for not using global feedback Pre-LC and mixed f/b are provably suboptimal

Digital PWM + local loop ("edge error correction")



### Hidden "analogue" amplifier:



No news at all, really:



Indirect "digital feedback"



...a remarkable similarity...



### Full ADC based feedback



## Full ADC based feedback

## Reasons for use

- Silicon area of ADC + loop control < equivalent analogue loop.
- Complicated linearization circuits
- Start/stop/overload recovery

### Not reasons for use

- Nearly anything else:
  - "digital, hence better"
  - investor retention

#### Effect of sampling on loop control



## Effect of sampling on loop control

### Noise Shaper Theorem holds



- Transform  $A_L$  to z domain
- Highly optimised  $A_{L}$  may seem instable in linear analysis and be critically damped in sampled system!

## Effect of sampling on loop control

Most PWM is double-sided

- $f_s = f_{sw}$  (low modulation index)
- $f_s = 0.5 \cdot f_{sw}$  (clipping)



• ETF (NTF) becomes modulation dependent

## **Ripple aliasing**



# **Ripple aliasing**

### Ripple distorts carrier





## Local Error Feedback (PEDEC etc)



- Operation
  - Minimal ripple in feedback loop.
- Pro
  - Theoretically perfect regardless of loop order
- Contra
  - Gains must be matched: 1-bit DAC and PWM must scale with supply
  - PWM generator is a problem in its own right
  - Not compatible with post-filter feedback

# Carrier slope correction (Candy)

- Operation
  - Dynamically modify triangle wave slopes
- Pro
  - Theoretically perfect for 1st order loop
  - Reasonably compatible with higher order including mixed post-filter f/b
- Contra
  - Complex triwave generation

## Minimum Aliasing Error filter (Risbo)



- Operation
  - Ripple in feedback loop not reduced, phase shift optimised for minimum impact.
- Pro
  - Grafts well onto "standard" control circuit.
  - Compatible with post-filter feedback (perhaps not fully global)

# "Invariant PWM" (Yours Truly)

- Operation
  - Secret
- Pro
  - Perfectible for any loop (5th order with global f/b demonstrated)
  - Compatible with global f/b
  - Closed-form analysis and design
- Contra
  - Complex triwave generation
  - High sensitivity to parts tolerance

# Self-Oscillating Loops

### Aim

- Getting rid of the oscillator
- Improving maximum modulation index

## Self-Oscillating Loops

#### Hysteresis modulator



Operation



### Improved version



### **Output Signal**



- Completely linear
- Switching frequency falls early
  - becomes audible near clip

#### Post-LPF added



- Less linear
- No-load stability not guaranteed

#### Capacitor current feedback (Mueta)



- Global loop
- Good linearity
- Current sense has low EMI sensitivity

## Phase-shift controlled oscillation

Operation

Oscillation frequency set by loop phase


#### Output signal



- Nonlinear, depends on design
- Switching frequency is more stable

Phase shift controlled oscillator with global loop (UcD)



# UcD

#### Operation

- Combined phase shift of output filter, lead network and propagation delay set f<sub>osc</sub>.
- Extra pole may be added

#### UcD



#### Modulator gain



#### Small-signal linearized model

$$A_{DC} = 2 \cdot V_{CC} \cdot f_{sw} \cdot \left(\frac{1}{dV1/dt} - \frac{1}{dV2/dt}\right)$$





Low-frequency EMI: Carrier and low harmonics.

- Close match with theory.
- Ripple cancelling possible.
- Not an EMI issue except for long cables
- Not a tweeter issue (come off it!)



Common and Differential Mode in H-Bridge Class D

• "Class AD". Carriers and modulation are out of phase



"Class BD".

• Carriers are in phase. Modulation is out of phase.



## Half bridge vs Full Bridge, Class AD vs BD

- Half-bridge
  - Can't cancel either CM or DM
  - Common-mode is half of differential mode
- AD
  - Common-mode voltage theoretically 0
  - Differential mode same as half bridge
- BD
  - Differential mode cancels at low modulation... ...but that was not really a problem anyway.
  - Common-mode voltage same as half bridge

High-Frequency EMI: Leaking switching transients

- Theoretical modeling is useless.
  - Capacitors become inductive
  - Inductors become capacitive
  - PCB becomes jumble of L's and C's.
- No tricks. Only good hardware design helps.
- Direct EMI problem under all circumstances.



#### Sensitive item 1: The capacitor.

- Myth of the "Low Inductance Capacitor". (An Audiophile Favourite)
  - All modern film caps have sprayed end contacts.
  - Inductance is determined by geometry only (mostly size).



#### Period.

#### Sensitive item 2: The inductor.

• Stray fields out of toroids



• Upright mounted toroids are worst.

#### Sensitive item 2: The inductor.

- Beware of indirect Capacitive Coupling through Core
  - Tight windings are better magnetically but worse electrostatically.
  - No external electrostatic shield: Capacitive coupling to chassis etc. can get significant.
- Toroids are not always optimal



Sensitive item 2: The inductor.

• Ferrite inductors: avoid direct capacitive coupling between windings



- "Hot" end sees "Cold" end
- 2 layers is worst case situation
- 1 layer is best

Sensitive item 3: The PCB layout.

- Contiguous ground plane
  Keep connectors together
- Avoid capacitive coupling to external parts
- Minimize loop area (≠short traces)

Checking for EMI without Spectrum Analyser

- Just probe around the external connections with a scope!!!
- If you see rubbish, there is rubbish
- The higher the frequency, the more you should worry



(sketch of circuit board found in commercially available amp)

Amplifier A, one output line

• 1V/div. Probe clip at RCA ground.



## Amplifier A, common mode

500mV/div. Amp is claimed to pass FCC???



## Amplifier A, differential mode

• 500mV/div. Note: relatively clean.



#### Example: Amplifier B, rated 2kW





## Amplifier B, common mode

• 250mV/div. Probe clip at power GND faston tab



# Amplifier B, differential mode

• 500mV/div.



## Class D EMI is no mystery

- Eyeballing components and PCB gives good indication
- Invest in an analogue scope
- Don't bother EMC testing if the scope pic isn't squeaky clean

## Summary

# All "Unique Class D Technologies" are related

- All draw from a limited set of concepts
  - Modulation technique
  - Power stage arrangement
  - Loop control
- Not all are optimal
  - Too complex
  - Missed opportunities

## Summary

Good design criteria: "black box"

- Audio performance
- Robustness
- Simplicity
- EMC, efficiency...

Bad design criteria: "open box"

- Perceived novelty and uniqueness
- Belief system
  - Digitalness
  - Feedbacklessness
- Powerpoint appeal

## Summary of summaries

The Road To Heaven

• Specify the performance and accept the design

The Road To Hell

• Specify the design and accept the performance

#### Thank you!

