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An Extensive Input Voltage and Fixed-Frequency Single Stage Series-Parallel LLC Resonant Converter for Dc Drive

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ABSTRACT: *In this paper design of a single-stage LLC resonant converter are presented. A single-stage converter uses only one control signal to drive two power converters, a power factor corrector (PFC) converter and a dc/dc converter, for reducing the cost of the system. However, this simplicity induces power imbalance between two converters, and then, the bus voltage between two converters drifts and becomes unpredictable. To ensure that the bus capacitor voltage can be kept in a tolerable region, the characteristics of a PFC converter and an LLC tank are investigated, and then, a design procedure is proposed correspondingly. Finally, a single-stage LLC resonant converter is implemented to verify the analysis.*

Key words: *AC–DC power conversion, resonant power conversion.*

I. INTRODUCTION

A conventional power supply was designed with two cells: The first cell functions as a Power Factor Corrector (PFC), and the second cell is a dc/dc converter which regulates system output voltage. To reduce the cost and complexity of the power supply, a single-stage topology [1]–[10] which uses only one control signal to drive two converters is presented.

It is common to insert a bulk capacitor between a PFC converter and a dc/dc converter to eliminate low-frequency noise at the system output [6]. However, since there is only one control signal in a single-stage converter, the power passing through the PFC converter is not equal to the power passing through the dc/dc converter. Therefore, the capacitor voltage drifts and becomes unpredictable.
An *LLC* resonant converter is employed as the dc/dc converter because *LLC* resonant converters have characteristics of high efficiency and low noise [10]–[13].

The works in [6]–[9] make efforts to control the drifting bus voltage. However, since lower cost is a major advantage in a single-stage converter, keeping the system simple and at low cost is important. The work in [10] investigated the characteristics of a single-stage *LLC* converter. However, the *LLC* converter characteristics are not well derived, so the bus voltage cannot be limited as much as well. In this paper, the relationship between the output powers of a boost stage and an *LLC* stage is derived.

Then, a single-stage *LLC* converter design procedure is proposed, which ensures that the bus capacitor voltage can be kept in a tolerable region. Finally, an experimental circuit is implemented to verify the analysis.

In resonant topologies, Series Resonant Converter (SRC), Parallel Resonant Converter (PRC) and Series Parallel Resonant Converter (SPRC, also called LCC resonant converter) are the three most popular topologies. The analysis and design of these topologies have been studied thoroughly. In next part, these three topologies will be investigated for front-end application.

1.1. CIRCUIT DESCRIPTION

Fig.1.1.1 shows a single-stage ac/dc *LLC* resonant converter. There is a bus capacitor between two converters, a boost like converter and a typical *LLC* converter. Two switches Q1 and Q2 are used to control these two converters.

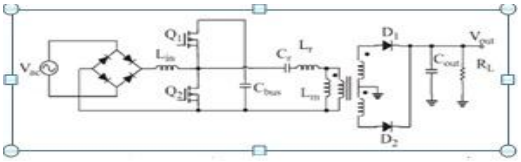


Fig.1.1.1: Single Stage LLC Converter

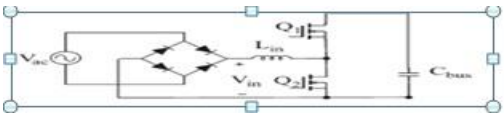


Fig.1.1.2: Simplified Circuit of the First Stage

The *LLC* converter is typical that has been presented in [7]–[10]. In the following, the operation details of the boost converter are introduced. Fig.1.1.2 shows the simplified circuit of the boost stage. The left-hand side of input inductor *L*in is a rectified half-wave voltage source. The input voltage source charges input inductor *L*in when the switch turns on. The energy stored in *L*in is released to bus capacitor *C* bus when the switch turns on. Because the boost cell uses the same switches with those in the *LLC* cell, the duty cycles of Q1 and Q2 are kept 50%.

Notice that the output power of this stage increases while the operating frequency decreases, because the inductor stores less energy in high frequency. The trend is the same with the *LLC* converter. Therefore, the fact that two converters can use the same control signal can be believed.

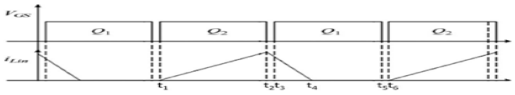


Fig.1.1.3 : Timing Diagram of Switch and inductor

The operational waveforms of the first stage are shown in Fig. 1.1.3.

*Stage I—t*1−*t*2*:* Switch Q2 turns on at *t*1. The voltage across the inductor is *V*in, and then, the inductor is charged by the slope

$$\frac{di_{Lin}}{dt} = \frac{V_{in}}{L_{in}} \quad \ldots (1)$$

Stage II—t2−t3: Switches Q1 and Q2 are turned off in this stage. The inductor current flows into the body diode of Q1 that helps achieve zero-voltage switching (ZVS).

Stage III—t3−t4: Switch Q1 turns on. The inductor current falls by the same slope

$$\frac{di_{Lin}}{dt} = -\frac{V_{cbus} - V_{in}}{L_{in}} \quad \dots (2)$$

To reduce the higher frequency harmonics of the inductor current, the system operates in discontinuous-conduction mode (DCM). Therefore, the period of falling slope has to be less than the one of rising slope. That means that the bus capacitor voltage should be twice larger than the input peak voltage as follows:

$$V_{cbus} > 2V_{in,max} \quad \dots (3)$$

Stage IV—t4−t5: There is no energy left in the input inductor. The inductor current is kept zero.

Stage V—t5−t6: Switches Q1 and Q2 turn off. Because the input impedance of the *LLC* converter is inductive, the input current of the *LLC* converter is lagged by the input voltage of the *LLC* converter. Therefore, the body diode of Q2 can be recharged by the *LLC* input current to achieve ZVS.

II. BUS VOLTAGE ESTIMATION

2.1 ENERGY EQUILIBRIUM

How to keep the voltage of the bus capacitor in a reasonable region is a major consideration in a single-stage converter analysis. Because there is only one control signal for two converters, the bus capacitor voltage varies due to energy imbalance of the two converters.

The bus capacitor voltage can be built by energy balance of two converters as shown in Fig 2.1.1When the boost output power P_{boost} is larger than the *LLC* output power *P*LLC, the bus voltage will rise until the two power flows are equal. Therefore, theoretically, given a switching frequency *f*sw, the steady-state bus voltage *V*bus can be found.

In the following, the relationship between the output power and the operating frequency of the boost stage and the *LLC* stage is derived.

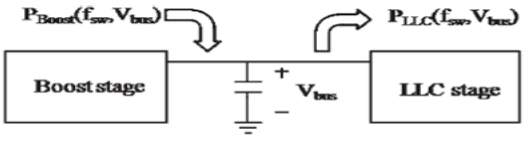


Fig 2.1.1 : Energy Balance At The Bus Capacitor

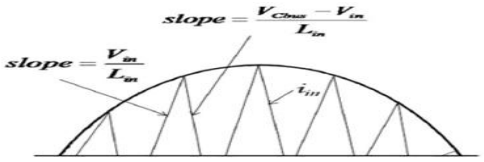


Fig. 2.1.2 : Waveform of the Input Voltage and Current

2.2 BOOST STAGE

First, consider the boost stage converter. Assume that the bus capacitor is large enough so that the voltage across the bus capacitor is stable in one cycle of an ac source. Given the inductor size *L*in, the designed bus capacitor voltage V_{bus}, and the ac source voltage V_{ac}, the waveforms of the input current and voltage can be determined as in Fig. 2.1.2.The average input current can be derived from (1) and (2)

$$i_{avg}(t) = \frac{V_{in}(t)T_{sw}}{8L_{in}}\left(\frac{V_{CBUS}}{V_{cbus} - V_{in}(t)}\right) \quad \dots (4)$$

$$P_{boost} == \frac{\int_0^{T_{sw}} i_{avg}(t)V_{in}(t)\,dt}{T_{sw}} \quad \dots (5)$$

where T_{sw} is the switching cycle. Then, the input power can be derived from the input voltage multiplied by the input current where V_{ac} is the amplitude of the ac input voltage.

Equation (5) shows an important fact that the input power is inversely proportional to the operating frequency since $V_{ac}(t)$ is given and $i_{avg}(t)$ in (4) is inversely proportional to the operating frequency.

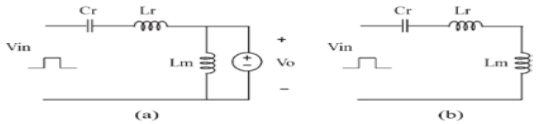


Fig.2.2.1 : Equivalent Circuit Of LLC Resonant Circuit (a).Secondary Sides Diodes Turn On (b).Secondary Sides Diodes Turn Off

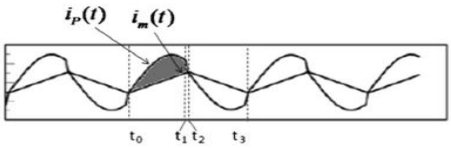


Fig.2.2.2 : waveform of ideal LLC converter ($f_{sw} > f_r$)

2.3. LLC CONVERTER STAGE

In this section, the goal is to find out the relationship between the operating frequency and the output power of the *LLC* converter. The previous works in [8]–[10] on a single-stage *LLC* converter did not derive the closed form of the *LLC* stage because of two major concerns.

First, the transient analysis is too complex. In a resonant circuit, the resonant current can be derived by the given driven source and loading condition. In the case of the *LLC* converter . the input voltage is a square waveform, and the output is a rectifier which behaves like a constant voltage load and behaves like an open circuit when two diodes are all reverse biased. The waveforms of the *LLC* converter are shown in Fig.2.1.2, where the operating frequency is larger than the resonant frequency in Fig.2.2.1 and the operating frequency is smaller than the resonant frequency . The primary side resonant current $i_p(t)$ can be substituted into the following equation to get the output power of the *LLC* converter:

$$P_{LLC} = \frac{E_{out}}{\frac{T_{sw}}{2}} = \frac{2\int_{t_0}^{t_1} V_0(i_P(t)i_m(t))\,dt}{T_{sw}} \quad \dots (6)$$

where E_{out} is the output energy in a half period and $(i_p(t) - i_m(t))$ is the shadow area in Fig.2.2.2. However, the resonant current derivation is too complex which makes transient not suitable for system analysis.

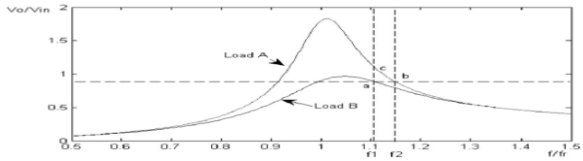


Fig .2.3.1 : Voltage Gain Versus Normalized Operating Frequency

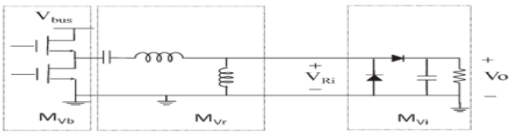


Fig .2.3.2 : Voltage Gain of the LLC Converter

The second consideration is that, in a dc/dc converter, the load is not constant, which may affect the system output power behaviors. However, since the system is frequency controlled, the frequency varies with loading condition so that there could be found load impedance corresponding to a given operating frequency. Fig. 9 explains the concept. In a dc/dc converter, the operating frequency varies with loading condition. When the load moves from load B to loadA, the operating frequency shifts from f_1 to f_2 correspondingly. That is, given a voltage gain and an operating frequency, corresponding load impedance can be found.

AC equivalent analysis helps to find out the corresponding load impedance. Fig .2.3.2 shows a typical ac circuit analysis. The system is divided into three parts, and the voltage gain is calculated separately.

The gain can be gotten as

$$M_v = \frac{V_0}{V_{bus}} = M_{vb}M_{vr}M_{vi} = \frac{V_i}{V_{bus}}\frac{V_{ri}}{V_i}\frac{V_0}{V_{ri}}$$

$$= \frac{\sqrt{2}}{\pi}\frac{1}{\sqrt{(1+A)^{2\left[1-\left(\frac{\omega_0}{\omega}\right)^2\right]} + \frac{1}{Q_L}\left(\frac{\omega}{\omega_0}\frac{A}{A+1} - \frac{\omega_0}{\omega}\right)^2 b^2}}\frac{\sqrt{2}}{\pi N} \quad (7)$$

where ω_o is the corner frequency $\frac{1}{\sqrt{L_r C_r}}$ A is the ratio of the leakage inductor to the magnetic inductor $\frac{L_r}{L_m}$, and Q_r is the loaded quality factor at the corner frequency

$$Q_L = \frac{\pi^2 n^2 R_L}{8}\sqrt{\frac{C_r}{(L_r + L_m)}} \quad \ldots(8)$$

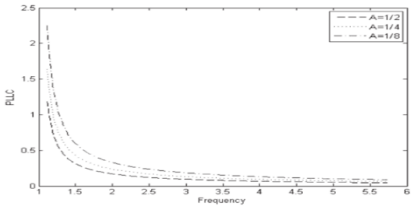


Fig.2.3.3 : PLLC versus frequency $(f_{sw} > f_r)$

Combining (7) and (8), the corresponding impedance *RL* can be derived.

Since the load impedance is gotten, the output power of the *LLC* converter can be derived easily as

$$P_{LLC} = \frac{{V_0}^2}{R_L} \quad \ldots(9)$$

Substituting *RL* into (9), the output power of the *LLC* converter is

Fig.2.3.4 helps to realize the equation. The voltage gain is set to half of the gain at resonant frequency *G*fr (the voltage gain at resonant frequency is constant under varied loading condition). The larger magnetic inductor *Lm* brings a flatter curve in the figure. The output power decreases when the operating frequency is lower than the resonant frequency. That is because the calculated corresponding impedance increases when the operating frequency decreases.

To have the same curve trend as the boost stage (output power increase with operating frequency) below resonant frequency, the voltage gain has to be set larger than *G*fr. In Fig.2.3.2, the voltage gain is set to 1.1*G*fr. When the frequency is around resonant frequency, no load impedance corresponding to the operating frequency could be found because no loading condition can reach 1.1*G*fr around resonant frequency. Therefore, the output power reduced to zero in Fig.2.3.5

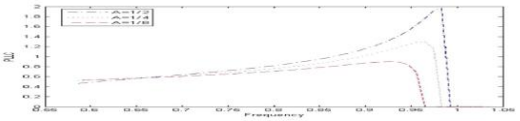


Fig.2.3.4 : PLLC versus frequency $(f_{sw} < f_r)$

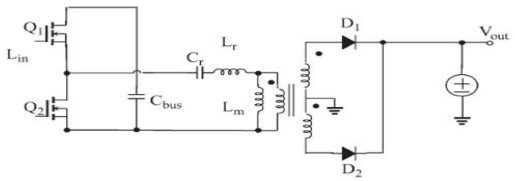


Fig.2.3.5: Simulation Model

In this paper, circuit simulation helps to find out the exact design parameters since there are errors between linear ac analysis and real circuit behaviors. Fig.2.3.5 shows the used simulation circuit. The load is replaced by a constant voltage source.

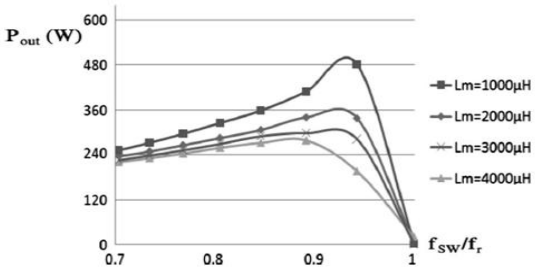


Fig.2.3.6: output power simulation $(f_{sw} < f_r)$

In Fig.2.3.6 are the simulation results which show the relationship between output power and frequency when the switching frequency f_{sw} is less than the resonant frequency f_r. In the period where the curve slope is negative, the input impedance of the *LLC* converter is inductive, and the ZVS can be achieved. The curve slope can be tuned by modifying the ratio of the magnetic inductor to the leakage inductor. In Fig. 9, *Cr* and *Lr* are given as 0.1 μF and 250 μH, respectively, and the magnetic inductor varies from 1000 to 4000 μH.

Fig.2.3.7 shows the relationship between output power and frequency (*f*sw > *fr*). Larger *Lm* let the curve more flat. It helps to match the curve of the boost stage. The ratio of *Cr* to *Lr* is modified by doubling *Cr* and decreasing *Lr* by half in Fig. 15, which shows that the relationship between the output power and system switching frequency is the same except that *P*out is doubled. That means that the power transferred into the system load doubles as the ratio of *Cr* to *Lr* doubles. Therefore, the system output power can be decided by modifying the ratio of *Cr* to *Lr*

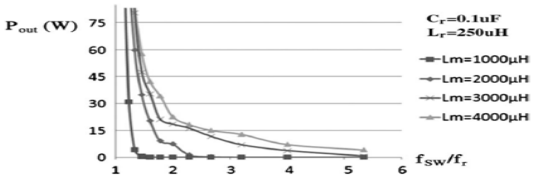


Fig.2.3.8: output power simulation $(fsw > fr)$

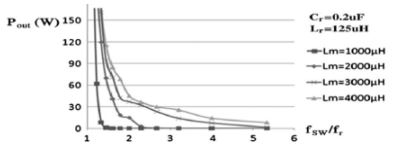
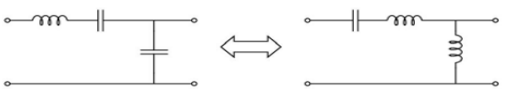


Fig.2.3.9: output power simulation after modifying the ratio of inductor to capacitor $(fsw > fr)$

III. LLC RESONANT CONVERTER

Three traditional resonant topologies were analyzed in above part. From the results, we can see that all of them will see big penalty for wide input range design. High circulating energy and high switching loss will occur at high input voltage. They are not suitable for front end DC/DC application. Although above analysis give us negative results, still we could learn something from it: For a resonant tank, working at its resonant frequency is the most efficient way. This rule applies to SRC and PRC very well. For SPRC, it has two resonant frequencies. Normally, working at its highest resonant frequency will be more efficient. To achieve zero voltage switching, the converter has to work on the negative slope of DC characteristic.



LCC Resonant Tank LLC Resonant Tank

Fig.3.1.1: LCC And LLC Resonant Tank

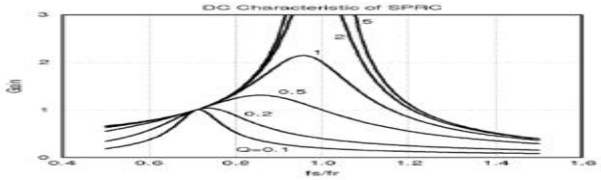


Fig.3.1.2: Dc Characteristics Of LCC Resonant Converter

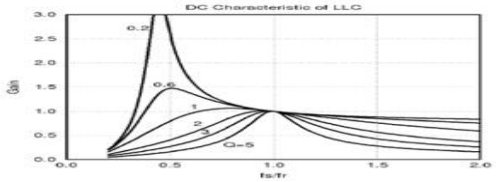


Fig.3.1.3: Dc Characteristics Of LLC Resonant Converter

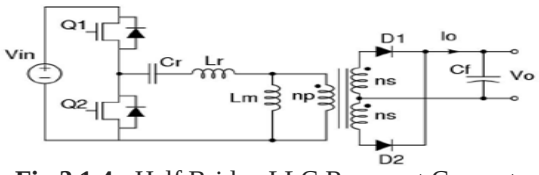


Fig.3.1.4: Half Bridge LLC Resonant Converter.

3.1 OPERATION OF LLC RESONANT CONVERTER

The DC characteristic of LLC resonant converter could be divided into ZVS region and ZCS region as shown in Fig.3.1.3.For this converter, there are two resonant frequencies. One is determined by the resonant components Lr and Cr. The other one is determined by Lm, Cr and load condition. As load getting heavier, the resonant frequency will shift to higher frequency. The two resonant frequencies are:

$$f_r1 = \frac{1}{2.\pi.\sqrt{L_r.C_r}} \quad \ldots(10)$$

$$f_r2 = \frac{1}{2.\pi.\sqrt{(L_m+L_r).Cr}} \quad \ldots(11)$$

With this characteristic, for 400V operation, it could be placed at the resonant frequency of fr1, which is a resonant frequency of series resonant tank of Cr and Lr. While input voltage drops, more gain can be achieved with lower switching frequency. With proper choose of resonant tank, the converter could operate within ZVS region for load and line variation.

From above discussion, the DC characteristic of LLC resonant converter could be also divided into three regions according to different mode of operation as shown in Figure 20 Our designed operating regions are region 1 and region 2. Region 3 is ZCS region. The converter should be prevented from entering region 3. In fact, there are many other operating modes for LLC resonant converter as load changes.

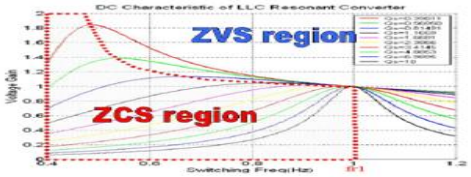


Fig.3.1.5: Dc Characteristics of LLC Resonant Converter

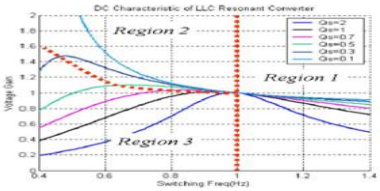


Fig.3.1.6: Three Operating Region of LLC Resonant Converter

In region 1, the converter works very similar to SRC. In this region, Lm never resonates with resonant capacitor Cr; it is clamped by output voltage and acts as the load of the series resonant tank. With this passive load,

LLC resonant converter is able to operate at no load condition without the penalty of very high switching frequency. Also, with passive load Lm, ZVS could be ensured for any load condition. Here the operation will not be discussed in detail. There are several other modes of operation for light load condition.

Mode 1 (t0 to t1):

This mode begins when Q2 is turned off at t0. At this moment, resonant inductor Lr current is negative; it will flow through body diode of Q1, which creates a ZVS condition for Q1. Gate signal of Q1 should be applied during this mode. When resonant inductor Lr current flow through body diode of Q1, ILr begins to rise, this will force secondary diode D1 conduct and Io begin to increase. Also, from this moment, transformer sees output voltage on the secondary side. Lm is charged with constant voltage.

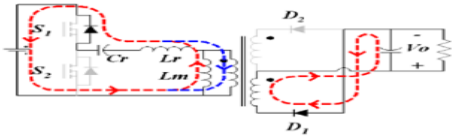


Fig.3.1.7: Circuit Diagram During Mode 1 In Region

Mode 2 (t1 to t2)

This mode begins when resonant inductor current ILr becomes positive. Since Q1 is turned on during mode 1, current will flow through MOSFET Q1. During this mode, output rectifier diode D1 conduct. The transformer voltage is clamped at Vo. Lm is linearly charged with output voltage, so it doesn't participate in the resonant during this period. In this mode, the circuit works like a SRC with resonant inductor Lr and resonant capacitor Cr. This mode ends when Lr current is the same as Lm current. Output current reach zero.

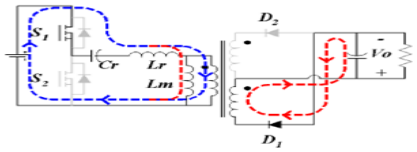


Fig.3.1.8: Circuit Diagram during Mode 2 In Region 2

Mode 3 (t2 to t3)

At t2, the two inductor's currents are equal. Output current reach zero. Both output rectifier diodes D1 and D2 is reverse biased. Transformer secondary voltage is lower than output voltage. Output is separated from transformer. During this period, since output is separated from primary, Lm is freed to participate resonant. It will form a resonant tank of Lm in series with Lr resonant with Cr. This mode ends when Q1 is turned off. As can be seen from the waveform, Q1 turn off current at t3 is small compare with peak current. For next half cycle, the operation is same as analyzed above

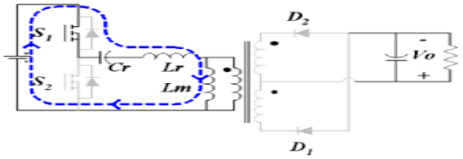


Fig.3.1.9: Circuit Diagram During Mode 2 In Region 2

IV. DESIGN PROCEDURE

Based on the analysis shown before, a design procedure is presented in the following. A 75-W 110-Vac-to-18-Vdc dc/dc converter is taken as a design example.

1) First, set the target voltage of the bus capacitor. Chosen in this case for DCM is 390 V.

2) Decide the minimum operating frequency. Higher operating frequency brings higher switching loss. Therefore,

50 kHz is chosen as the minimum operating frequency.

3) Given the bus voltage and the full-load switching frequency, input inductor *L*in can be gotten by (4) and (5) as 560 μH.

4) Select the resonant frequency of the *LLC* converter and the ratio of the magnetic inductor to the leakage inductor. To match *P*boost and *PLLC*, the smooth region of the curves in Figs. 11 and 14 is used. The curves are flatter when the ratio of the leakage inductor to the magnetic inductor is lower. On the other hand, the curves are much flat at the high-frequency region. However, being close to resonant frequency means higher efficiency. Finally, 1.2*fr* is chosen as the minimum operating frequency of the *LLC* converter, and the ratio of the magnetic inductor to the leakage inductor is set to eight. Therefore, the resonant frequency can be calculated as 41.6 kHz.

5) Decide the *LLC* series capacitor. The relationship between system power capacity and series capacitor is shown in Figs. 14 and 15. Then, the series capacitor is chosen as 0.1 μF. Then, the leakage inductor can be calculated as 175.2 μH by the equation

6) To avoid operating at extremely high frequency, the system enters burst mode while the operating frequency reaches triple the minimum operating frequency.

TABLE 4.1. Designed Parameters.

Input voltage	$110V_{ac}$
Output voltage	$18V_{dc}$
Output power	75 W
V_{cbus}	320V
Minimum switching frequency	50kHZ

TABLE 4.2. Component Parameters

L_r	135µH	L_{in}	180 µH
L_m	1.13mH	NF_p	45 turns
C_r	0.1µF	N_s	4 turns
C_{bus}	180 µF *2	Power mos	STP25NM5ON
C_{out}	470 µF *2	Rectify diode	STP30S45CT

V. SIMULATION RESULTS

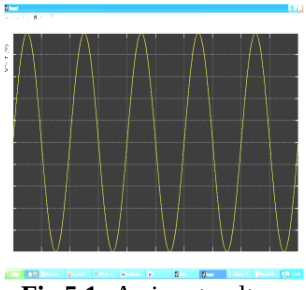


Fig.5.1: Ac input voltage

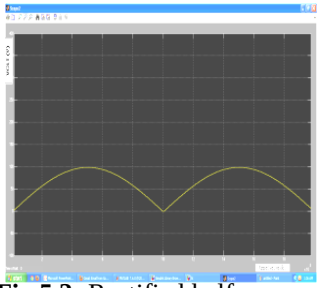


Fig.5.2: Rectified half wave dc voltage

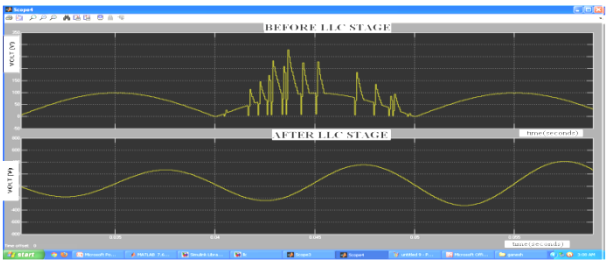


Fig.5.3: LLC output voltage

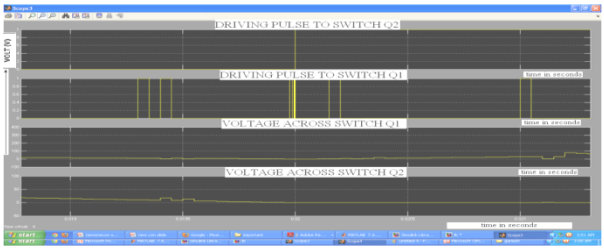


Fig.5.4: Voltage Across Switches

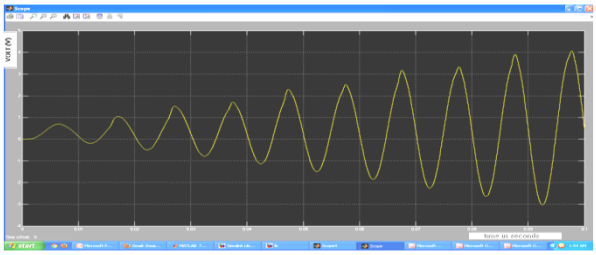


Fig.5.5: Load Voltage

VI. CONCLUSION

Analysis of a single-stage *LLC* converter has been presented in this paper. To stabilize the bus capacitor voltage, the power balance of the boost stage and the *LLC* converter has been investigated, and then, the design procedure has been presented. For verification, a 75-W 110-Vac-to-18-Vdc single-stage converter has been designed and implemented. The bus voltage can be kept around 390 V with a maximum variation of 38 V. The system efficiency can reach 90% while the loading condition is heavier than 20%.

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