

IRFP240, IRFP241, IRFP242, IRFP243

**18A and 20A, 200V and 150V, 0.18 and 0.22 Ohm,
N-Channel Power MOSFETs**

January 1998

Features

- 18A and 20A, 200V and 150V
- $r_{DS(ON)} = 0.18\Omega$ and 0.22Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFP240	TO-247	IRFP240
IRFP241	TO-247	IRFP241
IRFP242	TO-247	IRFP242
IRFP243	TO-247	IRFP243

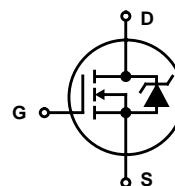
NOTE: When ordering, include the entire part number.

Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

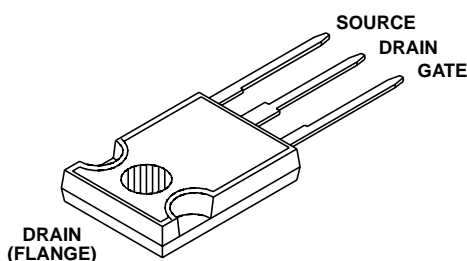
Formerly developmental type TA17422.

Symbol



Packaging

JEDEC STYLE TO-247



IRFP240, IRFP241, IRFP242, IRFP243

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	IRFP240	IRFP241	IRFP242	IRFP243	UNITS
Drain to Source Voltage (Note 1) V_{DS}	200	150	200	150	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1) V_{DGR}	200	150	200	150	V
Continuous Drain Current I_D	20	20	18	18	A
$T_C = 100^\circ\text{C}$	12	12	11	11	A
Pulsed Drain Current (Note 3) I_{DM}	80	80	72	72	A
Gate to Source Voltage V_{GS}	± 20	± 20	± 20	± 20	V
Maximum Power Dissipation P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	$W/^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 4) E_{AS}	510	510	510	510	mJ
Operating and Storage Temperature T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s T_L	300	300	300	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334 T_{pkg}	260	260	260	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

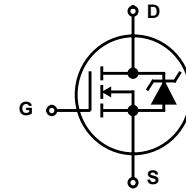
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage IRFP240, IRFP242	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$, (Figure 10)	200	-	-	V
IRFP241, IRFP243			150	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2.0	-	4.0	V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0V$	-	-	25	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0V, T_J = 125^\circ\text{C}$	-	-	250	μA
On-State Drain Current (Note 2) IRFP240, IRFP241	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, V_{GS} = 11V$, (Figure 7)	20	-	-	A
IRFP242, IRFP243			18	-	-	A
Gate to Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	-	-	± 100	nA
Drain to Source On Resistance (Note 2) IRFP240, IRFP241	$r_{DS(ON)}$	$V_{GS} = 10V, I_D = 10A$, (Figures 8, 9)	-	0.14	0.18	Ω
IRFP242, IRFP243			-	0.20	0.22	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V, I_D = 11A$	7.3	11	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 100V, I_D \approx 18A, R_G = 9.1\Omega, V_{GS} = 10V, R_L = 5.4\Omega$, (Figures 17, 18) MOSFET Switching Times are essentially Independent of Operating Temperature	-	14	21	ns
Rise Time	t_r		-	51	77	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	45	68	ns
Fall Time	t_f		-	36	54	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$		-	43	60	nC
Gate to Source Charge	Q_{gs}	$V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, I_{G(REF)} = 1.5mA$, (Figure 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	10	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	32	-	nC
Input Capacitance	C_{ISS}	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$, (Figure 11)	-	1275	-	pF
Output Capacitance	C_{OSS}		-	500	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	160	-	pF

IRFP240, IRFP241, IRFP242, IRFP243

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Internal Drain Inductance	L _D	Measured Between the Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	5.0	-	nH
Internal Source Inductance	L _S	Measured from the Source Lead, 6mm (0.25in) from Header to Source Bonding Pad		-	12.5	-	nH
Junction to Case	R _{θJC}			-	-	0.83	°C/W
Junction to Ambient	R _{θJA}	Free Air Operation		-	-	30	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I _{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode		-	-	20	A
Pulse Source to Drain Current (Note 3)	I _{SDM}			-	-	80	A
Source to Drain Diode Voltage (Note 2)	V _{SD}	T _J = 25°C, I _{SD} = 18A, V _{GS} = 0V, (Figure 13)		-	-	2.0	V
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _{SD} = 18A, dI _{SD} /dt = 100A/μs		120	250	530	ns
Reverse Recovered Charge	Q _{RR}	T _J = 25°C, I _{SD} = 18A, dI _{SD} /dt = 100A/μs		1.3	2.6	5.6	μC

NOTES:

- Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
- $V_{DD} = 50\text{V}$, starting $T_J = 25^\circ\text{C}$, $L = 1.9\text{mH}$, $R_{GS} = 50\Omega$, peak $I_{AS} = 20\text{A}$ (Figures 14, 15).

Typical Performance Curves Unless Otherwise Specified

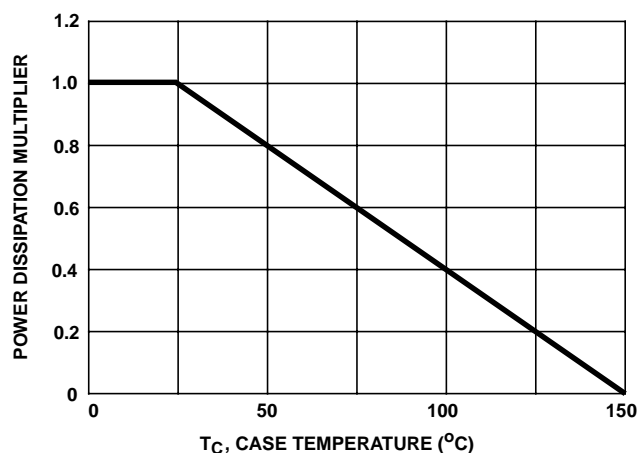


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

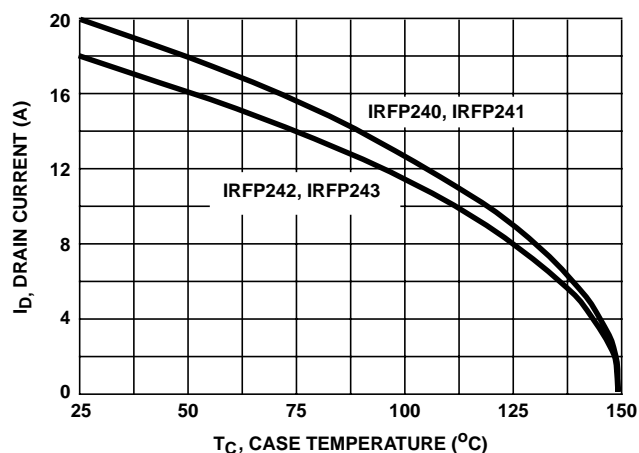


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

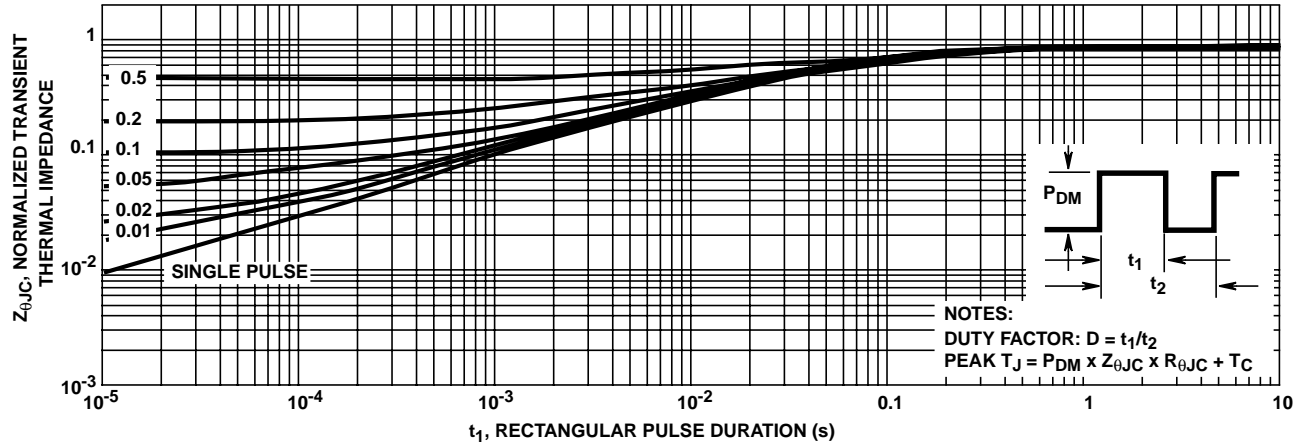


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

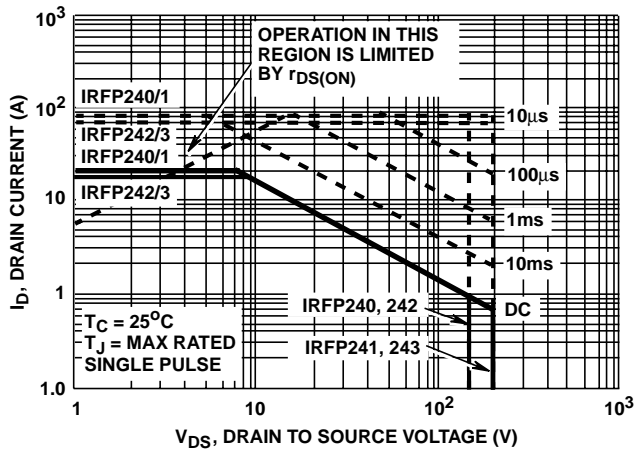


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

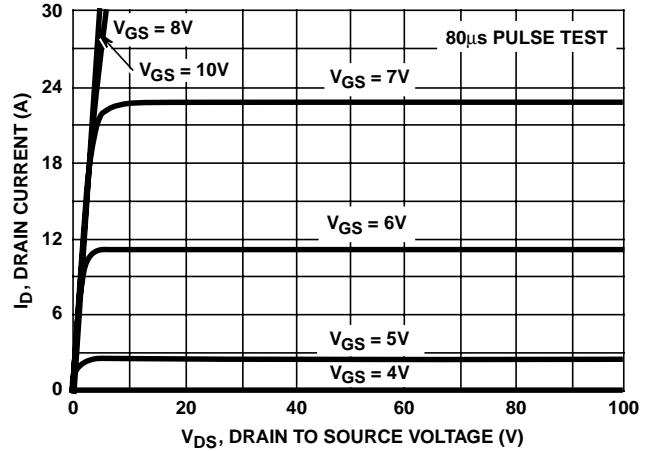


FIGURE 5. OUTPUT CHARACTERISTICS

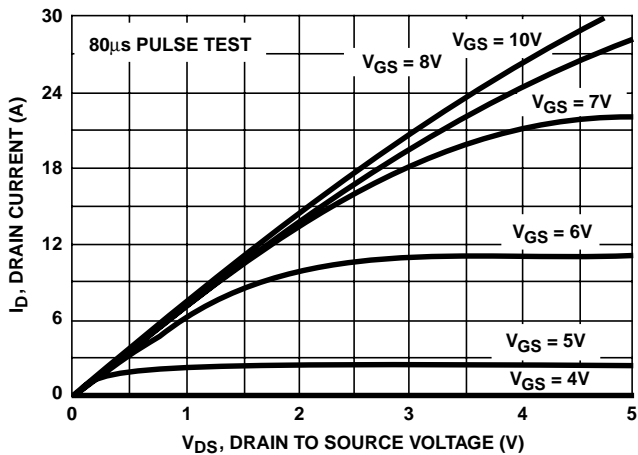


FIGURE 6. SATURATION CHARACTERISTICS

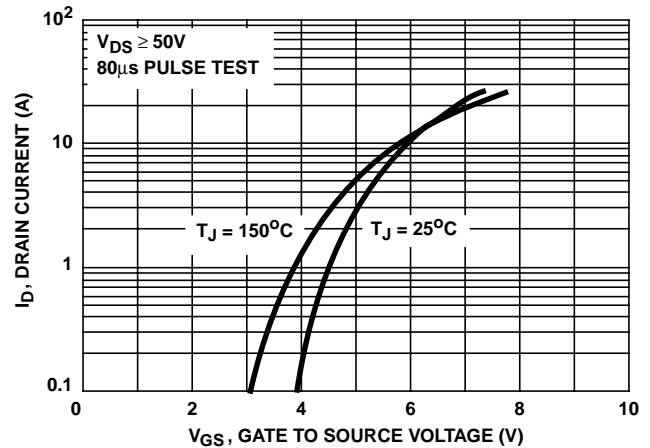
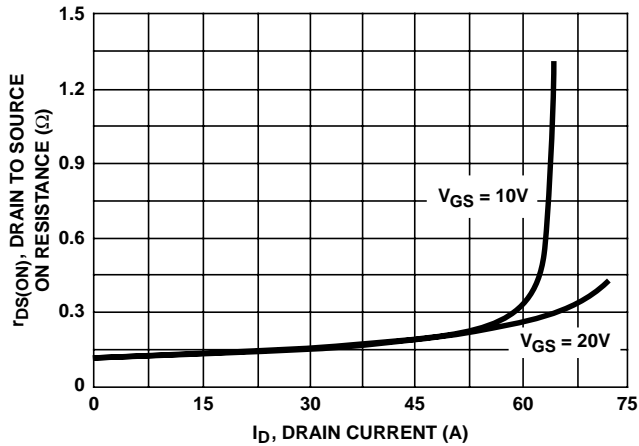


FIGURE 7. TRANSFER CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Heating effect of 2μs pulse is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE GATE VOLTAGE AND DRAIN CURRENT

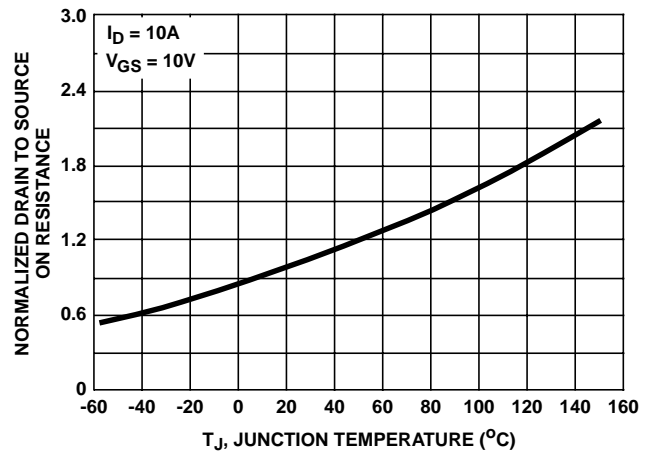


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

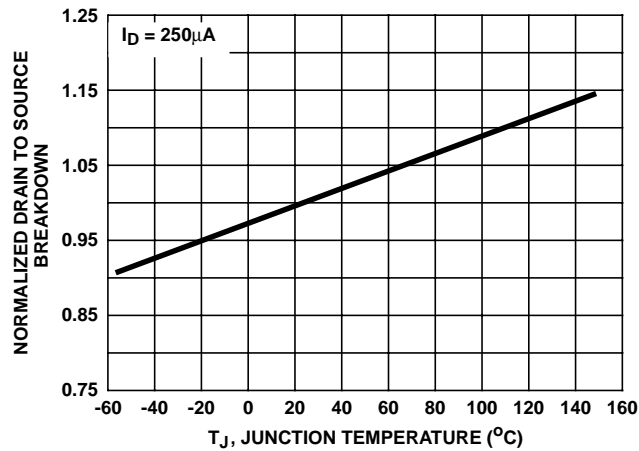


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

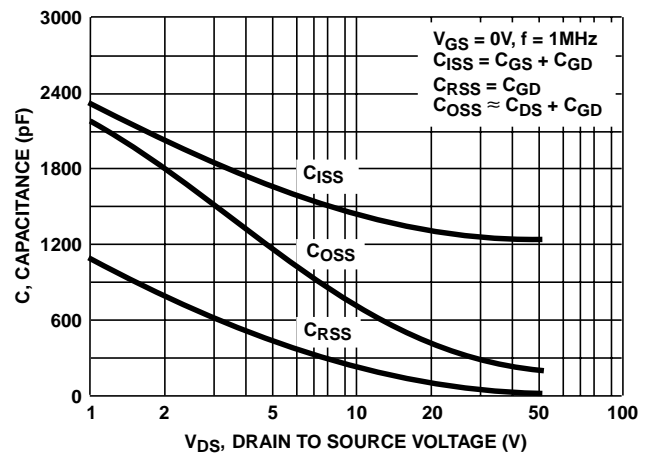


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

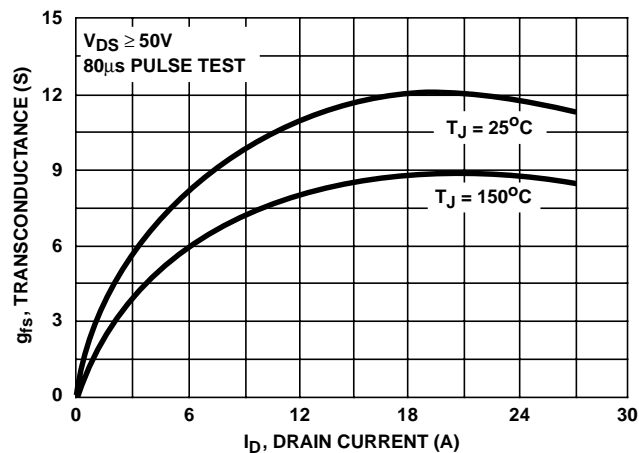


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

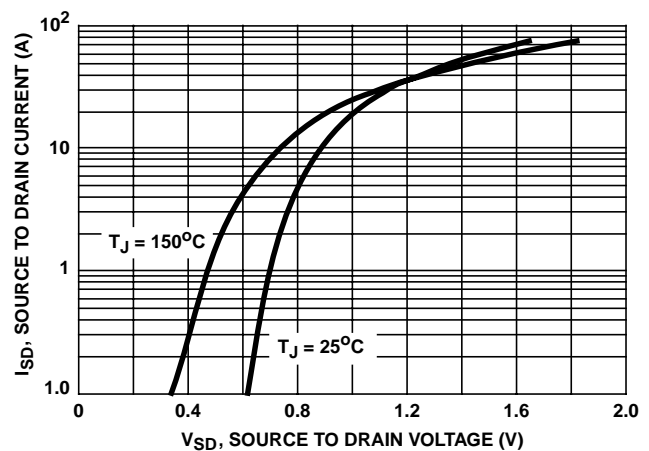


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

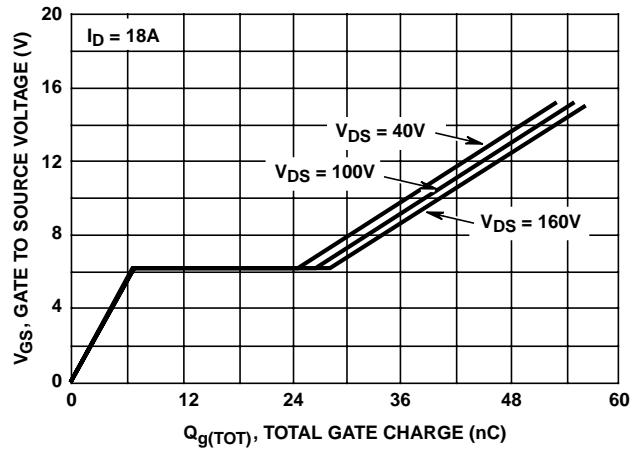


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

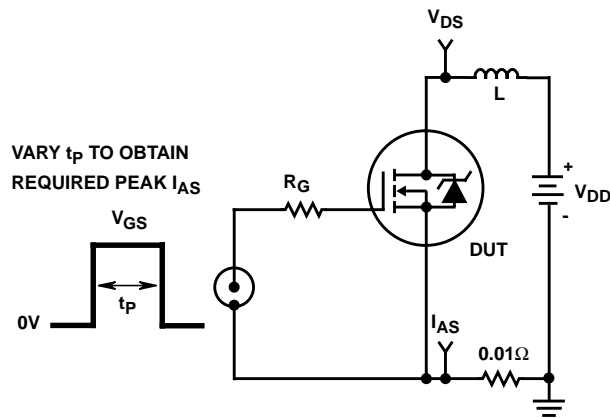


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

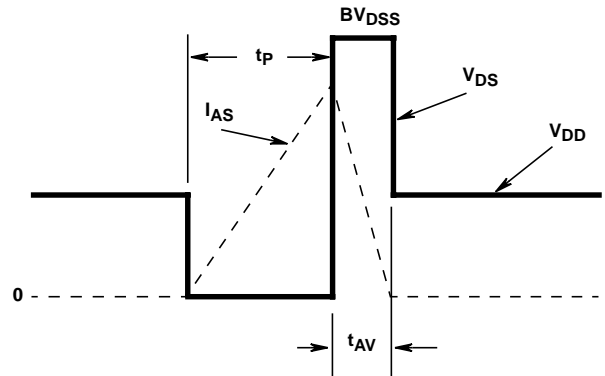


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

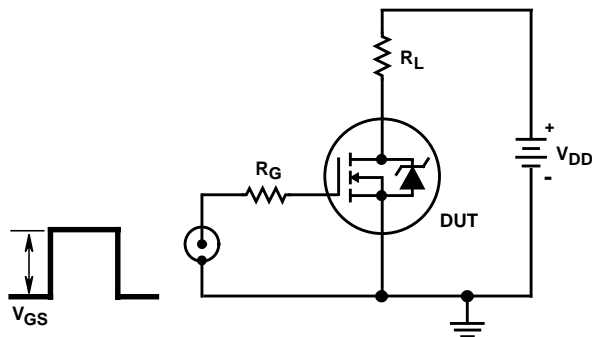


FIGURE 17. SWITCHING TIME TEST CIRCUIT

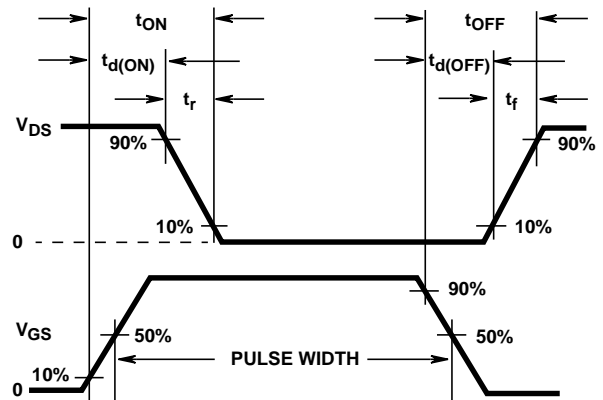


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

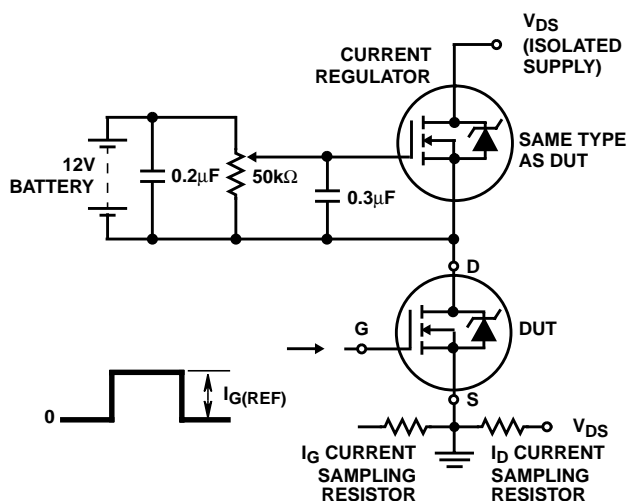


FIGURE 19. GATE CHARGE TEST CIRCUIT

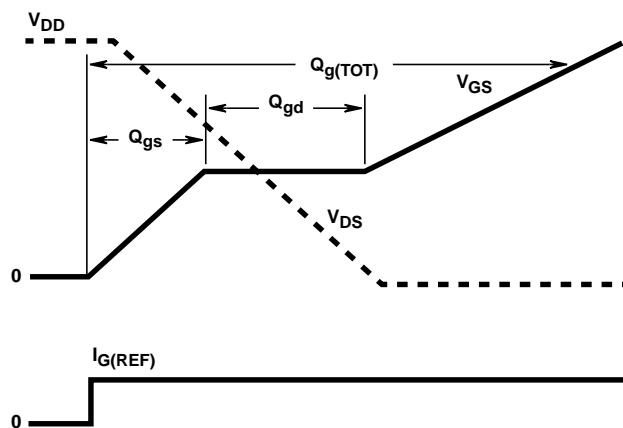


FIGURE 20. GATE CHARGE WAVEFORMS

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