

COMPAL CONFIDENTIAL

MODEL NAME : *NAL60*

PCB NO : *LA-5691P (DAA00001K00)*

BOM P/N : *43178731L01/43178731L02*

M10 Lafite

**BGA Arrandale (34 x 28 mm) +
SFF IBEXPEAK-M**

2009-07-07

REV : 0.1(X00)

@ : Nopop Component

MB Type	BOM P/N	CPU	With BLT	Non BLT	TCM		TPM		BOM CONFIG
			1@	2@	W(3@)	W/O(4@)	W(5@)	W/O(6@)	
BLT EN, TPM EN	43178731L01	SV 2.4G	*			*	*		1@, 4@, 5@
BLT EN, TPM EN	43178731L02	SV 2.0G	*		*			*	1@, 3@, 6@
BLT DIS, TCM EN	43178731L03	LV 1.8G		*		*	*		2@, 4@, 5@

MB PCB	
Part Number	Description
DAA00001K00	PCB 0AW LA-5691P REV0 M/B

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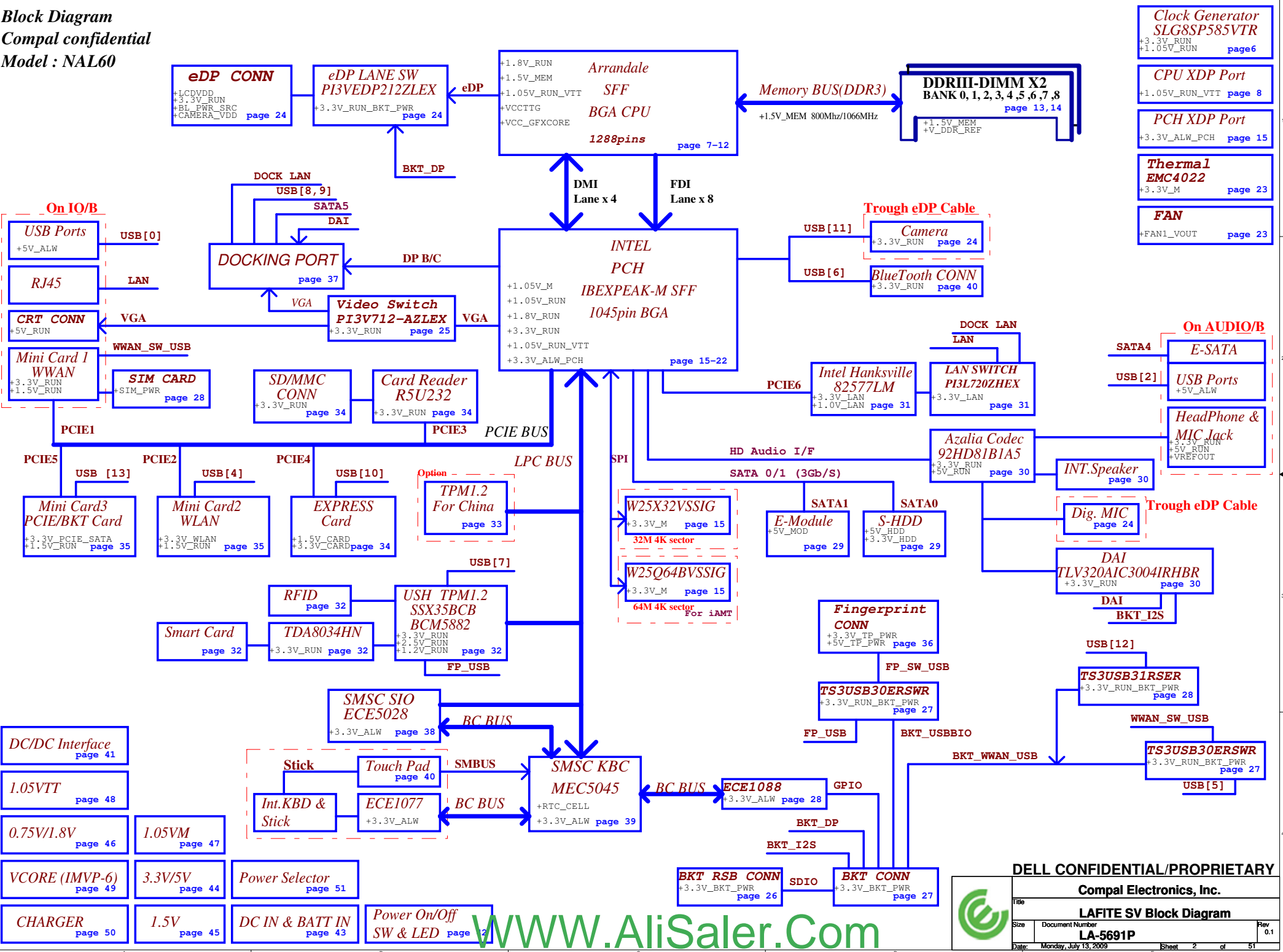
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Title: **Cover Sheet**

Size: **LA-5691P** Rev: **0.1**

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Block Diagram
Compal confidential
Model : NAL60



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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	ON
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	USB Port (Ext Right Side)
	1	NA
	2	USB Port (Ext Left Side)
	3	NA
	4	WLAN
	5	WWAN
	6	Bloetooth
	7	USB->BIO
	8	DOCKING
	9	DOCKING
	10	Express Card
	11	Camera
	12	BKT
13	WPAN/NVMHCI	

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Card Reader
Lane 4	EXPRESS CARD
Lane 5	MINI CARD-3 WPAN/NVMHCI
Lane 6	10/100/1G LAN
Lane 7	None
Lane 8	None

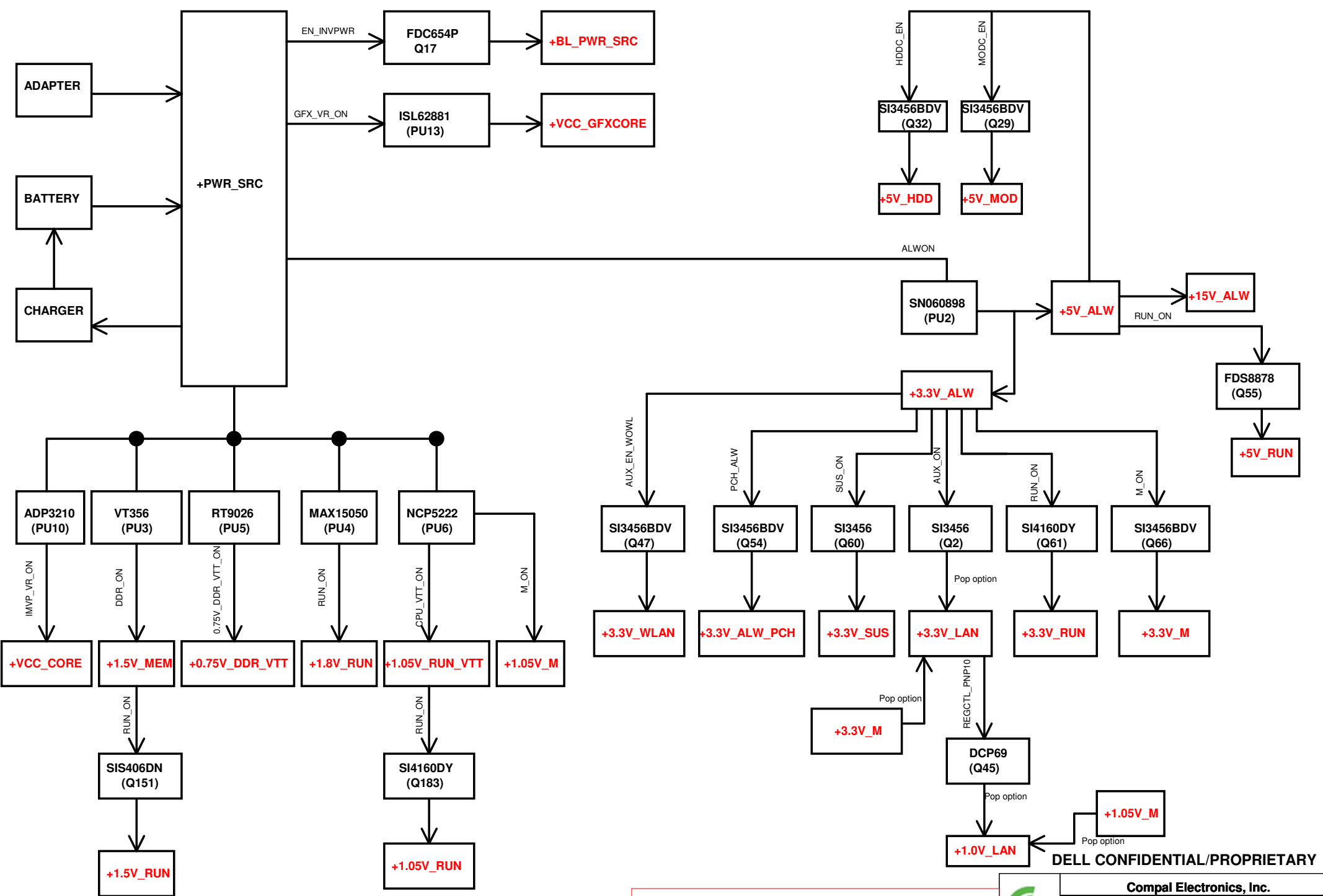
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Index and Config.

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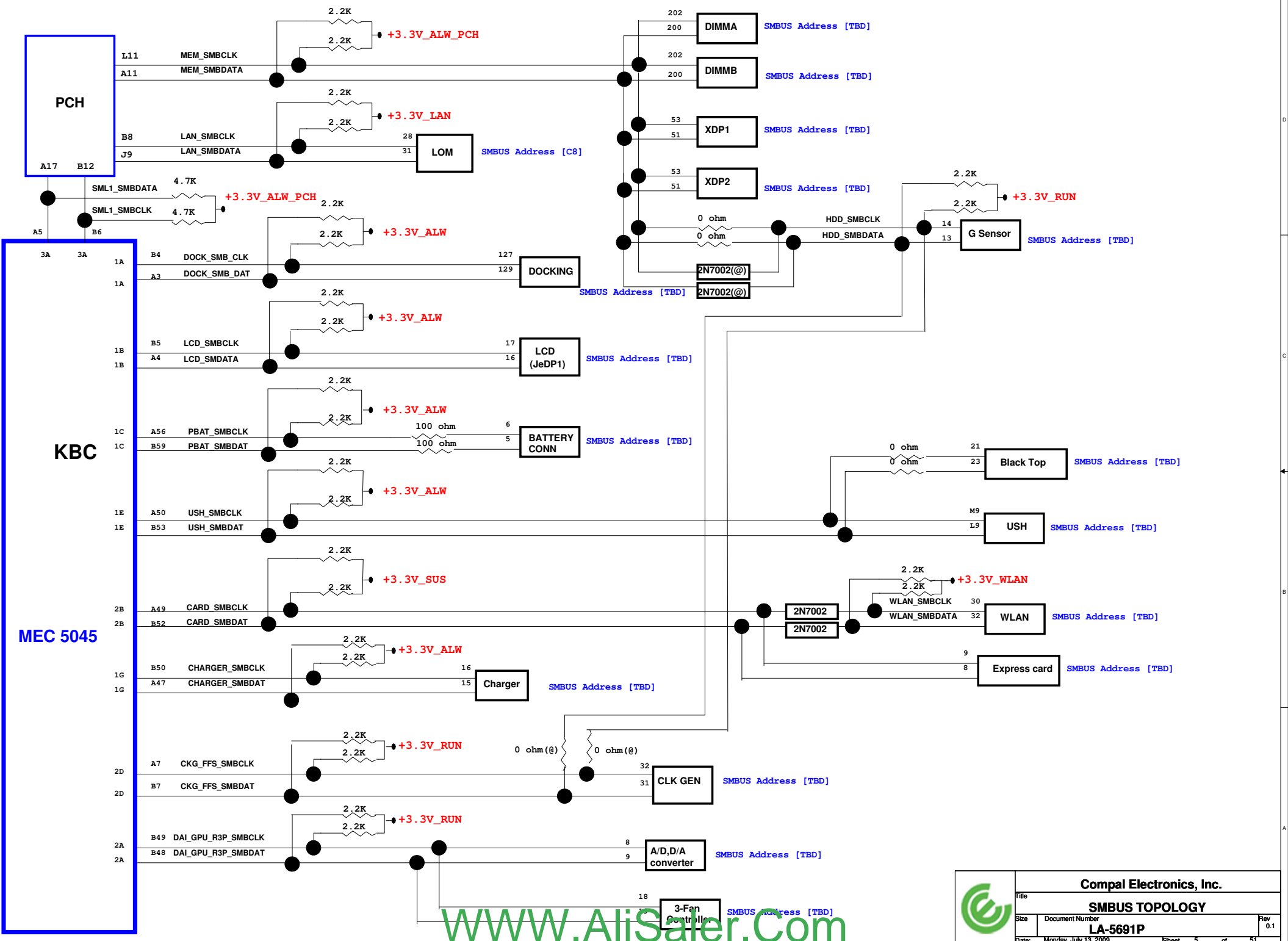
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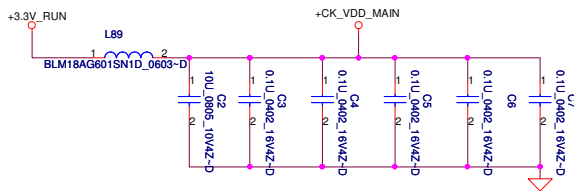


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Power Rail			
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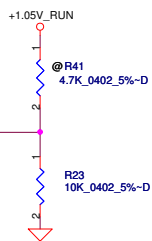
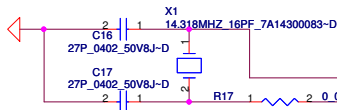
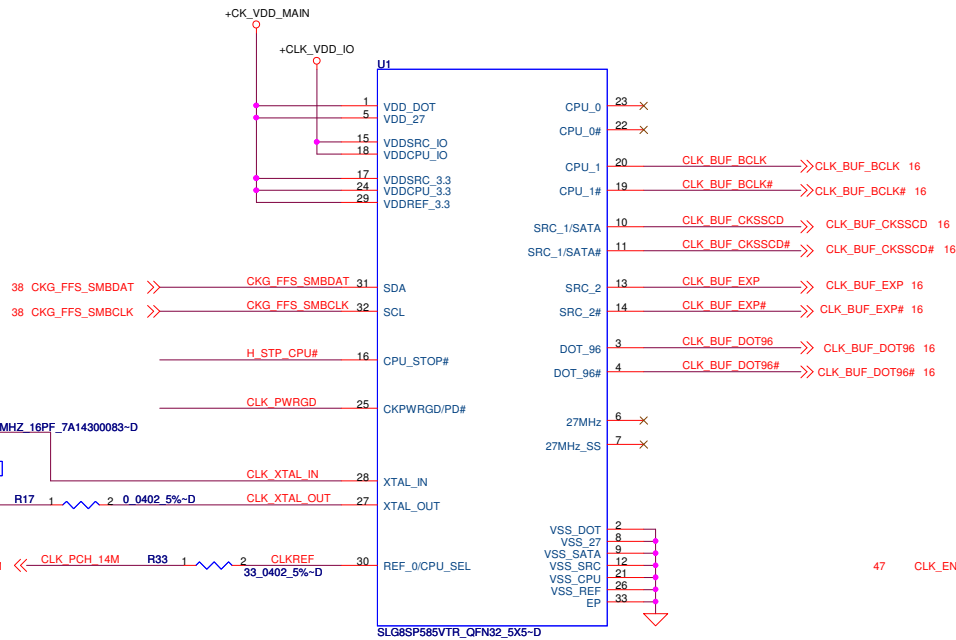
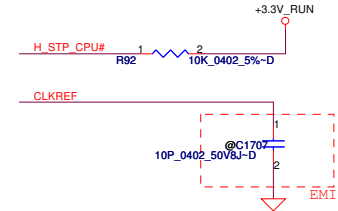
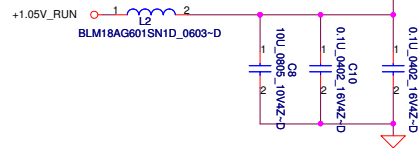


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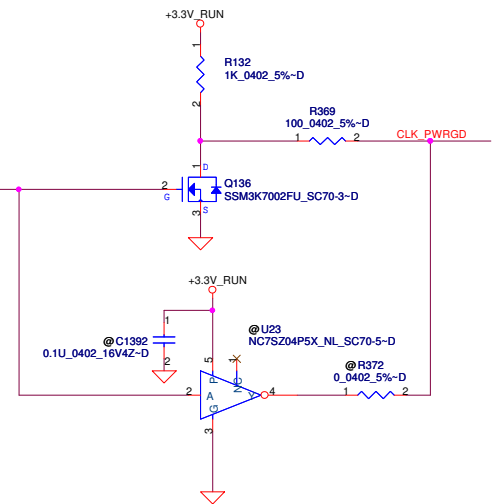
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+CLK_VDD_IO CAN BE RANGE FROM 1.05V TO 3V



PIN 30	CPU0	CPU1
1 (0.7~1.5v)	100MHz	100MHz
0 (DEFAULT)	133MHz	133MHz



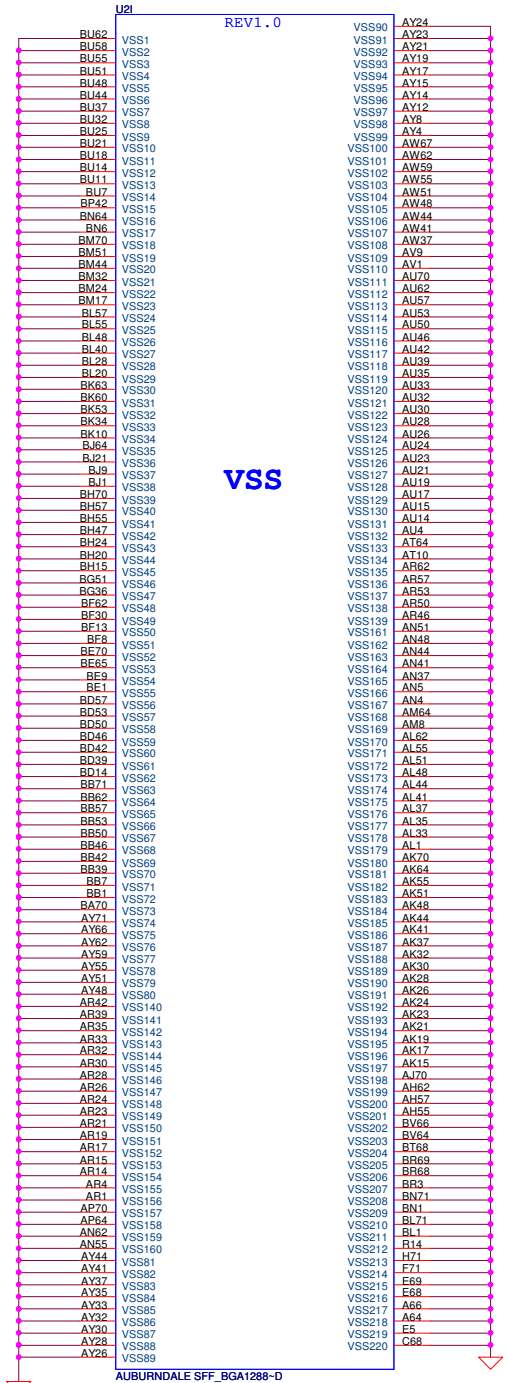
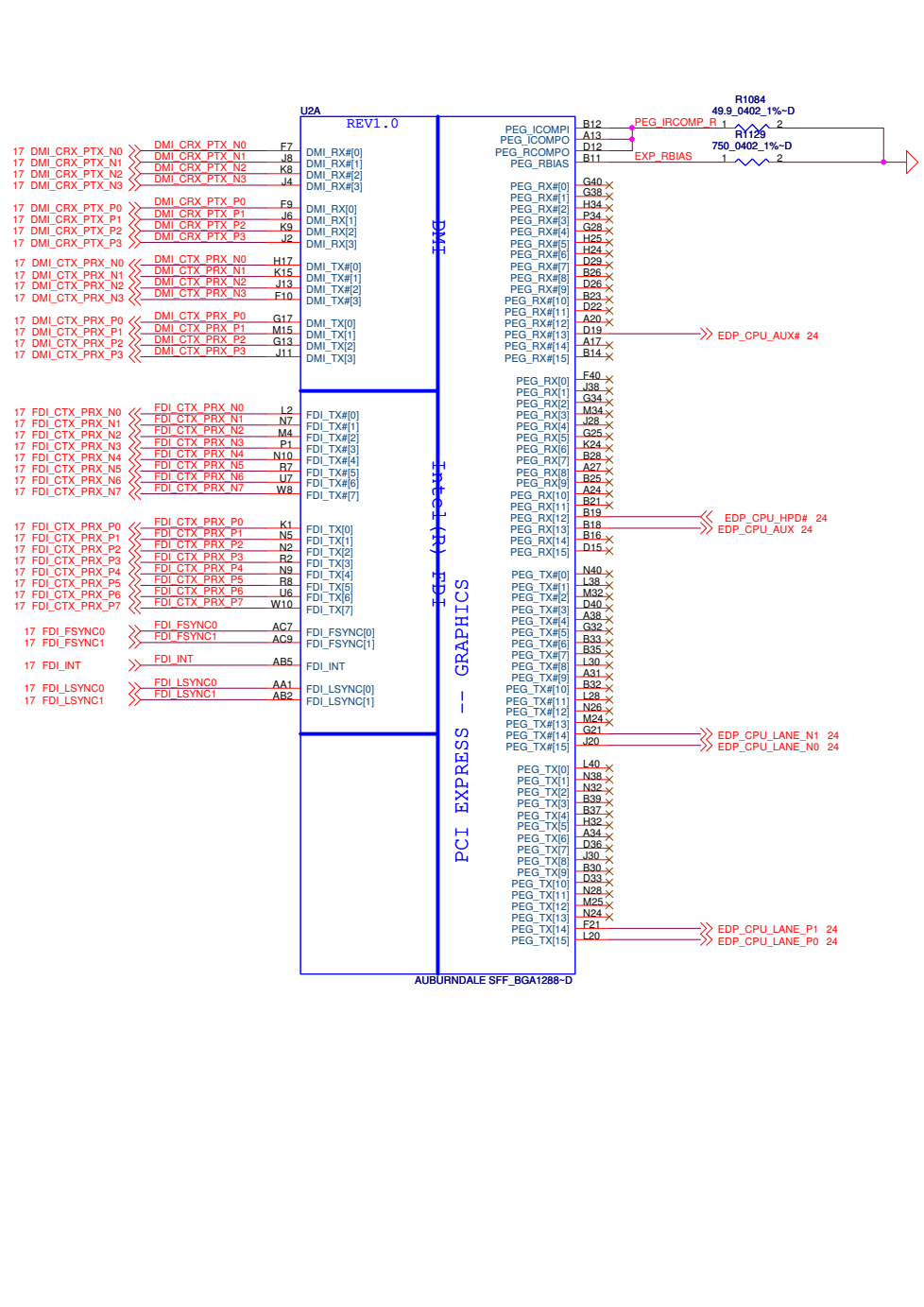
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Title			
Clock Generator			
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AUBURDALE SFF_BGA1288-D

R18 0.0402_5%-D

AUBURDALE SFF_BGA1288-D

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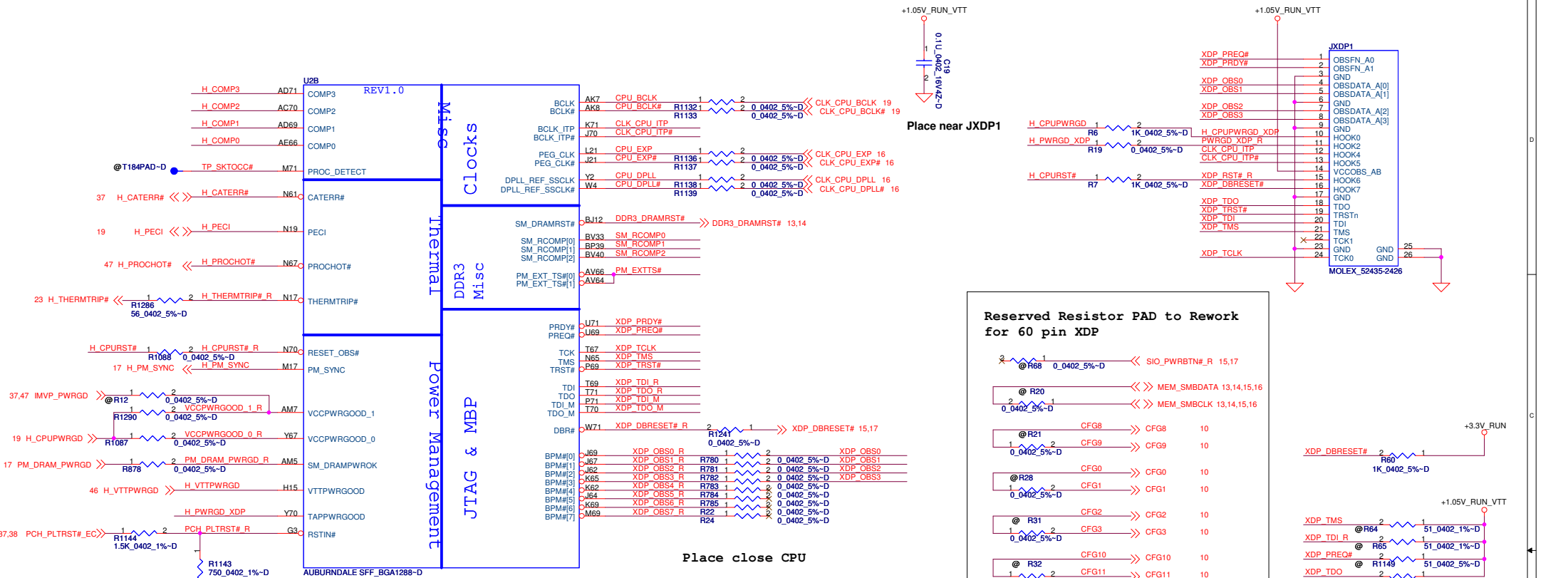
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Auburdale (1/6)

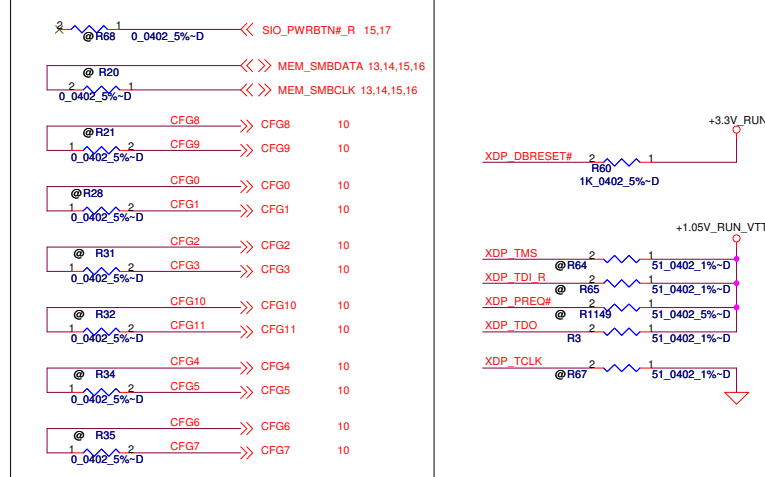
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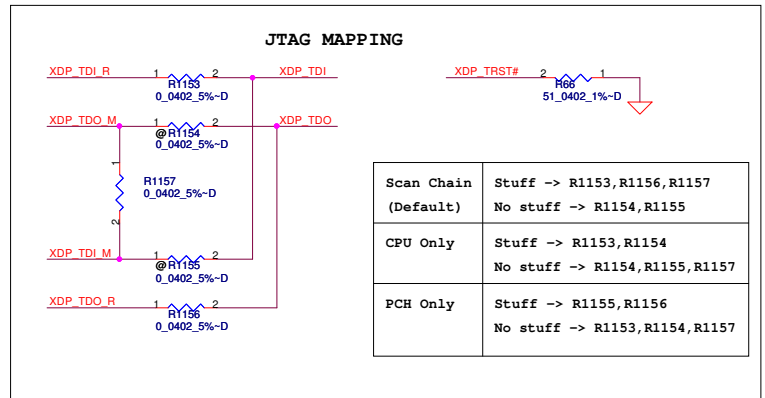
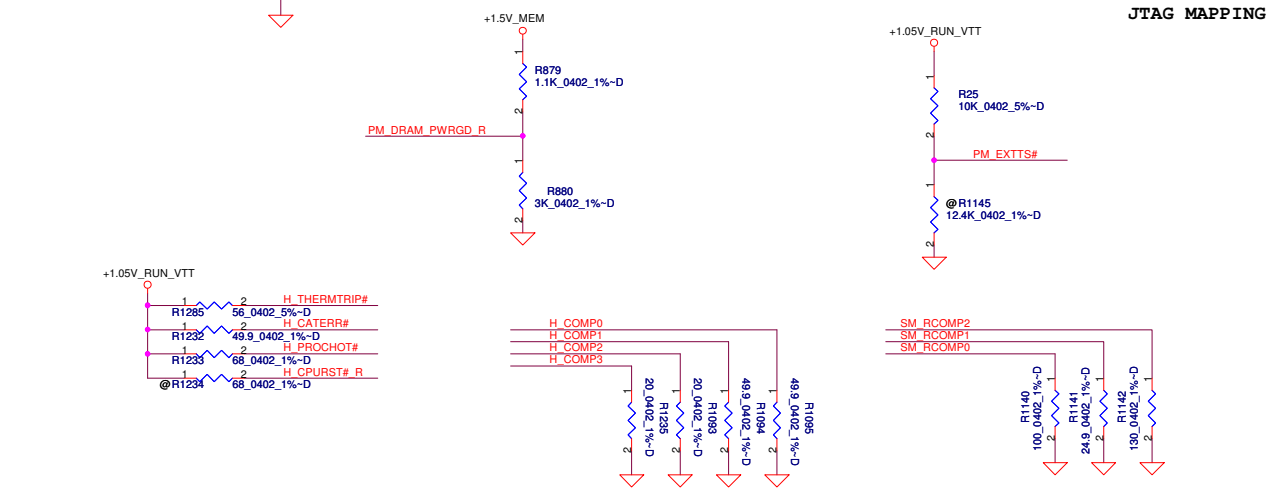
Place near JXDP1

Reserved Resistor PAD to Rework for 60 pin XDP



Place close CPU

JTAG MAPPING



Scan Chain	Stuff ->
(Default)	Stuff -> R1153, R1156, R1157 No stuff -> R1154, R1155
CPU Only	Stuff -> R1153, R1154 No stuff -> R1154, R1155, R1157
PCH Only	Stuff -> R1155, R1156 No stuff -> R1153, R1154, R1157

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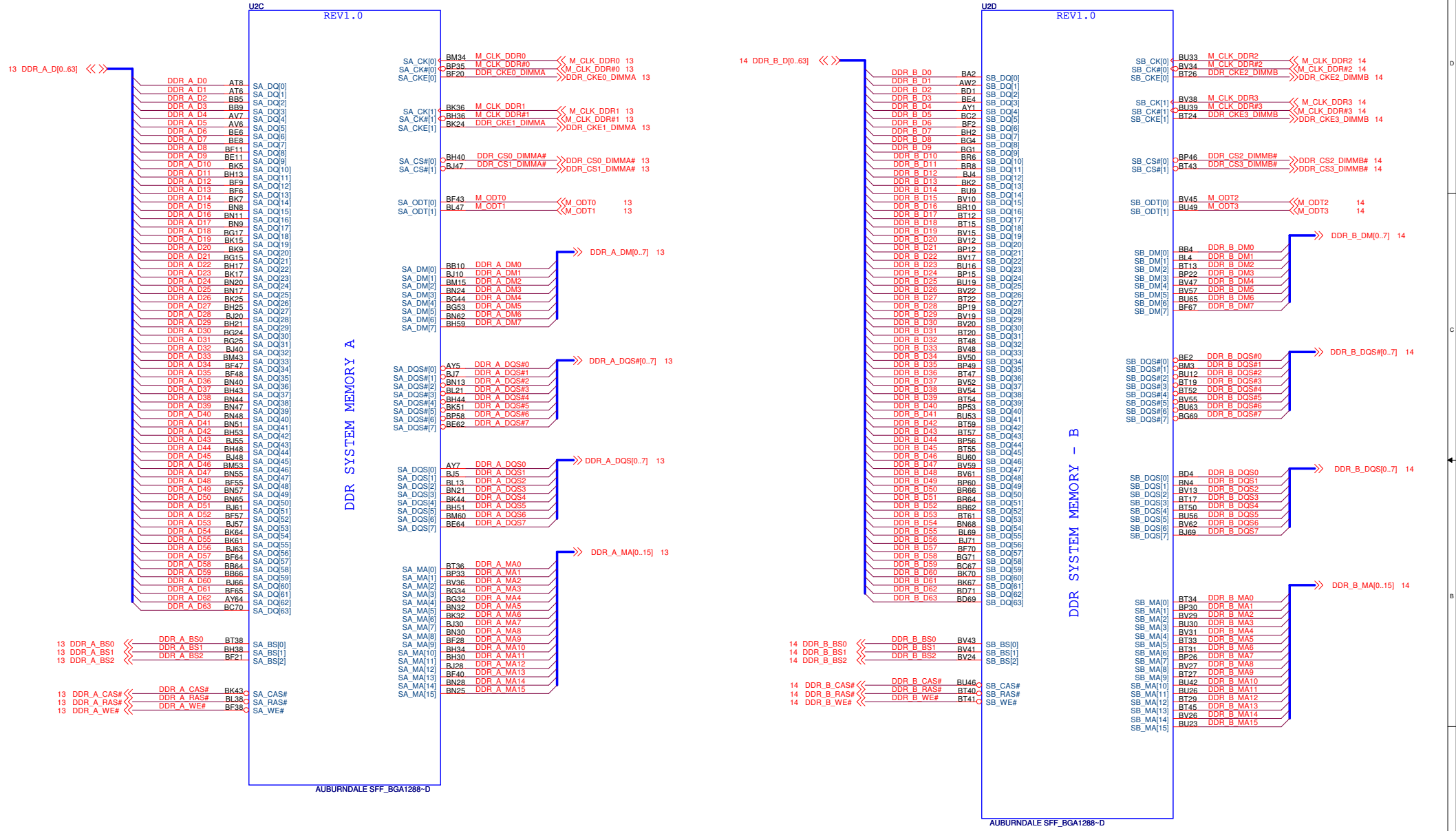
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DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY - B

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AUBURDALE SFF_BGA1288-D

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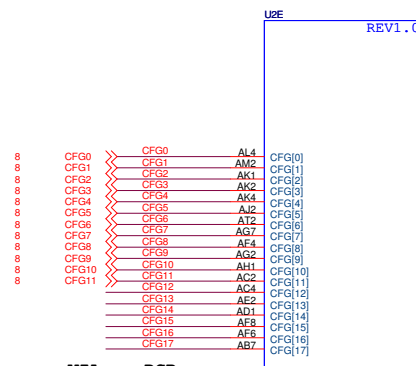
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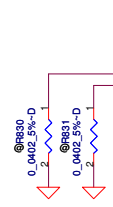
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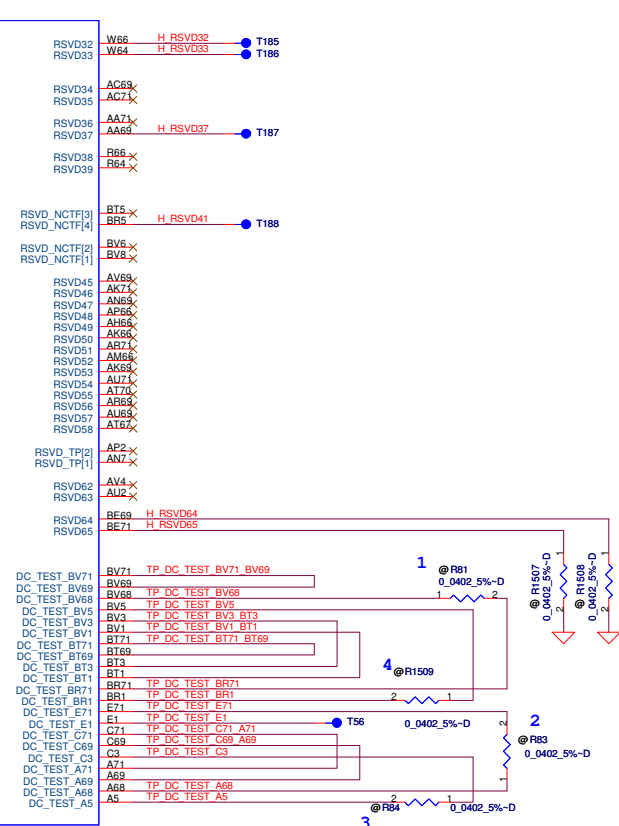




Reserve VIA on PCB



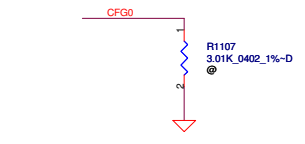
RESERVED



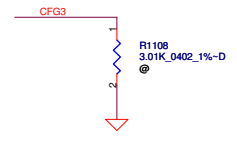
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Package Daisy Chain:

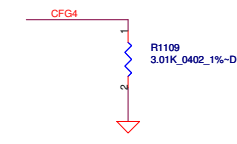
- 1: BR71 - pkg - BT71- board - BT69 - pkg - BV71 - board - BV69 - pkg - BV68
- 2: A68 - pkg - A69 - board - C69 - pkg - A71 - board - C71 - pkg - E71
- 3: A5 - pkg - C3
- 4: BR1 - pkg - BT1 - board - BV1 - pkg - BT3 - board - BV3 - pkg - BV5



PCI-Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enable



PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Number Reversed 15->0, 14->1 ...



Display Port Presence	
CFG4*	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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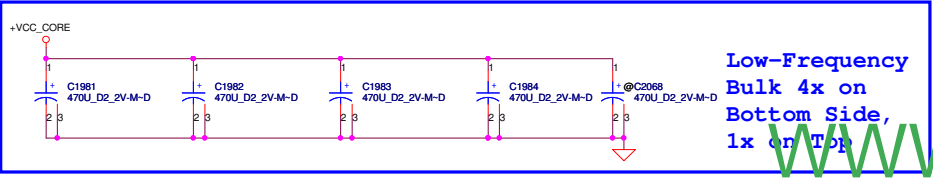
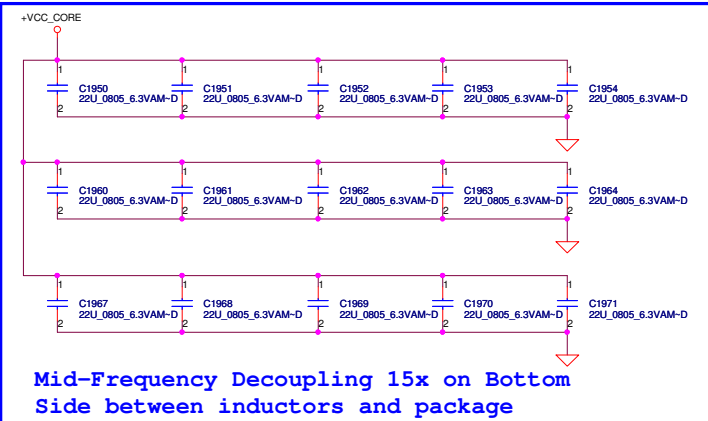
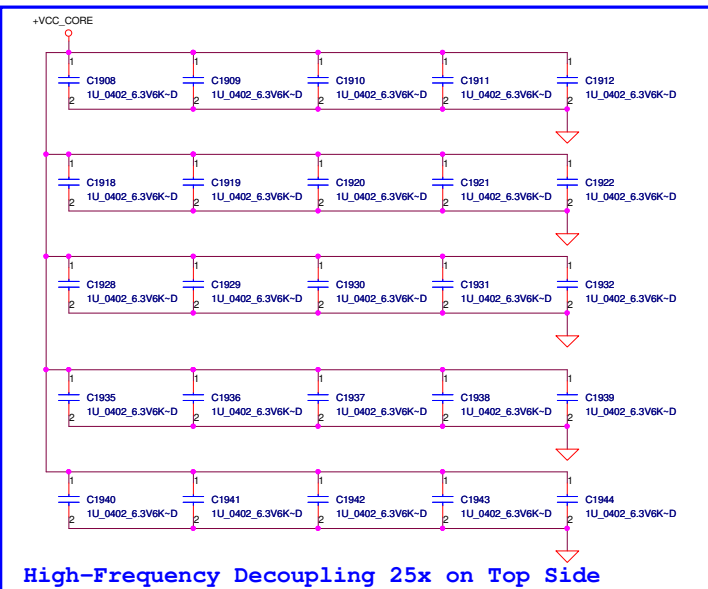
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Auburndale (4/6)

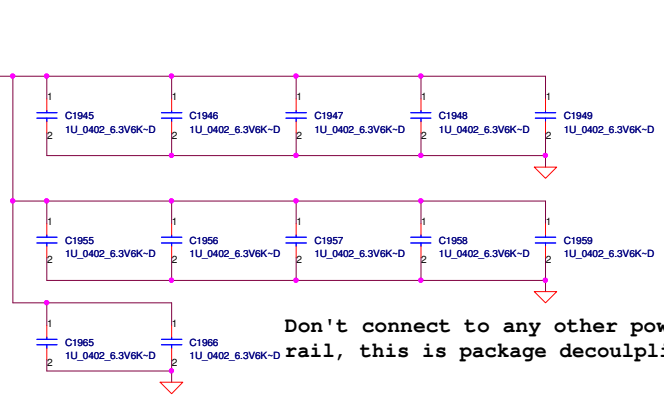
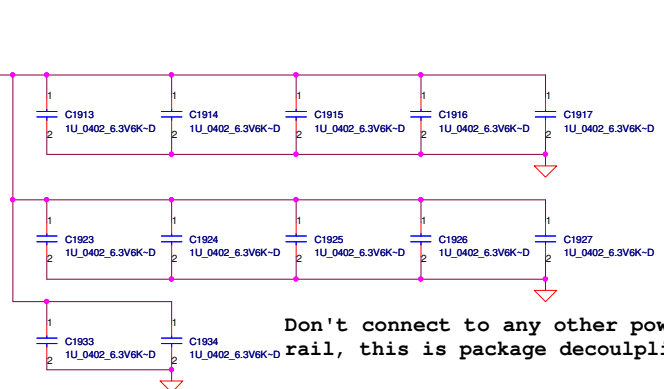
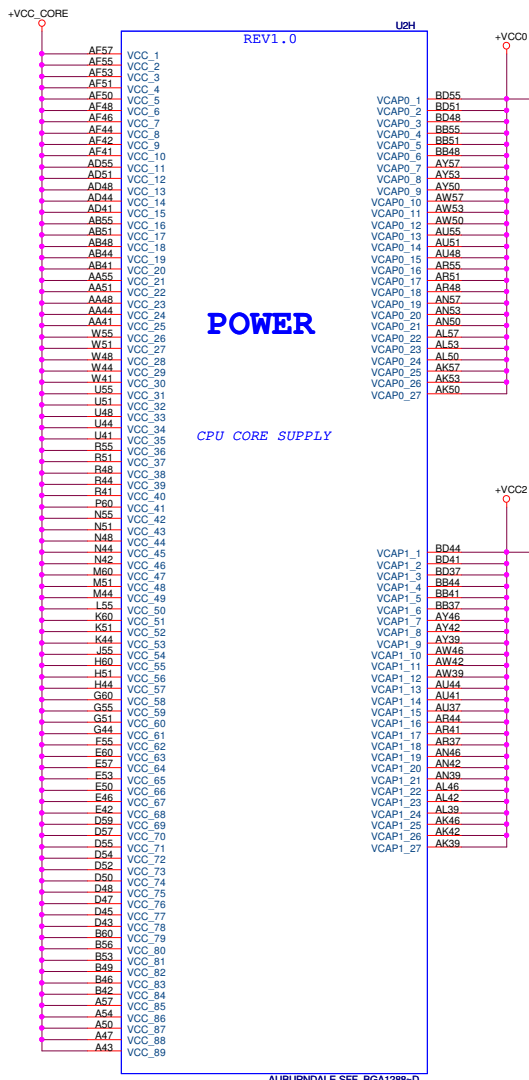
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Current =48A



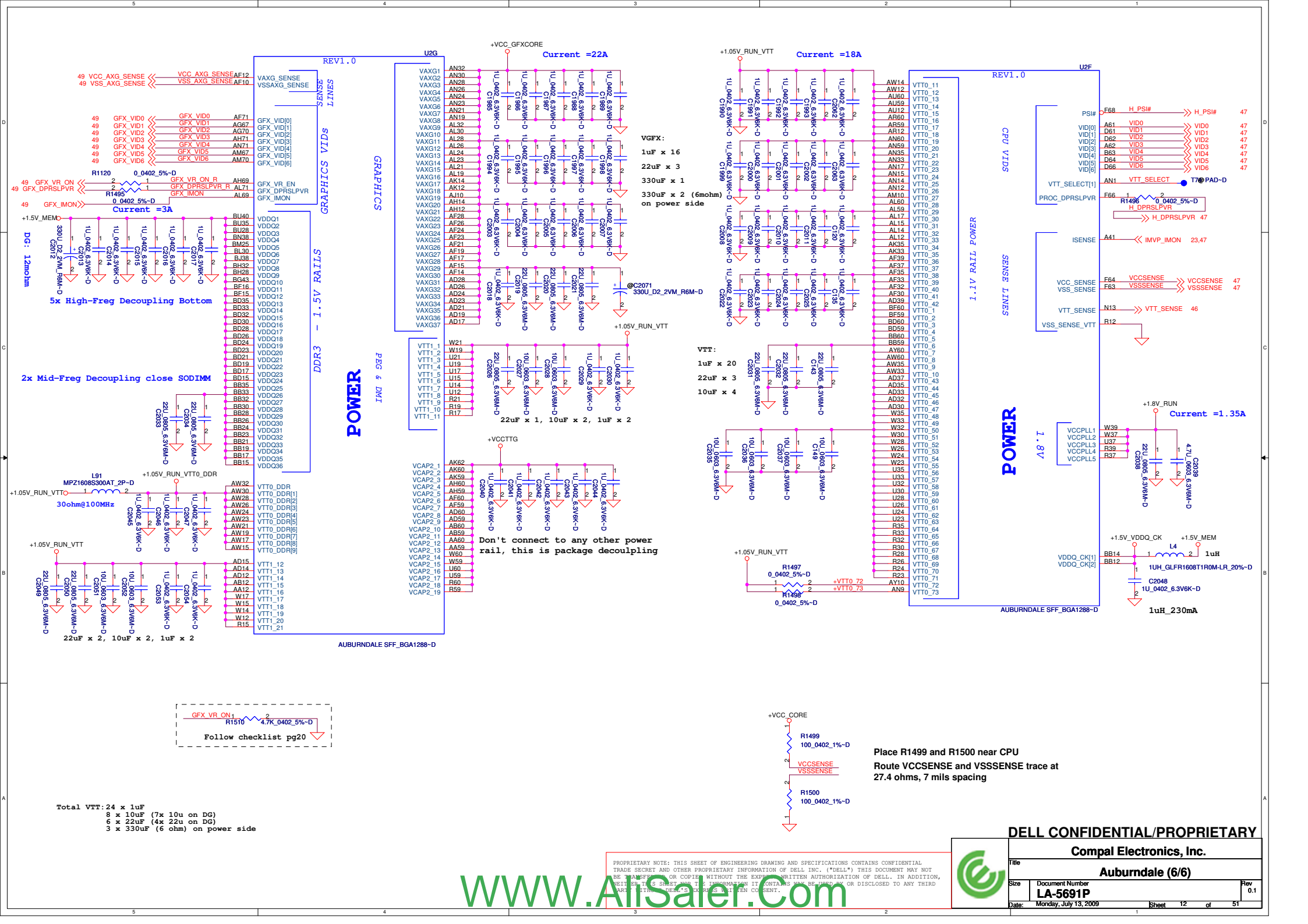
PROCESSOR Power Rail Table (EDS V1.0)		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VAXG	1.5	22
VccPLL	1.8	1.35
VCORE	0.75	48
VDDR	1.5	3
VTT	1.05	18

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GFX_VR_ON; R1510 4.7K_0402_5%-D
Follow checklist pg20

Total VTT: 24 x 1uF
8 x 10uF (7x 10u on DG)
6 x 22uF (4x 22u on DG)
3 x 330uF (6 ohm) on power side

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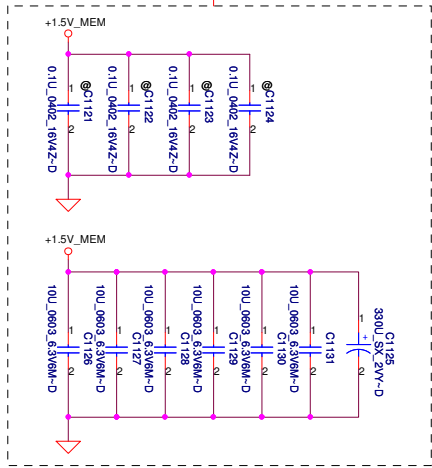
Auburndale (6/6)

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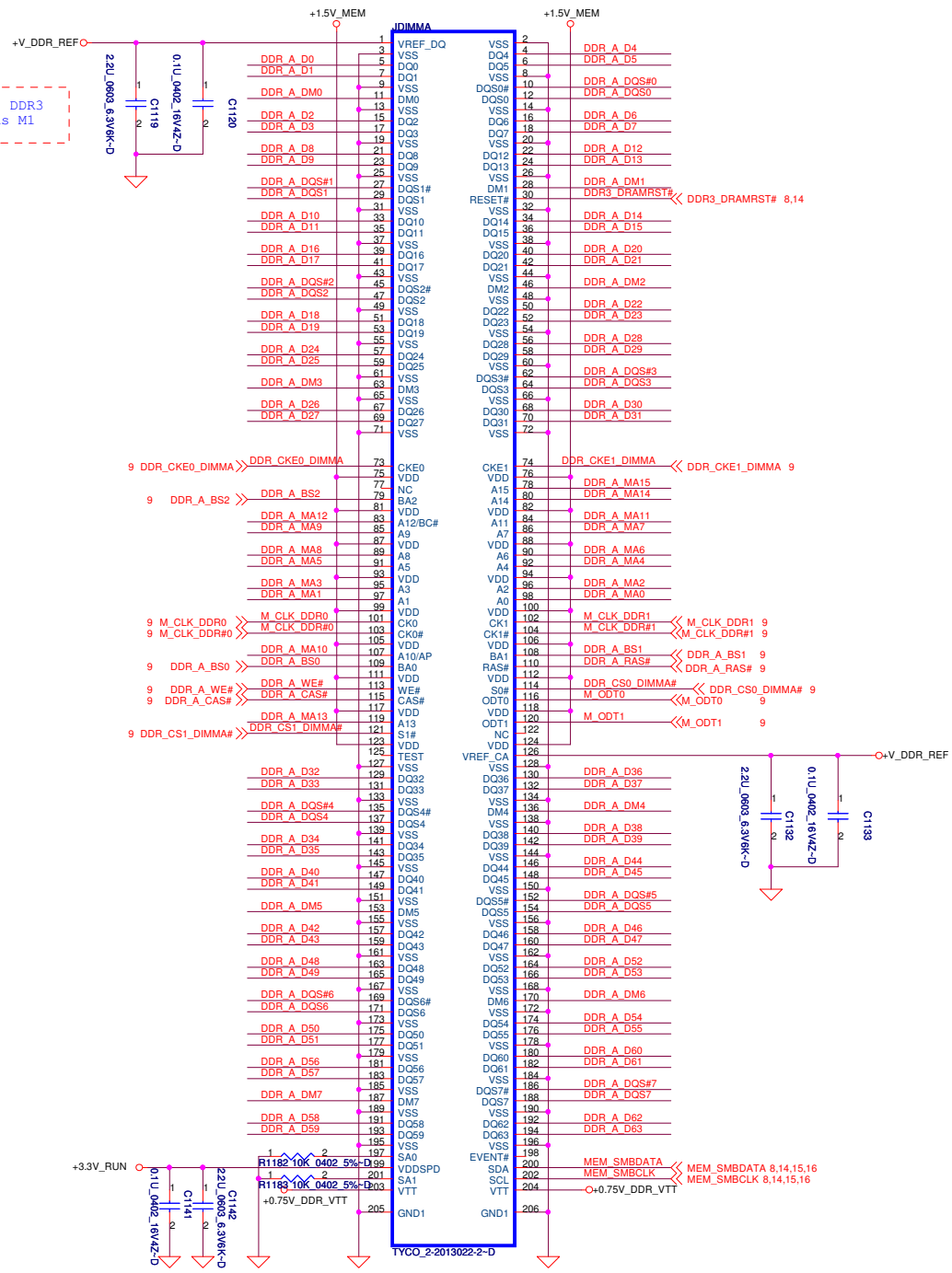
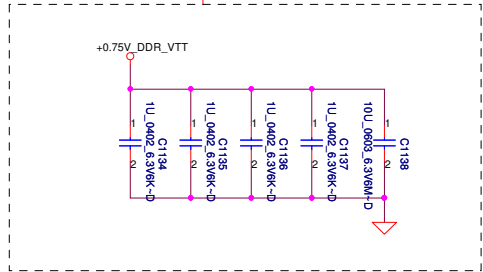
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- 9 DDR_A_D[0..63] <<>
- 9 DDR_A_DM[0..7] <<>
- 9 DDR_A_DQS#[0..7] <<>
- 9 DDR_A_MA#[0..15] <<>

Populate R87 for Intel DDR3 VREFDQ multiple methods M1

Layout Note:
Place near JDIMMA



Layout Note:
Place near JDIMMA. 203, 204



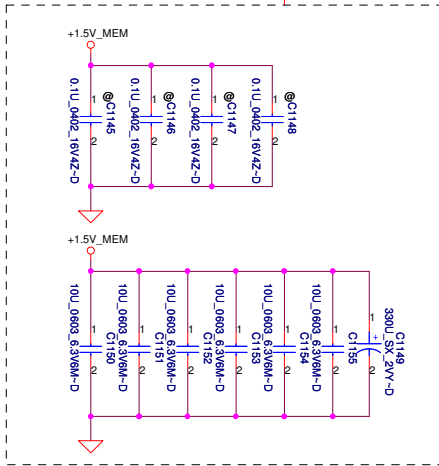
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DDR3II-SODIMM SLOT1			
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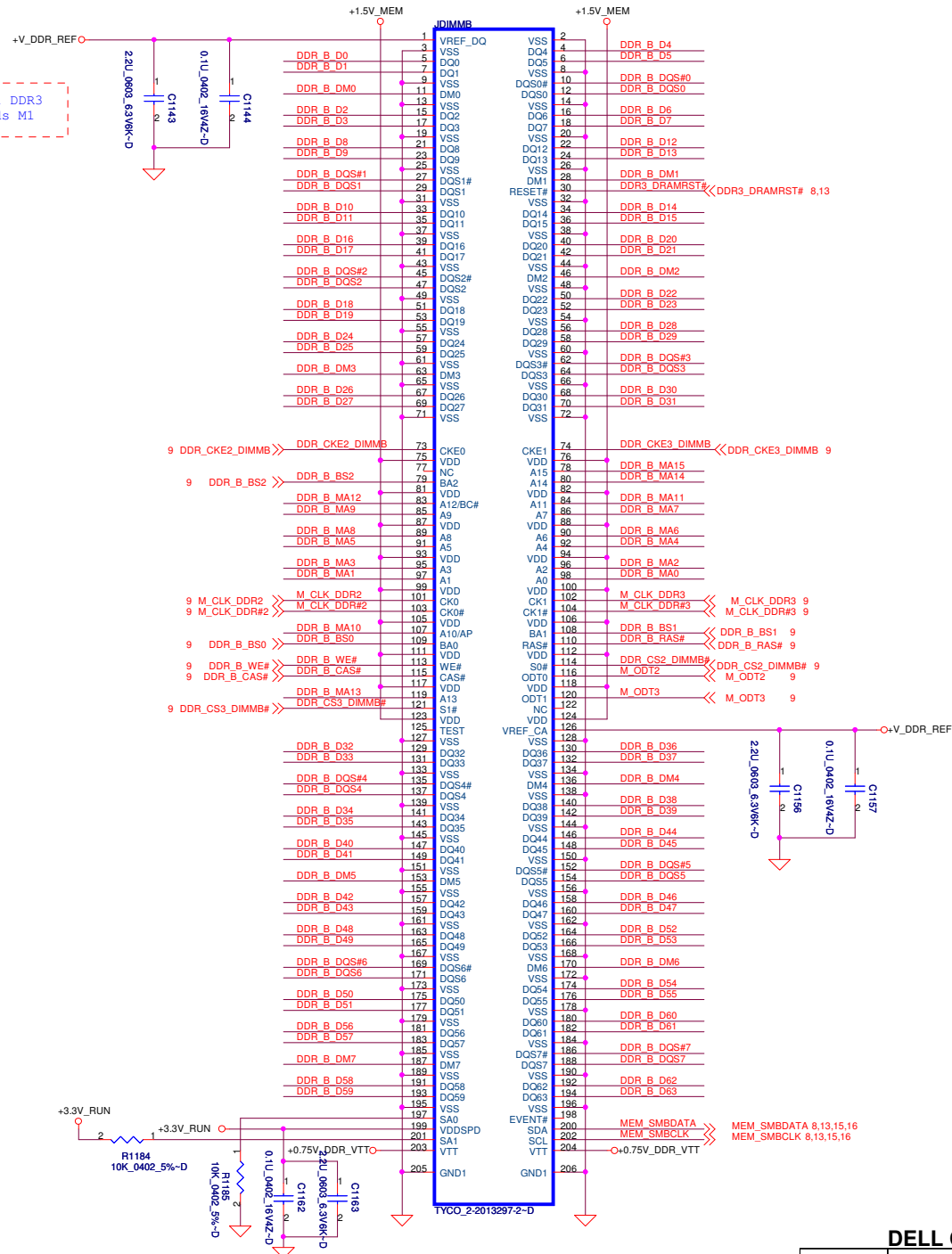
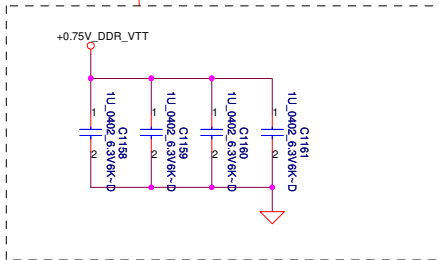
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- 9 DDR_B_DM0..63 <<>
- 9 DDR_B_DM[0..7] <<>
- 9 DDR_B_DQS#0..7 <<>
- 9 DDR_B_MA[0..15] <<>

Populate R88 for Intel DDR3 VREFDQ multiple methods M1

Layout Note:
Place near JDIMMB



Layout Note:
Place near JDIMMB.203,204



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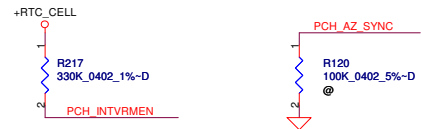


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Title DDR3-SODIMM SLOT2			
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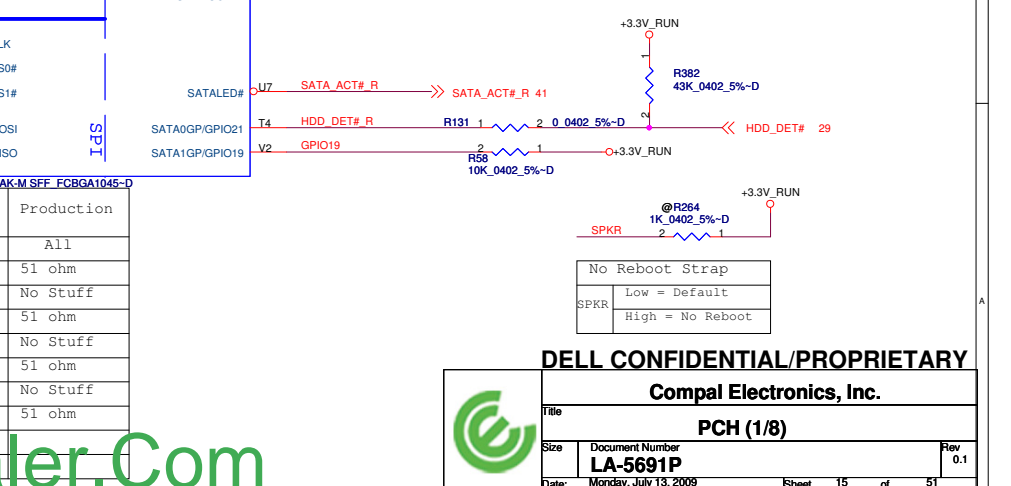
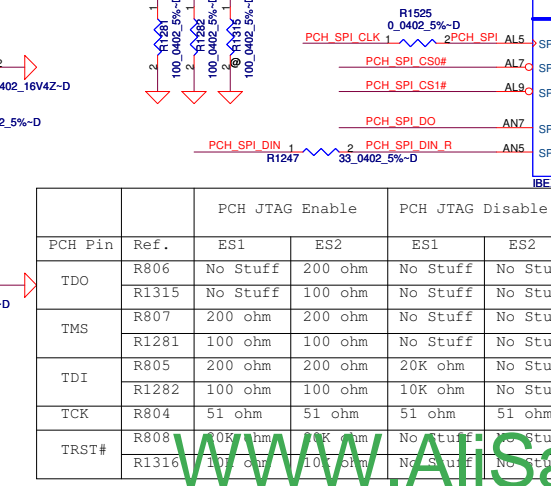
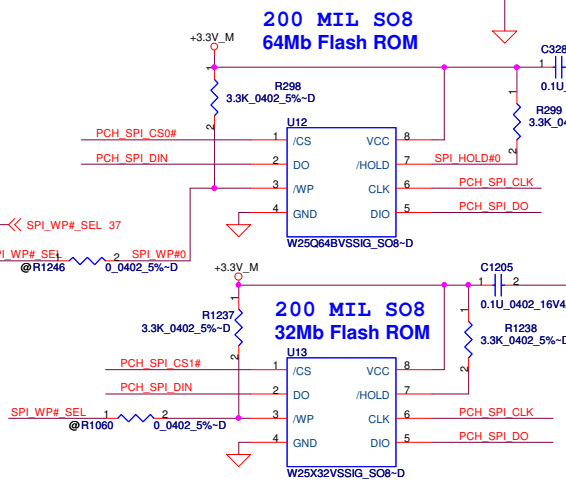
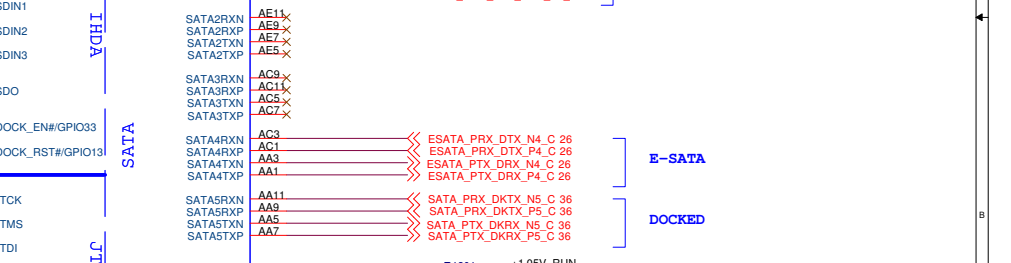
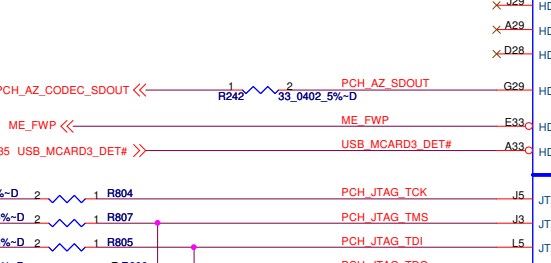
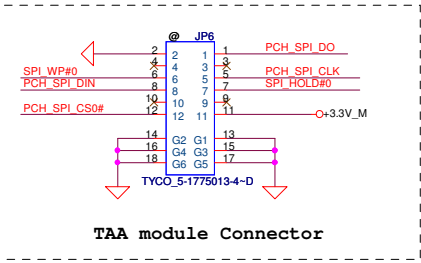
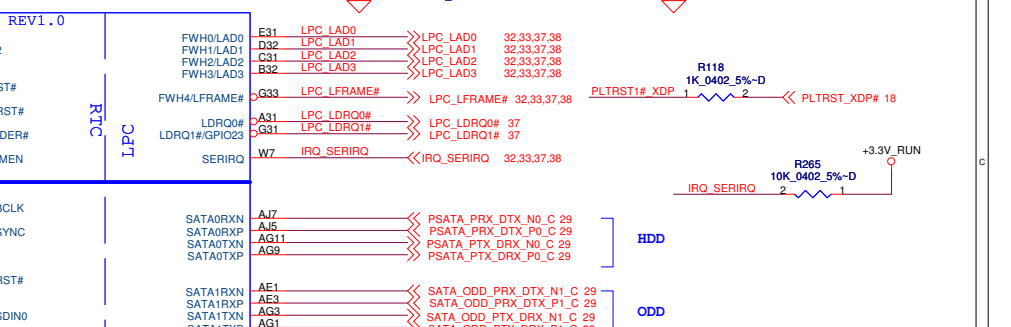
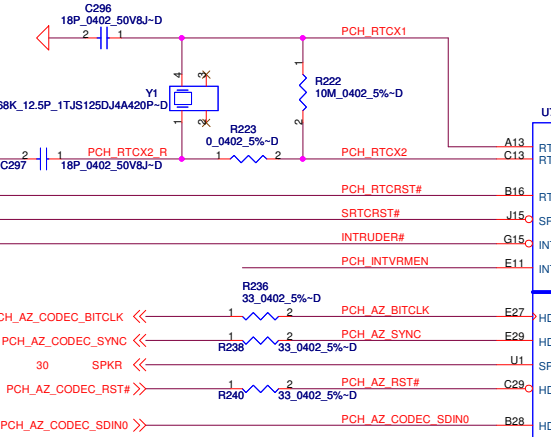
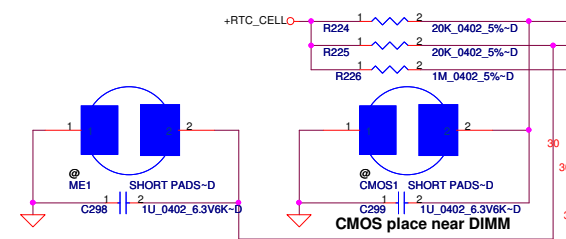
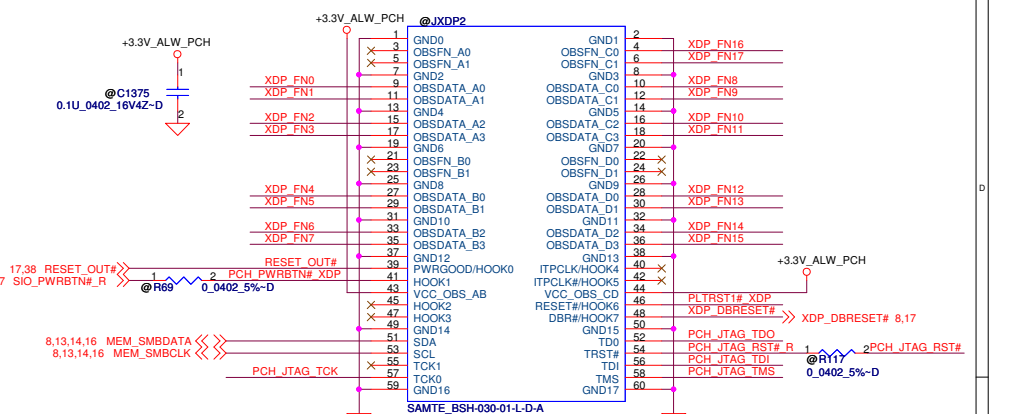
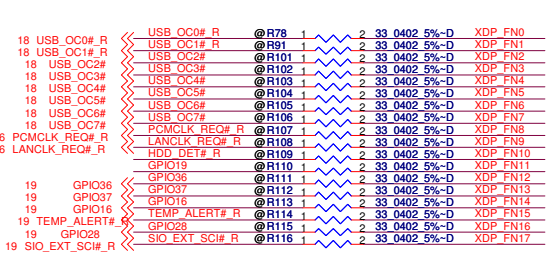
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



INTRVEM - Integrated SUS
 1.1V VRM Enable
 High - Enable Internal VRs

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low



PCH Pin	Ref.	PCH JTAG Enable		PCH JTAG Disable		Production
		ES1	ES2	ES1	ES2	
TDO	R806	No Stuff	200 ohm	No Stuff	No Stuff	51 ohm
	R1315	No Stuff	100 ohm	No Stuff	No Stuff	No Stuff
TMS	R807	200 ohm	200 ohm	No Stuff	No Stuff	51 ohm
	R1281	100 ohm	100 ohm	No Stuff	No Stuff	No Stuff
TDI	R805	200 ohm	200 ohm	20K ohm	No Stuff	51 ohm
	R1282	100 ohm	100 ohm	10K ohm	No Stuff	No Stuff
TCK	R804	51 ohm	51 ohm	51 ohm	51 ohm	51 ohm
TRST#	R808	20K ohm	20K ohm	No Stuff	No Stuff	No Stuff
	R1316	100 ohm	100 ohm	No Stuff	No Stuff	No Stuff



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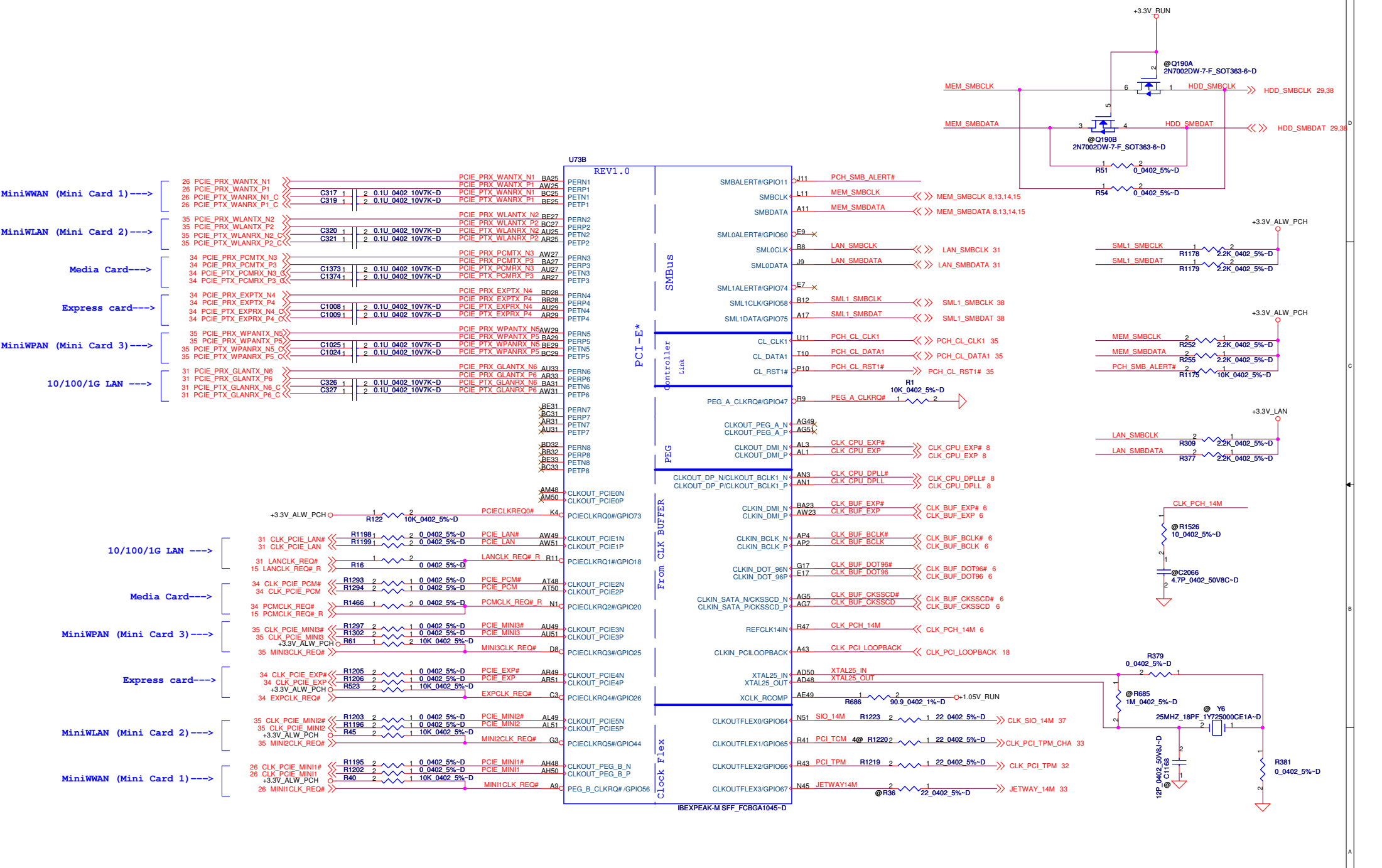
PCH (1/8)

Title: _____

Size: _____ Document Number: **LA-5691P** Rev: 0.1

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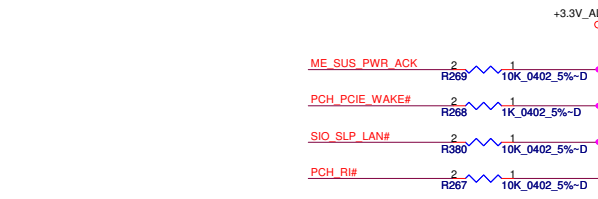
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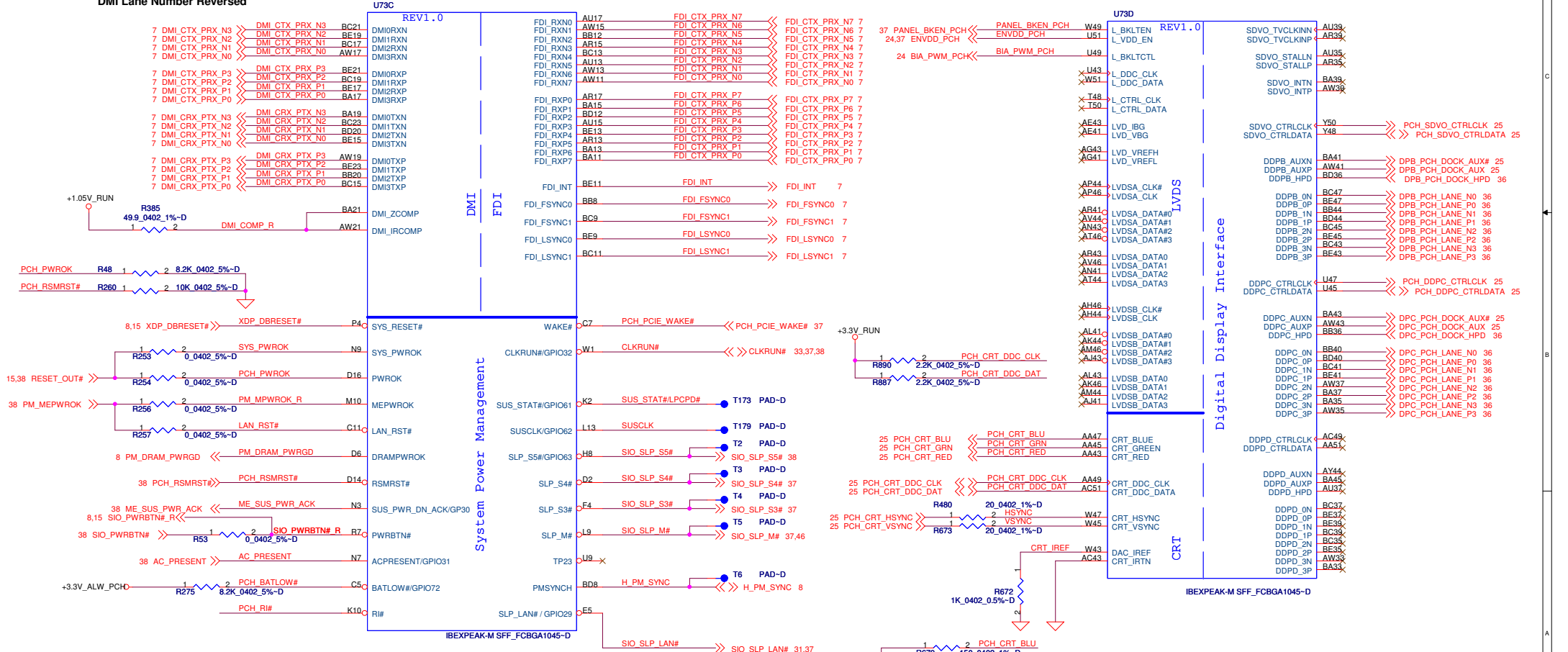
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PCH (2/8)		
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DMI Lane Number Reversed

FDI Lane Number Reversed



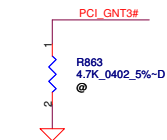
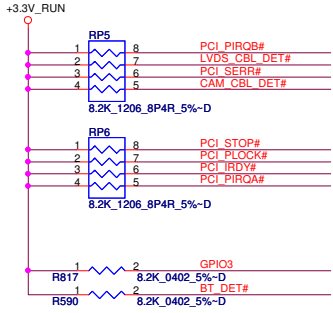
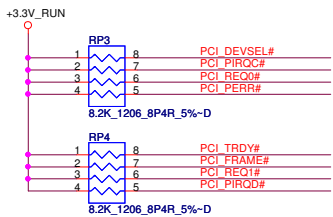
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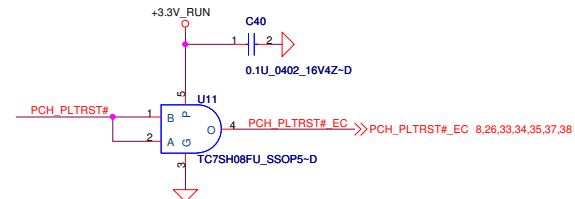
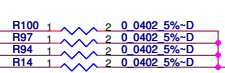


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Size	Document Number	Rev		0.1	
	LA-5691P				
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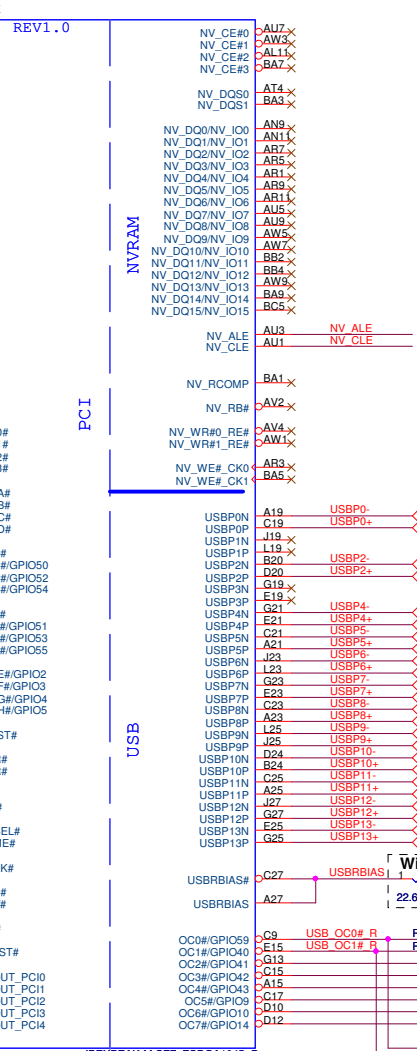
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A16 swap override Strap/Top-Block	
Swap Override jumper	
PCI_GNT#3	Low = A16 swap
	High = Default

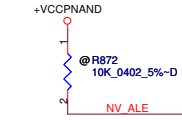
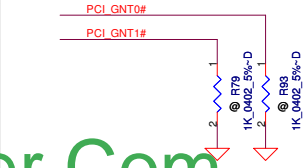


U73E
REV1.0

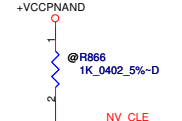


- >Right Side
- >Left Side
- >WLAN
- >WWAN
- >Blue Tooth
- >BIO
- >DOCK
- >Express Card
- >Camera
- >BKT
- >WPAN

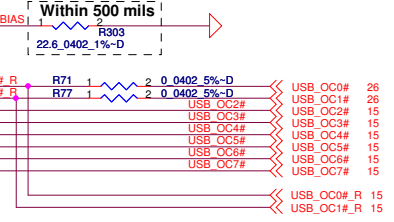
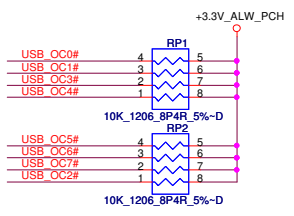
Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	Reserved



Danbury Technology Enabled	
NV_ALE	High = Enabled (Default) Low = Disabled



DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

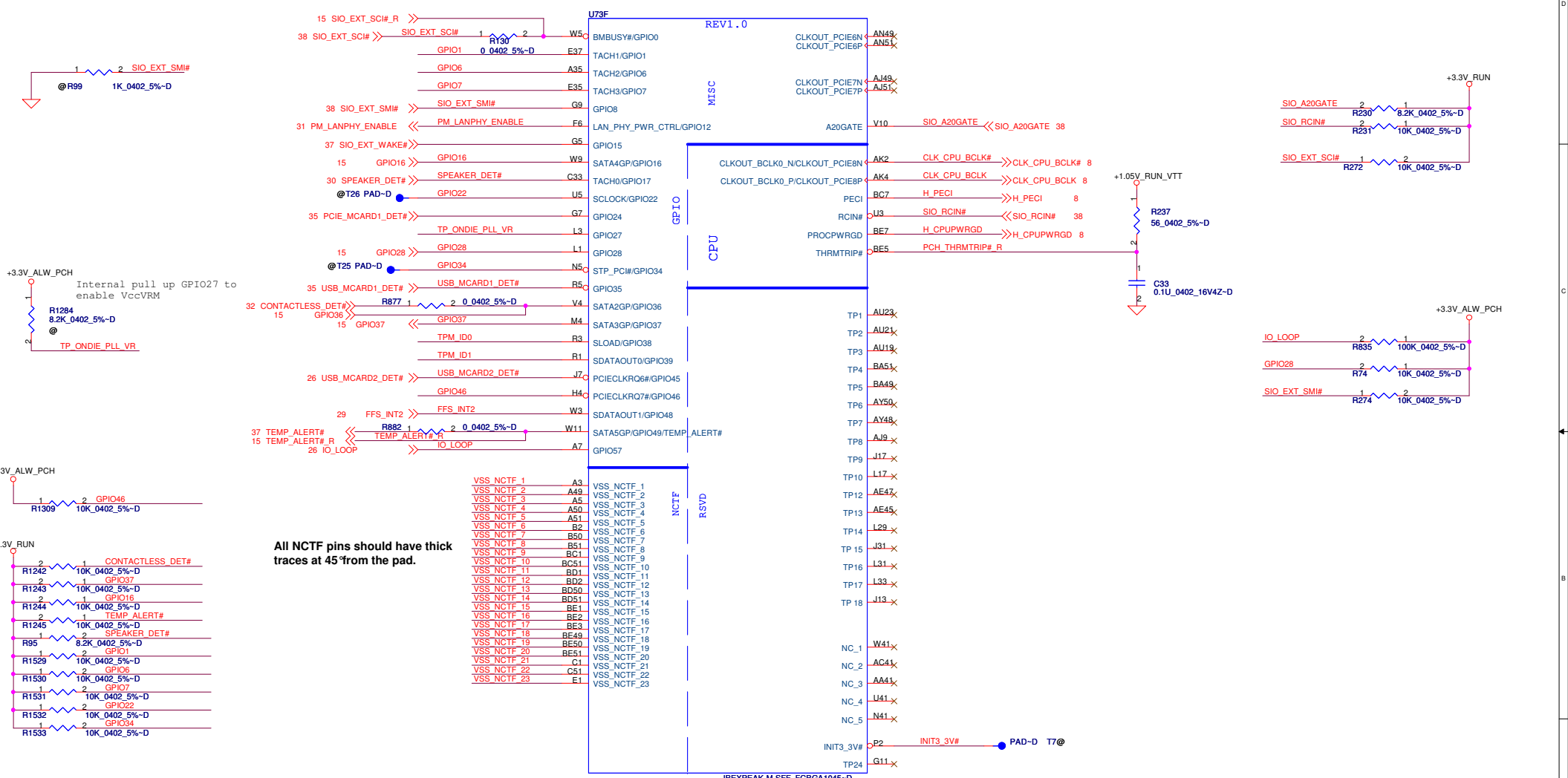


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All NCTF pins should have thick traces at 45° from the pad.

- VSS_NCTF_1 A3
- VSS_NCTF_2 A49
- VSS_NCTF_3 A5
- VSS_NCTF_4 A50
- VSS_NCTF_5 A51
- VSS_NCTF_6 B2
- VSS_NCTF_7 B50
- VSS_NCTF_8 B51
- VSS_NCTF_9 BC1
- VSS_NCTF_10 BC51
- VSS_NCTF_11 BD1
- VSS_NCTF_12 BD2
- VSS_NCTF_13 BD50
- VSS_NCTF_14 BD51
- VSS_NCTF_15 BE1
- VSS_NCTF_16 BE2
- VSS_NCTF_17 BE3
- VSS_NCTF_18 BE49
- VSS_NCTF_19 BE50
- VSS_NCTF_20 BE51
- VSS_NCTF_21 C1
- VSS_NCTF_22 C51
- VSS_NCTF_23 E1

	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
USH1.0 (For SSI)	1	0
USH1.0	1	1

-----> will use MEMO control pop R339 & de-pop R787 when USH1.0 enable for SSI build only

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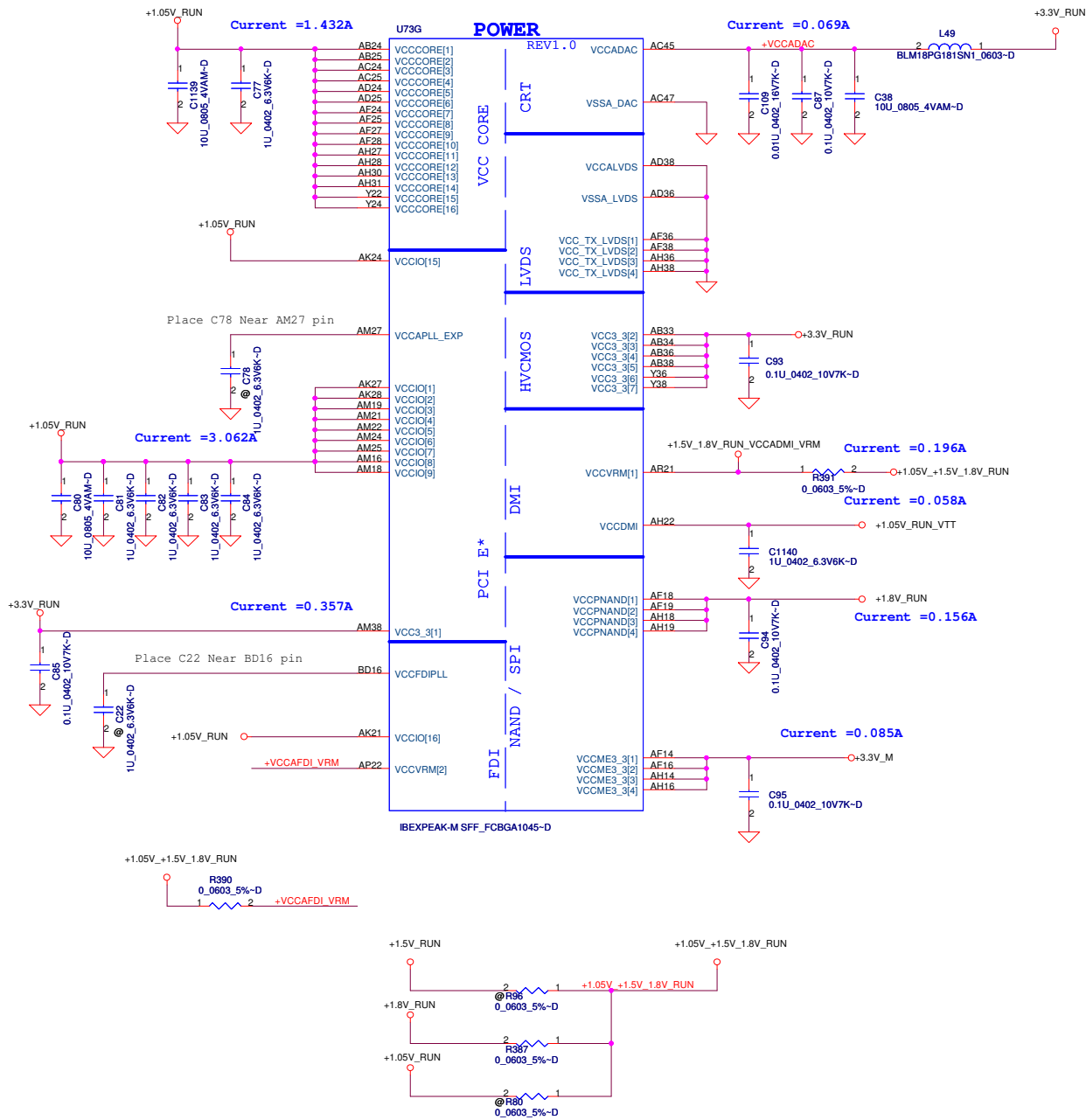
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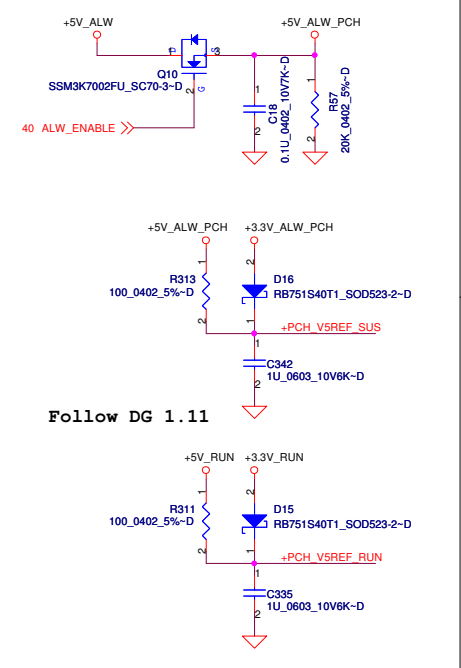
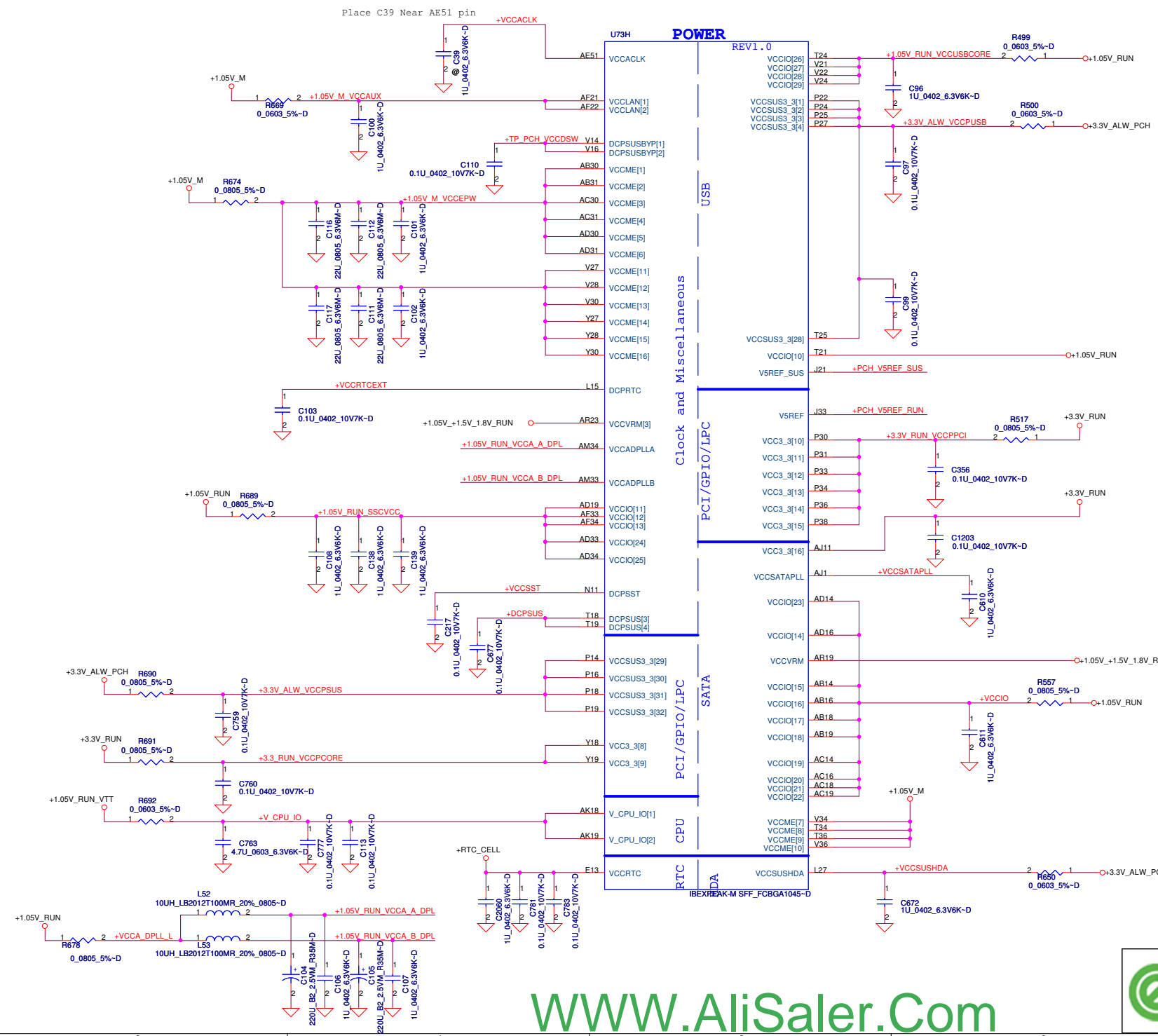
PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_CPU_IO	1.1/1.05	< 1 (mA)
V5REF	5	< 1 (mA)
V5REF_Sus	5	< 1 (mA)
Vcc3_3	3.3	0.357
VccAC1k	1.1	0.052
VccADAC	3.3	0.069
VccADPLLA	1.1	0.068
VccADPLLB	1.1	0.069
Vccap11EXP	1.1	0.04
VccCore	1.1	1.432
VccDMI	1.1	0.058
VccDMI	1.1	0.061
VccFDIPLL	1.1	0.037
VccIO	1.1	3.062
VccLAN	1.1	0.32
VccME	1.1	1.849
VccME3_3	3.3	0.085
VccpNAND	1.8	0.156
VccRTC	3.3	2 (mA)
VccSATAPLL	1.1	0.031
VccSus3_3	3.3	0.163
VccSusHDA	3.3	0.006
VccVRM	1.8 / 1.5	0.196
VccALVDS	3.3	< 1 (mA)
VccTX_LVDS	1.8	0.059

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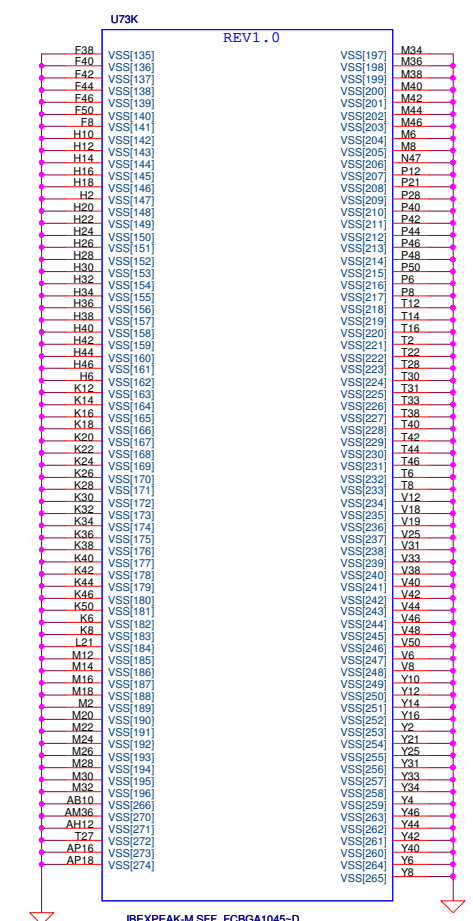
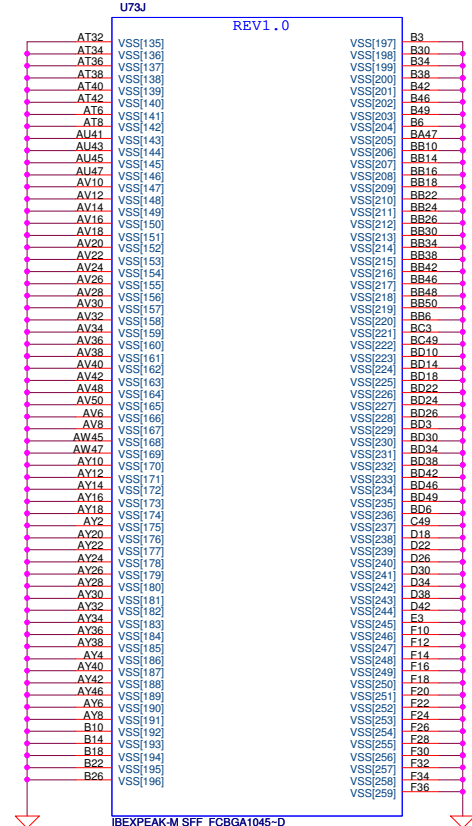
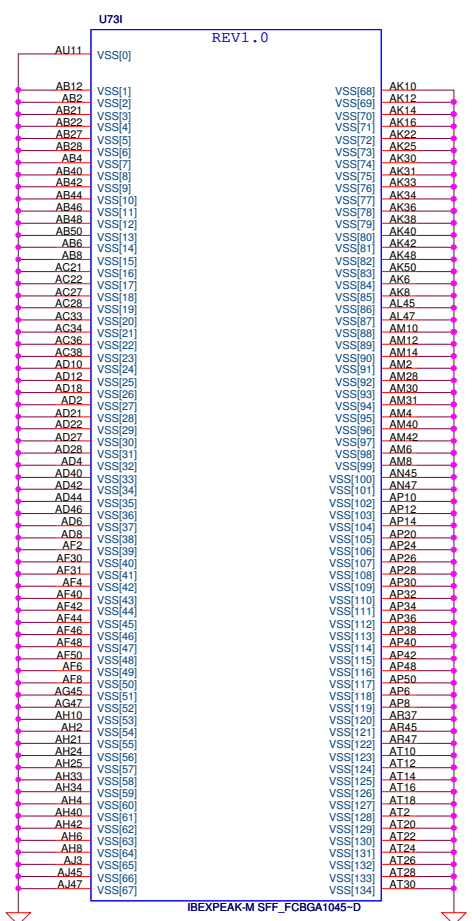


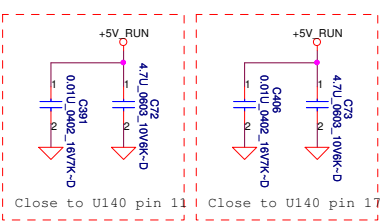
Follow DG 1.11

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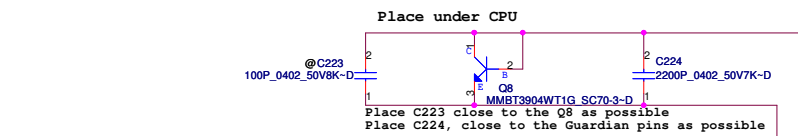
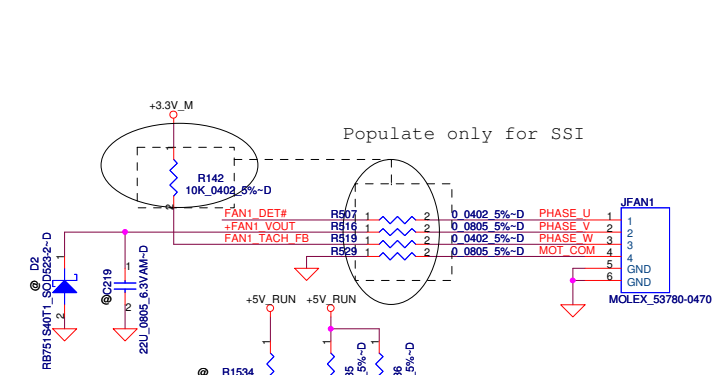
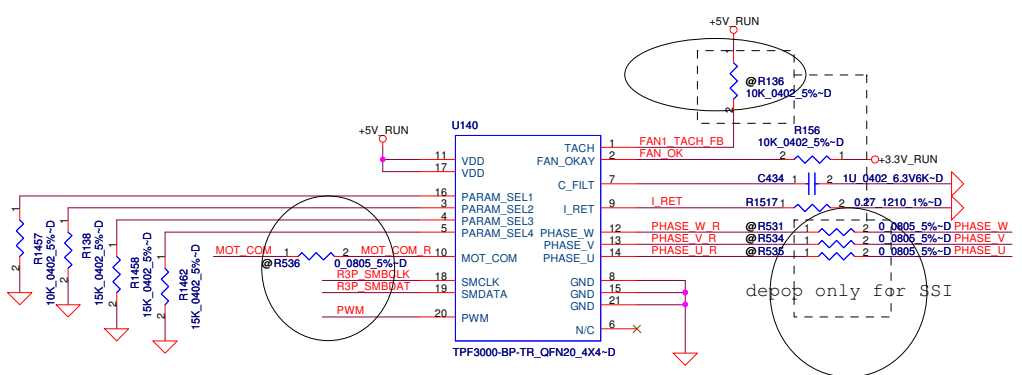
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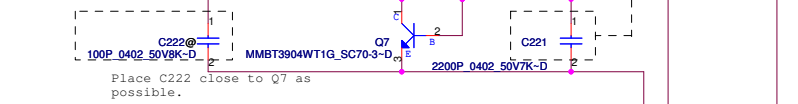




Close to U140 pin 11 Close to U140 pin 17

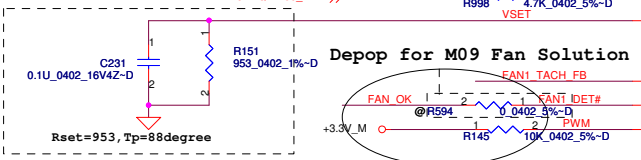
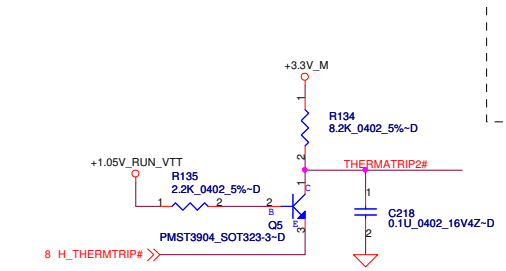


Place under CPU
Place C223 close to the Q8 as possible
Place C224, close to the Guardian pins as possible

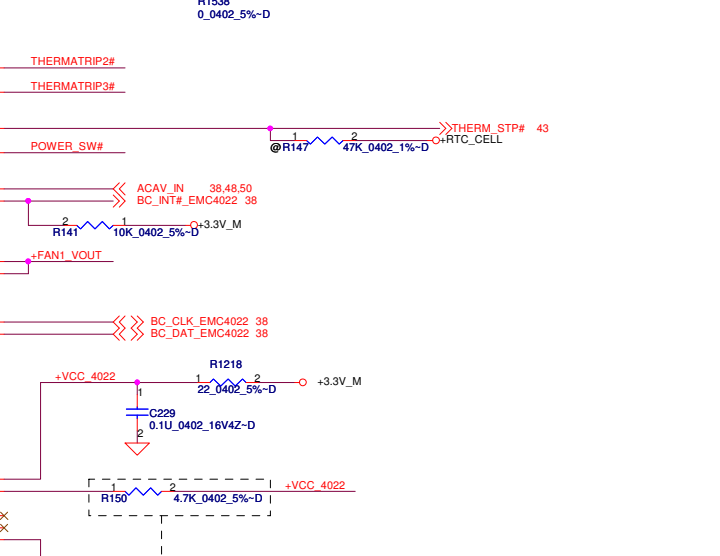
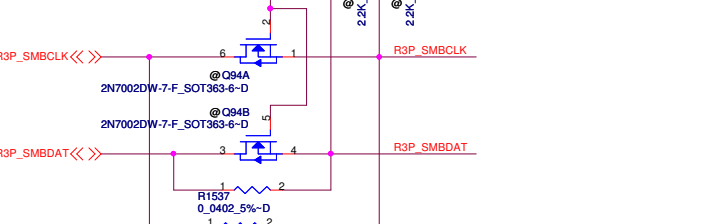
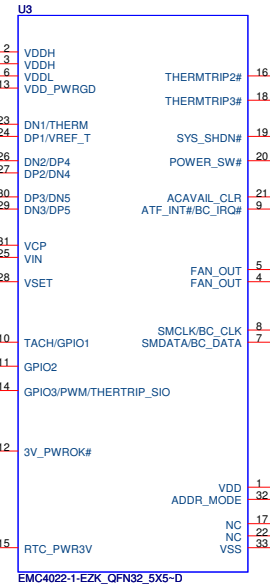
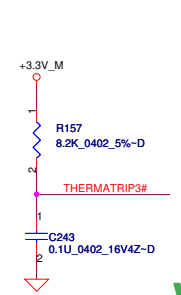


Diode circuit at DP4/DN4 is used for skin temp sensor (placed optimally between CPU, PCH).
Place C222 close to Q7 as possible.

Q9 Place near DIMM
Place C227 close to Q9



Depop for M9 Fan Solution
Rset=953, Tp=88degree



Pull-up Resistor on ADDR_MODE/XEN	For Remote mode	SMBUS Address
<= 4.7K +/- 5%	2N3904	2F (r/w)
10K	2N3904	2E (r/w)
18K	Thermistor	2F (r/w)
>= 33K	Thermistor	2E (r/w)

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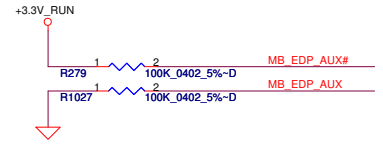
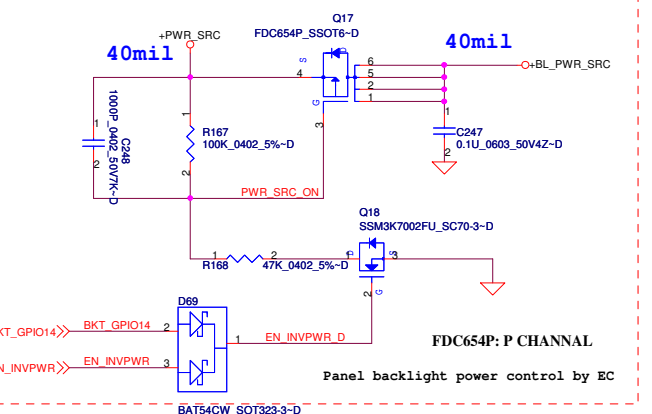
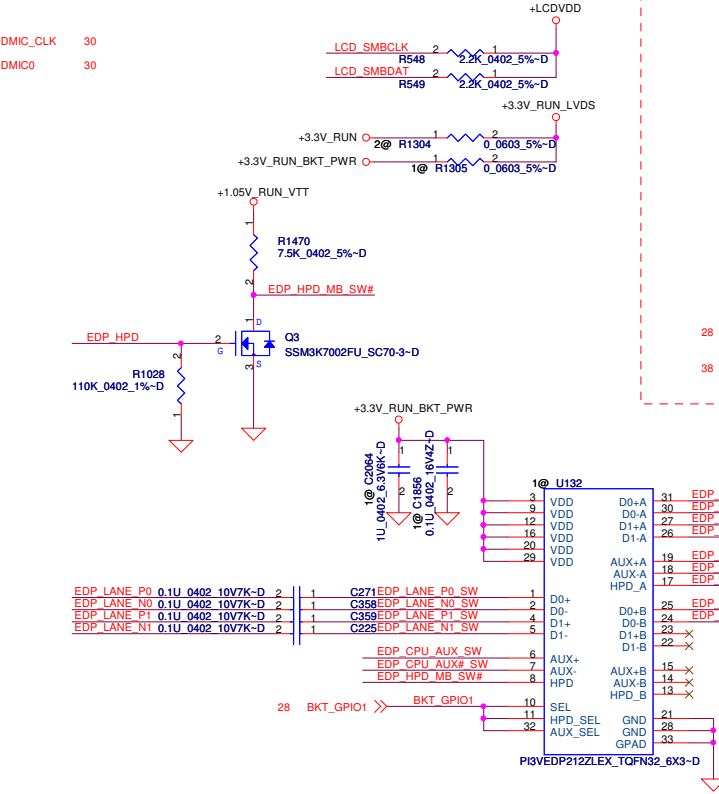
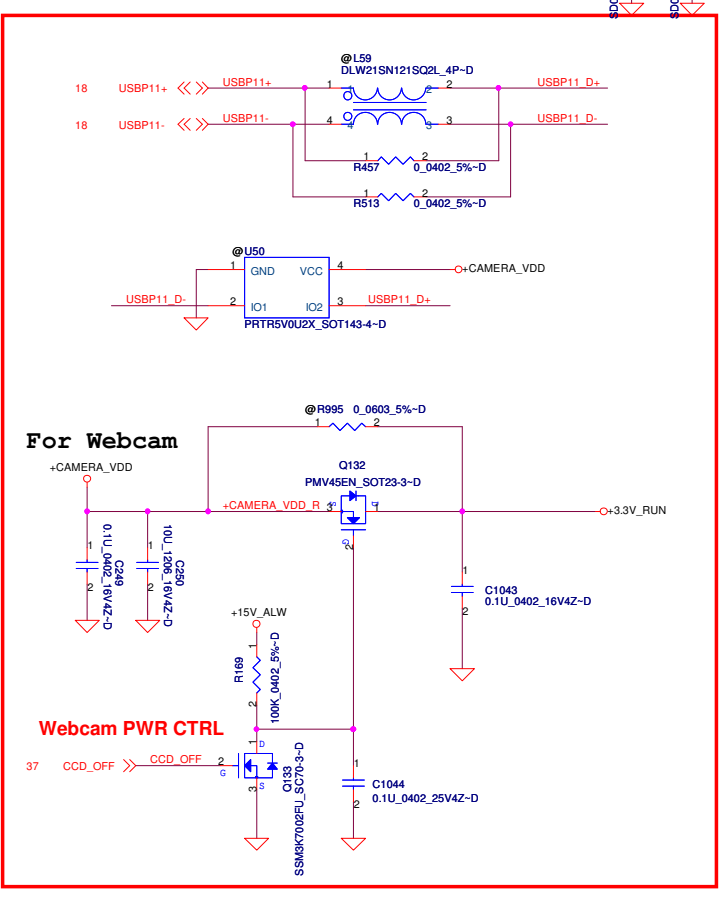
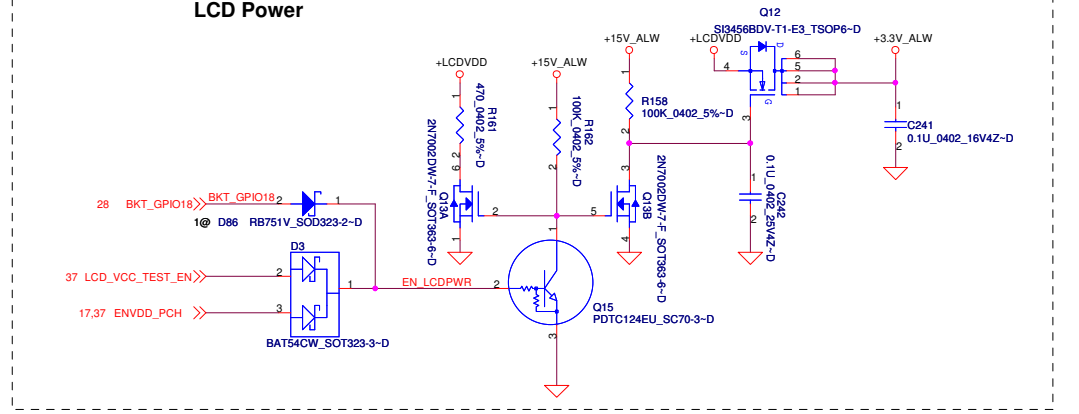
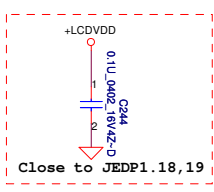
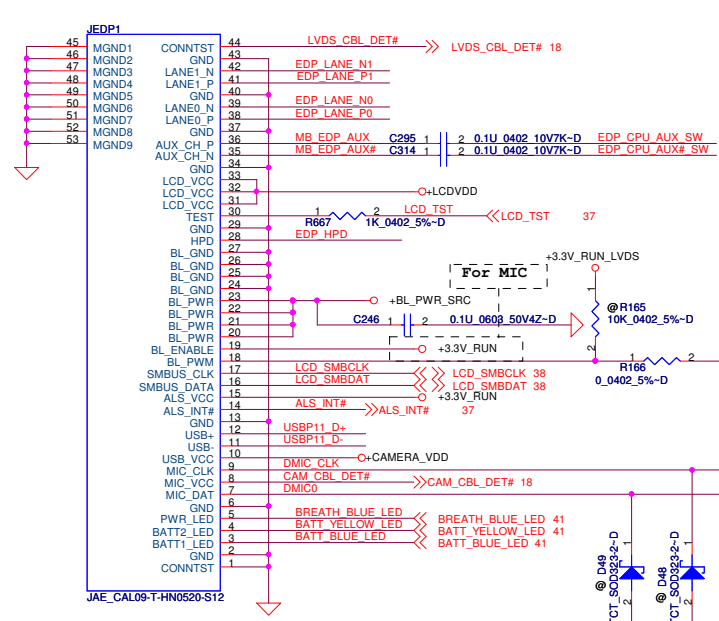
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FAN & Thermal Sensor

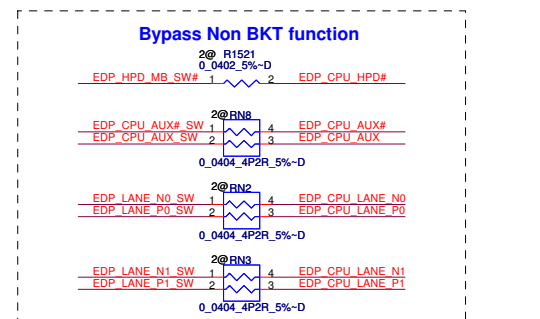
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Function	SEL/HPD_SEL/AUX_SSEL
Port A active	L
Port B active	H

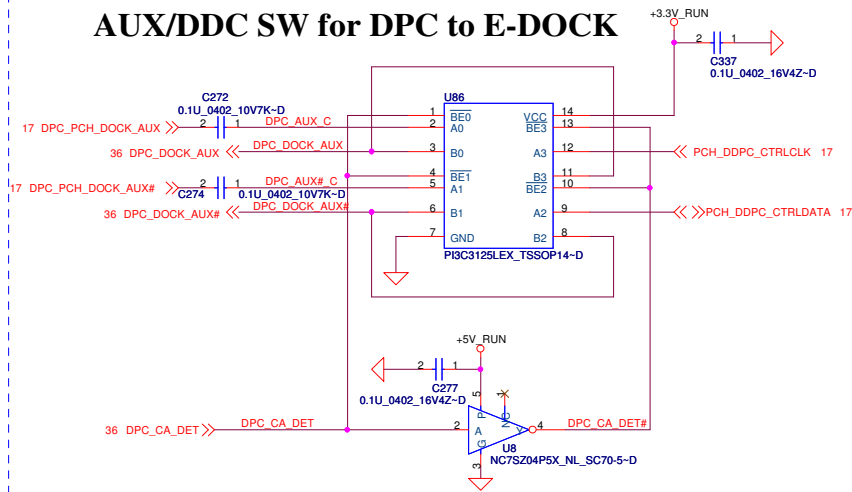


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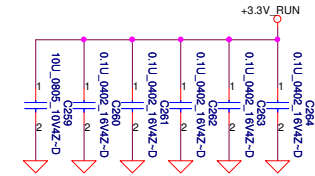
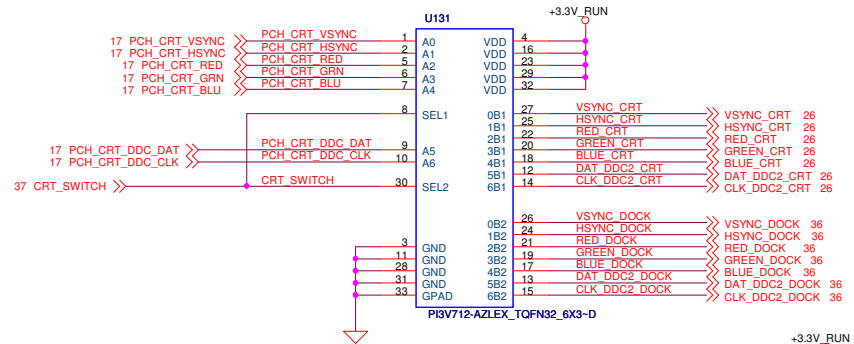
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eDP & CAM Conn

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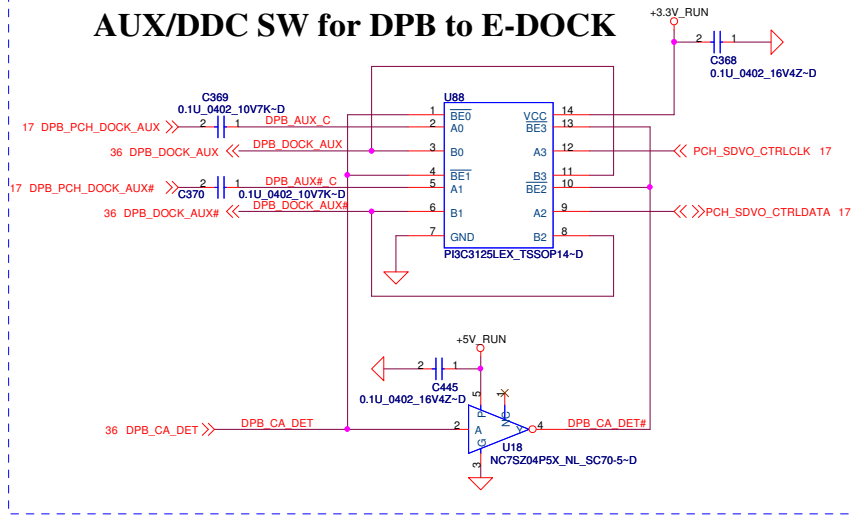
AUX/DDC SW for DPC to E-DOCK



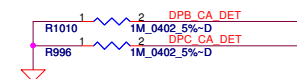
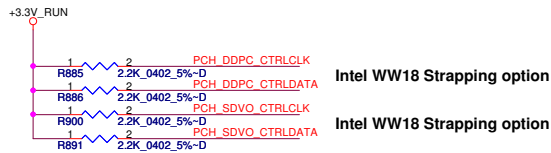
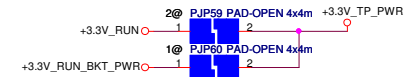
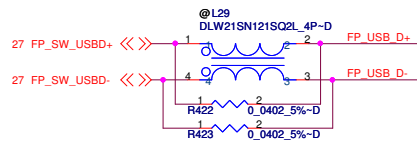
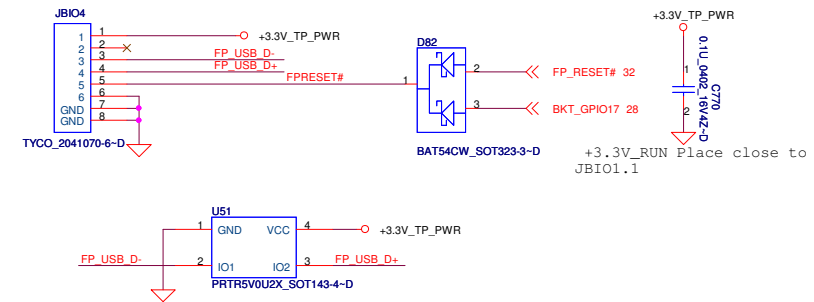
VGA SW for MB/DOCK



AUX/DDC SW for DPB to E-DOCK



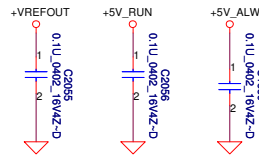
Fingerprint CONN.



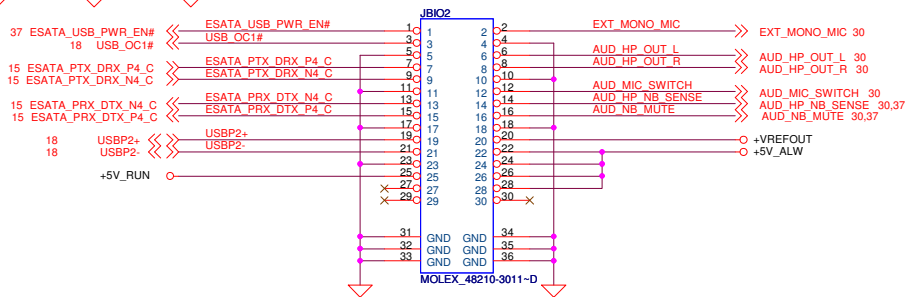
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Title: DPC DPD SW for DOCK			
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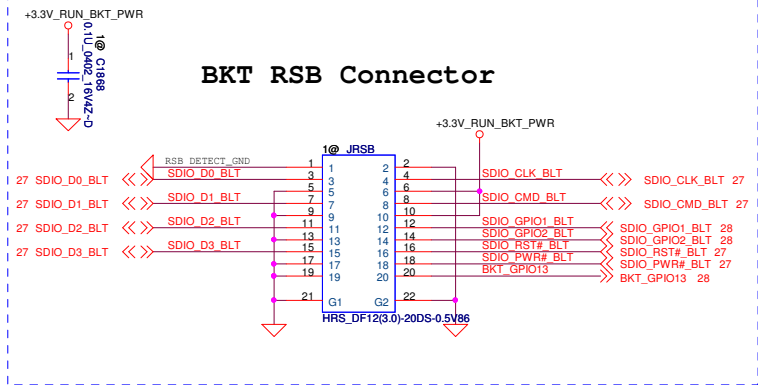
Close to JP1



E-SATA/Jack Connector

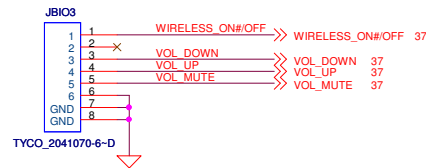


BKT RSB Connector

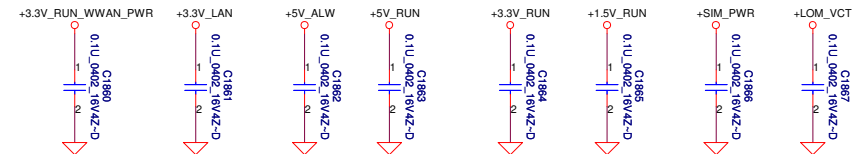
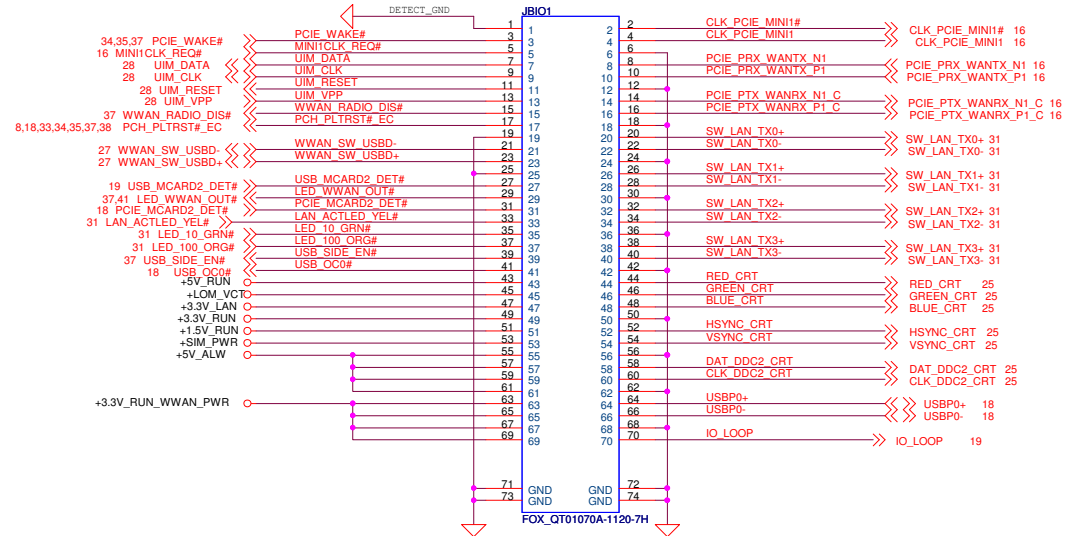


Volume + Sniffer

Change to 6 pins connector




BTB Connector



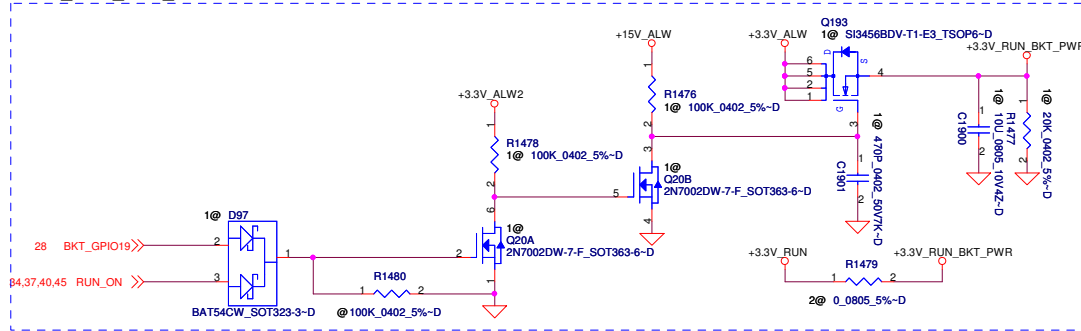
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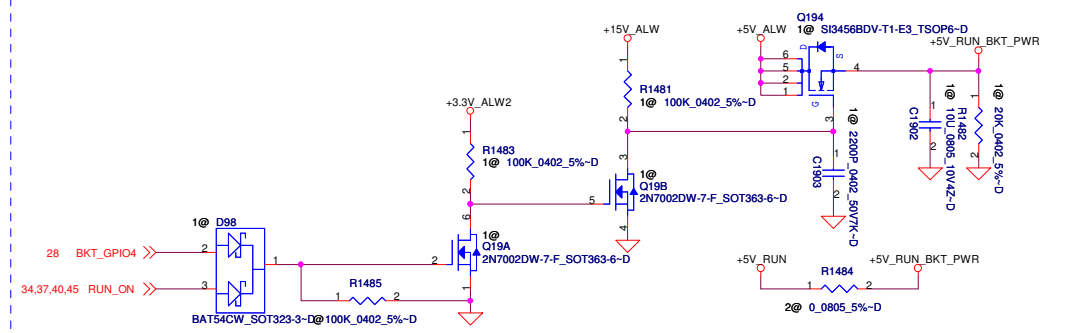
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	LA-5691P	0.1		

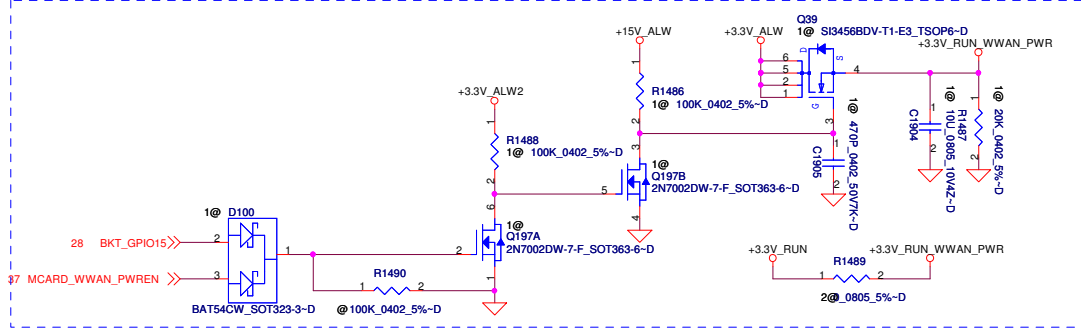
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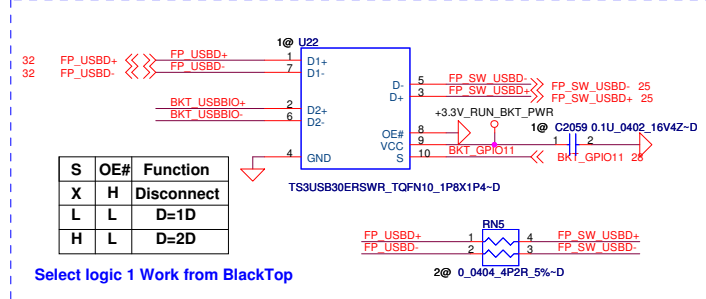
+5V_RUN_BKT_PWR Source, for Touch Pad and Audio Amplifier



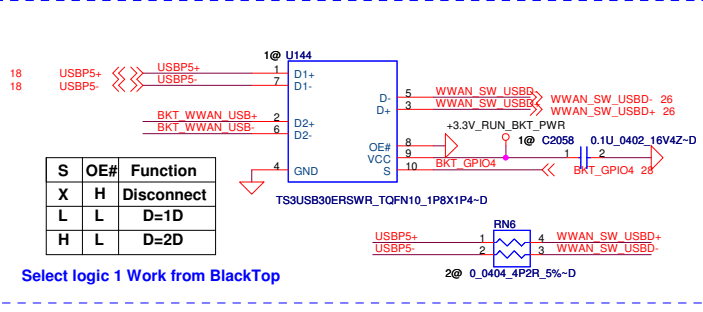
+3.3V_RUN_WWAN_PWR Source, for WWAN



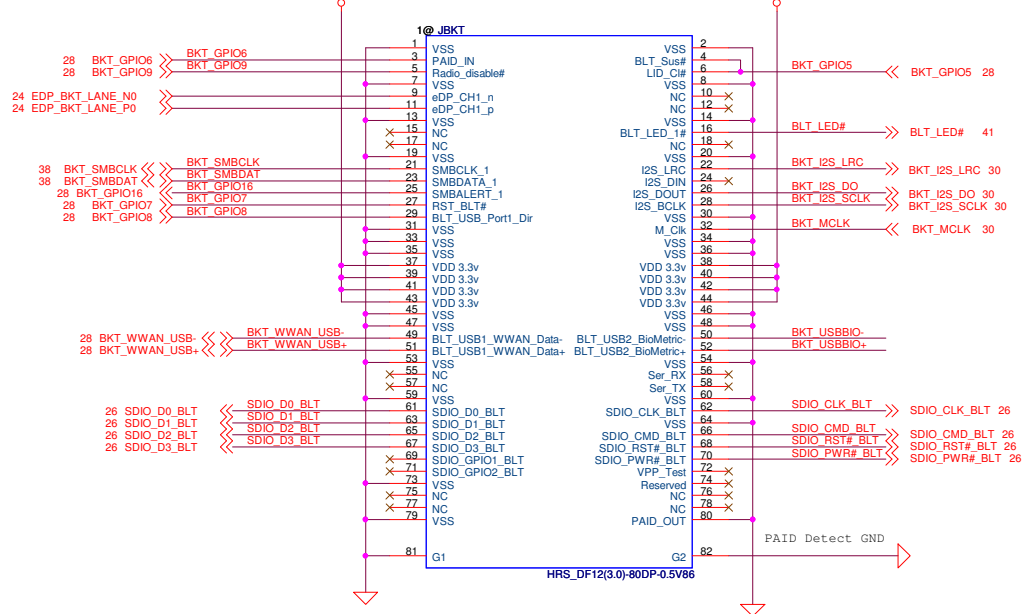
For Biometric USB signals isolation



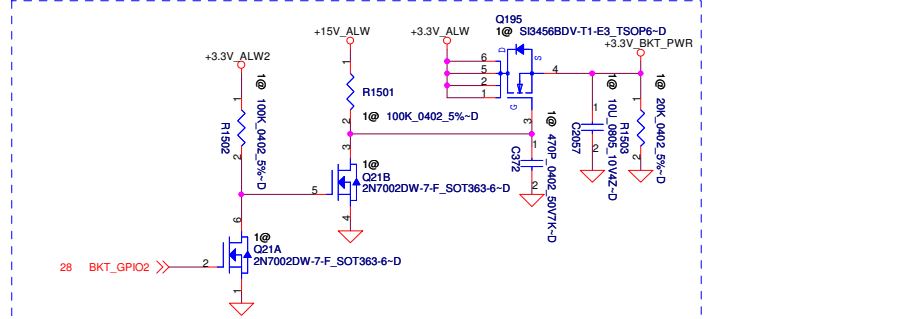
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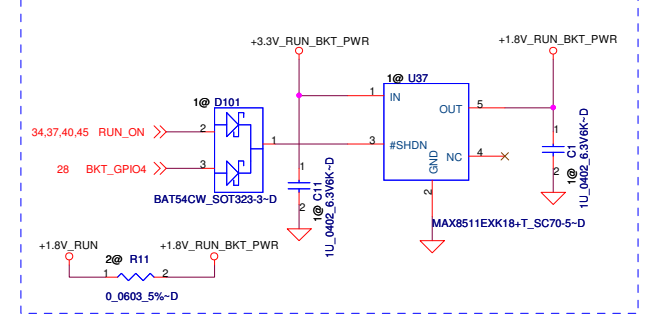
+3.3V_BKT_PWR



Enable BlackTop POWER



For Audio I2S



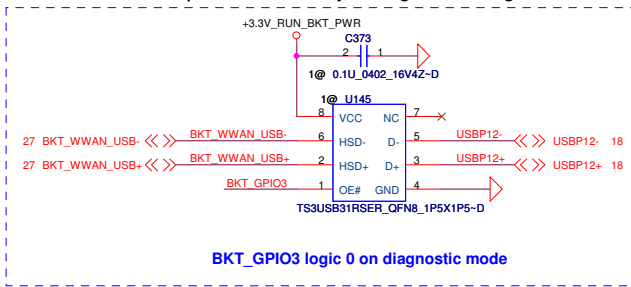
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Compal Electronics, Inc.
BlackTop POWER and CONN
 Document Number: LA-5691P
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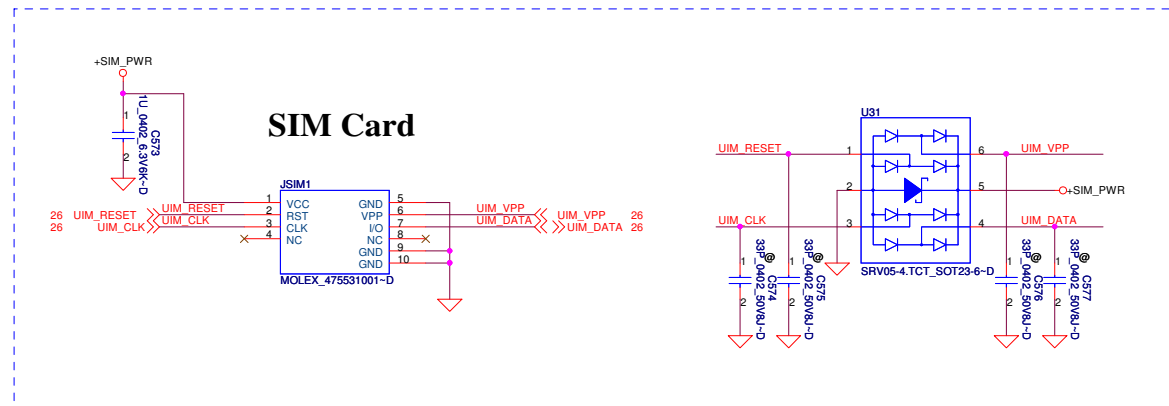
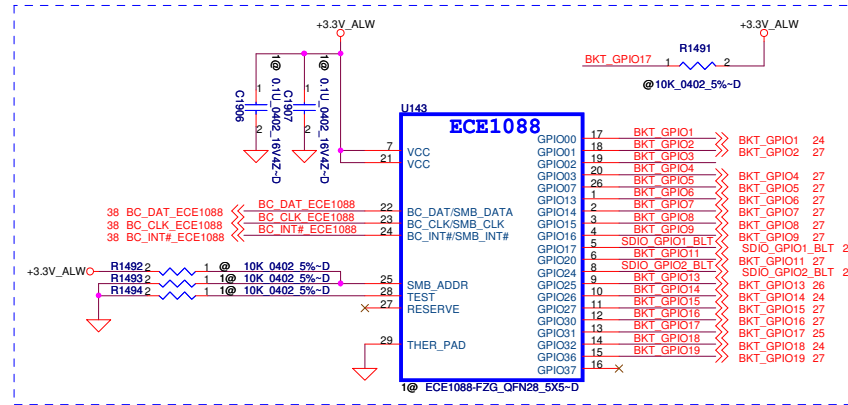
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Add BlackTop to PCH interface by USB signal when diagnostic mode



- BKT_GPIO1 → For eDP signals switch
- BKT_GPIO2 → For BKT power switch
- BKT_GPIO3 → For TP power switch & USB signal switch
- BKT_GPIO4 → For AMP/TP power source & USB signal switch
- BKT_GPIO5 → For LID_Closed
- BKT_GPIO6 → For PAD_Out
- BKT_GPIO7 → For BKT Reset
- BKT_GPIO8 → For USB_SEL_BLK
- BKT_GPIO9 → For Radio_OFF
- BKT_GPIO11 → Biometric mux switch
- BKT_GPIO12 → For WLAN antenna mux control
- BKT_GPIO13 → RSB_DET#
- BKT_GPIO14 → For Inverter Power
- BKT_GPIO15 → For WWAN Power
- BKT_GPIO16 → For SMBALERT
- BKT_GPIO17 → For Biometric reset signal
- BKT_GPIO18 → For LVDS Power switch
- BKT_GPIO19 → For TP Power

GPIO Expander for BlackTop



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Title: Braidwood/ SATA repeater & PCIE SATA SW

Size: Document Number

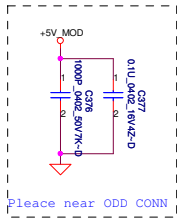
LA-5691P

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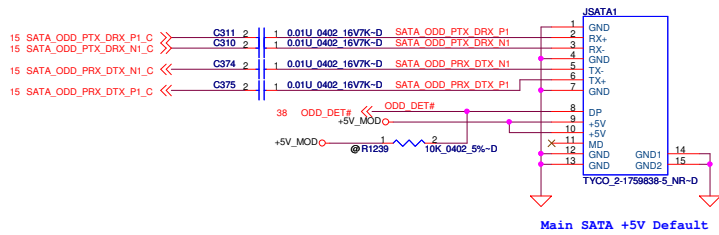
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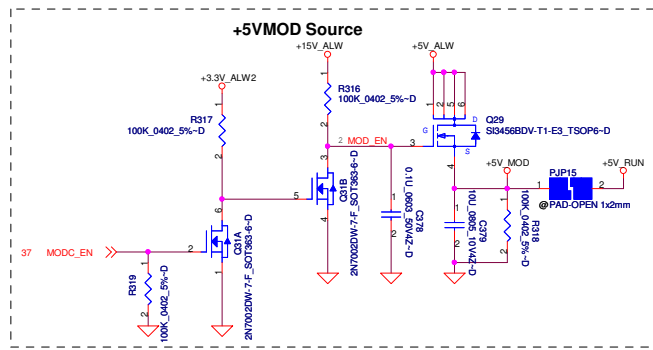


Please near ODD CONN

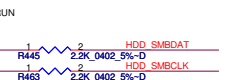
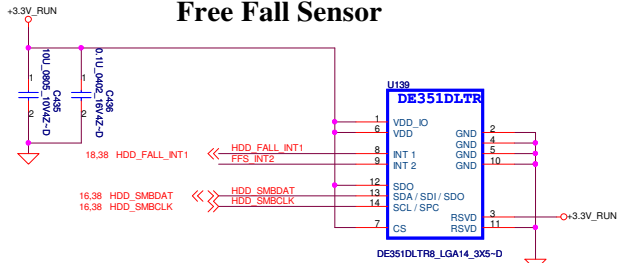
For ODD



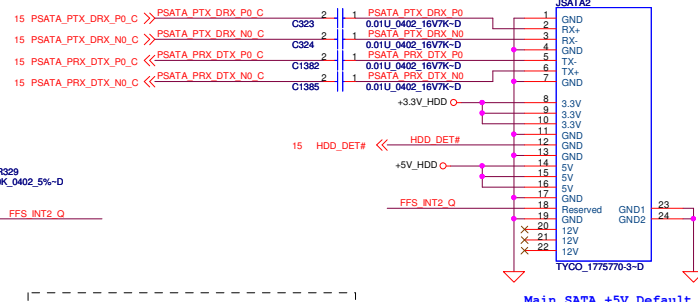
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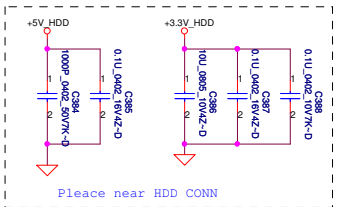
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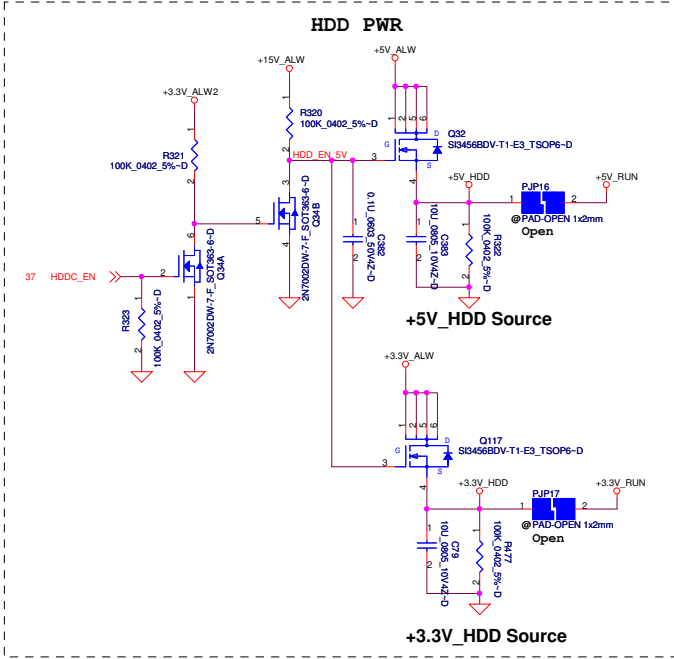
For HDD



Main SATA +5V Default

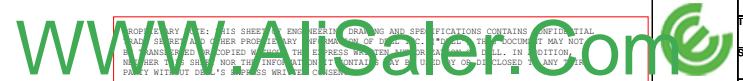


Please near HDD CONN



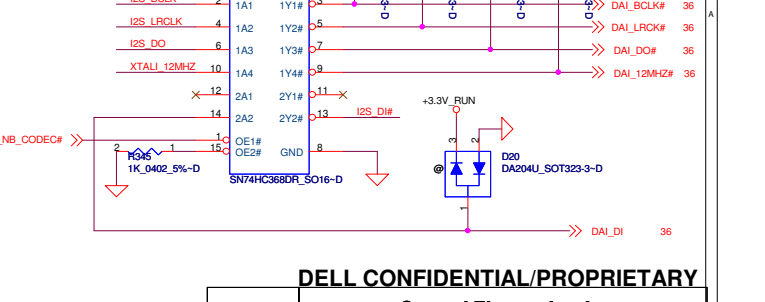
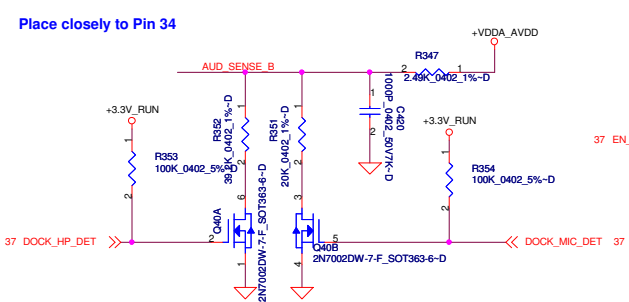
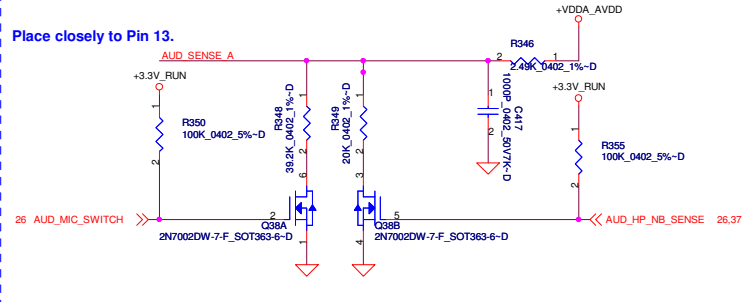
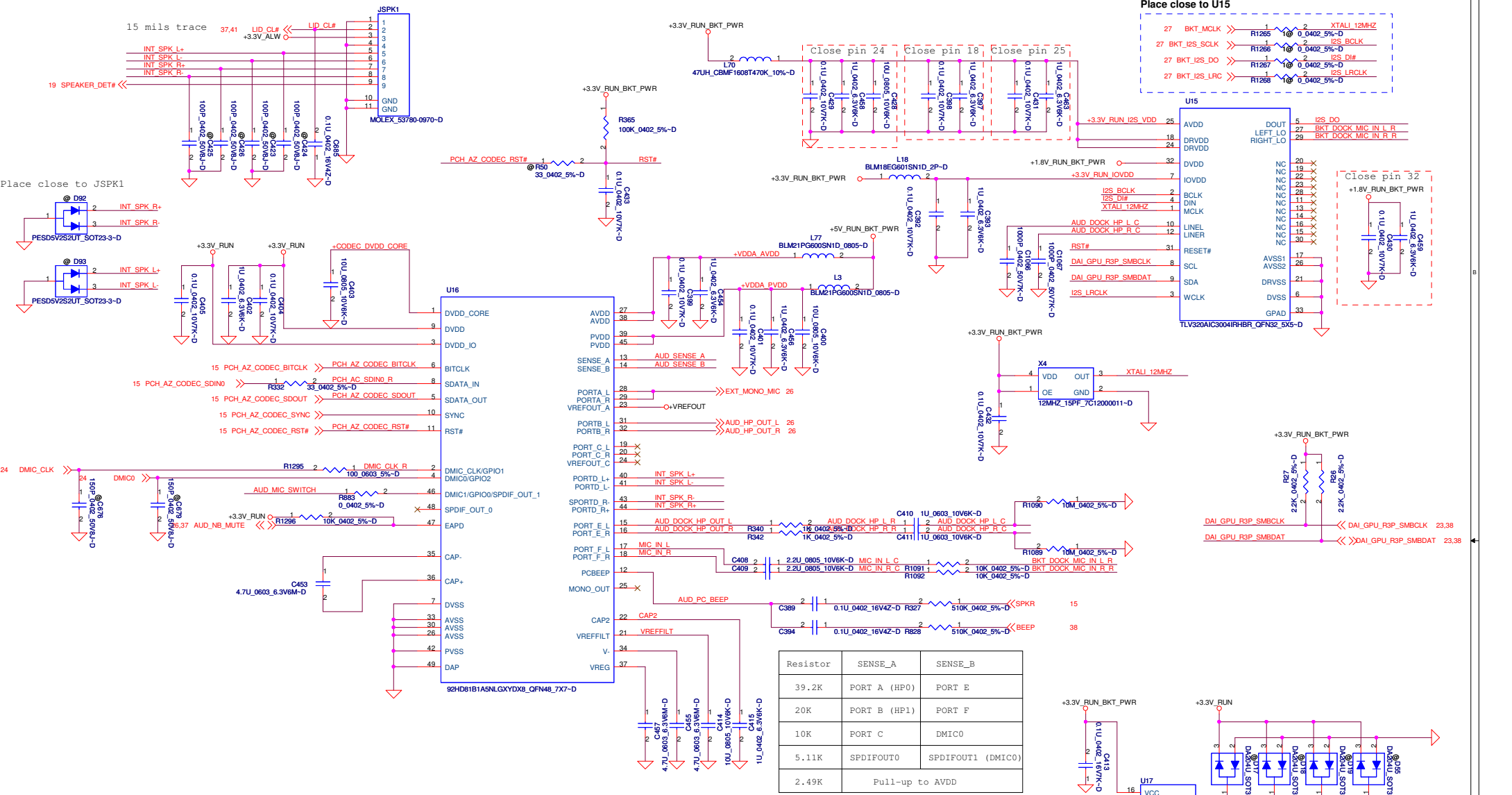
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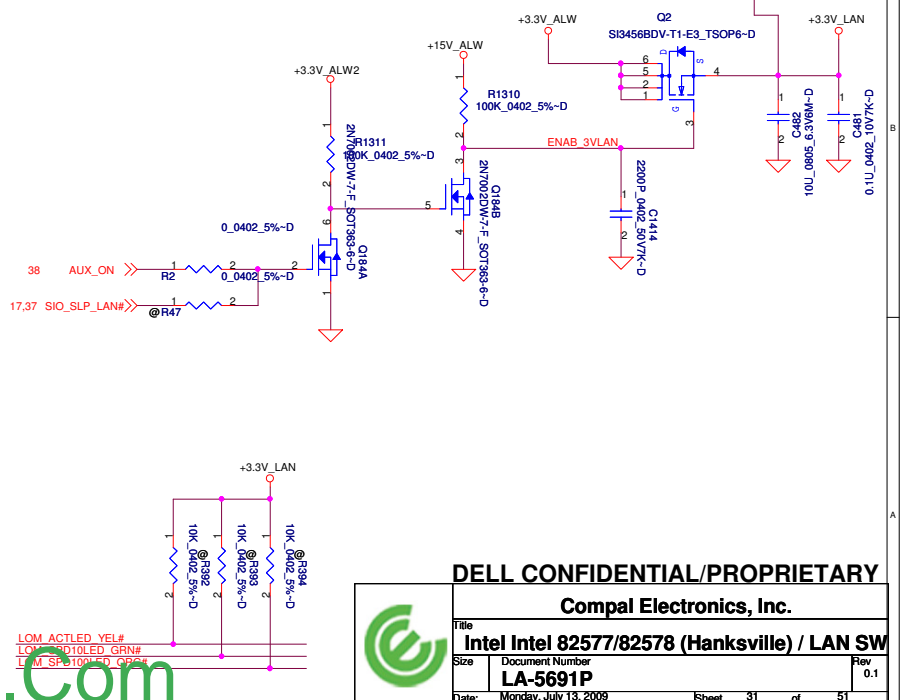
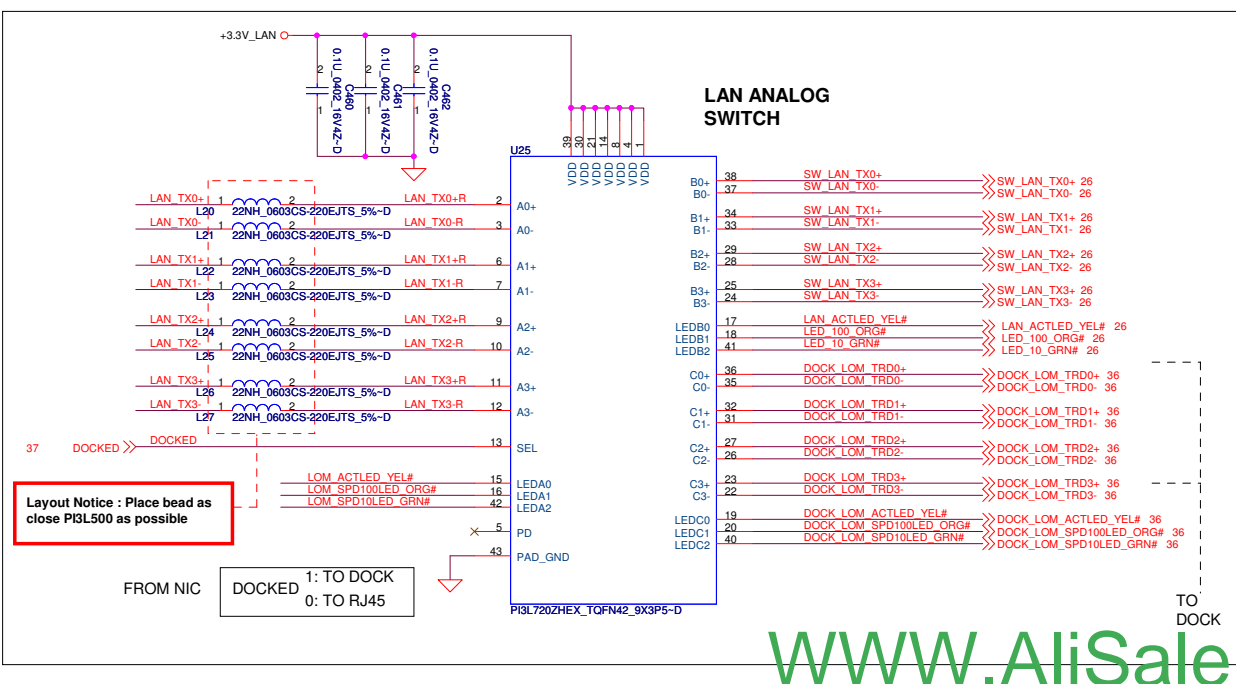
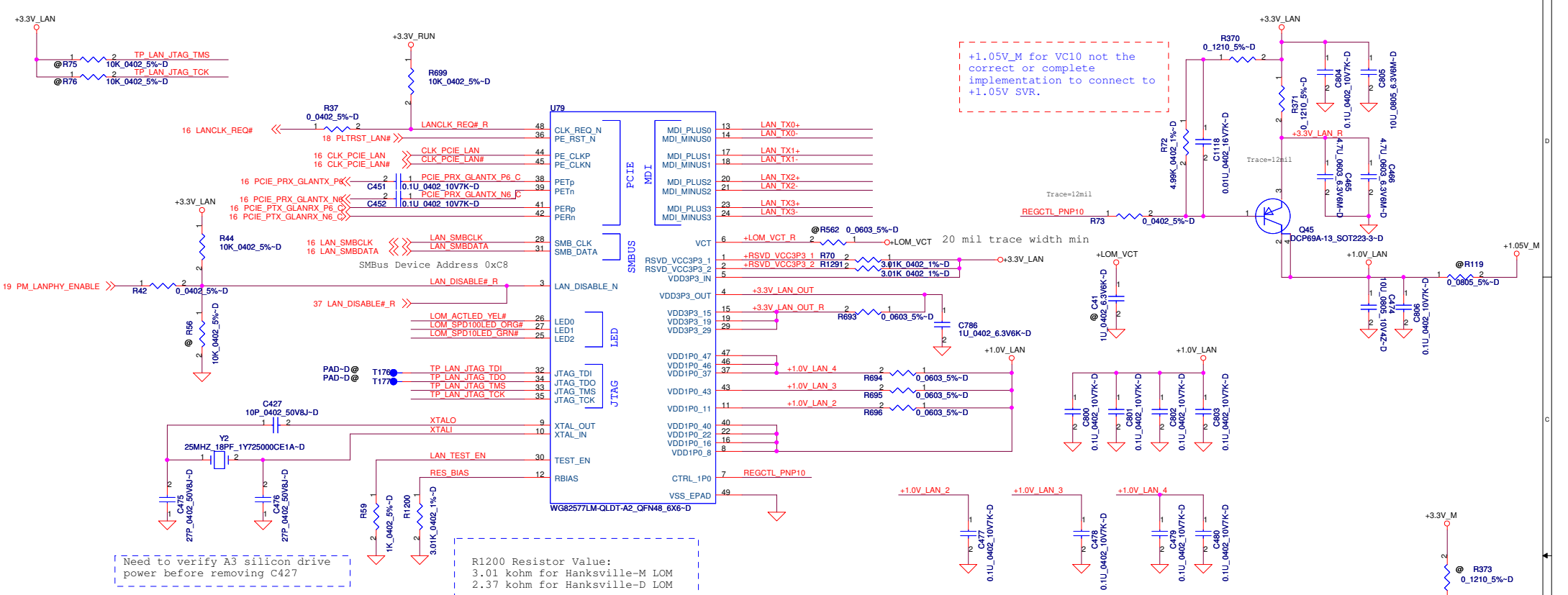
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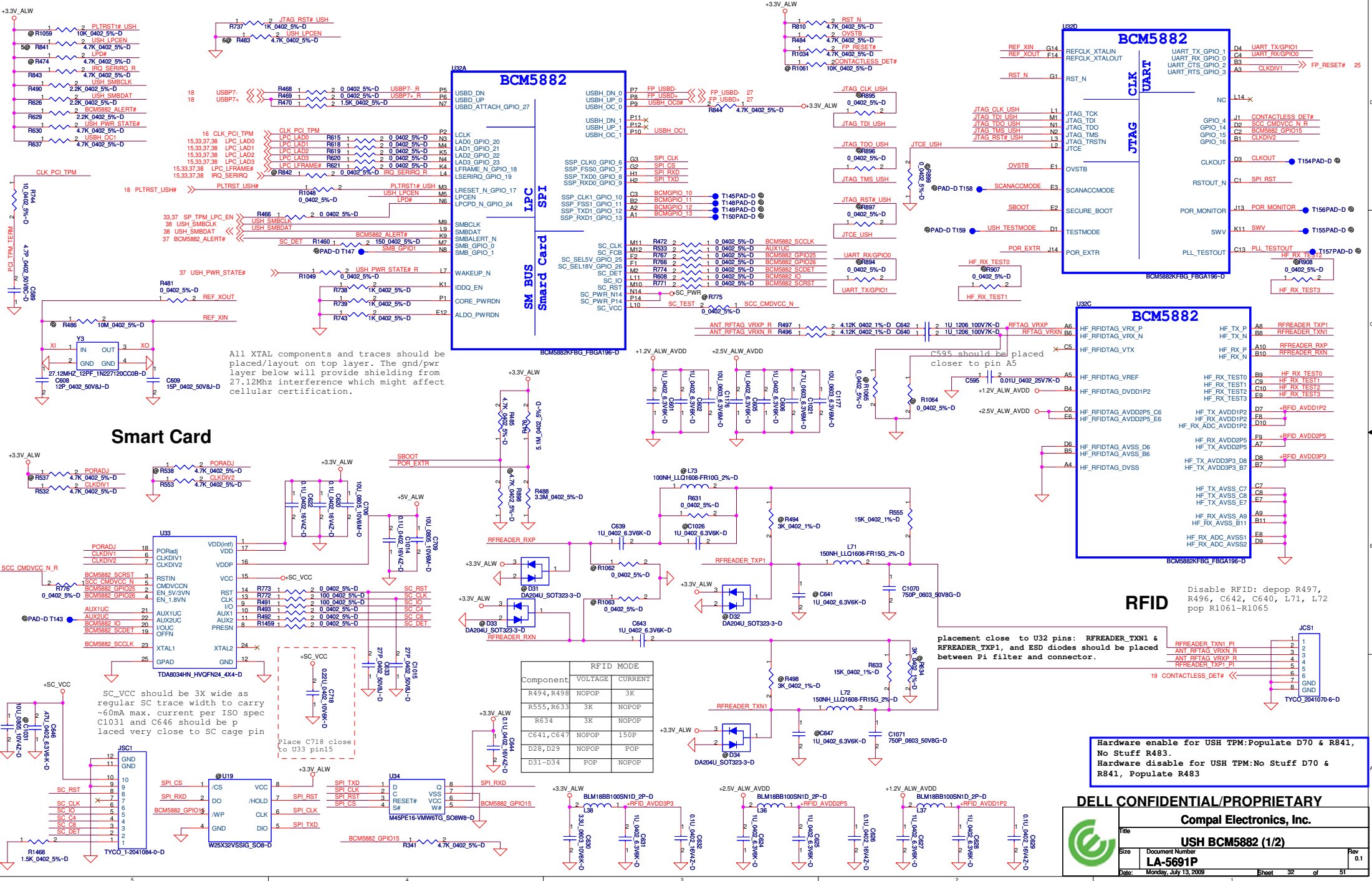


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USH BCM5882 (1/2)

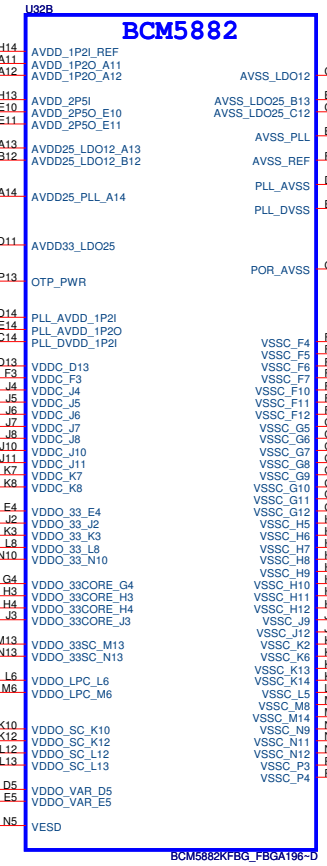
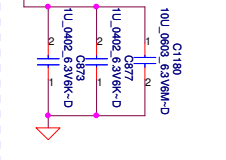
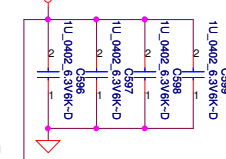
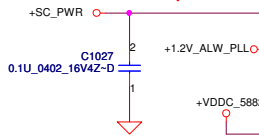
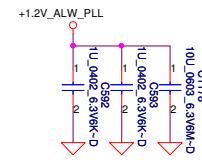
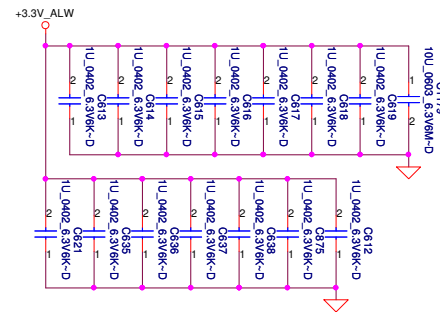
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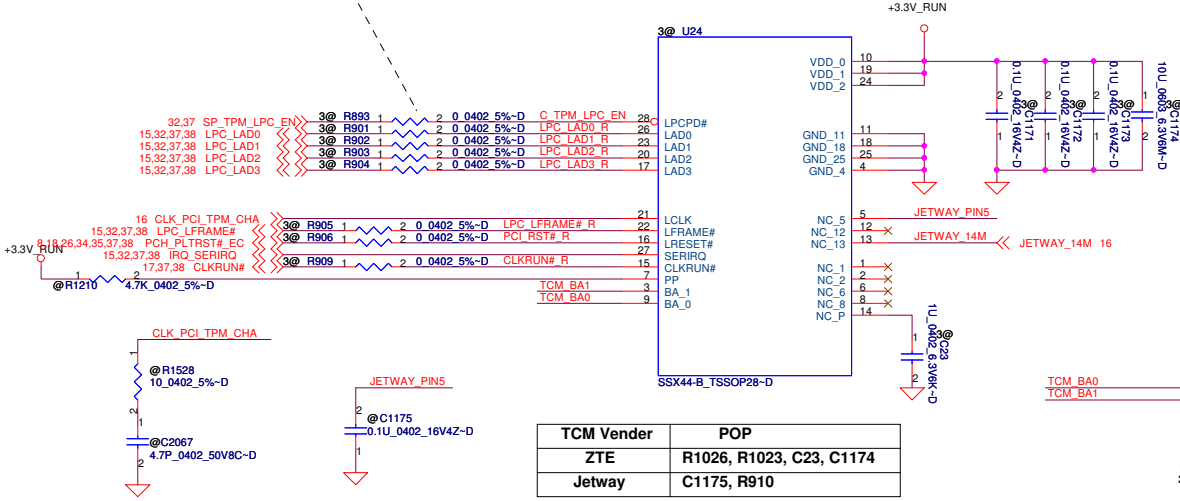
Sheet 32 of 51

USH BCM5882 and China TPM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 3@	POP	@	@
SIO 5028 ->SP_TPM_LPC_EN	PU R841	@	POP	@
	PD R483	POP	@	@
	PU R788	@	@	@
PCH GPIO39 ->TPM_ID1	PU R787	@	@	POP
	PD R339	POP	POP	@
PCH GPIO38 ->TPM_ID0	PU R273	POP	POP	@
	PD R922	@	@	POP



LOW:Power Down Mode
High:Working Mode

China TPM



TCM Vender	POP
ZTE	R1026, R1023, C23, C1174
Jetway	C1175, R910

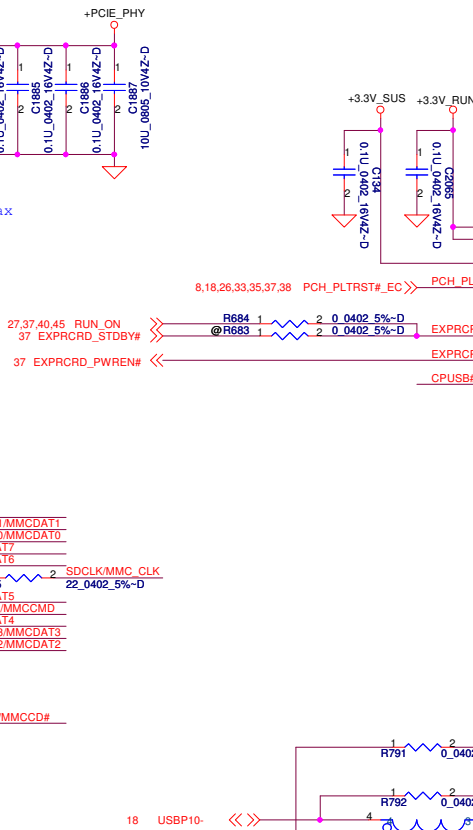
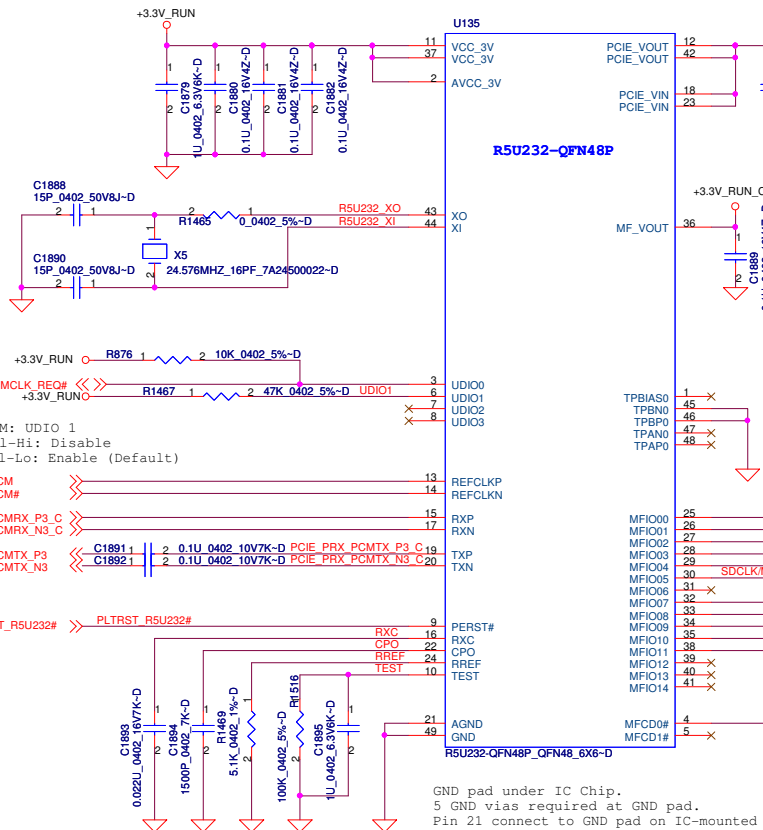
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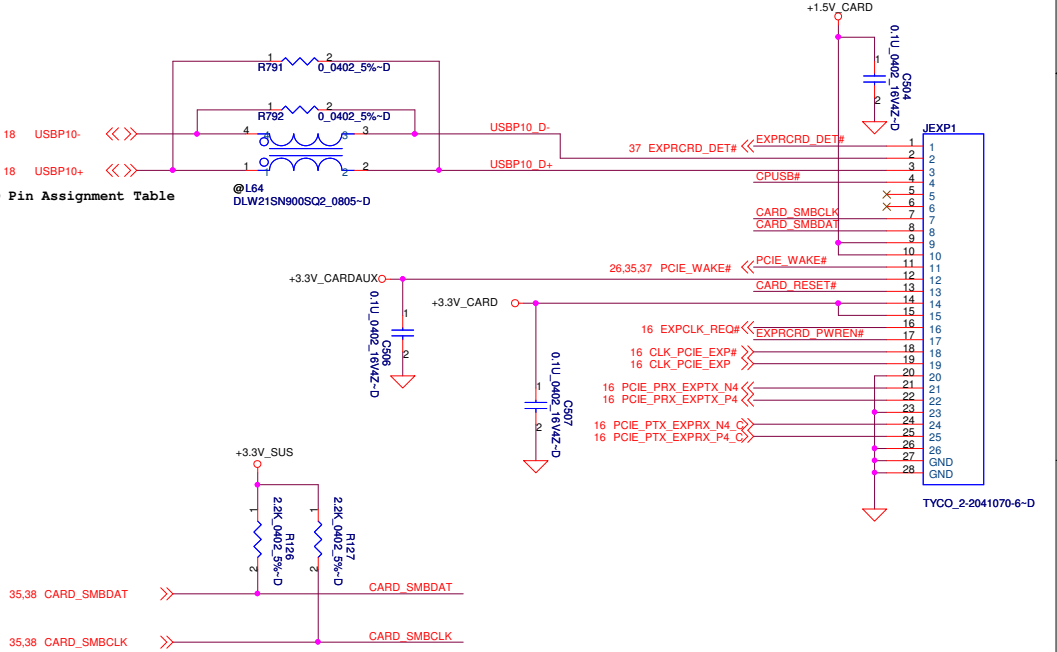
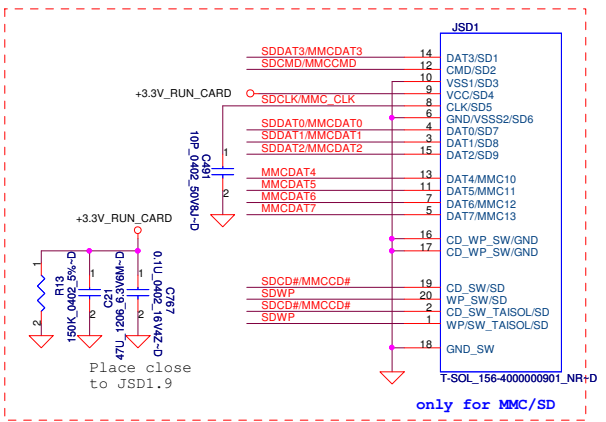


Express Card

+1.5V_CARD: Max. 650mA, Average 500mA
+3.3V_CARD: Max. 1300mA, Average 1000mA

MFIO Pin Assignment Table

MFIO	SD8	XD	MS8
00	WP	D7	BS
01	D1	D6	-
02	D0	D5	D1
03	D7	D4	-
04	D6	D3	D5
05	CLK	D2	D0
06	-	D1	-
07	D5	D0	D4
08	CMD	WP#	D2
09	D4	WE#	D6
10	D3	ALE	D3
11	D2	CLE	-
12	-	CE#	-
13	-	RE#	D7
14	-	R/B#	CLK



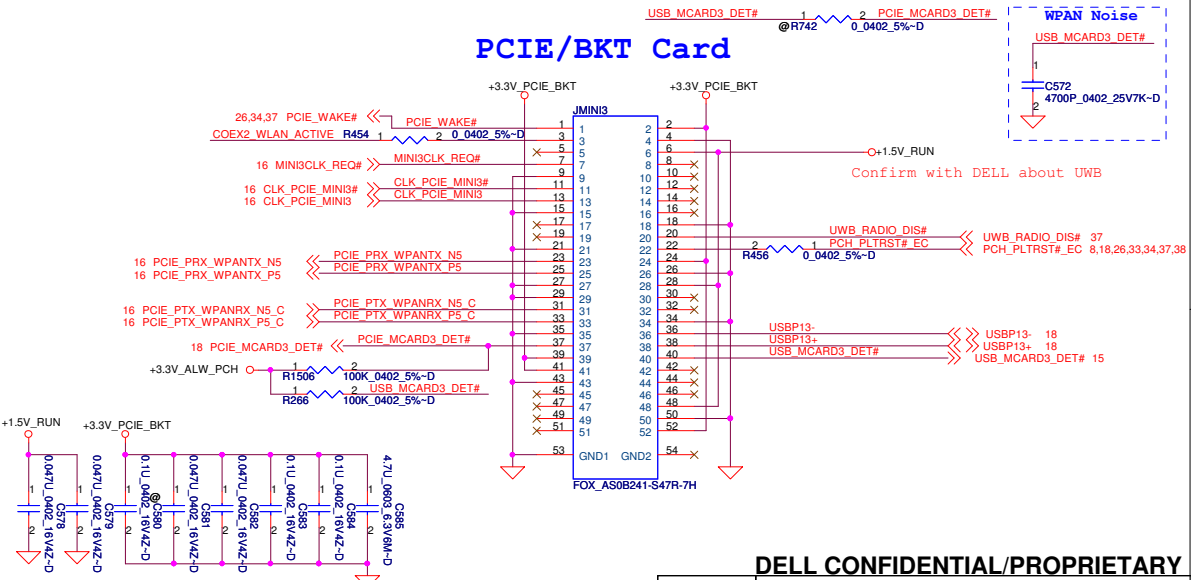
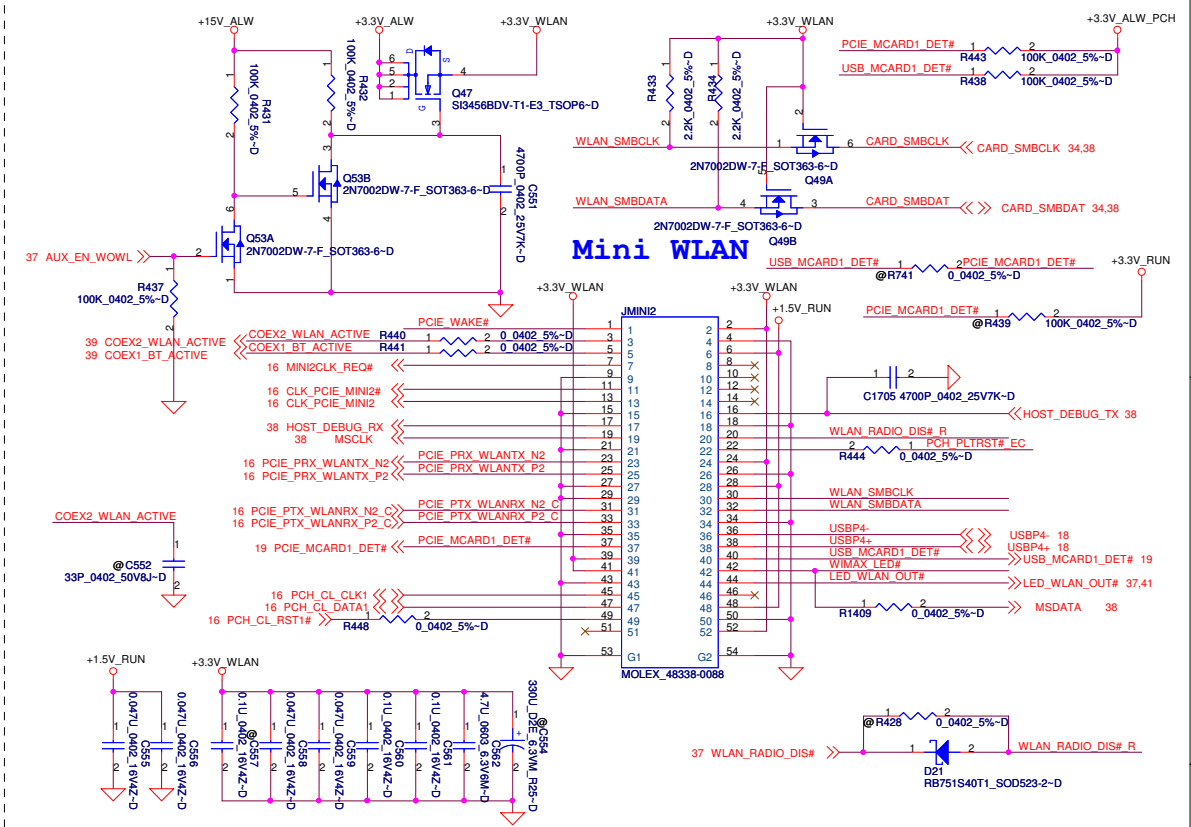
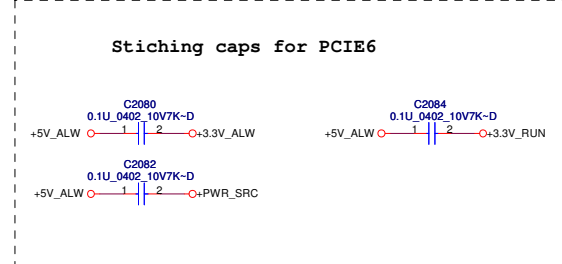
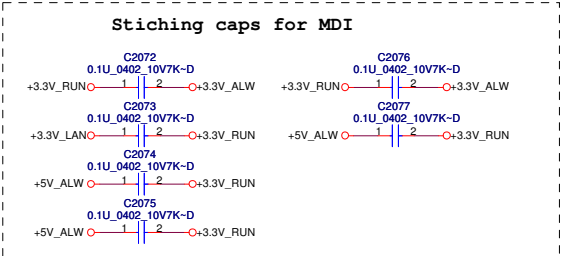
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R5U232			
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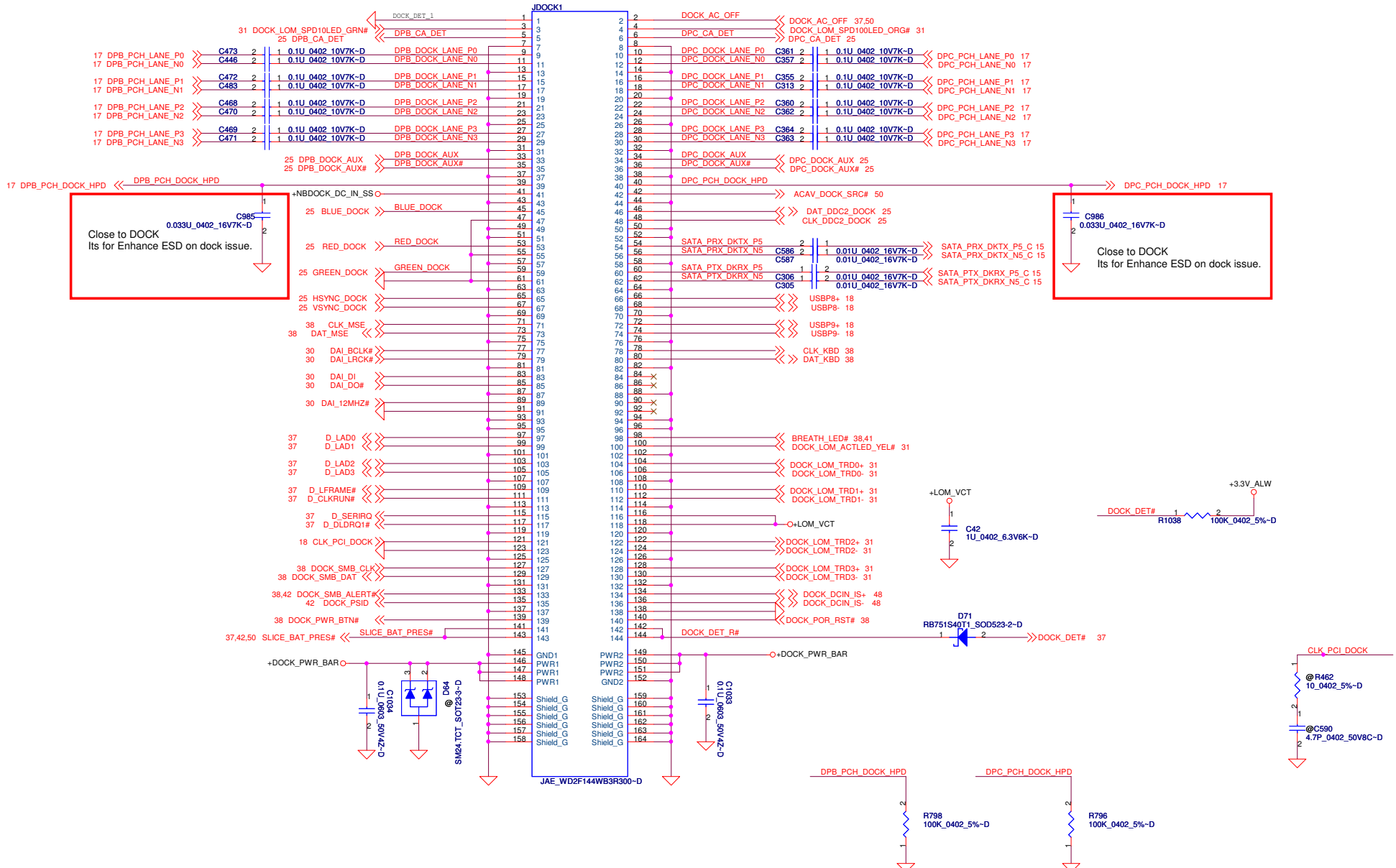
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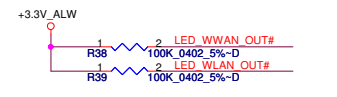
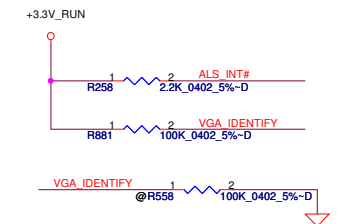
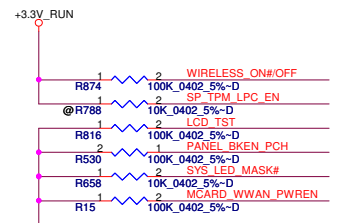
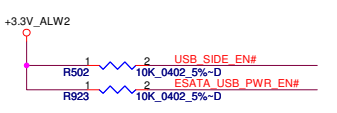
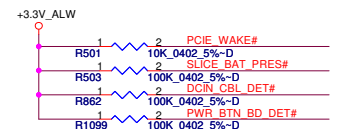


Close to DOCK
Its for Enhance ESD on dock issue.

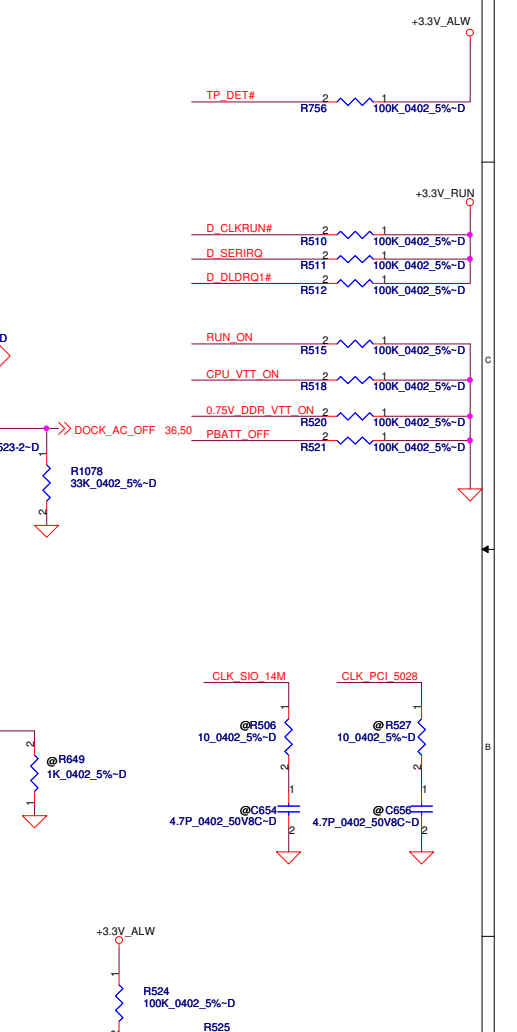
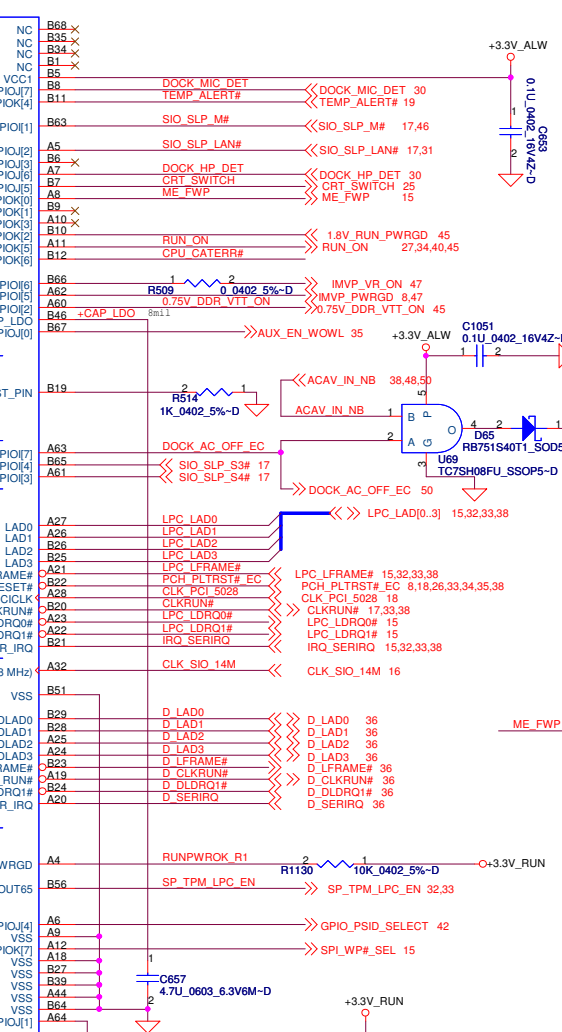
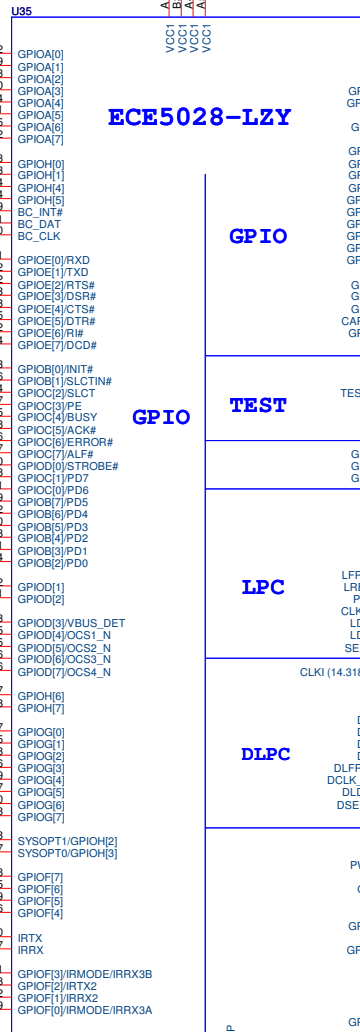
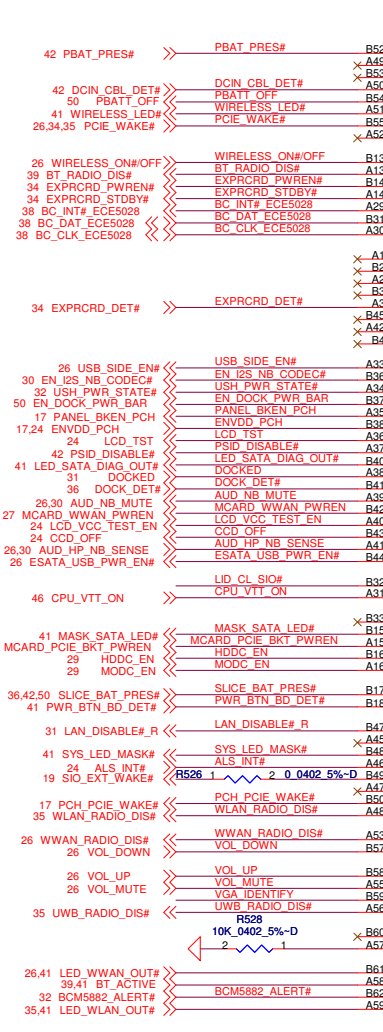
Close to DOCK
Its for Enhance ESD on dock issue.

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DOCKING CONN			
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	VGA_IDENTIFY
Discrete	0
UMA	1



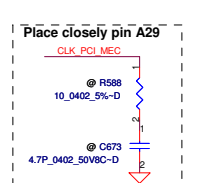
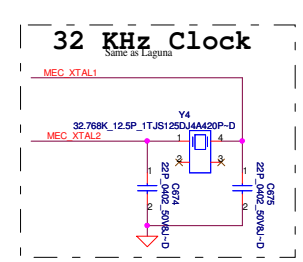
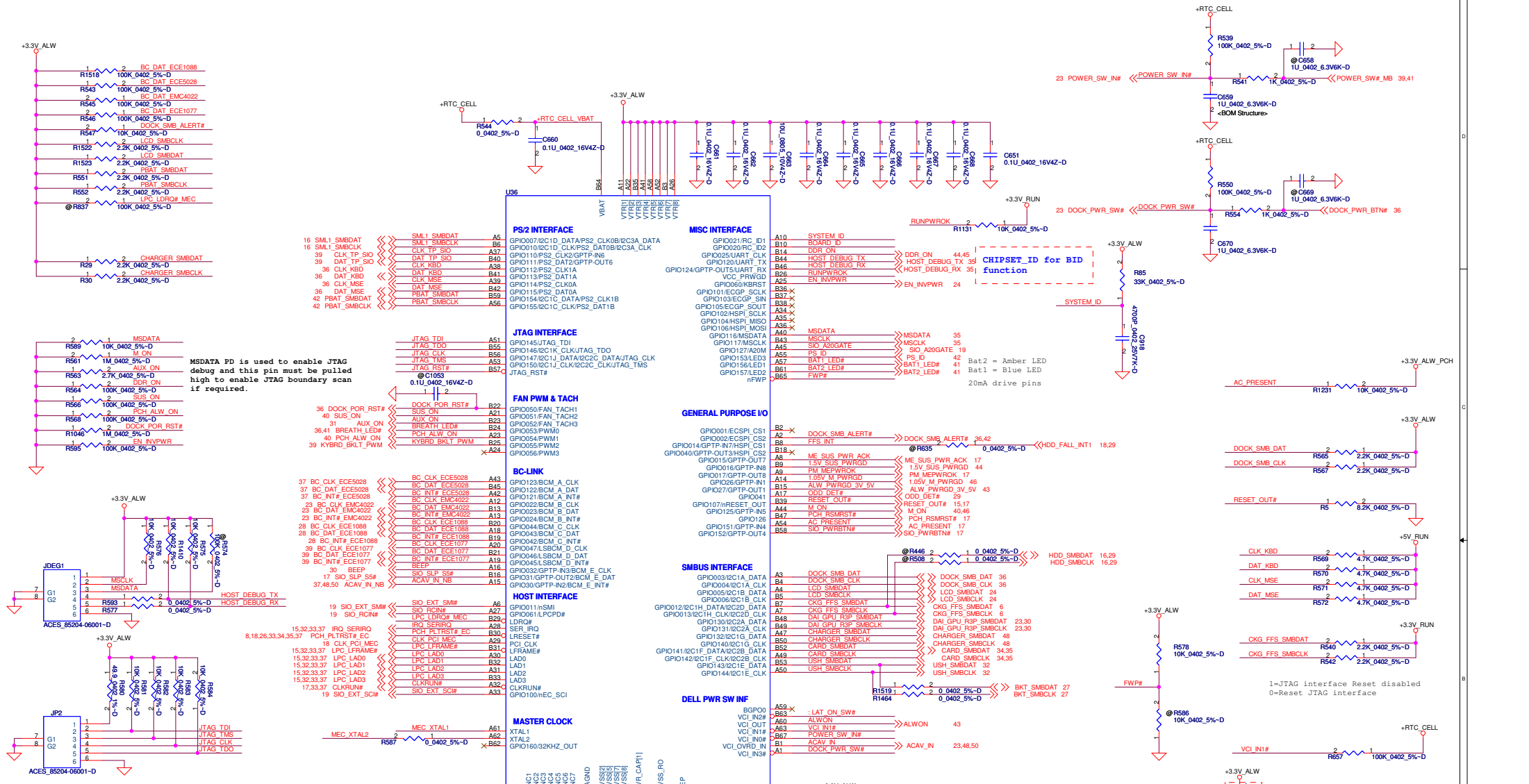
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R98	C919	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	

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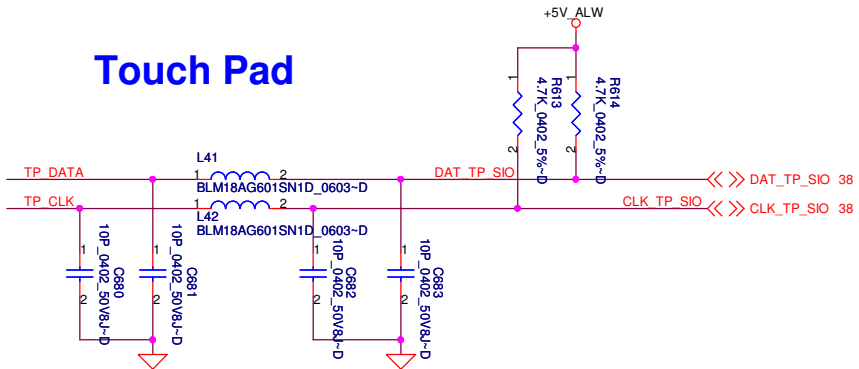


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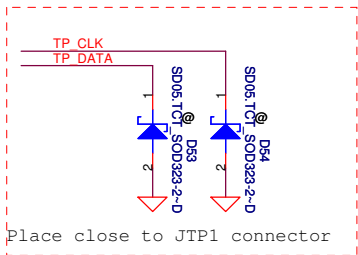
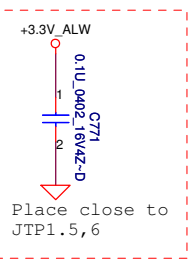
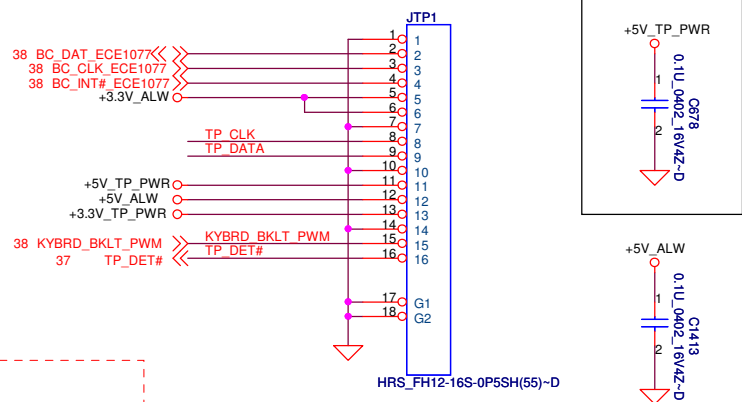
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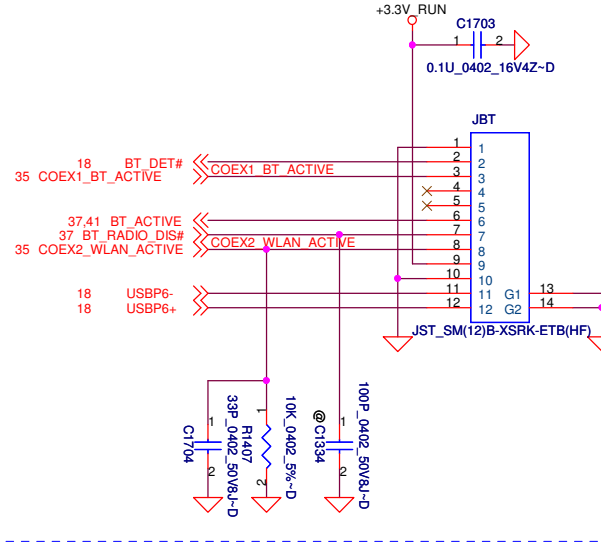
Touch Pad



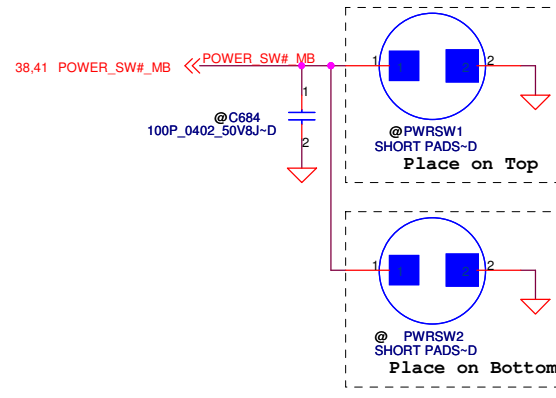
New Keyboard connector assignment



BlueTooth



Power Switch for debug



@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

@SM CARD BODY

Part Number	Description
SP070007V0L	\$ SOCKET TYCO 1770551-1 10P H5.9 SMART

@PCMCIA BODY

Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

@MDC wire set cable

Part Number	Description
DC02000CS0L	H-CONN SET 2GX MB-MDC

@T/P wire set cable

Part Number	Description
DC02000840L	H-CONN SET ZJX MB-B/T-TP-FP

@LVDS cable

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+(-1ch)

@LVDS cable

Part Number	Description
DC02000870L	H-CONN SET ZJX MB-LCD 14 WXGA+(-2ch)

@RTC BATT

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

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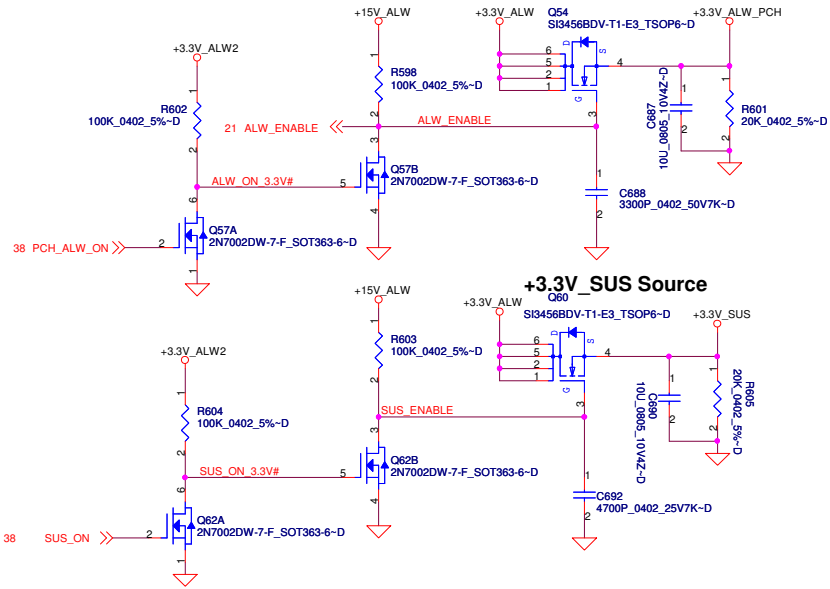
Title: **Touch PAD/Int KB/LID**

Size: Document Number **LA-5691P** Rev **0.1**

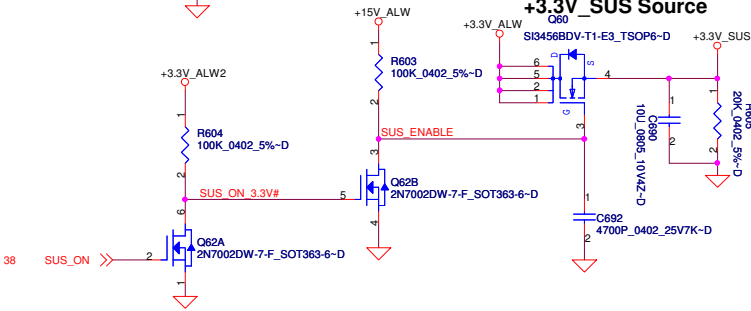
Date: Monday, July 13, 2009 Sheet 39 of 51

DC/DC Interface

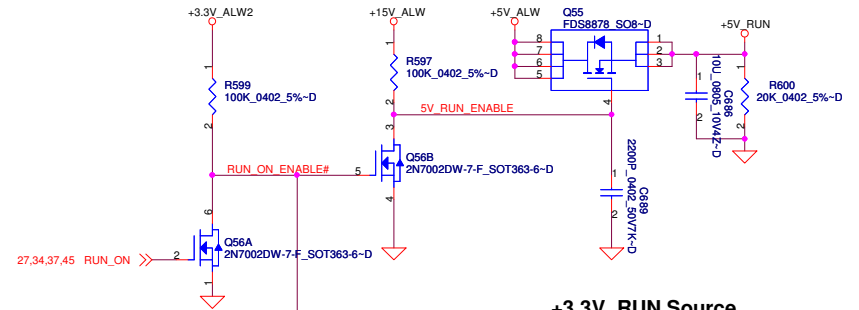
+3.3V_ALW_PCH Source



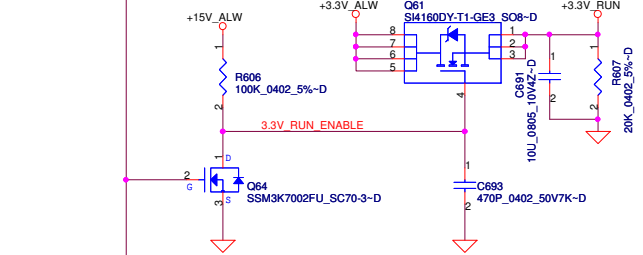
+3.3V_SUS Source



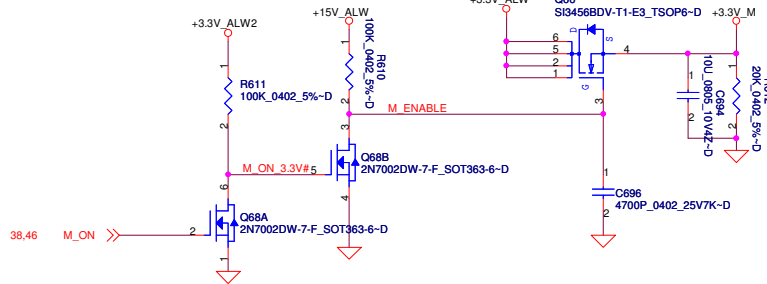
+5VRUN Source



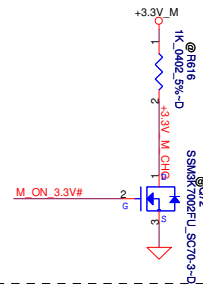
+3.3V_RUN Source



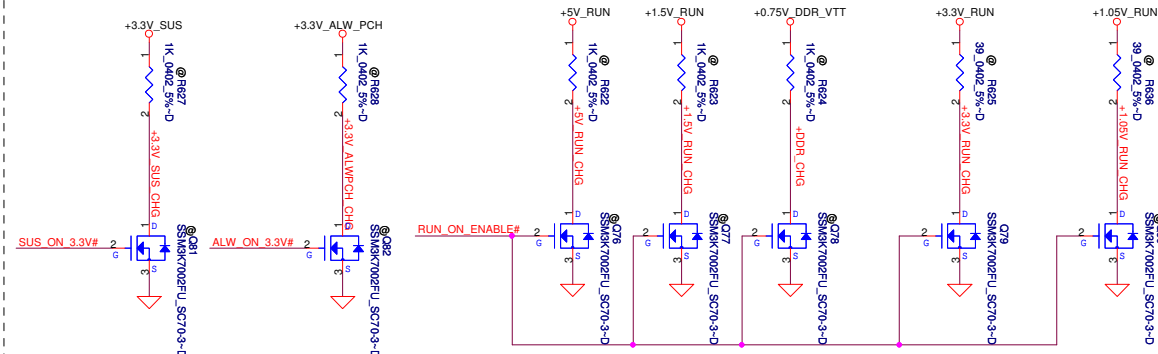
+3.3VM Source



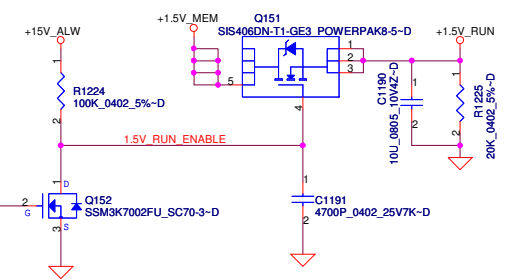
Discharg Circuit



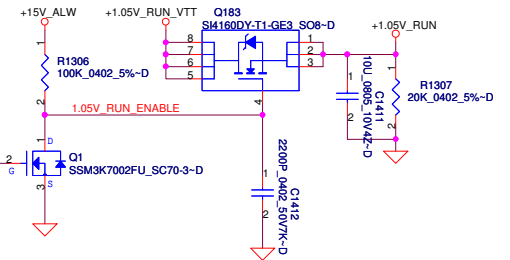
Discharg Circuit



+1.5V_RUN Source



+1.05V_RUN Source



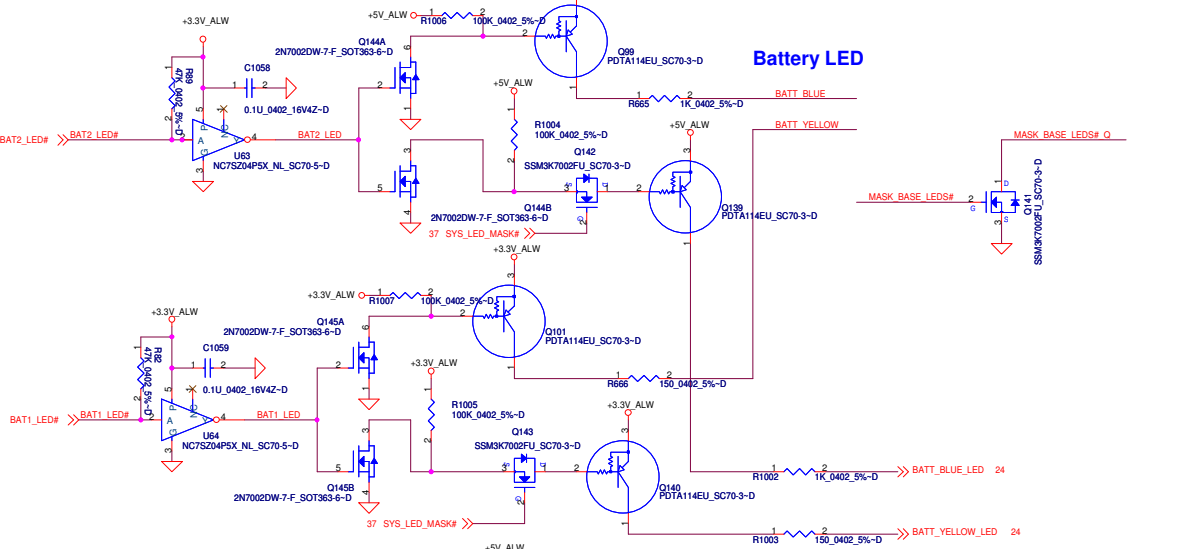
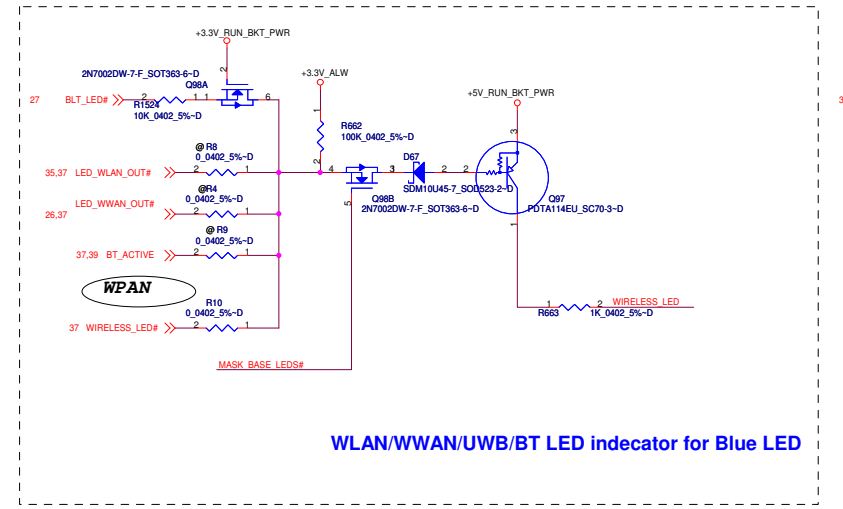
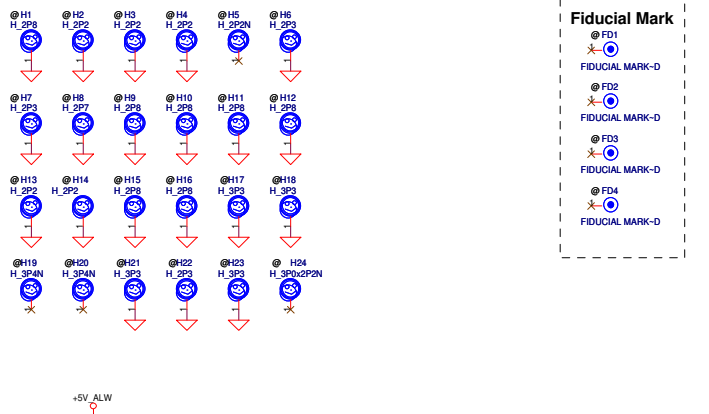
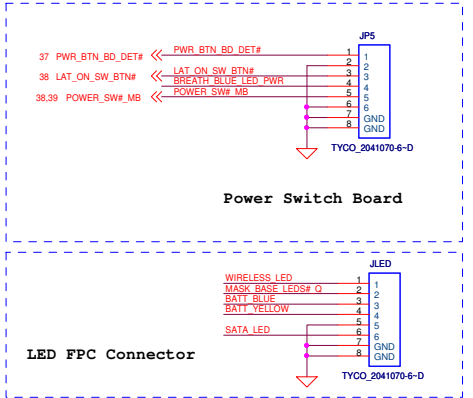
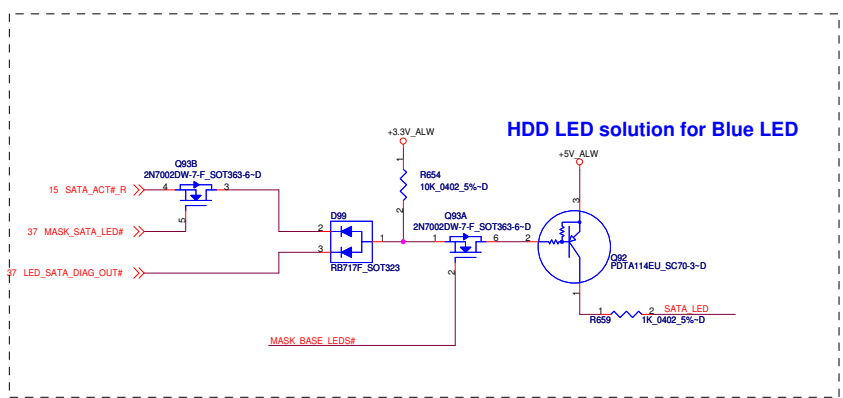
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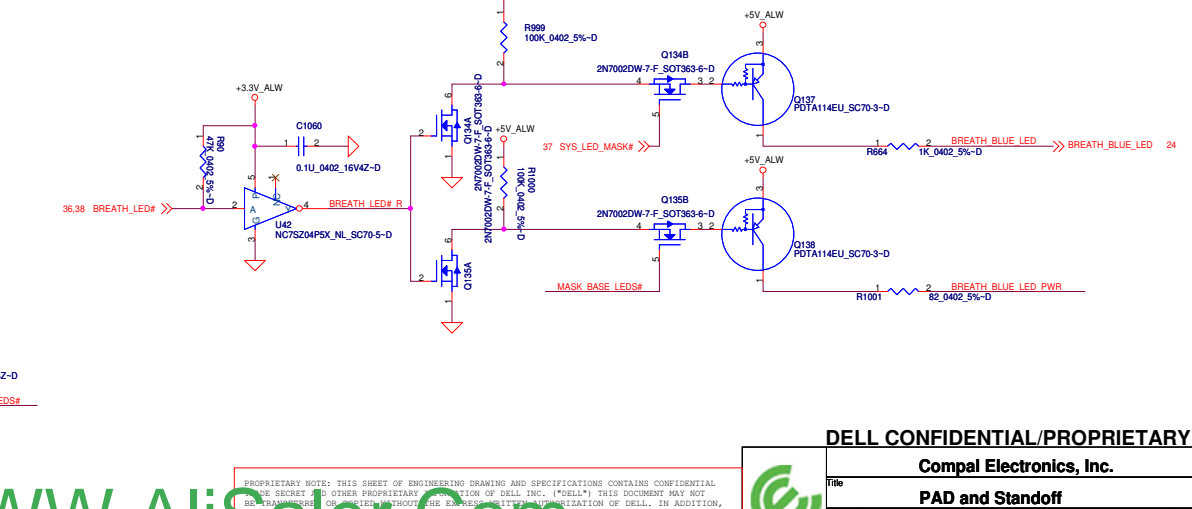
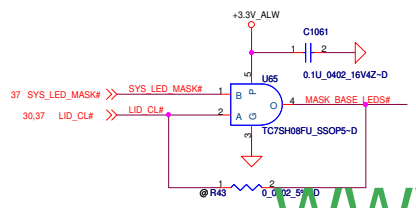
Title		
POWER CONTROL		
Size	Document Number	Rev
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Date:	Monday, July 13, 2009	Sheet 40 of 51

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LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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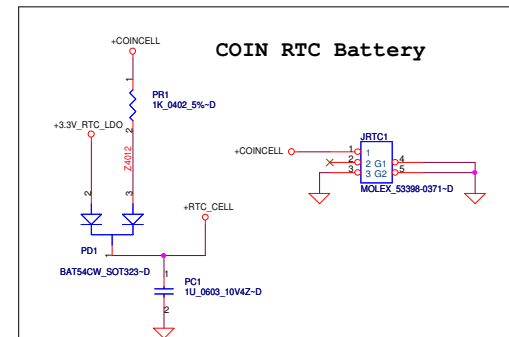
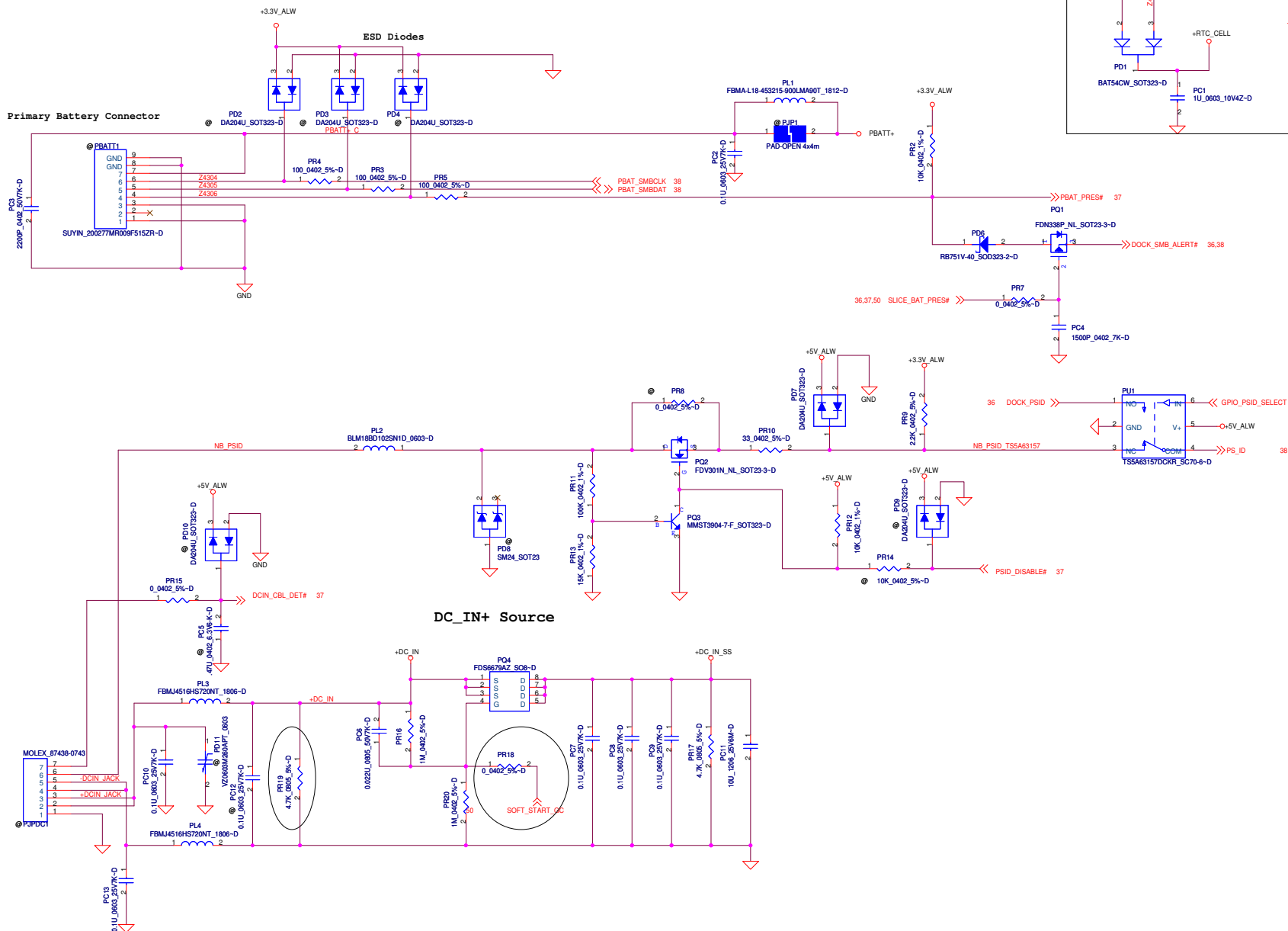
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Size: Document Number LA-5691P

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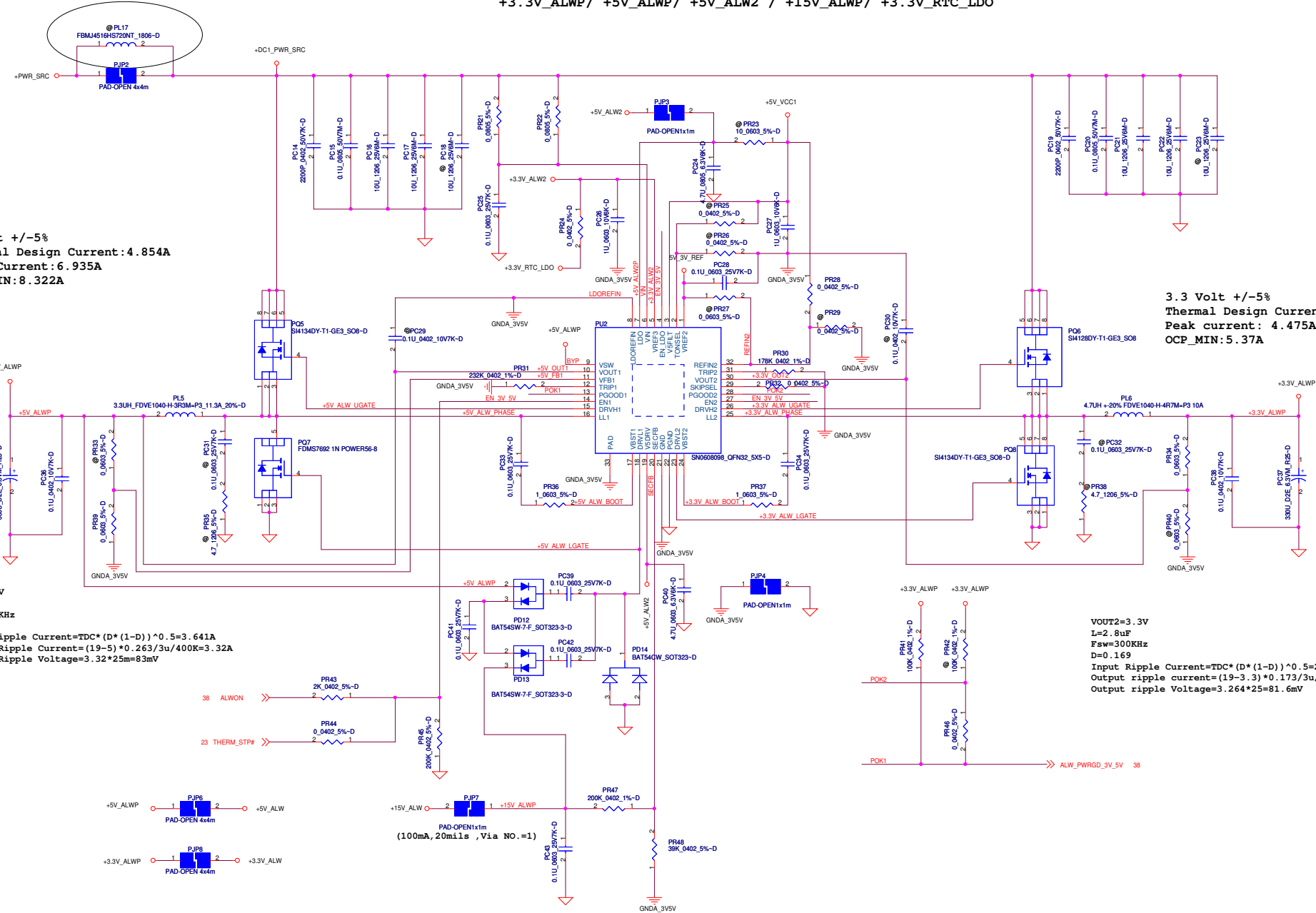
+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP/ +3.3V_RTC_LDO

5 Volt +/-5%
 Thermal Design Current: 4.854A
 Peak Current: 6.935A
 OCP_MIN: 8.322A

3.3 Volt +/-5%
 Thermal Design Current: 3.133A
 Peak current: 4.475A
 OCP_MIN: 5.37A

VOUT2=5V
 L=2.8uF
 Fsw=400KHz
 D=0.256
 Input Ripple Current=TDC*(D*(1-D))^0.5=3.641A
 Output Ripple Current=(19-5)*0.263/3u/400K=3.32A
 Output Ripple Voltage=3.32*25m=83mV

VOUT2=3.3V
 L=2.8uF
 Fsw=300KHz
 D=0.169
 Input Ripple Current=TDC*(D*(1-D))^0.5=2.051A
 Output ripple current=(19-3.3)*0.173/3u/300K=3.264A
 Output ripple Voltage=3.264*25=81.6mV



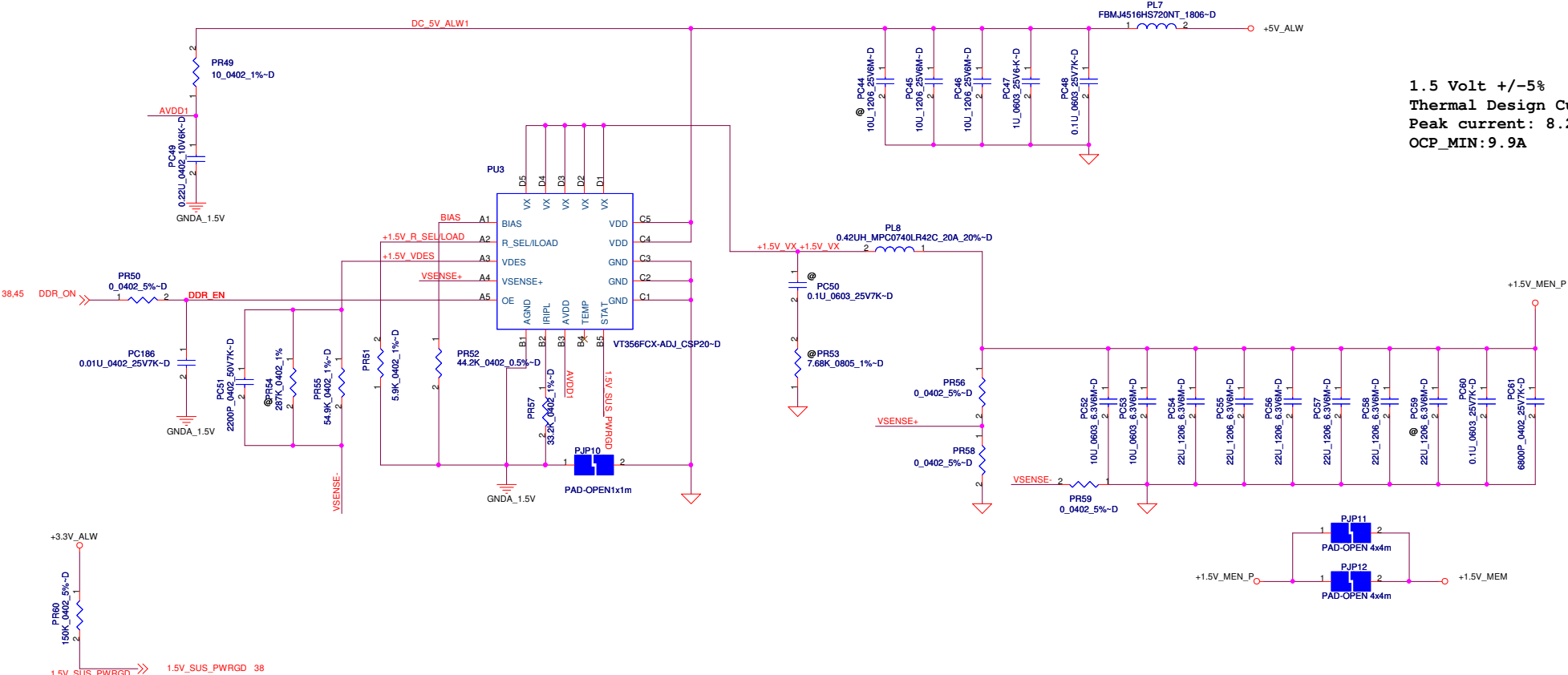
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		Title DC/DC +3V/ +5V	
Size	Document Number	LA-5691P	
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+1.5V_MEN_P (VT356)



1.5 Volt +/-5%
 Thermal Design Current: 5.775A
 Peak current: 8.25A
 OCP_MIN:9.9A

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+1.5V_MEM

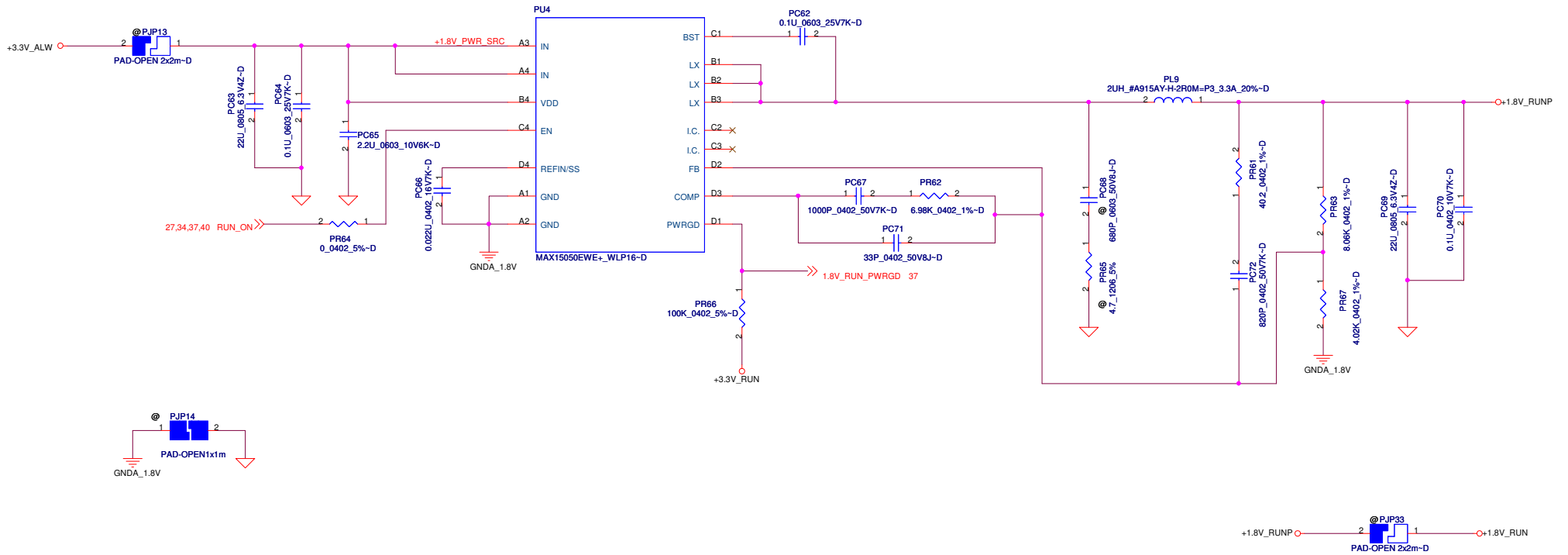
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+1.8V_RUN

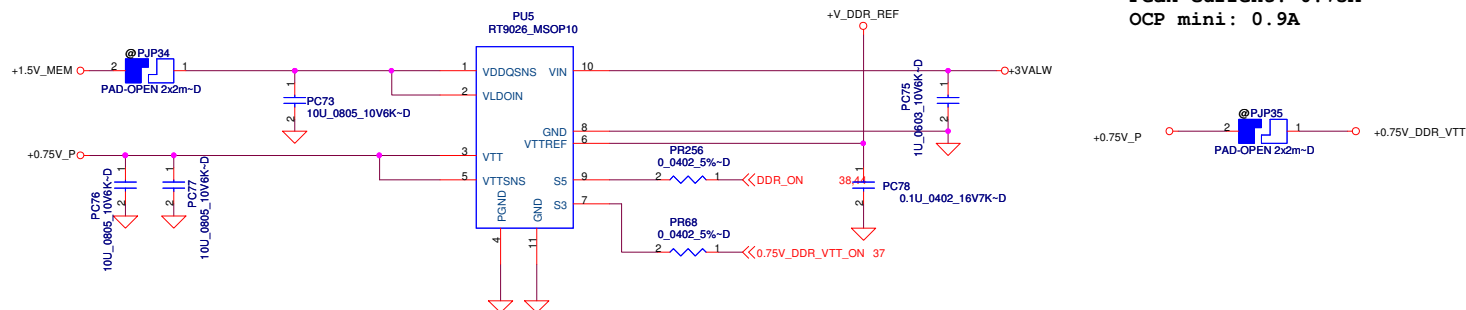
1.8 Volt +/-5%
 Thermal Design Current: 0.894A
 Peak current: 1.277A
 OCP_min:1.532A



+0.75V_DDR_VTT

DDR3 Termination

0.75Volt +/-5%
 Thermal Design Current: 0.525A
 Peak current: 0.75A
 OCP mini: 0.9A



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Title		
+1.8V_RUN/+0.75V DDR VT		
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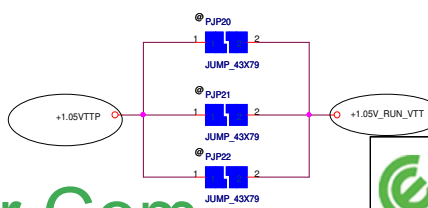
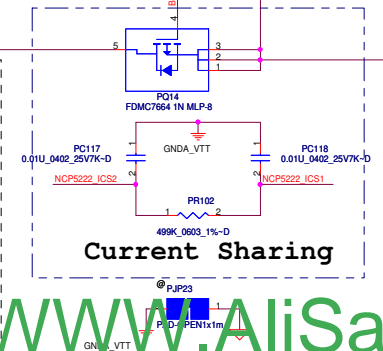
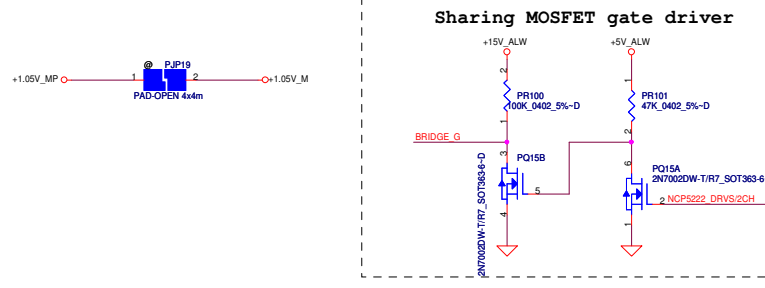
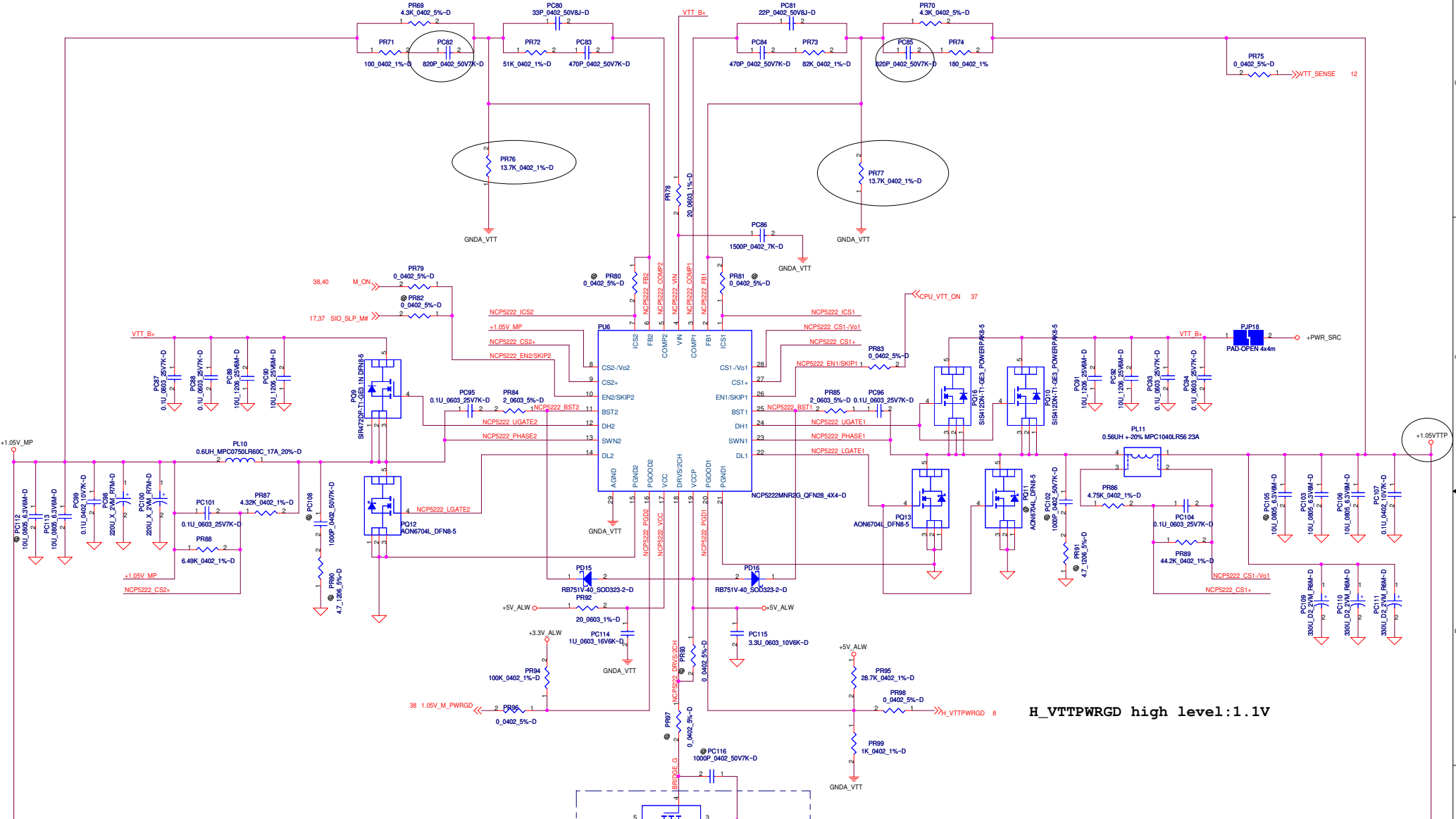
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1.05 Volt +/-5%
Thermal Design Current: 1.51A
Peack current: 2.17A

+1.05V_M/+1.05VTT_RUN

1.05 Volt +/-5%
Thermal Design Current: 15.9A
Peack current: 22.7A



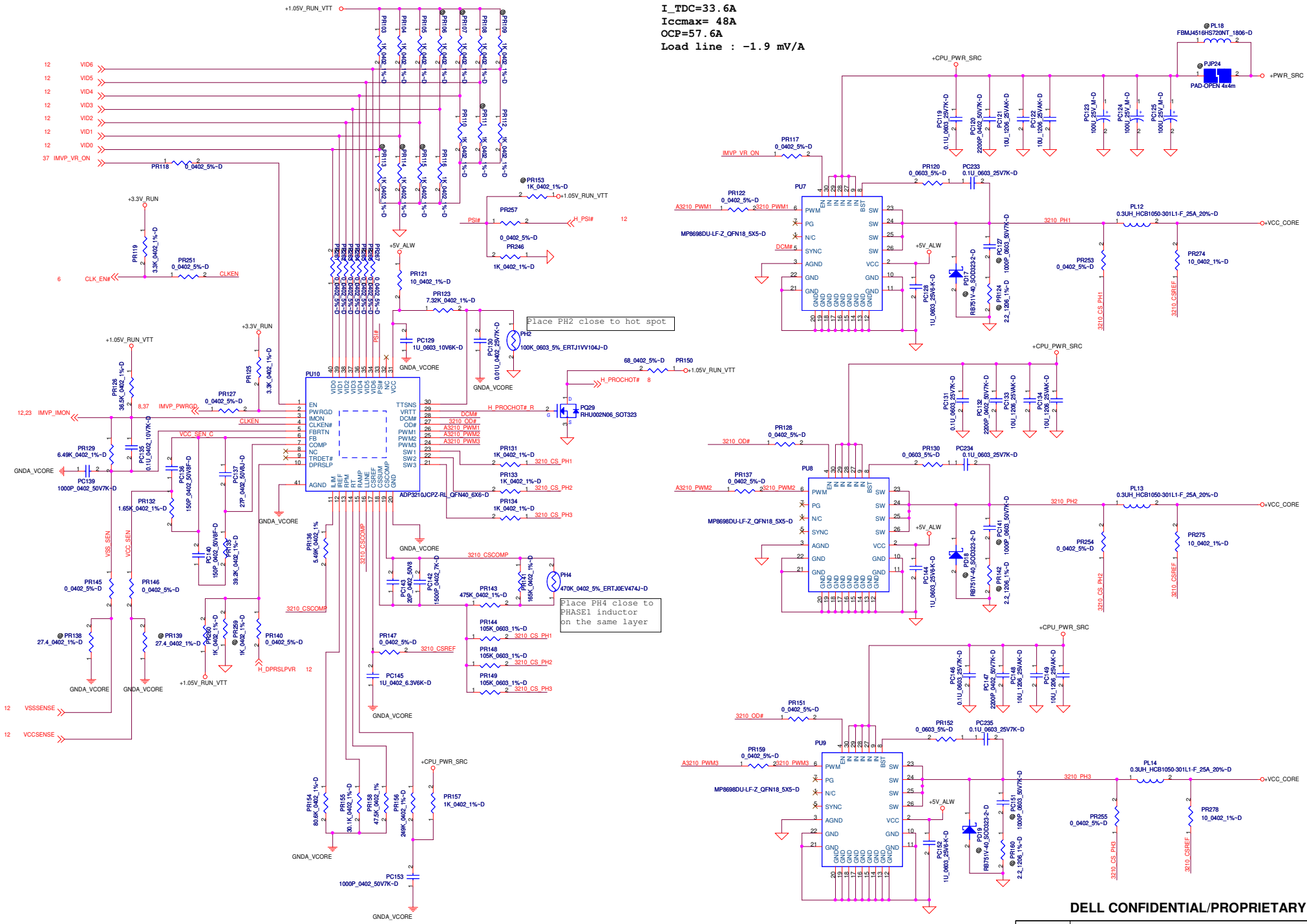
H_VTTPWRGD high level: 1.1V

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+1.05V_M/+1.05V_RUN_VTT		
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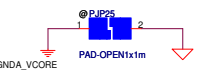
I_TDC=33.6A
 Iccmax= 48A
 OCP=57.6A
 Load line : -1.9 mV/A



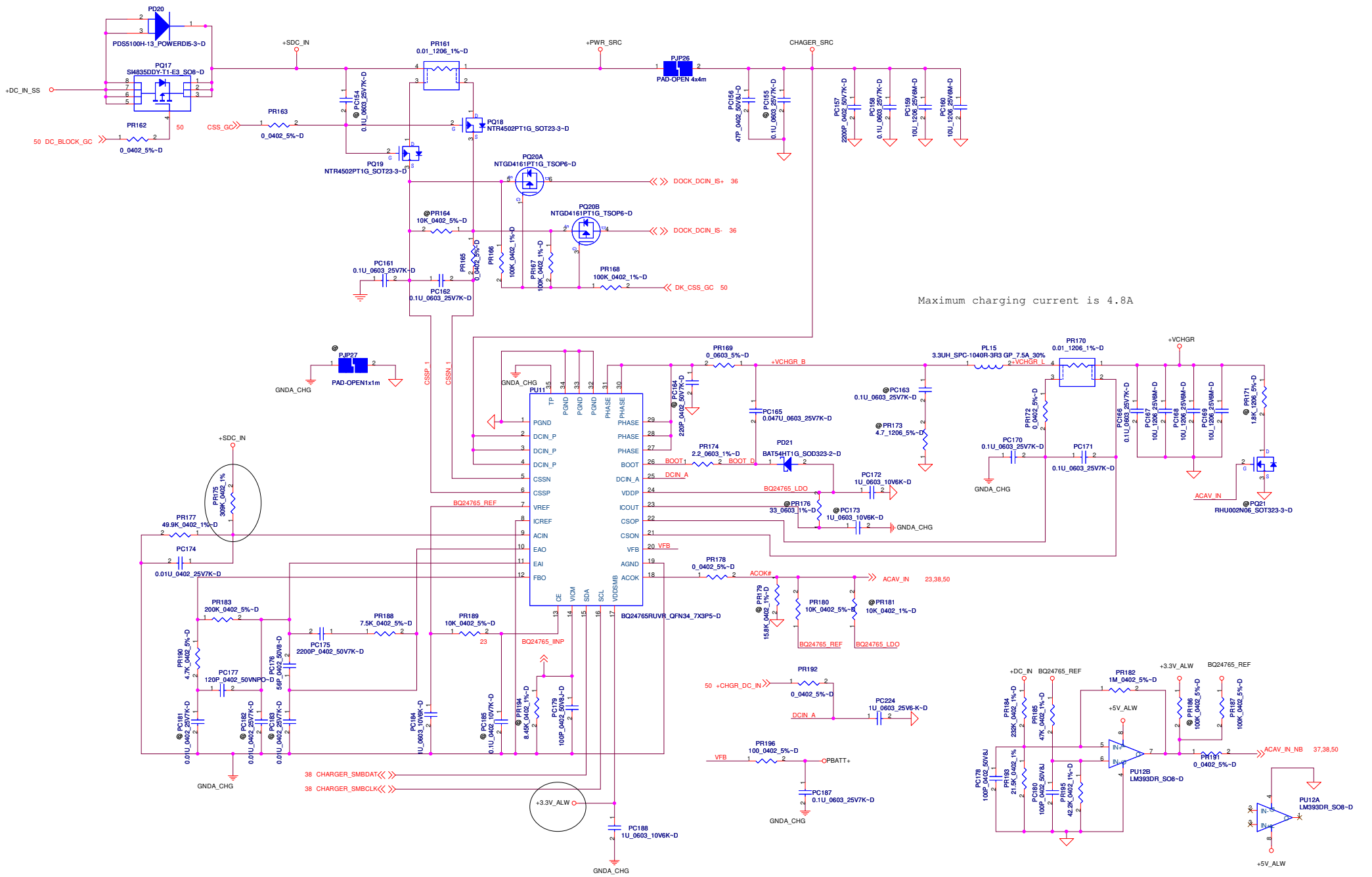
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		+VCC CORE	
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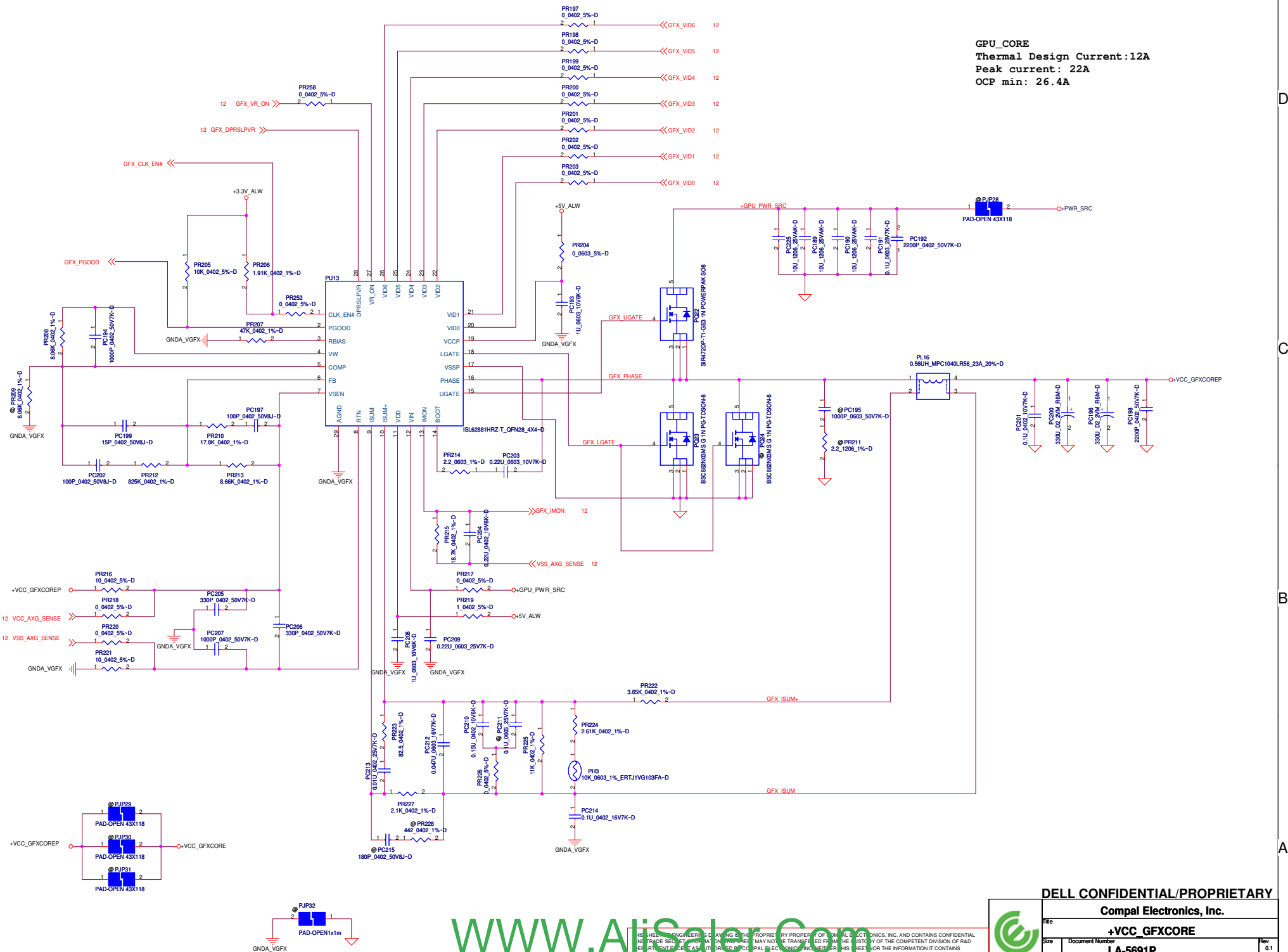
Maximum charging current is 4.8A

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Charger		
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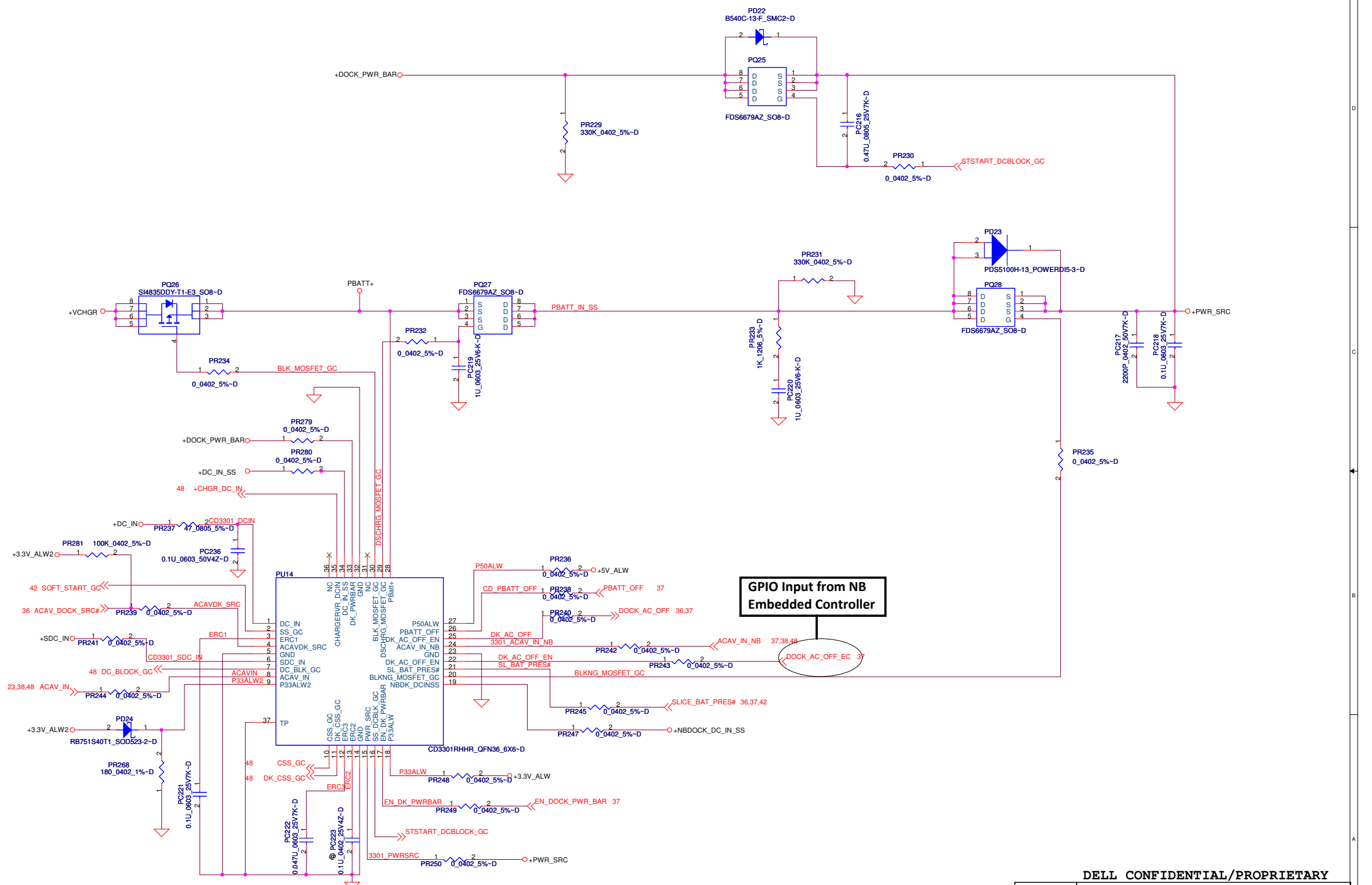


GPU_CORE
 Thermal Design Current:12A
 Peak current: 22A
 OCP min: 26.4A

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Title		+VCC GFXCORE	
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GPIO Input from NB Embedded Controller

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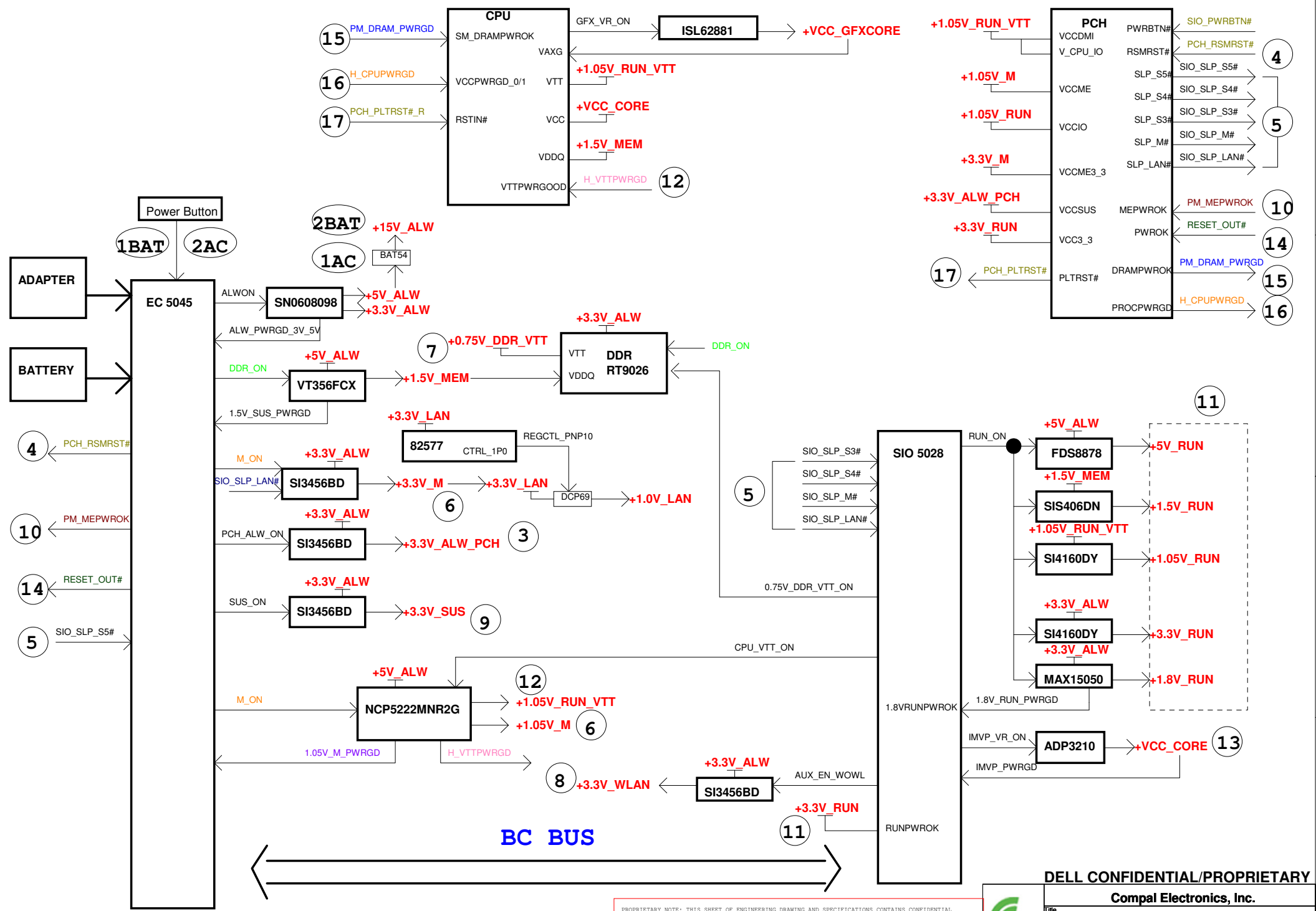
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Title		Selector	
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Power Sequence			
File			
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