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Analysis of Two-Pole Compensation in Linear Audio Amplifiers

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ABSTRACT

An analysis of the two-pole compensation technique used in three-stage linear audio amplifiers is presented. An expression for the loop gain of a linear amplifier incorporating two-pole compensation is derived, allowing the designer to easily select the unity loop gain frequency and zero location by choosing appropriate values for the compensation components.

Also presented is a simulation method that allows the designer to observe an amplifier's closed-loop and loop gain responses in a single pass without requiring modification to the circuit's feedback path; and two separate modifications to the usual two-pole compensation approach which improve phase margin and significantly enhance negative-rail power-supply rejection ratio.

1. INTRODUCTION

1.1. Review of Negative Feedback Theory

Figure 1 shows generic block-diagram representations for systems employing non-inverting or inverting negative-feedback. The systems' closed-loop input to output transfer functions are given by:

$$\frac{out}{in} = \frac{G(s)}{1 + H(s)G(s)} \quad (1.)$$

(non-inverting)

$$\frac{out}{in} = \frac{G(s)(H(s) - 1)}{1 + H(s)G(s)} \quad (2.)$$

(inverting)

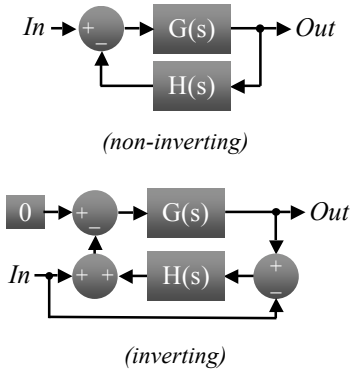


Figure 1: Block Diagram Representations of Negative-Feedback

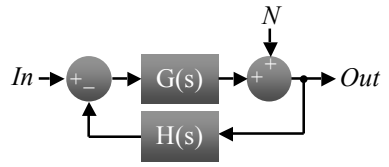
If some unwanted disturbance (such as noise and distortion) N is introduced as shown in Figure 2, the output signals become:

$$out = in\frac{G(s)}{1+H(s)G(s)} + \frac{N}{1+H(s)G(s)} \quad (3.)$$

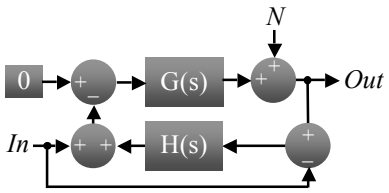
(non-inverting)

$$out = in\frac{G(s)(H(s)-1)}{1+H(s)G(s)} + \frac{N}{1+H(s)G(s)} \quad (4.)$$

(inverting)



(non-inverting)



(inverting)

Figure 2: Negative Feedback Systems with Noise and Distortion Introduced at the Output Node

It is desirable for G(s) to be as large as possible, as this will minimise the unwanted disturbance and the input-to-output transfer functions will tend to:

$$\frac{out}{in} = \frac{1}{H(s)} \quad (5.)$$

(non-inverting)

$$\frac{out}{in} = \frac{H(s)-1}{H(s)} \quad (6.)$$

(inverting)

Where H(s) can be defined using passive components with tight tolerances, resulting in a well-defined frequency response and high manufacturing repeatability.

However, a potentially conflicting requirement is to maintain system stability. If there is a frequency at which the phase of the loop gain (H(s)G(s)) is equal to −180°, the loop gain will be a negative real number and the negative feedback becomes positive feedback. If the modulus of H(s)G(s) at this frequency is greater than or equal to unity, the loop is unstable and the system will oscillate [1]. System stability can be investigated through a bode-plot of the H(s)G(s) function; a stable system has a "gain margin" and "phase margin" as shown in Figure 3. Ensuring that the slope of H(s)G(s) is −20 dB/decade or lower as it crosses 0 dB should guarantee stability.

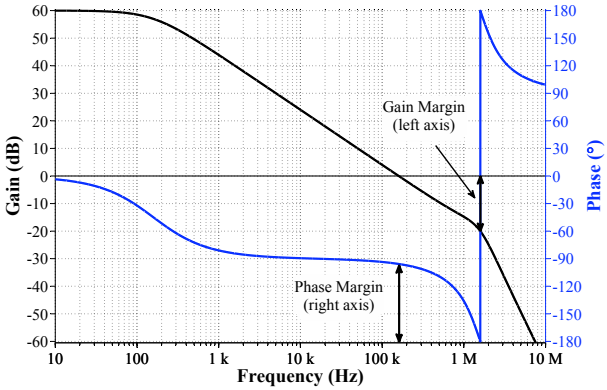


Figure 3: Bode Plot of Loop Gain for an Example Stable System

Whilst the block diagrams and expressions shown here for the non-inverting case will be familiar from the literature, those for the inverting case are less commonly seen and bear further explanation. Consider the classic inverting op-amp configuration as shown in Figure 4.

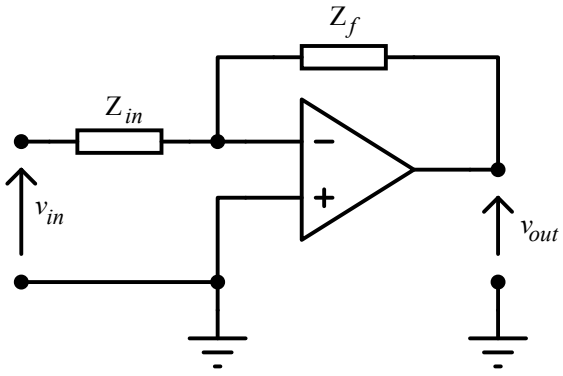


Figure 4: Inverting Op-Amp Configuration

For this configuration, H(s) is given by:

$$H(s) = \frac{Z_{in}}{Z_{in} + Z_f} \tag{7.}$$

Substituting into (2.) gives:

$$\frac{out}{in} = \frac{G(s)(\frac{-Z_f}{Z_{in} + Z_f})}{1 + \frac{Z_{in}}{Z_{in} + Z_f} G(s)} \tag{8.}$$

The op-amp's open-loop gain, G(s), is large such that (8) simplifies to the well-known expression:

$$\frac{out}{in} = -\frac{Z_f}{Z_{in}} \tag{9.}$$

In summary, an amplifier's loop gain should:

- Be maximised in the audio band in order to ensure a well-defined system frequency response, maximise input impedance, minimise output impedance, and minimise distortion.
- Be reduced in magnitude to below unity before its phase shift reaches −180°.

1.2. Three-Stage Linear Amplifiers

Figure 5 shows a schematic of a classic three-stage amplifier. Such a configuration is commonly used in linear audio amplifiers; often more elaborate circuitry is employed for each of the three stages, but the basic approach of differential input stage, voltage amplification stage (VAS) and current-gain output-stage remains [2][3][4][5].

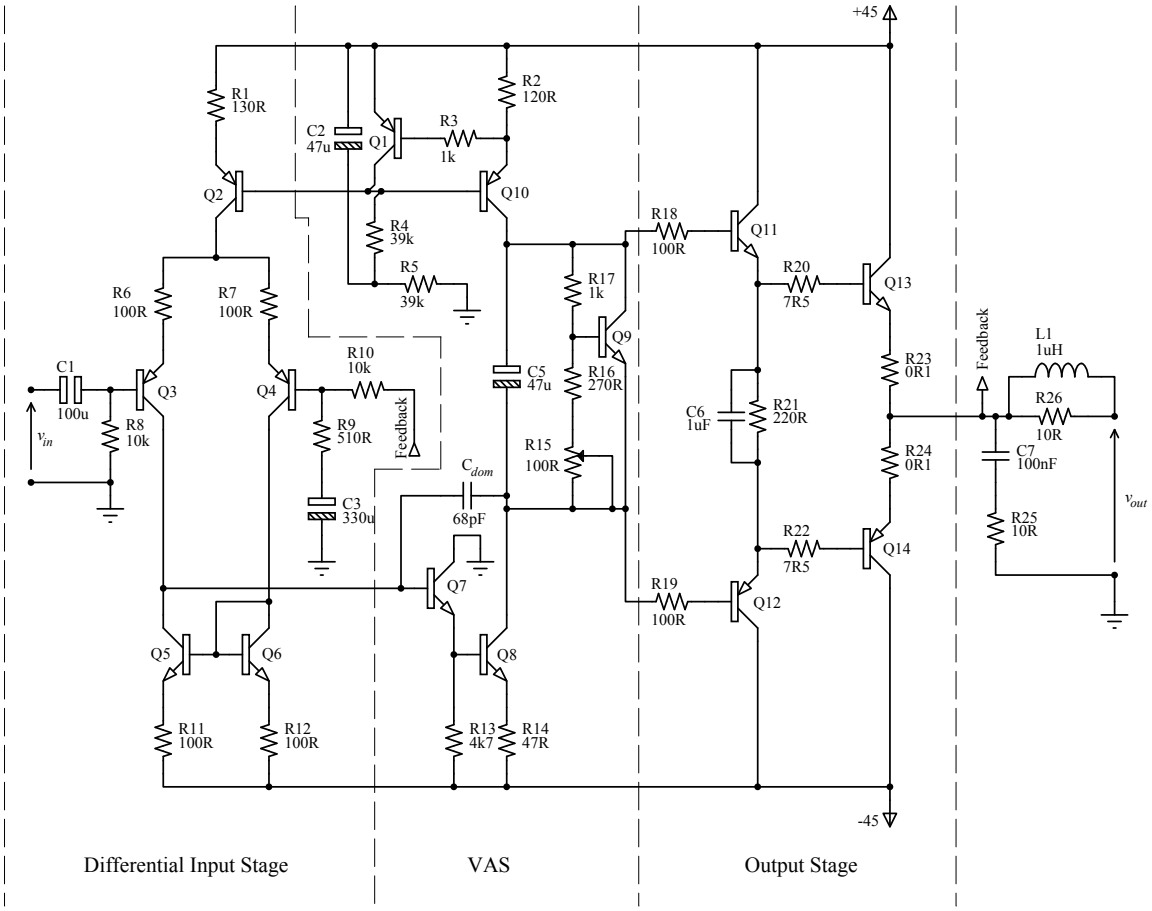


Figure 5: Schematic of Three-Stage Linear Amplifier

A vital feature of this amplifier configuration is the feedback capacitor, C_{dom}, that appears in the VAS. Without compensation, poles in the forward gain path of the amplifier, contributed by the input stage, VAS and output stage, prevent the application of stable global negative feedback. It is therefore necessary to introduce at least one low-frequency dominant pole, to ensure that the loop gain falls below unity before the output stage poles frequency. Local feedback around the VAS transistor has several additional benefits including: linearisation of the VAS, increase of the second VAS pole frequency (a phenomenon known as "pole splitting" [1]), and a reduction of VAS output resistance which reduces distortions due to loading by the non-linear input impedance of the output stage.

The value of C_{dom} also influences the amplifier's slew rate; the input stage and VAS must both be able to provide all the current required to charge and discharge C_{dom}, with the slew-rate limit defined as:

$$\left(\frac{dv_{out}}{dt}\right)_{max} = \frac{i_{max}}{C_{dom}} \qquad (10.)$$

Where i_{max} is the maximum current available to charge and discharge C_{dom}. As such, the input stage tail current and VAS load current must be large enough to comfortably supply the current required in order to avoid slew-rate-limit induced distortion. In terms of sinusoidal signals, as frequency increases, so does the current flowing in C_{dom}; Figure 6 shows the current flowing when the amplifier is outputting a 40 V peak 20 kHz sinewave.

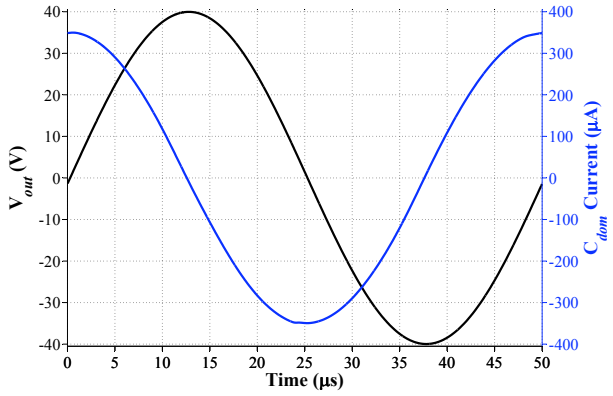


Figure 6: Current Flowing in C_{dom} with 20 kHz Amplifier Output Signal

2. SIMULATING LOOP GAIN WITH SPICE-BASED CIRCUIT SIMULATORS

When designing a circuit employing negative feedback, it is desirable to be able to simulate its loop gain using a SPICE-based circuit simulator. This allows the designer to check the magnitude of the loop gain in the pass band and ensure there are sufficient gain and phase margins to guard against instability.

For some systems, it is possible to open the feedback path and inject an input signal at the opening, allowing loop gain to be directly observed (by observing the output signal) as shown in Figure 7.

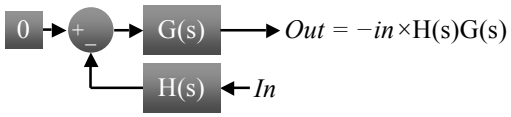


Figure 7: Observing Loop Gain by Opening the Feedback Loop

However, in the case of a three-stage amplifier the loop must be closed in order to correctly bias the amplifier stages; without any feedback, the amplifier will saturate to one of the supply rails. The solution often suggested in the literature is to modify the feedback loop to provide feedback at DC, but no feedback for AC signals [1][6]; again allowing an input signal to be applied at the loop "opening" and the loop gain to be observed by observation of the resulting output signal, as shown in Figure 8.

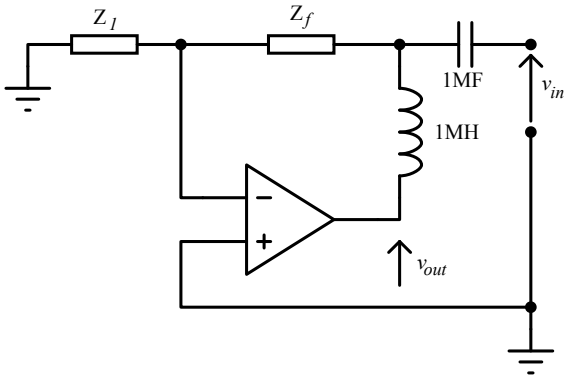


Figure 8: Observing Loop Gain in High-Gain Circuits by Modification of the Feedback Loop

This approach has some drawbacks:

- At higher frequencies where the loop gain is approaching unity, the output impedance of the circuit is increasing and its input impedance (at the non-inverting and inverting inputs) is decreasing. As such, the feedback network can load the output and the input can load the feedback network, altering both G(s) and H(s). The opening of the feedback loop will isolate either the output stage or input stage from the feedback network, eliminating the loading effects and therefore providing inaccurate results.

- Loop gain and input to output closed-loop response must be simulated using two separate circuits.

These problems can be avoided in circuit simulators that allow the user to perform maths functions on circuit probes. With the feedback loop left unmodified, by building a suitable function of the voltages at observable nodes in the circuit, the simulator can be configured to display a bode plot of the loop gain.

If the signals at the non-inverting and inverting inputs are denoted v_+ and v_- respectively, from inspection of Figure 1 it can be seen that for the non-inverting case:

$$\begin{aligned} \mathrm{H(s)} &= \frac{v_-}{out} \\ \mathrm{G(s)} &= \frac{out}{v_+ - v_-} \end{aligned} \tag{11.}$$

Multiplying the two expressions gives:

$$\mathrm{H(s)G(s)} = \frac{v_-}{v_+ - v_-} \tag{12.}$$

Therefore, the loop gain of a non-inverting amplifier can be calculated by voltage probing the non-inverting and inverting inputs and applying the function shown in (12.).

For the inverting case:

$$\begin{aligned} \mathrm{H(s)} &= \frac{v_- - in}{out - in} \\ \mathrm{G(s)} &= \frac{out}{-v_-} \end{aligned} \tag{13.}$$

Multiplying the two expressions gives:

$$\mathrm{H(s)G(s)} = \frac{1 - \frac{in}{v_-}}{\frac{in}{out} - 1} \tag{14.}$$

Therefore, the loop gain of an inverting amplifier can be calculated by voltage probing the input, output and inverting input nodes and applying the function shown in (14.).

3. TWO-POLE COMPENSATION

3.1. Introduction

The voltage gain of a three-stage amplifier is given by the product of the input stage transconductance ($\frac{i_{out}}{v_+ - v_-}$), the VAS transresistance ($\frac{v_{out}}{i_{in}}$) and the output stage voltage gain. At DC, the output stage gain is approximately unity and the other parameters are equal to:

$$g_m = -\frac{1}{r_e + R_e} \tag{15.}$$

$$r_m = -\beta \mathrm{R_c} \tag{16.}$$

Where $r_e = \frac{25}{\mathrm{I_c}/2}$, $\mathrm{I_c}$ is the input stage tail current in mA, $\mathrm{R_e}$ is the value of the emitter degeneration resistors (R6 and R7 in Figure 5), β is the current gain of the VAS transistor and $\mathrm{R_c}$ is the effective collector load of the VAS. For a dominant-pole compensated amplifier such as that shown in Figure 5, the feedback capacitor C_{dom} modifies the VAS transresistance to:

$$r_m = -\frac{\beta \mathrm{R_c}}{1 + j\omega\beta \mathrm{C}_{dom} \mathrm{R_c}} \tag{17.}$$ [2] p64

Whilst the open-loop DC gain and dominant-pole frequency of the amplifier depend upon VAS β and will therefore vary from one instance of the amplifier to another; as ω increases, the amplifier's open-loop gain tends to $\frac{g_m}{j\omega \mathrm{C}_{dom}}$. The unity-loop-gain frequency

therefore does not vary with difficult-to-control circuit parameters such as transistor β, leading to good manufacturing repeatability.

A consequence of dominant-pole compensation is that the loop gain increases at only 20 dB per decade as frequency falls from the unity-loop-gain point. This limits the loop gain at high audio frequencies to modest values as shown in Figure 9.

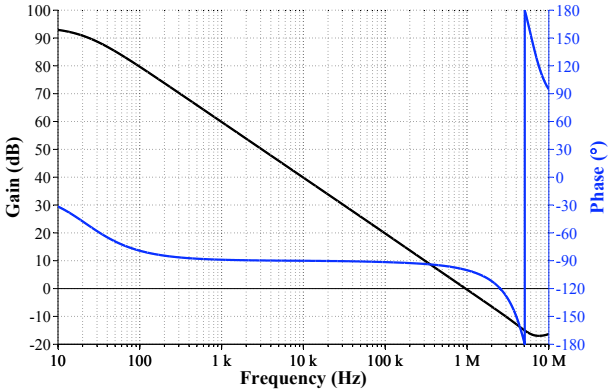


Figure 9: Loop Gain of Amplifier with Dominant-Pole Compensation

A solution is the use of two-pole compensation. This consists of introducing an additional low-frequency pole, followed by a zero at a higher frequency, placed to bring the gain slope back to −20 dB/decade before the loop gain crosses 0 dB. In this way, as frequency falls from the unity-loop-gain point, the loop gain initially increases at 20 dB per decade, as in the single dominant pole case. However, at the zero frequency, this rate increases to 40 dB per decade, resulting in much higher loop gains in the audio band. The placement of the zero is a compromise between maximising feedback factor in the audio band and maintaining stability (the closer the zero to unity-loop-gain frequency, the lower the amplifier's phase margin).

3.2. Analysis

Whilst the two-pole compensation technique is mentioned in the literature [2][4][5], an analysis is not provided. Circuit analysis results in expressions that enable the designer to easily select the unity-loop-gain and zero frequencies of an amplifier by choosing appropriate values for the compensation components.

Figure 10 shows a VAS circuit with two-pole compensation components and each voltage and current signal labelled.

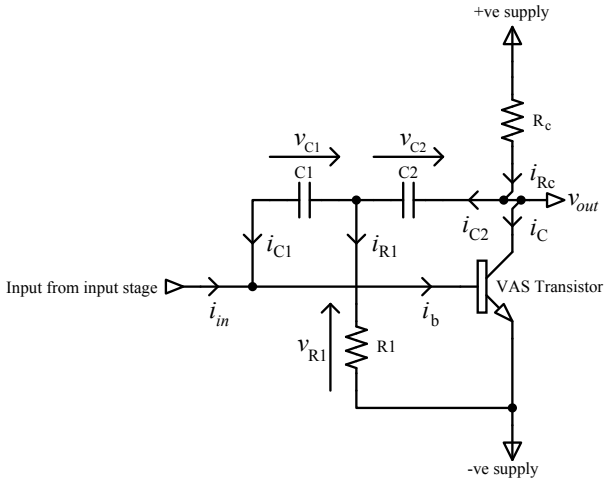


Figure 10: VAS Transistor Circuit with Two-Pole Compensation Components

From small-signal analysis of Figure 10, the small-signal transresistance can be found. Firstly, inspection of Figure 10 gives:

$$i_{\mathrm{Rc}} = i_{\mathrm{C}} + i_{\mathrm{C2}} \tag{18.}$$

$$i_{\mathrm{b}} = i_{in} + i_{\mathrm{C1}} \tag{19.}$$

$$i_{\mathrm{C}} = \beta i_{\mathrm{b}} \tag{20.}$$

$$v_{out} = -i_{\mathrm{Rc}}\mathrm{R_c} \tag{21.}$$

Substituting (18.), (19.) and (20.) into (21.) yields:

$$-\frac{v_{out}}{\mathrm{R_c}} = \beta\left[i_{in} + i_{\mathrm{C1}}\right] + i_{\mathrm{C2}} \tag{22.}$$

For AC signals, R1 and C1 are in parallel. Denoting the parallel impedance of R1 and C1 as Z1:

$$i_{\mathrm{C2}} = \frac{v_{out}}{\frac{1}{\mathrm{sC2}} + \mathrm{Z1}} = v_{out}\frac{\mathrm{sC2}}{1 + \mathrm{sC2Z1}} \tag{23.}$$

$$v_{C1} = v_{out}\frac{Z1}{\frac{1}{sC2}+Z1} = v_{out}\frac{sC2Z1}{1+sC2Z1} \quad (24.)$$

$$i_{C1} = v_{out}\frac{s^2C1C2Z1}{1+sC2Z1} \quad (25.)$$

Substituting (23.) and (25.) into (22.):

$$-\frac{v_{out}}{R_c} = \beta\left[i_{in} + \frac{v_{out}s^2C1C2Z1}{1+sC2Z1}\right] + \frac{v_{out}sC2}{1+sC2Z1} \quad (26.)$$

re-arranging:

$$r_m = -\beta R_c\frac{1+sC2Z1}{1+sC2(Z1+R_c)+s^2\beta R_cC1C2Z1} \quad (27.)$$

Substituting $Z1 = \frac{R1}{1+sR1C1}$ and re-arranging yields:

$$r_m = -\beta R_c\frac{1+sR1(C1+C2)}{1+s(R1C1+R1C2+R_cC2)+s^2\beta R_cR1C1C2} \quad (28.)$$

As with the single dominant pole compensation technique, DC gain is dependant upon transistor β and collector load. The poles vary with β and collector load, falling in frequency as β or R_c rise. High-frequency behaviour depends only on the compensation components, with a zero at:

$$f_z = \frac{1}{2\pi R1(C1+C2)} \quad (29.)$$

And high-frequency transresistance of:

$$r_m = -\frac{C1+C2}{sC1C2} \quad (30.)$$

The unity-loop-gain frequency of the complete amplifier is therefore given by:

$$f_0 = H(s)g_m\frac{C1+C2}{2\pi C1C2} \quad (31.)$$

The VAS and input stage current sourcing/sinking requirements for two pole compensation can be derived from equations (23.) and (25.):

$$\hat{i}_{C2} = \hat{v}_{out}\frac{\sqrt{(\omega C2)^2+(\omega^2R1C1C2)^2}}{\sqrt{1+(\omega R1[C1+C2])^2}} \quad (32.)$$

$$\hat{i}_{C1} = \hat{v}_{out}\frac{\omega^2R1C1C2}{\sqrt{1+(\omega R1[C1+C2])^2}} \quad (33.)$$

At audio frequencies, the low values of C1 and C2 dominate and these expressions simplify to:

$$\hat{i}_{C2} = \hat{v}_{out}\omega C2 \quad (34.)$$

$$\hat{i}_{C1} = \hat{v}_{out}\omega^2R1C1C2 \quad (35.)$$

At high frequencies, (32.) and (33.) both simplify to the same expression:

$$\hat{i} = \hat{v}_{out}\frac{\omega C1C2}{C1+C2} \quad (36.)$$

Therefore, taking a single-pole compensated amplifier and selecting C2 equal to C_{dom} and C1 at least an order of magnitude larger will result in an unchanged unity-loop-gain frequency and amplifier slew rate but with much reduced input-stage current requirement at audio frequencies. Note that in the audio band, R1 determines how the current flowing in C2 will be divided between C1 and R1. As such, as R1 increases, so does the current required from the input stage, but VAS current requirement does not change.

If C_{dom} in the circuit of Figure 5 is replaced with two-pole compensation components, then selecting C1 = 1.2 nF, C2 = 68 pF and R = 390 Ω results in unchanged unity-loop-gain frequency, with a zero at approximately 320 kHz. The simulated loop gain is now as shown in Figure 11 and the simulated currents in C1 and C2 are shown in Figure 12.

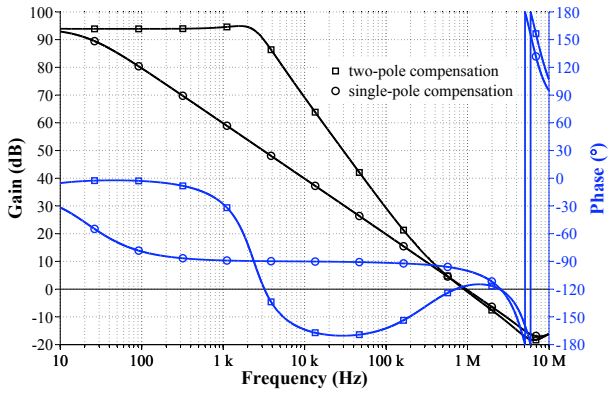


Figure 11: Loop Gain for Amplifier with Two-Pole Compensation

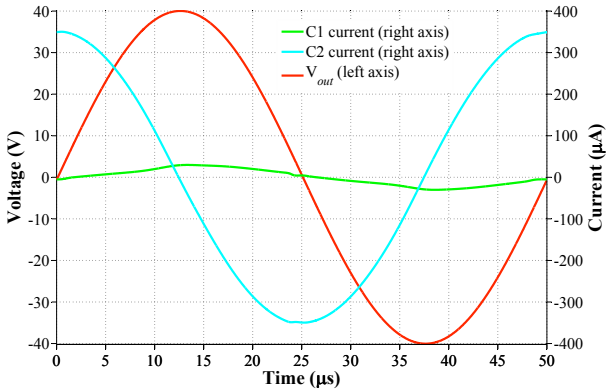


Figure 12: Current Flowing in Compensation Capacitors of an Amplifier with Two-Pole Compensation; 20 kHz Signal Frequency

The amplifier retains sufficient gain and phase margins, but the magnitude of the loop gain is considerably higher across the audio band. It must be noted that this is a small-signal simulation of loop gain; to generate these bode plots the circuit simulator will have determined a DC operating point, created linearised small-signal models for the active circuit components based on this operating point, then computed the frequency response of the complete circuit. As such, the voltage and current swings caused by AC excitation do not change the parameters of the small-signal models. However, several transistor parameters such as f_T and parasitic capacitance vary with V_{ce} and I_c so in real-world large-signal operation, the loop gain of an amplifier will vary with signal conditions. As a further test, a transient analysis can be performed, using as the input signal a series of small pulses superimposed onto a low-frequency sinusoid as shown in Figure 13 [7].

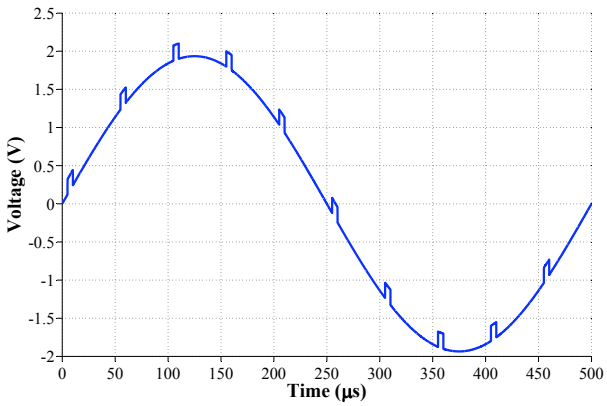


Figure 13: Amplifier Input Signal for Transient-Analysis Investigation of Stability [7]

Several analyses can be performed, with the input sinusoid having an amplitude that results in maximum amplifier output amplitude, and the amplifier's load impedance stepped to result in different output stage current levels; in this way, the circuit is tested across its operating range. Phase margin can be inferred from the amplifier's response to each pulse; the greater the ringing after a pulse, the lower the phase margin. Instability would result in the output ceasing to follow the input, or possibly even the failure of the simulation as SPICE is unable to find a convergent solution. The result of performing such a test on the circuit of Figure 5, with C_{dom} replaced with the two-pole compensation components previously discussed, is shown in Figure 14.

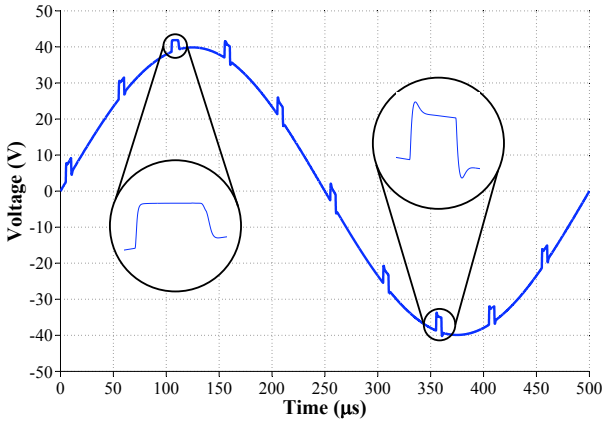


Figure 14: Results of Transient Analysis of Amplifier with Two-Pole Compensation (8 Ω load, voltage measured at output before inductor.)

3.3. Improving the Phase Response

The loop gain phase between the pole and unity-loop-gain frequencies falls as low as −170°. This is not usually a concern since the magnitude of the loop gain is very large at this point; the amplifier output impedance is therefore negligible and normal loads will not push the amplifier into instability. However, should a greater phase margin in this region be desired, adding a 15 nF capacitor in series with the compensation resistor introduces a further pole-zero pair, giving the loop gain frequency response shown in Figure 15. Relative to the two-pole case, some loop gain is sacrificed in the audio band but the minimum phase shift before the unity-gain frequency is increased to −151°; loop gain remains significantly higher than the single-pole case.

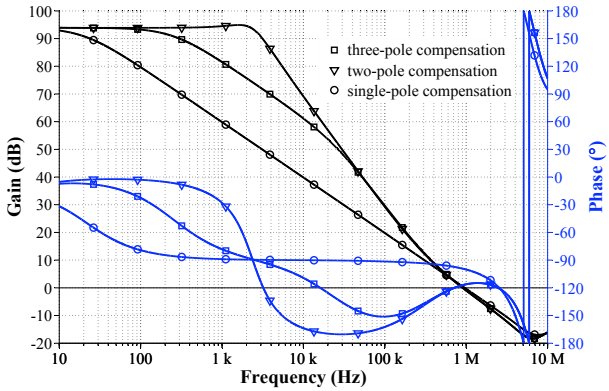


Figure 15: Loop Gain Frequency Response for "Three-Pole" compensation by Addition of a Capacitor in Series with R1

3.4. Improving Power Supply Rejection Ratio

Power supply rejection ratio (PSRR) is a measure of the degree to which variations on a power amplifier's supply rails will affect the output signal. Ideally, the rejection ratio should be infinite such that any power supply variation results in no change in amplifier output. In an amplifier employing dual positive and negative supply rails, two PSRRs can be defined: one measuring the effects of variations on the positive rail ("positive-rail PSRR"), and the other the effects of variations on the negative rail ("negative-rail PSRR").

Power supply rejection on a given rail can be simulated by keeping the opposite rail fixed and grounding the input node. A small ac signal (v_{ps}) is added to the DC level of the rail in question, and the output signal is observed. PSRR is then defined in dB as:

$$\text{PSRR} = 20\log_{10}\left(\frac{v_{ps}}{v_{out}}\right) \qquad (37.)$$

Figure 16 shows plots of positive- and negative-rail PSRR against frequency for the single-dominant-pole amplifier of Figure 5.

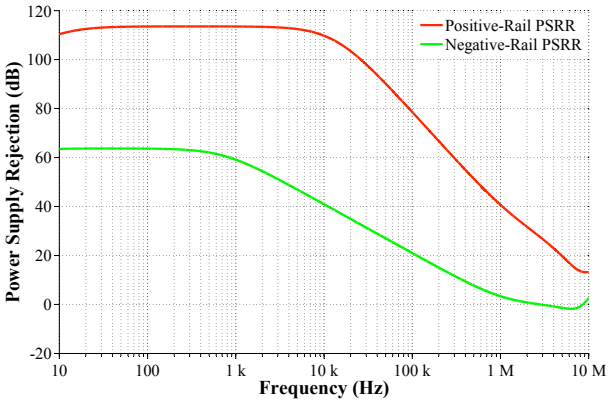


Figure 16: PSRR in a Single-Dominant-Pole Amplifier

Introducing a cascode to the input stage and VAS and moving the connection for C_{dom} as shown in Figure 17, results in improved PSRR as demonstrated in Figure 18. The cascodes have the additional benefits of allowing the use of low-noise, high-beta devices in the input stage (which have too-low V_{ceo} ratings to be used otherwise) and eliminating the early effect in the VAS transistor.

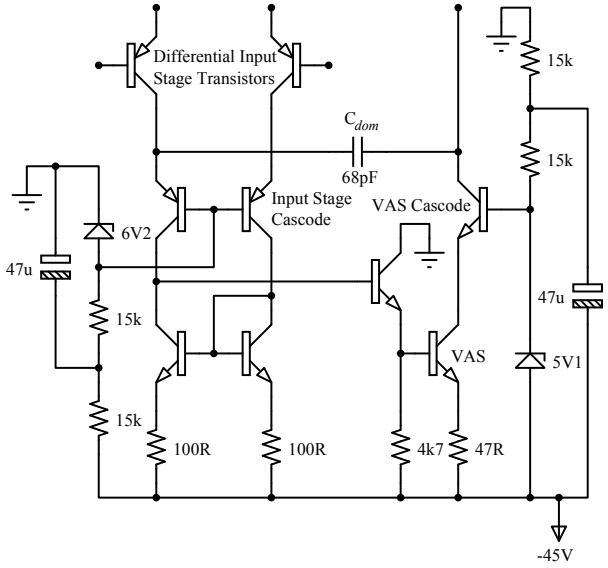


Figure 17: Cascoding in a Single-Dominant-Pole Amplifier

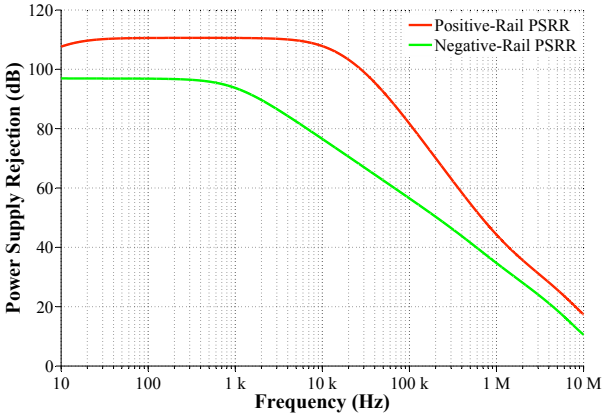


Figure 18: Improved PSRR due to Cascoding and Altered C_{dom} connection

Retaining the cascodes and changing to the usual two-pole compensation configuration (Figure 19) results in the PSRR shown in Figure 20.

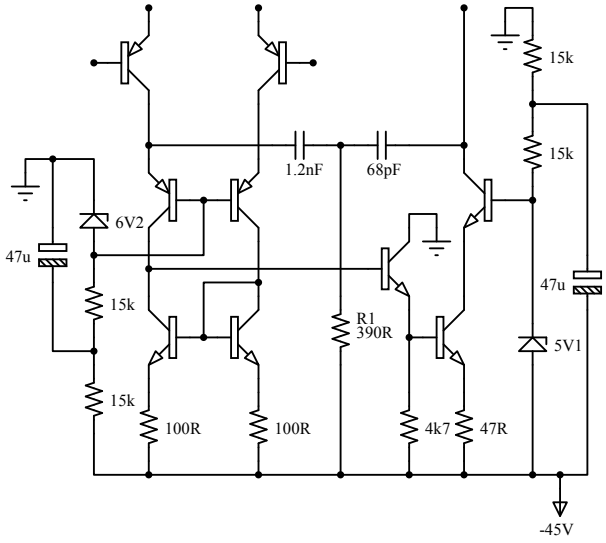


Figure 19: Traditional Two-Pole Compensation Connection

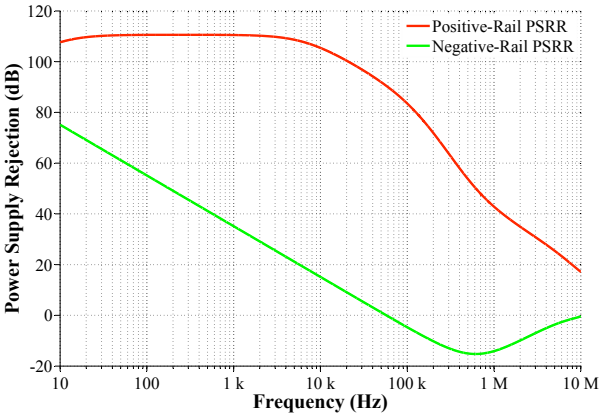


Figure 20: PSRR for Amplifier with Traditional Two-Pole Compensation

Whilst positive-rail rejection has remained high, negative-rail rejection has deteriorated. This can be solved by connecting the compensation resistor (R1 in Figure 19) to ground instead of the negative power rail. This results in PSRR as shown in Figure 21.

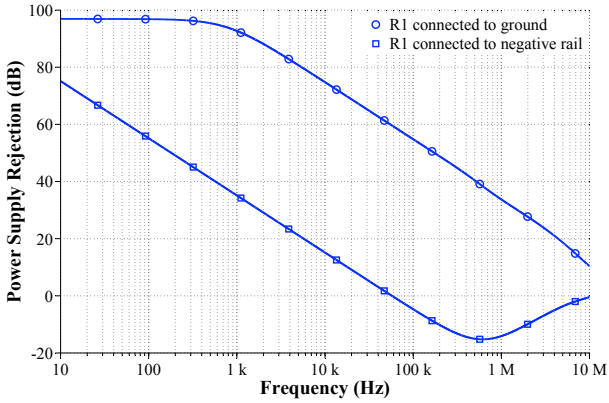


Figure 21: Improved Negative-Rail PSRR in Two-Pole Compensated Amplifier by Moving Resistor Connection

4. CONCLUSION

An analysis of the two-pole compensation technique for linear amplifiers has been presented, providing expressions that relate the amplifier's unity-loop-gain and zero frequencies to the values of the compensation components. It is shown that these frequencies are independent of poorly toleranced circuit parameters such as transistor β, so loop-gain behaviour will vary little from one instance of an amplifier to another.

An improved method of loop-gain simulation has been presented, ensuring interaction between output-impedance, feedback network and input impedance is accurately captured at high frequencies, and allowing closed-loop response to be simulated simultaneously. The well-known improvement in audio-band loop-gain magnitude with two-pole compensation is confirmed, and it has also been shown that the technique reduces loading of the input stage whilst leaving VAS loading unaltered if appropriate component values are selected.

Two modifications to the traditional two-pole technique have been proposed. The addition of a capacitor will introduce a further pole-zero pair, improving the loop-gain phase response if required. Altering the resistor connection in conjunction with cascoding in the input stage and VAS dramatically improves negative-rail power-supply rejection ratio.

5. REFERENCES

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ADDENDUM

Addendum added 9 June 2012 by Harry Dymond.

Since presenting this paper a number of shortcomings have come to my attention that I would like to address, these are:

Inaccuracy of proposed loop-gain simulation method. The proposed method of simulating loop gain gives incorrect results above the unity-loop-gain frequency (ULGF) and at very low frequencies (< 5 Hz); this means it cannot be used to predict gain margin. However, for 5 Hz $\leq f \leq$ ULGF, the method does give more accurate results than breaking the loop and inserting a large inductor to maintain feedback at DC, then injecting a test signal to the loop via a large capacitor. The proposed method can therefore be used to observe the "correct" behaviour of the loop gain for these frequencies, and the resulting figure for phase margin will be correct. This has been verified by comparing the method to a fully accurate way to simulate loop gain: the General Feedback Theorem (GFT) [1][2].

Stability of inner feedback loop. It is important to ensure that the inner feedback loop (that formed by the compensation components around the VAS), in addition to the global feedback loop, is stable; it is possible that when cascodes are added to the input stage and VAS that the inner loop becomes unstable.

The loop gain of the inner loop can be simulated by disabling the global feedback loop at AC (short out both inverting and non-inverting inputs by connecting 1 kF capacitors to ground) and inserting a GFT probe in the inner loop e.g. between C2 and the junction of C1 and R1. If the loop is found to be unstable or have insufficient phase and/or gain margin, this can be ameliorated by connecting a resistor and capacitor in series from the VAS collector to ground. The additional resistor will typically have a resistance in the order of tens to hundreds of Ω, and the capacitor a capacitance in the order of tens to hundreds of pF. Depending on the values required, this may have an adverse affect on slew rate. This can be alleviated by bootstrapping the network [3].

Simplicity and accuracy of VAS model. The model used to derive the equation for the loop-gain response assumes a "perfect" VAS transistor with no parasitic elements and that the VAS behaves like a transimpedance stage (current in, voltage out) for all frequencies from DC ("VAS" is therefore a misnomer and "TIS" (TransImpedance Stage) is more appropriate). However, at low frequencies before the feedback around the VAS has taken effect, this stage behaves more like a true VAS (voltage in, voltage out) and the model is therefore inaccurate. This inaccuracy manifests as an overestimation of the Q of the complex poles and of the loop gain at DC.

Fortunately, the main insights delivered - the ULGF frequency, zero frequency, current requirements of the VAS/TIS and input stage, that C2 should be small and C1 should be large, and the fact that the value of R1 only has an effect on the loading of the input stage and a higher value makes the loading worse - are all valid regardless of the simplicity of this model.

"Three pole" compensation misnomer. In section 3.3 it is proposed that a capacitor can be added in series with the compensation resistor (R1 in figure 10) to improve the phase response of the loop gain. This has been referred to as "three pole" compensation but this is a misnomer; inspection of figure 15 shows the "three pole" curve to exhibit just two poles and one zero. Upon further analysis it appears that if an additional capacitor (let this be referred to here as "C3") is placed in series with the resistor (R1), the impedance of the resistor-capacitor combination does indeed now have a pole and a zero. However, when substituted into the expression for r_m, this results in a new pole and zero both at DC; these cancel and what is left is still a two-pole, one zero response but the designer now has much more control over the pole frequencies.

Taking C3 large (in the order of 1 μF) will give an unchanged response with two complex poles. As C3 is decreased, this damps the poles and eventually splits them into two real poles and moves them further apart in frequency, as shown in figure 15. Decreasing C3 further will move the loop gain response closer and closer to the single-pole response. It is proposed that a more suitable name for this compensation technique is "split two-pole" compensation.

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