ITRI
ERSO

ES52099

10-bit A/D Converter

Features

- 10-Bit Resolution.
- 5MHz Sampling Rate.
- Intermal S/H Function.
- Signal 5V Power Supply.
- V_{IN} Input Range : 0V to AV_{DD}.
- V_{REF} DC Range : 1V to AV_{DD}.
- Low Power : 175mW.
- Three – State Digital Outputs.
- Latch – Up Free

Applications

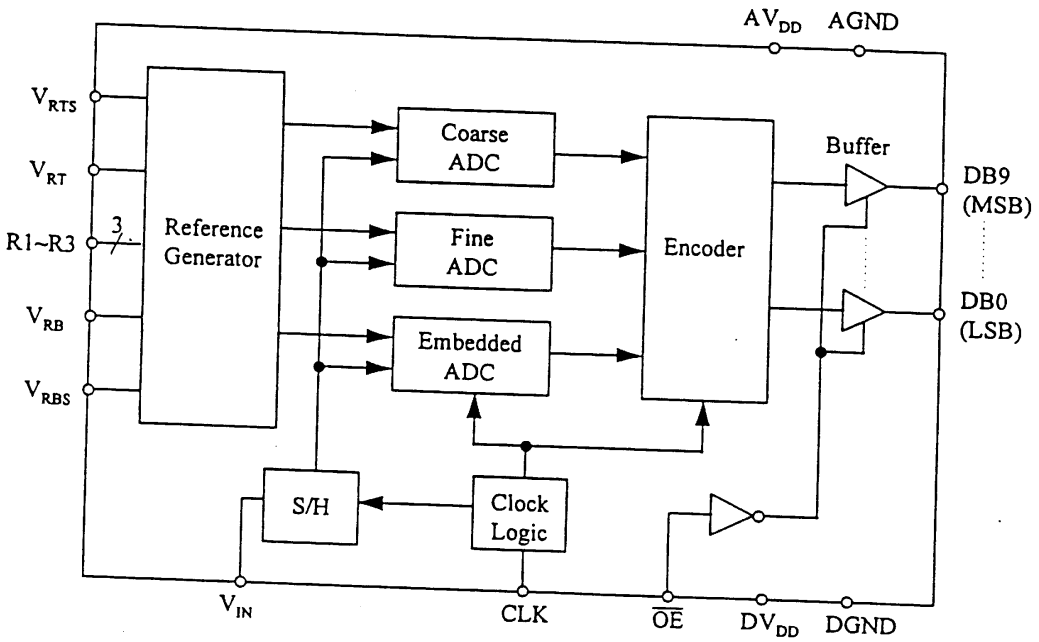
- Scanner

DESCRIPTION

The ES52099 is a 10 bit , 5MSPS, Analog to Digital Converter for applications that require high speed and high accuracy. Designed with advanced 5V CMOS process, this device offres excellent performance. Low power consumption and latch-up free operation.

The ES 52099 maintains low power conssumption at high conversion rates with subranging architecture, and the comparator design achieves a low analog input capacitance. The input circuitry of the input circuitry of the ES52099 includes an on-chip S/H function that allows this part to digitize analog input signals between AGND and AV_{DD}.

Block Diagram



The ES52099 has been patented at R.O.C. and the patent number is 076864.

Absolute Maximum Rating (TA = 25℃ unless otherwise noted)

Supply voltage(V_{DD})---------- 7V

Reference voltage(V_{RT}, V_{RB}) ---------- V_{DD}+0.5~GND-0.5V

Analog input voltage(V_{IN}) ---------- V_{DD}+0.5~GND-0.5V

All input voltage(CLK) ---------- V_{DD}+0.5~GND-0.5V

All output voltage(V_{OH}, V_{OL})---------- V_{DD}+0.5~GND-0.5V

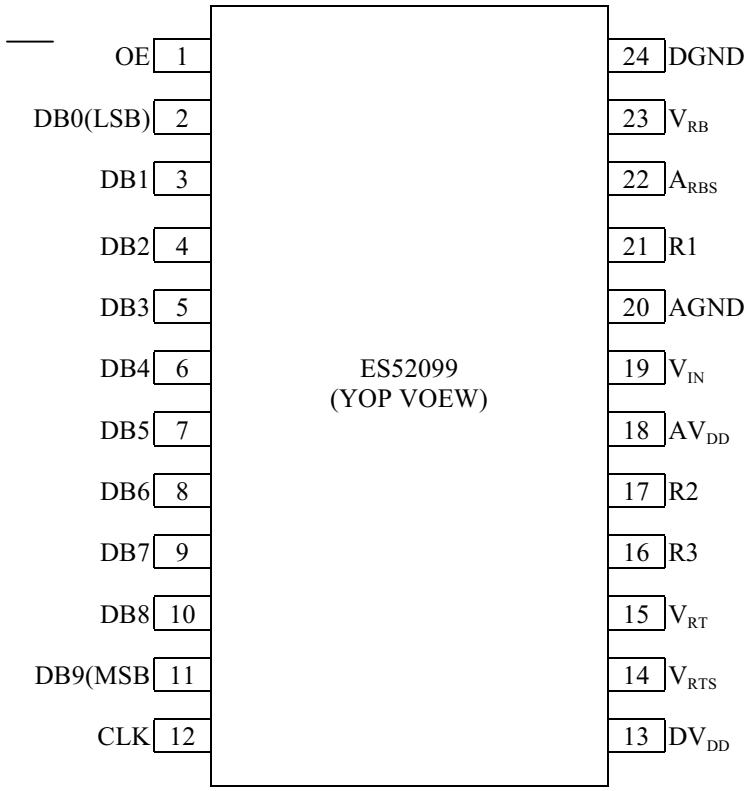
Storage temperature(T_{STG}) ---------- -65~+150℃

Lead Temperature(Soldering 10 Seconds) --------- 300℃

Recommended Operating Conditions

Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, AV_{SS}	4.75 to 5.25	V
	｜DGND-AGND｜	0 to 100	mV
Reference input voltage	V_{RB}	0 and above	V
	V_{RT}	AV_{DD} and below	V
	V_{RT} -V_{RB}	1.0 to V_{DD}	V
Analog input voltage	V_{IN}	V_{RB} to V_{RT}	V

PIN Assignment



Pin Description

Pin NO.	Symbol	Description	Pin NO.	Symbol	Description
1	OE	Output Enable	13	DV_{DD}	Digital Power Supply
2	DB0	Data Ouptput Bit 0 (LSB)	14	V_{RTS}	Top Internal Reference
3	DB1	Data Ouptut Bit 1	15	V_{RT}	Top Internal Reference
4	DB2	Data Ouptut Bit 2	16	R3	3/4 Reference Tap Point
5	DB3	Data Ouptut Bit 3	17	R2	1/2 Reference Tap Point
6	DB4	Data Ouptut Bit 4	18	AV_{DD}	Analog Power Supply
7	DB5	Data Ouptut Bit 5	19	V_{IN}	Analog Input Voltage
8	DB6	Data Ouptut Bit 6	20	AGND	Analog Ground
9	DB7	Data Ouptut Bit 7	21	R1	1/4 Reference Tap Point
10	DB8	Data Ouptut Bit 8	22	V_{RBS}	Bottom Internal Reference
11	DB9	Data Ouptut Bit 9(MSB)	23	V_{RB}	Bottom of Reference
12	CLK	Clock Input	24	DGND	Digital Ground

Electrical Characteristics

Unless Otherwise Specified :

$AV_{DD} = DV_{DD} = 5℃$ ，Fs = 5MSPS(50% Duty Cycle)，$V_{RT} = 4.0V$, $V_{RB} = 1.0V$ ，$T_A = 25℃$

Characteristic	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Key Features						
Resolution			10			Bits
Sampling Rate	Fs				5	MHz
Digital Outputs						
Logical”1”Current	I_{OH}	$V_{OH} = 4.5V$	3.5			mA
Logical”0”Current	I_{OL}	$V_{OH} = 0.5V$	3.5			mA
Tristate Leakage	I_{OZ}	V_{OUT} = DGND to DV_{DD}		10		μA
Data Valid Delay	T_{OL}			40		ns
Data Enalb Delay	t_{OL}			25		ns
Data Tristate Delay	T_{DHZ}			25		ns
Digital Inputs						
Logical”1”Voltage	V_{IH}		4			V
Logical”0”Voltage	V_{IL}				1	V
DC Leakage Current	I_{IN}	V_{IN} = DGND to DV_{DD}				
CLK				5		μA
$\overline{OE}$				15		μA
Input Capacitance				5		pF
Clock Timing						
Clock Period	1/Fs		200			ns
Rise & Fall Time	tR,tF			5		ns
“High’Pulse Width	t_{PWH}			100		ns
“LOW’Pulse Width	t_{PWH}			100		ns
Duty Cycle				50		%

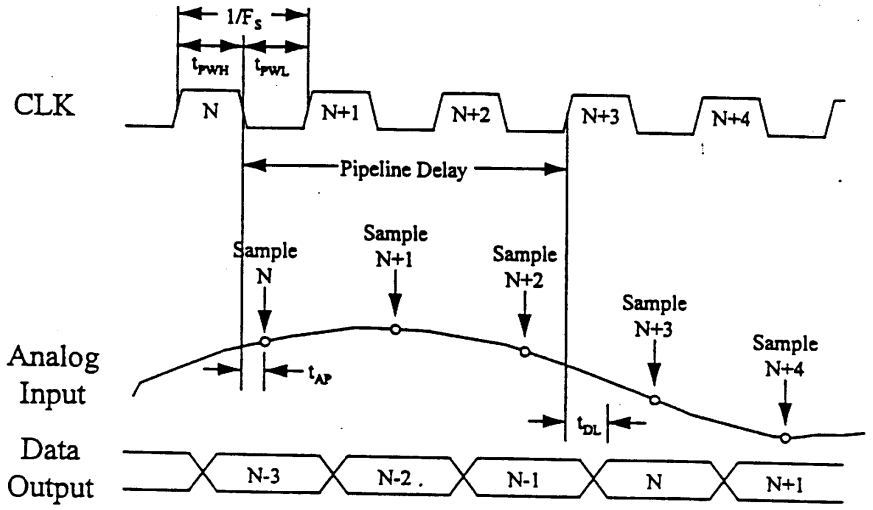
Electrical Characteristics

Unless Otherwise Specified:

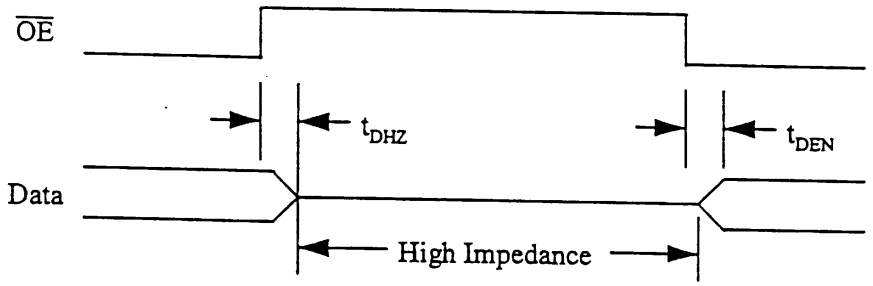
AVDD = DVDD = 5V, FS = 5MHz(50% Duty Cycle),VRT = 4.0V, VRB = 1.0 V, TA = 25℃

Characteristic	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Reference Voltage						
Positive Ref. Voltage	V_{RT}				AV_{DD}	V
Negative Ref. Voltage	V_{RB}		AGND			V
DifferentialRef. Voltage	V_{REF}	$V_{REF} = V_{RT}-V_{RB}$	1.0		AV_{DD}	V
Ladder Resistance	R_L				375	Ω
Ladder Temp. Coefficient	R_{TCO}				2000	Ppm/℃
Top Internal Reference	V_{RTS}	V_{RTS} Connected to V_{RTS}		4		V
Bottom Internal Refence	V_{RBS}	V_{RB} Connected to V_{RTS}		1		V
Accuracy						
Differential Non-linearity	DNL				±0.8	LSB
Integral Non-linearity	INL		-1		+4	LSB
Zero Scale Offset Error	E_{OB}			-20		mV
Full Scale Offset Error	E_{OT}			-40		mV
Power Supplies						
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}				5	V
Current(AV_{DD}, DV_{DD})	I_{DD}			35	40	mA
Analog Input						
Input Voltage Range	V_{IN}		V_{RB}		V_{RT}	V
Input Capacitance Sample	C_{IN}			25		pF
Input Capacitance Convert				5		pF
Aperture Delay	t_{AP}			25		ns
Aperture Uncettainty(jitter)	T_{AJ}			50		ps

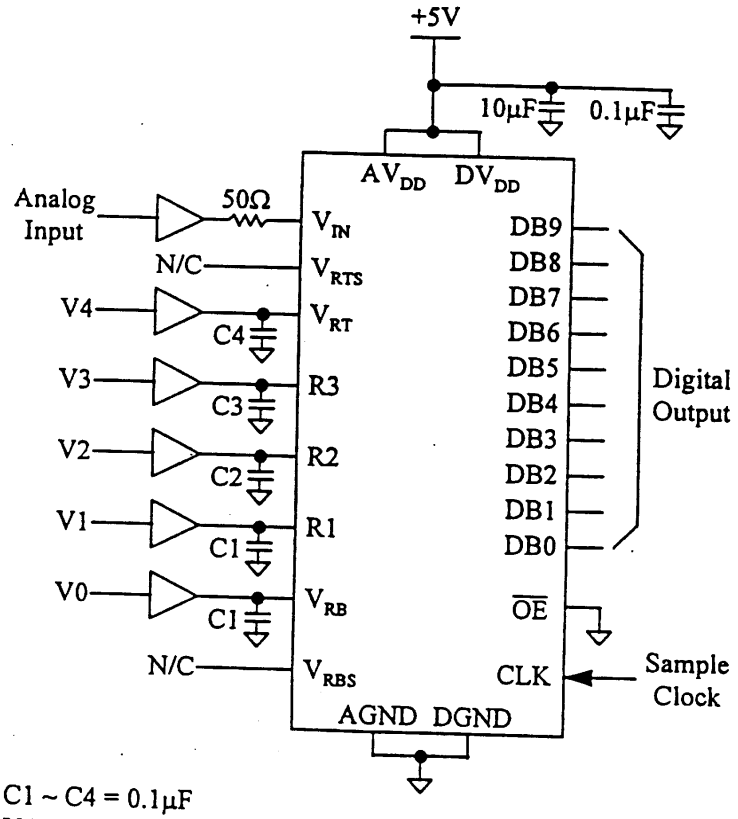
Timing Diagram



Tri-State Timing Diagram



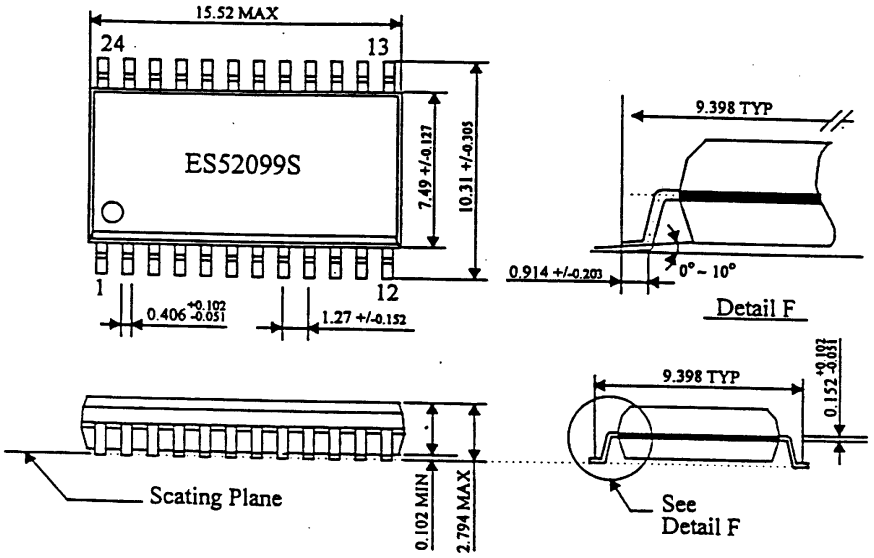
Application Circuit



C1 ~ C4 = 0.1μF
V4 > V3 > V2 > V1 > V0 ≥ GND

Package Outline Unit: mm

ES52099S 24-pin SOP N.B. (Plastic)



ES52099E 24-pin SKINNY DIP (Plastic)