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Error Correction and Non-Switching Power Amplifier Output Stages **Preprint 4492 (M5)**

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Error correction and non-switching power amplifier output stages

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Abstract
A non-switching output stage topology is presented which can control the distribution of signal current in the output transistors. The method is contrasted against more established configurations and the fundamentals of error correction theory reviewed. The technique creates a non-linear current distribution where the distribution law can be controlled and bias current programmed. Circuits are supported with Spice simulations and considerations of overall amplifier topology.

0 Introduction

A wide range of power amplifier topologies exist where error correction strategies can be used to give a local reduction in output-stage distortion. Error correction is essentially a standard feedback/feedforward loop but usually where the circuits are local correction loops placed in close proximity to the output power transistors. The aim is to achieve partial linearization of the output stage by using rapidly acting circuitry which can then prevent broad-band distortion from entering the overall feedback loop.

A brief review of error correction principles is presented and a circuit example given. In addition, an output-stage configuration is described that uses a matched transistor array in conjunction with output current sensing to give tight control of both the output device bias current and dynamic current control under large-signal conditions. The technique is supported by a series of Spice simulations to investigate the output transistor collector current distribution and distortion characteristics. The circuit also allows rapid programming of the quiescent output bias current which in principle can be controlled externally by either an analogue or a digital controller to implement a sophisticated system of dynamic bias. A secondary advantage of the proposed topology is the elimination of the emitter degeneration resistors within the signal path yet retaining predictable and thermally insensitive bias control.

We commence with a review of the basic principles of error correction and describe two established correction methods.

1 Principles of error correction

The conceptual modal for error correction uses both feedforward and feedback and is shown in Figure 1-1. The system consists of a non-linear amplifier N (the main output stage) and an error amplifier with feedback and feedforward transfer functions a and b respectively. The overall transfer function then follows as,

$$G = \frac{N - b(N - 1)}{1 + a(N - 1)} \qquad \ldots 1\text{-}1$$

If the target gain is G_t, then a transfer error function E can be defined as,

$$E = \frac{G}{G_t} - 1 \qquad \ldots 1\text{-}2$$

where substituting for G noting that in this case $G_t = 1$, then

$$E = (N - 1)\frac{1 - a - b}{1 + a(N - 1)} \quad \ldots 1\text{-}3$$

In this example, equation 1-3 shows that the error function E tends to zero when either N = 1 and/or when the numerator contains the relationship,

$$a + b = 1 \quad \ldots 1\text{-}4$$

Equation 1-4 defines the balance condition that enables the overall system to be independent of the non-linear amplifier N. Two extreme cases can be selected which meet the balance condition, i.e. a = 1, b = 0 and a = 0, b = 1. However, when the system of Figure 1-1 is translated into circuitry, these ideals are not necessarily realisable as the transfer function of parameter 'a' must now be selected in association with the frequency dependence of the non-linear stage N such that closed-loop stability is achieved. Even the pure error feedforward correction scheme {a = 0, b = 1} requires the difference amplifier to have infinite bandwidth. In a practical amplifier employing error correction, parameter 'a' is normally selected to achieve both closed-loop stability and high low-frequency distortion reduction and 'b' is aligned according to equation 1-4 to achieve a broad-band distortion null having greater effect at high frequency as 'a' becomes progressively attenuated. The analysis can also include "current dumping [1-5]" where at low frequency error correction is achieved mainly with feedback while at high frequency where the loop gain falls, there is a progressive increase in error feedforward. By balancing feedback and feedforward a broad-band correction amplifier is possible even with a finite loop gain.

To illustrate error correction in a typical power amplifier application, two techniques are shown in the basic circuit of Figure 1-2. Local error feedback correction was first described in [6-8] while differential current-derived feedback (DCDF) was reported more recently [9]. It is assumed that the forward-gain amplifier has a first-order response which allows correct implementation of a DCDF loop where a current sensor detects rate of change of current, while examination of the output stage reveals a classic bias arrangement configured as a local error correction loop [6,8]. Additional work on error correction has also been reported by Sandman [10] and a technique suitable for bridge output stages described under a CMAC [11].

2 Non-switching output stage

The concept of non-switching amplifiers has been reported by Tanaka [12]. However, a circuit technique is presented here that considers the principal operational requirements to both prevent the output transistors from turning off under dynamic conditions and to enable a stable yet programmable output bias current. The technique is useful when it is required to dynamically program the quiescent operating current under real-time signal conditions and also because it gives immunity against thermal drift.

It is fundamental to a class AB non-switching output stage that a non-linear processor is required to both monitor and control the output bias current of each power transistor. The non-linear process must be placed within a local feedback path so that the true bias current can be monitored, yet the correction signals must not distort the main signal path by the injection of non-linear current. Also, if this process is not correctly implemented then non-linear output-current derived feedback can modulate the open-loop output impedance within the crossover region which is in addition to distortion arising from base-emitter and control error voltages. As such, the non-switching bias circuitry although performing its primary function may actually accentuates crossover distortion. We demonstrate how the non-switching control function can be made orthogonal to the main amplification process so as to reduce output impedance modulation in the crossover region.

The method described in this paper achieves a high degree of output stage linearity by current driving the output transistors. For this purpose, bipolar power transistors have been identified[1] that show an extended operating range with a near constant beta. Also, current driving reduces substantially the dependence upon base-emitter voltage non linearity while maintaining the output transistors in an active state reduces beta modulation within the crossover region. Such nonlinearities can otherwise give rise to transient phase effects rather akin to correlated jitter in a digital system.

Consider a transconductance stage of mutual conductance g_m, having an output impedance R_N and driving an output stage with an effective voltage gain A_v with a current gain A_i. The amplifier shown in Figure 2-1 is enclosed within a loop with unity-gain feedback where the closed-loop gain G for a load impedance Z_L is,

$$G = \frac{g_m}{g_m + \frac{1}{A_v R_N} + \frac{1}{A_i Z_L}} \qquad \ldots 2\text{-}1$$

Non linearity in the output stage occurs both within the voltage transfer function A_v and the current transfer function A_i, where in this expression the symmetry should be observed, that is R_N is associated with A_v and Z_L is associated with A_i. However, by making $(A_v R_N) >> (A_i Z_L)$ then dependence on the non linearity $R_N A_v$ is reduced and by choosing power transistors with wide-range beta linearity, overall amplifier linearity is enhanced.

The equation for closed-loop gain G indicates that it is expedient to increase the loop gain by increasing g_m rather than the output-stage current gain A_i as this lowers dependence upon both $A_i Z_L$ and $A_v R_N$. This effect can be quantified by applying the error function defined in equation 1-2, where making G_t the target gain defined when the output resistance of the transconductance stage $R_N = \infty$ then ,

$$E = \frac{\frac{A_i Z_L}{A_v R_N}}{1 + \{A_i g_m\} Z_L + \frac{A_i Z_L}{A_v R_N}} \approx \frac{A_i}{A_v} \frac{1}{\{\gamma R_N\}} \qquad \ldots 2\text{-}2$$

where $\gamma = \{g_m A_i\}$ and for simplification $\gamma Z_L >> \{1 + (A_i Z_L)/(A_v R_N)\}$. If γ is held notionally constant, then the larger the value of g_m the lower is the value of A_i and consequently the lower is the overall distortion. The product $\{\gamma R_N\}$ also represents a distortion reduction factor and should therefore be large. This expedience can reduce output-stage complexity by eliminating the need for error-correction circuitry to compensate for any voltage transfer error in A_v.

To reduce dynamic modulation of the output-stage current gain A_i, an approach is presented which applies a controlled bias voltage to maintain both power transistors of a complementary emitter follower in a state of conduction. However, to prevent the bias control signals from injecting additional distortion then the bias voltage generators should be floating and preferably isolated from the main signal path. In effect, the bias voltage then appears only as a series component in the voltage transfer function of the output stage while the current gain remains unchanged. Consequently, bias voltage modulation can be reduced by following the same argument as that presented above for reducing dependence upon A_v. The conceptual bias

[1] Toshiba power transistors [see Profusion catalogue UK Tel: 01702 543500]

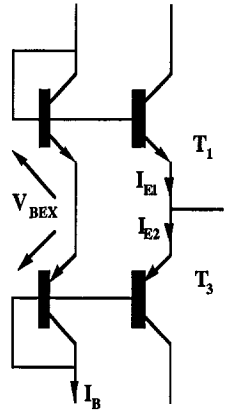
configuration is shown in Figure 2-2 where an imperfectly isolated bias control is assumed to inject a current $2*I_{con}$ into the loop. The design aim is to minimise I_{con} either by using a buffered or isolated driving circuitry or by configuring a differential drive circuit so that no net current enters the loop.

Bias control is derived from two complementary but independent non-linear current mirror stages that sense the respective collector currents of each output transistor, where three example current mirror circuits are shown in Figures 2-3, 2-4, 2-5, designated Type 1, Type 2 and Type 3 respectively. The Type 1 mirror presented in Figure 2-3 uses two pairs of complementary transistors which are individually biased by two controllable current sources and two additional pairs of transistors that simultaneously provide both diode voltage compensation and thermal compensation. The two complementary pairs of transistors are linked via a resistor, where a reference voltage is set by a resistor that also introduces a degree of non-linear regeneration. The input functions to the two non-linear current mirrors are derived independently from the collector currents of the output transistors while the output signals are formed by current sources which feed directly to the bias control circuitry. The functionality of the Type 1 non-linear mirror is described mathematically and then verified by simulation.

Analysis
The analysis is performed with reference to the diagram in Figure 2-3 where the following assumptions are made:

- all transistors have accurate logarithmic conformity
- transistors are parametrically and thermally matched with identical saturation currents, I_S
- all base currents are assumed negligible

Initially, consider part of the Type 1 cell as shown below,



Bias circuit taken from within a Type 1 non-linear current mirror.

where using the diode equation,

$$V_{BE1} = \frac{kT}{q} \ln\left[\frac{I_{E1}}{I_s}\right]$$

$$V_{BE3} = \frac{kT}{q} \ln\left[\frac{I_{E3}}{I_s}\right]$$

$$V_{BEX} = \frac{kT}{q} \ln\left[\frac{I_{EB}}{I_s}\right]$$

where k is Boltzman's constant, T is the junction temperature in degrees absolute and q is the charge on an electron.

From the bias circuit illustrated, $V_{BE1} + V_{BE2} = 2\,V_{BEX}$ giving

$$\frac{kT}{q} \ln\left[\frac{I_{E1}}{I_s}\right] + \frac{kT}{q} \ln\left[\frac{I_{E3}}{I_s}\right] = \frac{2kT}{q} \ln\left[\frac{I_{EB}}{I_s}\right]$$

which reduces to,

$$I_{E1}\, I_{E3} = I_B^2 \qquad \ldots 2\text{-}3$$

Observing the circuit symmetry in Figure 2-3 it follows that $I_{E1} = I_{E4}$ and $I_{E2} = I_{E3}$ and applying Kirchhoff' voltage law,

$$-(I_B + I_{E2})R_2 - V_{BE1} - (I_{E1} - I_{E3})R_1 + V_{BE2} + (I_X + I_B)R_0 = 0$$

but, $V_{BE2} - V_{BE1} = \frac{kT}{q} \ln\left[\frac{I_{E2}}{I_{E1}}\right]$ and $I_{E2} = I_{E3} = I_Y$ therefore

$$I_{E1} = \frac{I_B^2}{I_{E3}} = \frac{I_B^2}{I_Y} \text{ yielding } V_{BE2} - V_{BE1} = \frac{2kT}{q} \ln\left[\frac{I_Y}{I_B}\right]$$

Substituting for (V_{BE2} - V_{BE1}), I_{E1}, I_{E2} and I_{E3} gives,

$$(I_B + I_Y)R_2 - \frac{2kT}{q} \ln\left[\frac{I_Y}{I_B}\right] + \left(\frac{I_B^2}{I_Y} - I_Y\right)R_1 = (I_X + I_B)R_0$$

whereby,

$$I_X = I_B\left(\frac{R_2}{R_0} - 1\right) + I_Y\left(\frac{R_2 - R_1}{R_0}\right) + \frac{I_B^2}{I_Y}\frac{R_1}{R_0} + \frac{2kT}{qR_0} \ln\left(\frac{I_B}{I_Y}\right) \qquad \ldots 2\text{-}4$$

Make $R_1 = R_2$, then

$$I_X = I_B\left(\frac{R_1}{R_0} - 1\right) + \frac{I_B^2}{I_Y}\frac{R_1}{R_0} + \frac{2kT}{qR_0} \ln\left[\frac{I_B}{I_Y}\right] \qquad \ldots 2\text{-}5$$

Figure 2-6 shows a plot of I_Y against I_X derived for various I_B. The function is approximately an inverse relationship revealing a rapid increase in I_Y as I_X is reduced in value. An intrinsic characteristic of the non-linear current mirrors is their rapid increase in output current with a reduction in output transistor collector current, while an increase in output transistor collector current causes the output current to approach zero.

The current mirrors of Figure 2-3 can be simplified to Type 2 and then to Type 3 and are shown in Figures 2-4, 2-5 respectively, where the Type 3 mirror uses only a grounded-base stage and a thermally compensated bias network.

3 Output stage circuitry for non switching applications

To form a complete dynamic bias circuit, two complementary non-linear current mirrors are configured as shown in Figure 3-1. To achieve current isolation and prevent output impedance modulation in the crossover region, the currents are initially converted into voltages and then a unity-gain, voltage-controlled voltage source (VCVS) with a floating output drives directly the transistor bases. To complete the output-stage, a unity-gain current-feedback loop [13] is employed that uses a complementary input stage driving a linear current mirror with overall output-voltage derived current feedback.

The overall circuit can be explained by first considering its operation in the quiescent state where the output current is zero. If the quiescent current decreases, then the output currents of both non-linear current mirrors will increase which causes a reduction in the bias voltage applied to the output transistors while if the output current increases then the converse is true. At the quiescent operating point, the loop gain within this compensation circuitry is such that good bias stability is achieved and the bias circuitry in each non-linear current mirror provides thermal compensation.

However, when an output current flows to the amplifier load, the output transistor that experiences a reduction in current now causes a disproportionate increase in the bias voltage in what is effectively a current-feedback loop and because of the non-linear law there is effectively an increase in loop gain such that the current in the transistor stabilises at a value > 0 A. Of course, the other transistor has to provide the output current so its value increases above the quiescent value.

Figure 3-2 presents a circuit to illustrate a possible configuration for a VCVS as used in Figure 3-1. The two transistors act in a similar way to amplified diodes but their bases are driven indirectly from the output of the two complementary non-linear current mirrors and thus respond to the output stage bias/signal currents. The additional bias transistor should have a high beta so that significant base current does not enter the feedback loop and thus modulate the output stage impedance. An alternative arrangement is to use complementary JFETs as these give much better gate to drain isolation. A Type 3 current mirror example is shown in Figure 3-3 where the JFETs operate in their triode mode, acting more like voltage-controlled resistors. A further advantage of the JFET circuit is the auto-bias characteristic which eliminates the need for current source biasing, however it is necessary to select devices with a sufficiently high I_{DSS} to meet the peak current demand.

For the simulations of the circuit in Figure 3-2(right), the output-stage quiescent bias current was controlled directly by setting the bias current of the non-linear transconductance stage. In Figure 3-5 the law of control current versus output stage quiescent bias current is shown. This result is achieved applying a dc + triangular waveform bias control current I_B and then monitoring the quiescent bias current in each output transistors, where

$$I_B = 1\ mA + 0.5\ mA\ (pk-to-pk\ triangular\ wave)$$

This result shows that the bias circuitry is capable of rapid control of the output transistor collector currents such they remain in a state of conduction, the triangular wave also demonstrates the good linearity of the bias control current I_B to output-transistor quiescent bias current offered by this technique.

To demonstrate the validity of the circuit concept in Figure 3-2, two sets of simulations are shown in Figures 3-4(a,b) to demonstrate the current distribution in each power output transistor. The simulation presented in Figure 3-4a has a quiescent bias current of ≈ 300 mA while in Figure 3-4b it is ≈ 130 mA. It will be noted that the "span" that is {quiescent current - minimum current} of the collector currents below the quiescent value is the same in both cases. The span is determined by the current-gain characteristic of each non-linear current mirror and is adjusted for example by the resistor R_1 in Figure 2-3. However, it should be observed that with the specific configurations of the Type 1, 2 and 3 mirrors, that the span remains constant as the bias current is programmed, where it is important to make the minimum current greater than zero for true non switching action. More complicated scenarios can be envisaged where the span is effectively modulated by making the bias control current a function of the amplifier's output current demand.

Finally, to demonstrate the low non-linear distortion of this arrangement, the overall input-output error voltage is shown in Figure 3-7 for an input signal of 30 volt peak amplitude and a frequency of 10 kHz.

4 Enhanced loop transconductance

To increase the loop gain of the amplifier and thus lower both distortion and output impedance, the second stage can be designed to have a larger transconductance. Two methods of implementation are reported:

4-1 Positive feedback

Figure 4-1 shows a method of increasing the transconductance of the second stage of the amplifier loop by using positive feedback. The drive to the output transistors is formed from two weighted paths where a fraction of this drive current is combined with the input to the second stage. By choosing the weighting, a range of transconductance can be selected approaching infinity.

4-2 Negative feedback

Figure 4-2 shows a similar arrangement but where the second stage is now formed using two pairs of complementary transistors in a dc-coupled pair configuration. This circuit is appropriate where class A driving is used and the second stage of the amplifier needs both high transconductance and a high bias current.

5 Conclusion

This paper has reviewed the basic techniques of error correction with an orientation towards analogue audio power amplifier output stages. Of particular interest is a technique for both actively controlling the quiescent bias current where an approach was described that enabled rapid programming of the instantaneous bias current. The technique employed a non-linear current mirror that was external and in addition to the main output stage feedback loop, the non-linear current mirrors were subdivided into 3 types. This secondary loop effectively monitored the output transistor currents and controlled their bias so to prevent turn off. As such, conduction is always ensured and consequently modulation of power transistor beta is reduced. The bias circuit also enables a good approximation to class A operation to be achieved under low output signal conditions with a near symmetrical current distribution between the output transistors.

Only the output-stage design was considered where either additional circuitry can be added to give both voltage gain and enhanced overall feedback or a separate voltage

amplifier unity-gain output stage [14] can be followed. Section 4 presented two methods for increasing the loop gain while maintaining current drive directly to the output transistors. Overall, the approach should find application in systems requiring improved bias stability and also where the operating point is to be modulated in accordance with some designer selected function.

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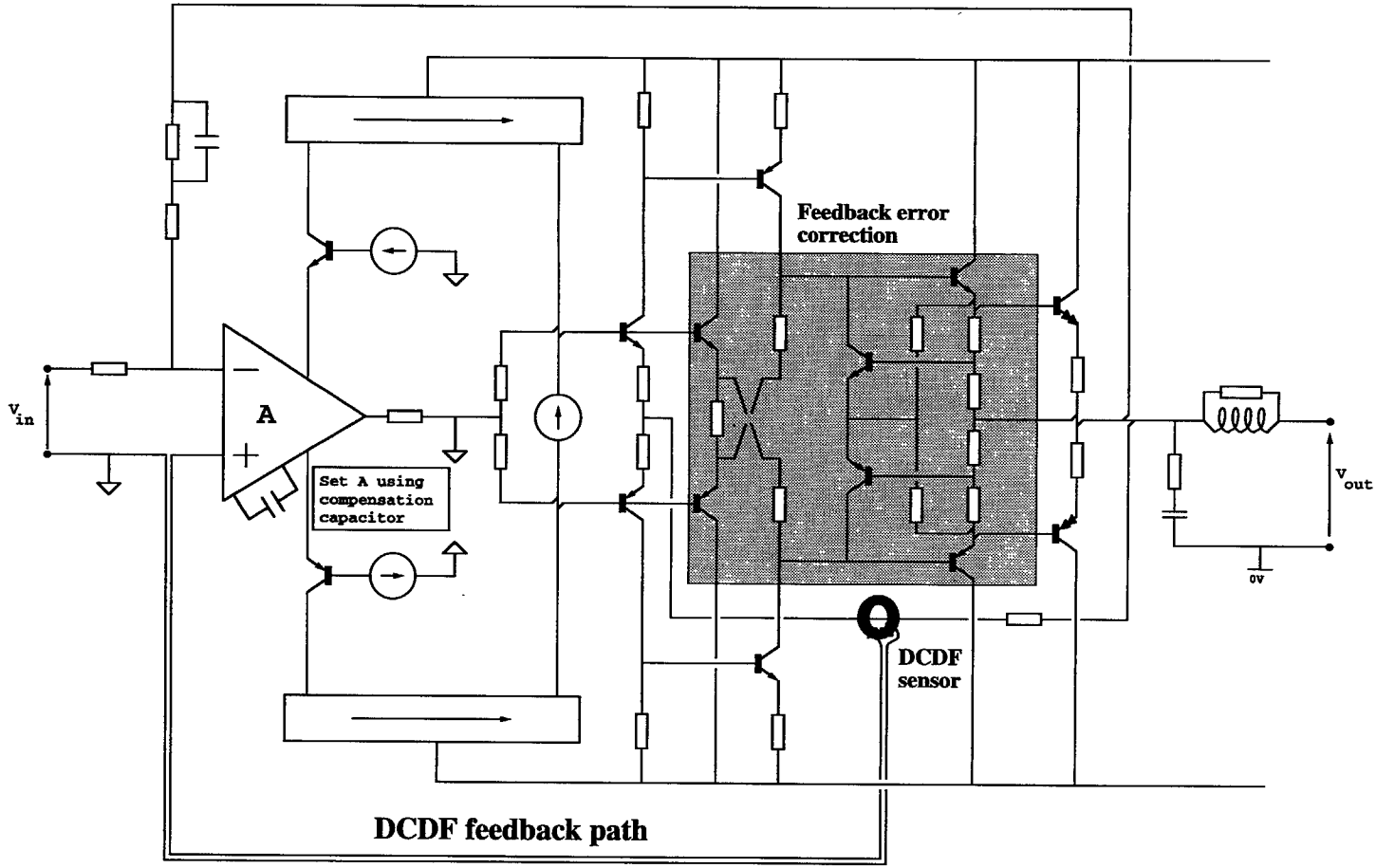

Figure 1-2 Power amplifier with feedback error-correction and DCDF.

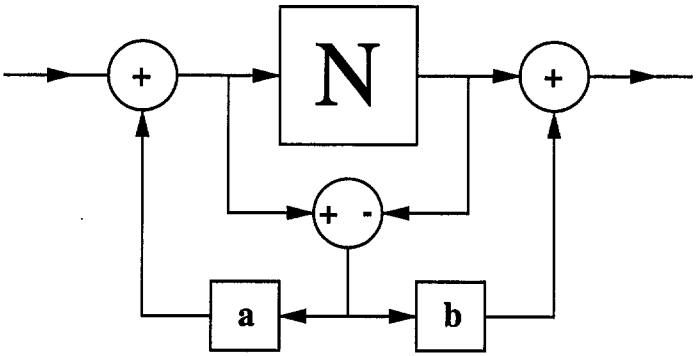

Figure 1-1 Conceptual error feedback-feedforward correction system.

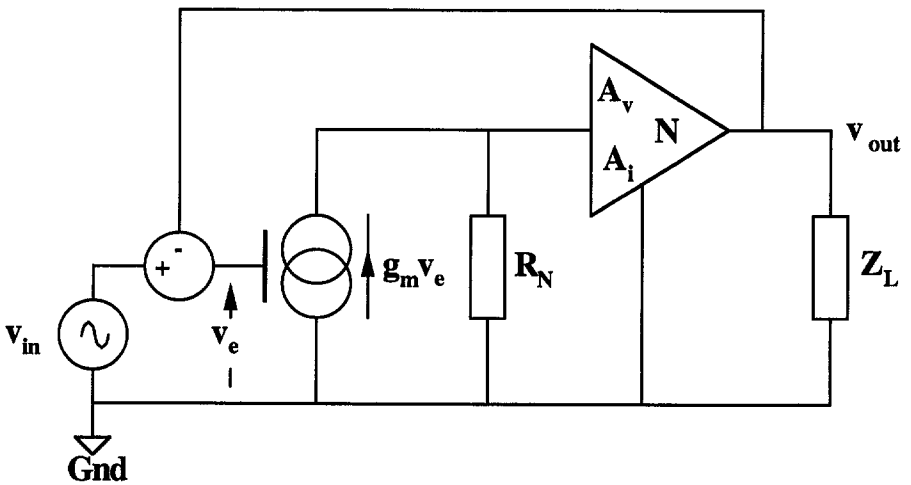

Figure 2-1 Negative feeedback loop with transconductance input stage.

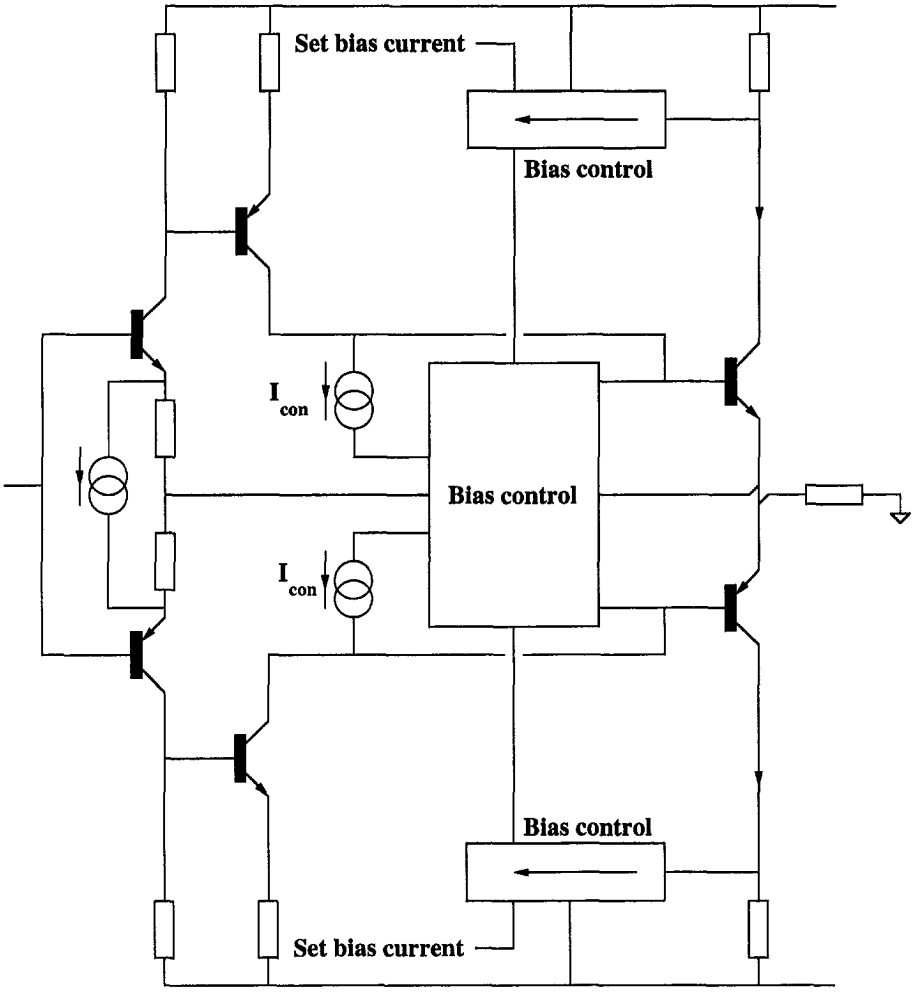

Figure 2-2 Basic bias control system showing control current injection.

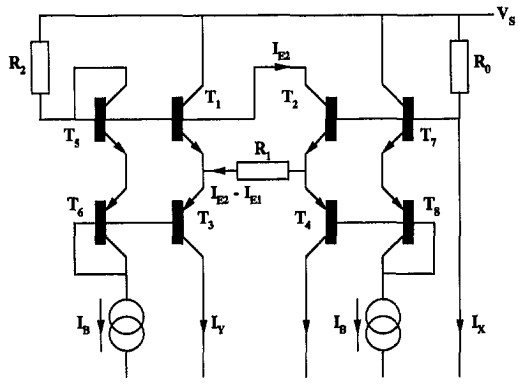

Figure 2-3 Type 1 nonlinear current mirror.

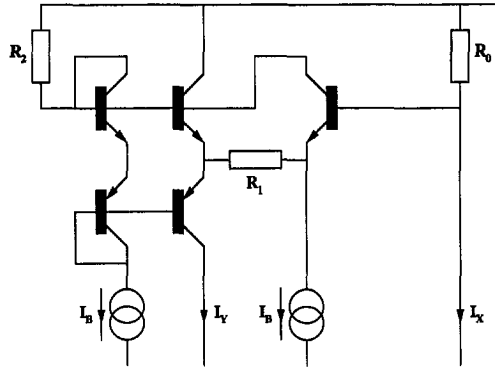

Figure 2-4 Type 2 nonlinear current mirror.

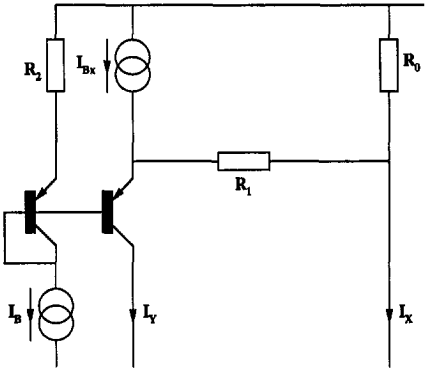

Figure 2-5 Type 3 nonlinear current mirror.

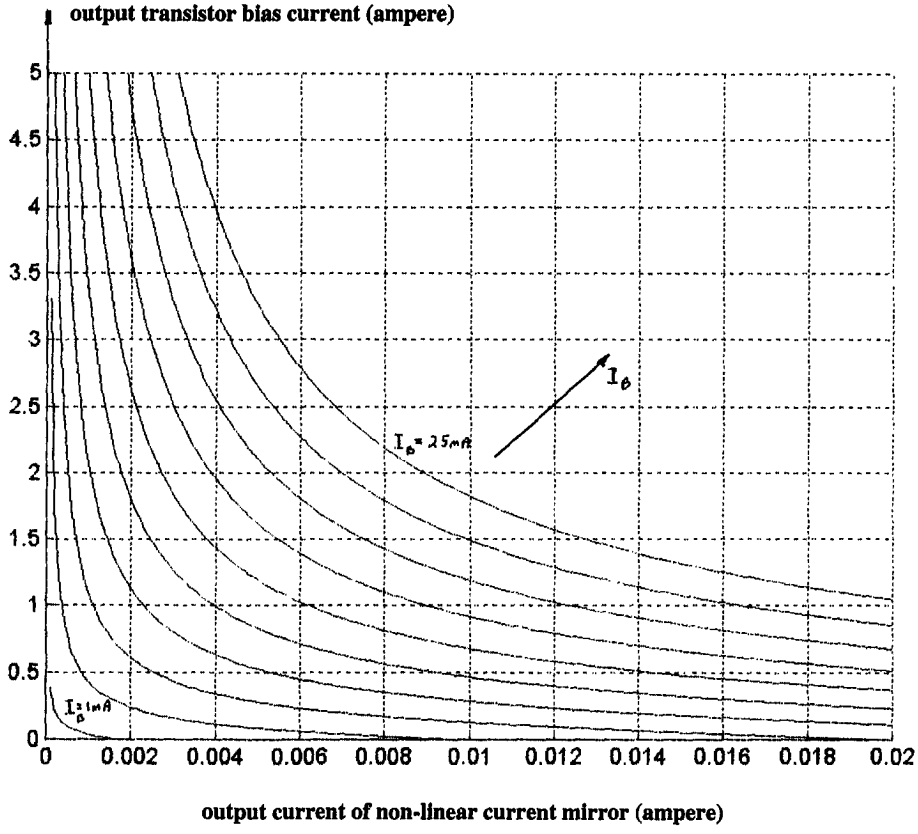

Figure 2-6 Type 1: Contours of I_X against I_Y for I_B in a range 1 mA to 25 mA.

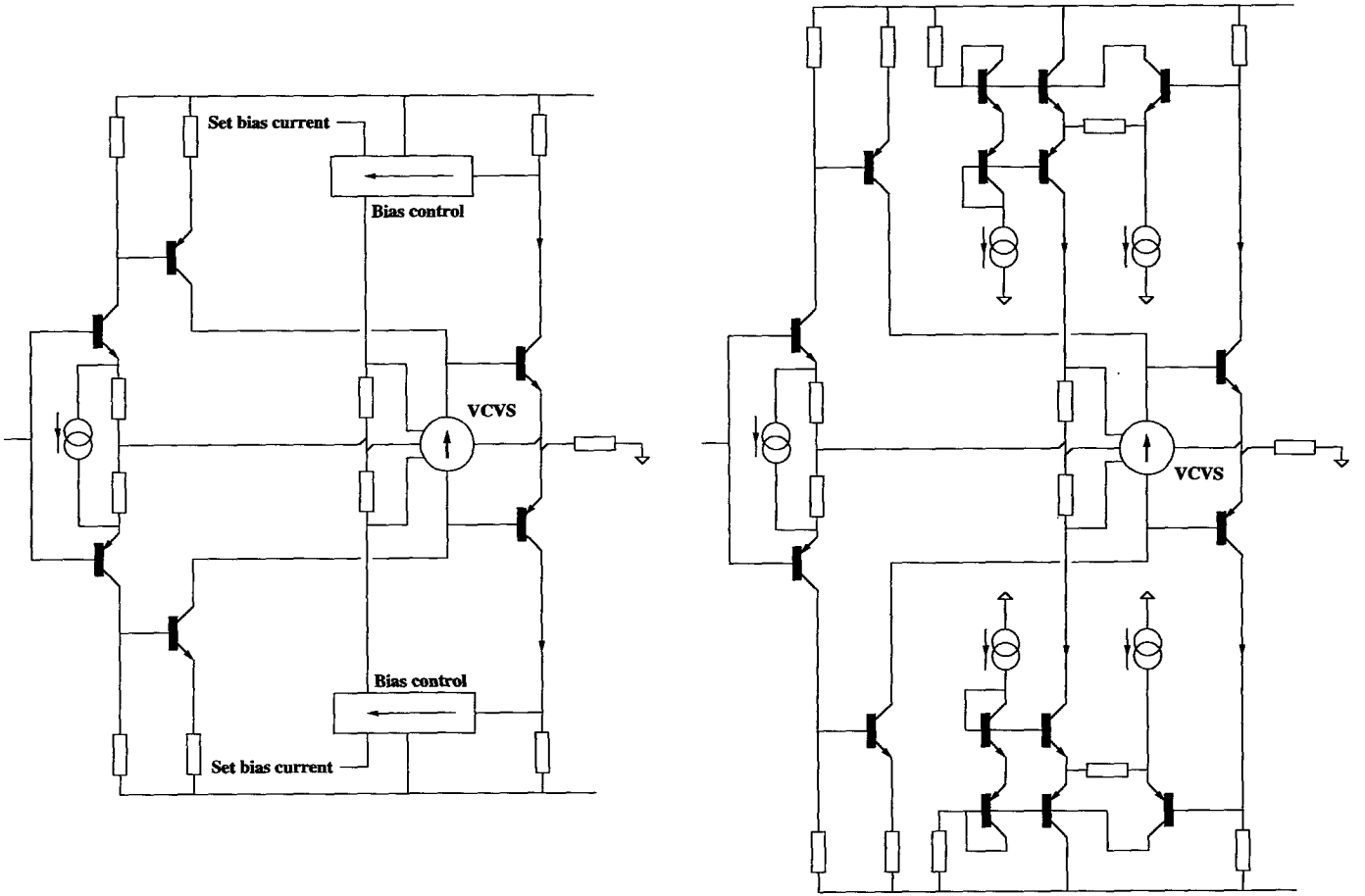

Figure 3-1 Bias system using VCVS stage to isolate control current.

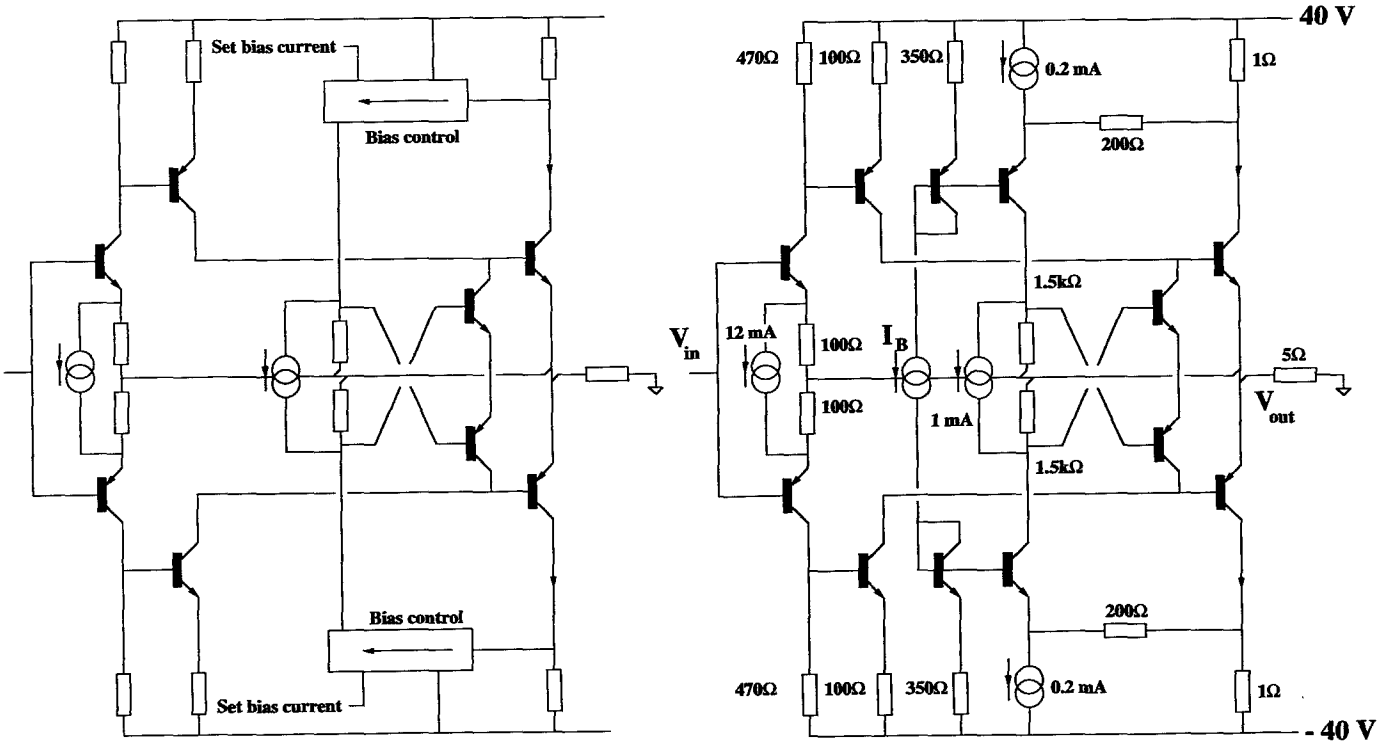

Figure 3-2 Type 3 current mirror with bipolar VCVS bias control.

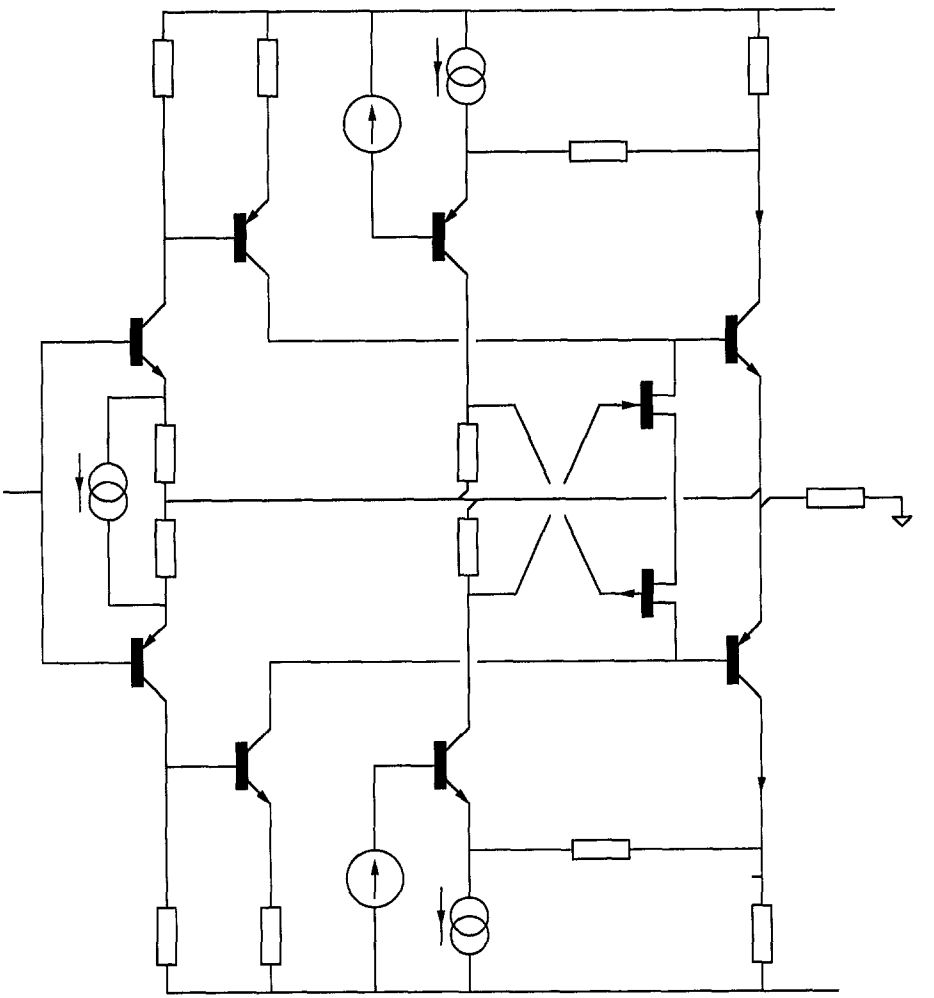

Figure 3-3 Type 3 current mirror with JFET VCVS bias control.

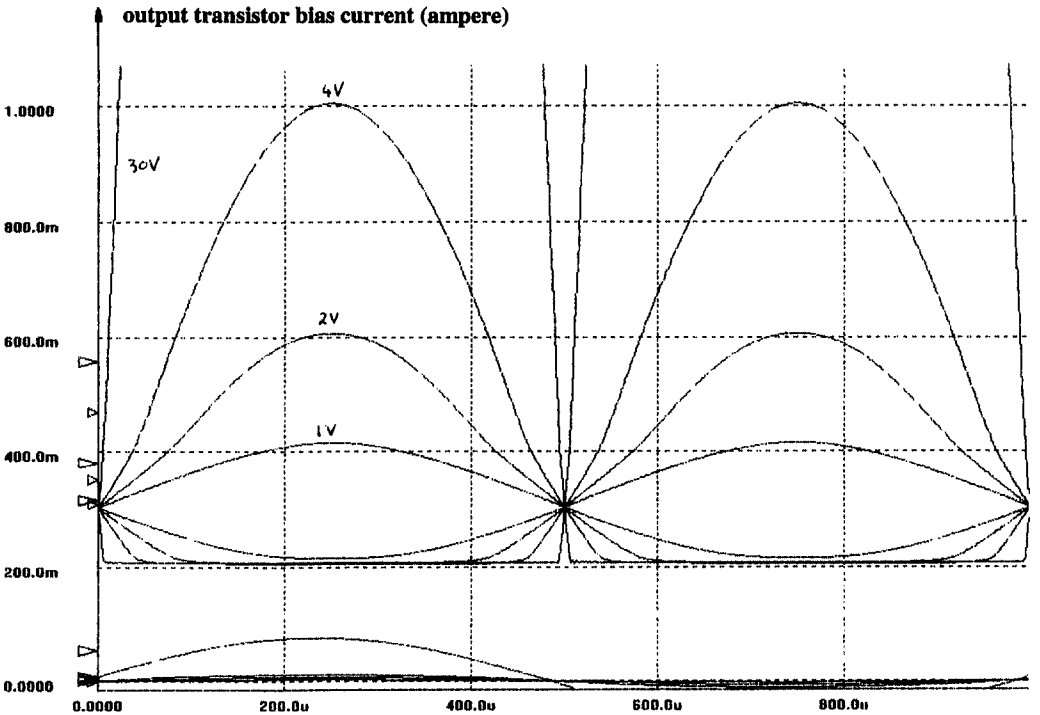

Figure 3-4a Output-transistor current distribution I_B = 1 mA, re-Figure 3-2.

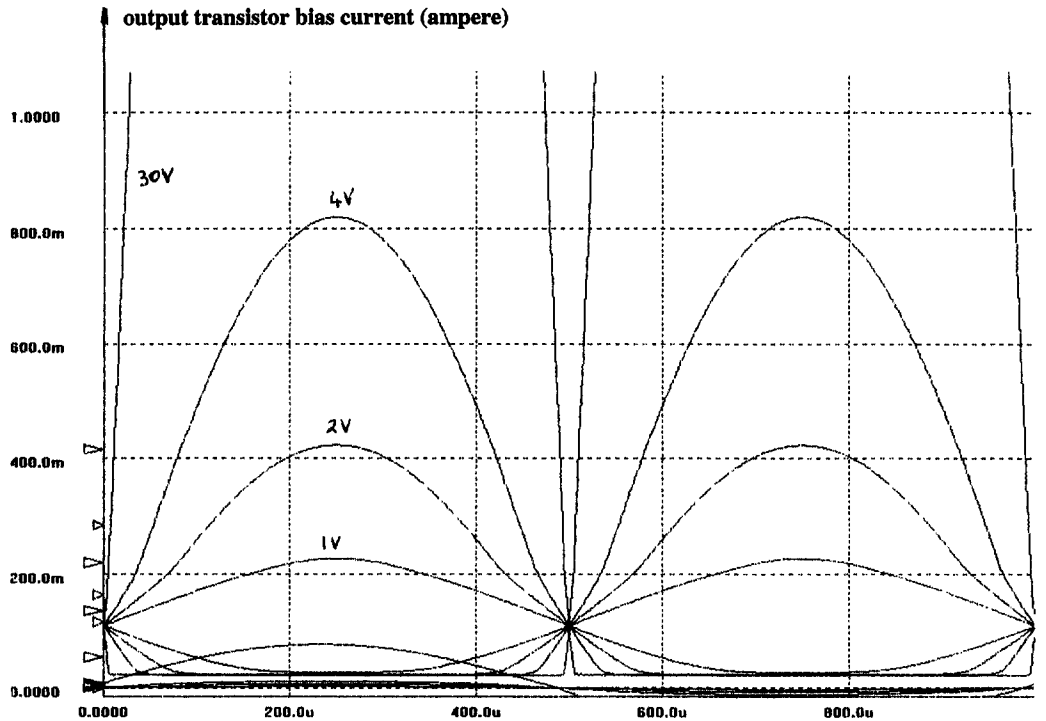

Figure 3-4b Output-transistor current distribution I_B = 0.5 mA, re-Figure 3-2.

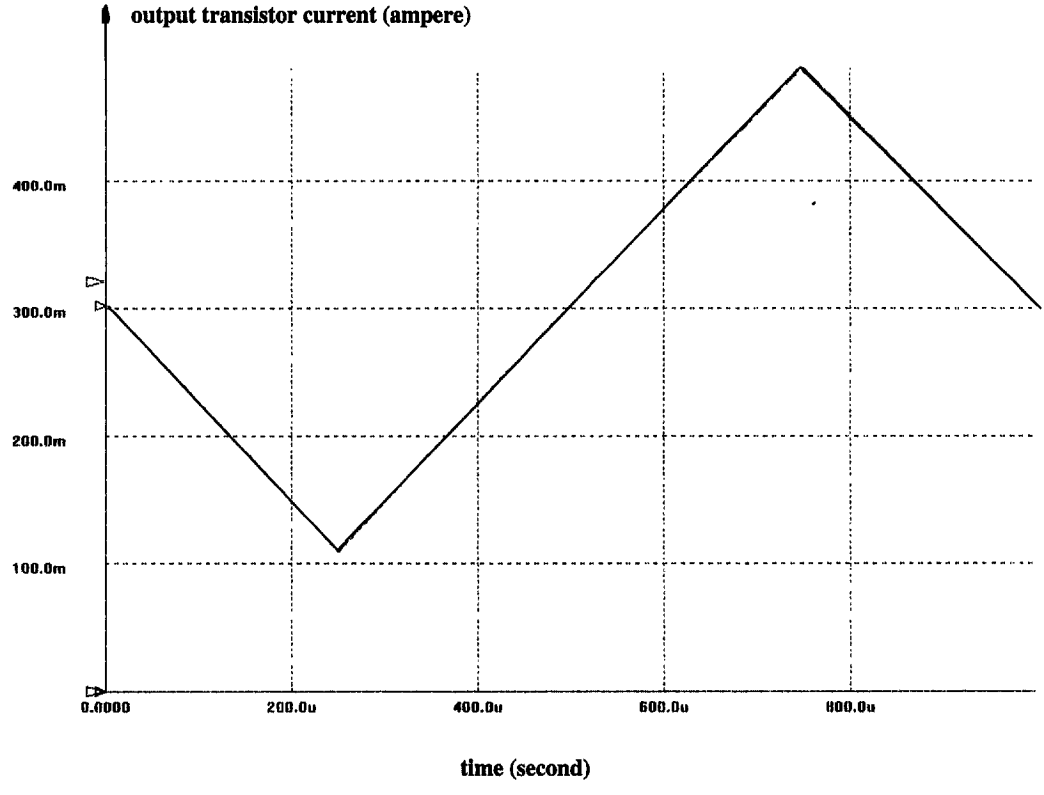

Figure 3-5 Quiescent output-bias current versus time-varying I_B, re-Figure 3-2.

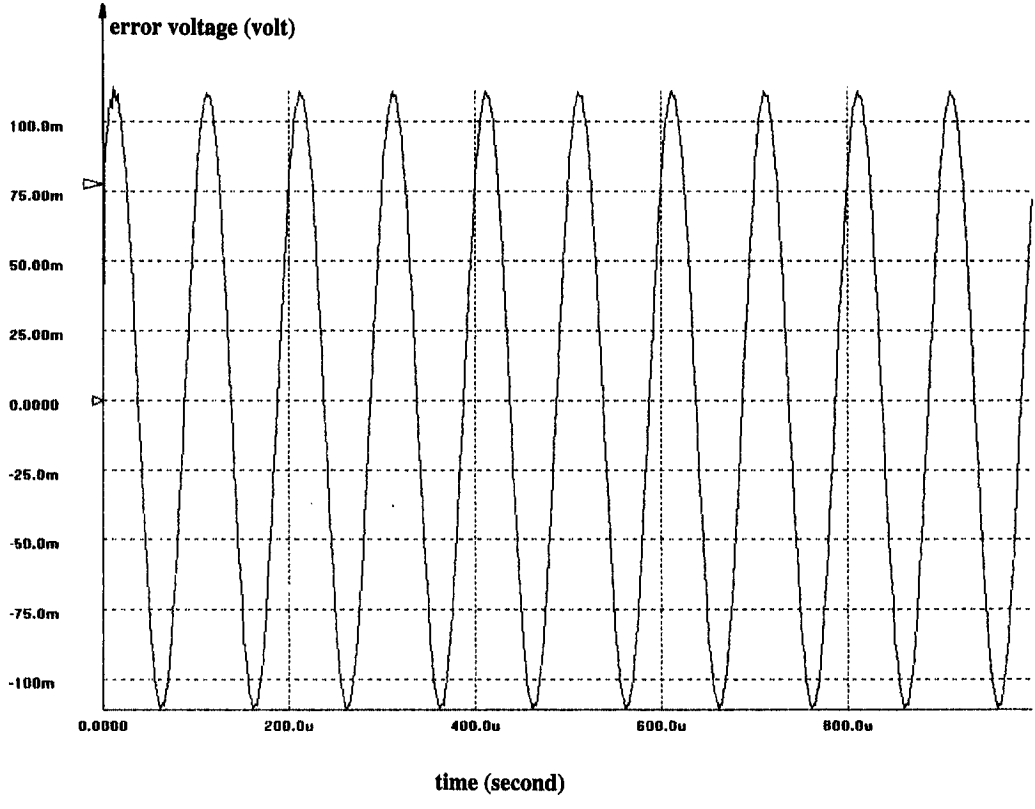

Figure 3-6 Input-output error voltage, V_{in} = 30 V @ 10 kHz, re-Figure 3-2.

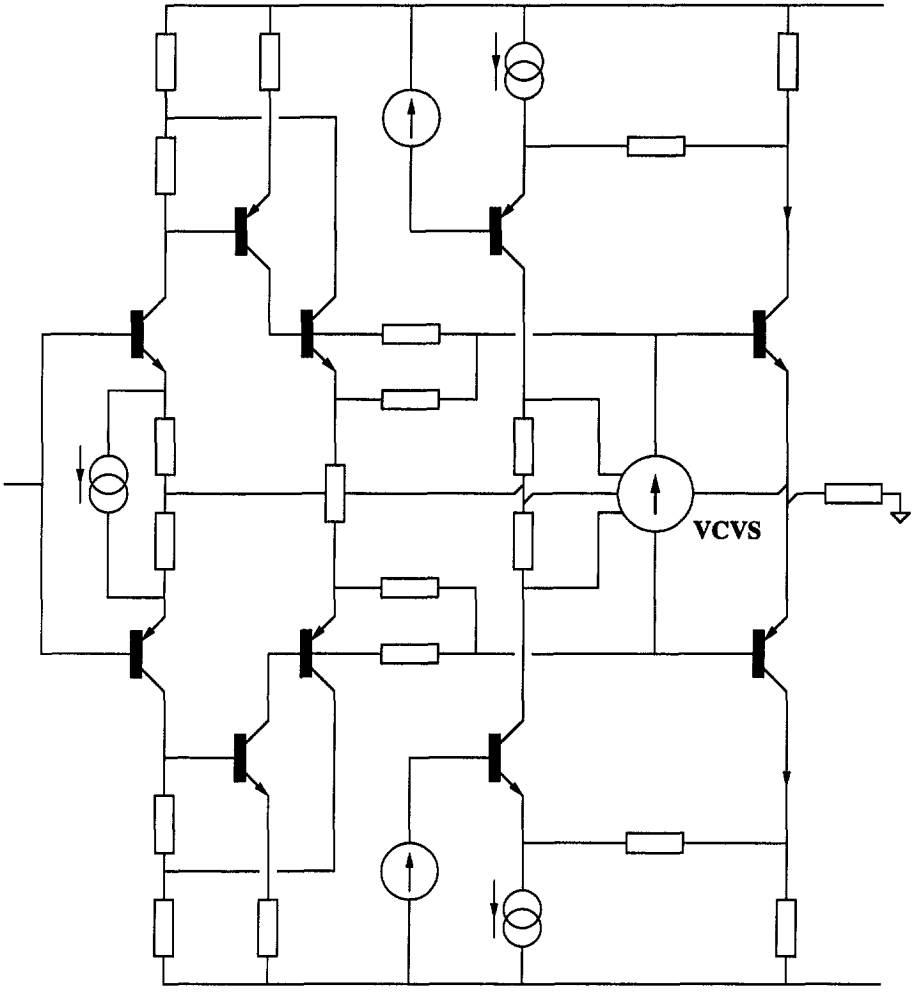

Figure 4-1 Positive feedback: Current drive of output transistors .

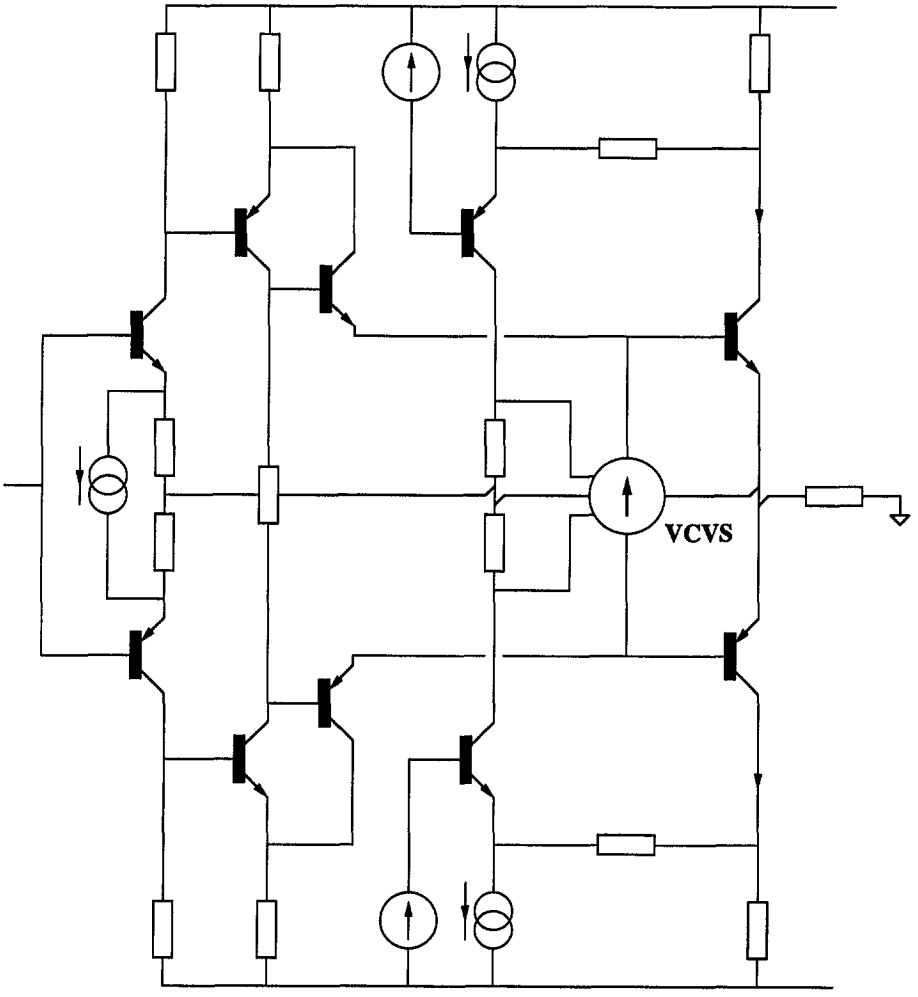

Figure 4-2 Negative feedback: Current drive of output transistors .