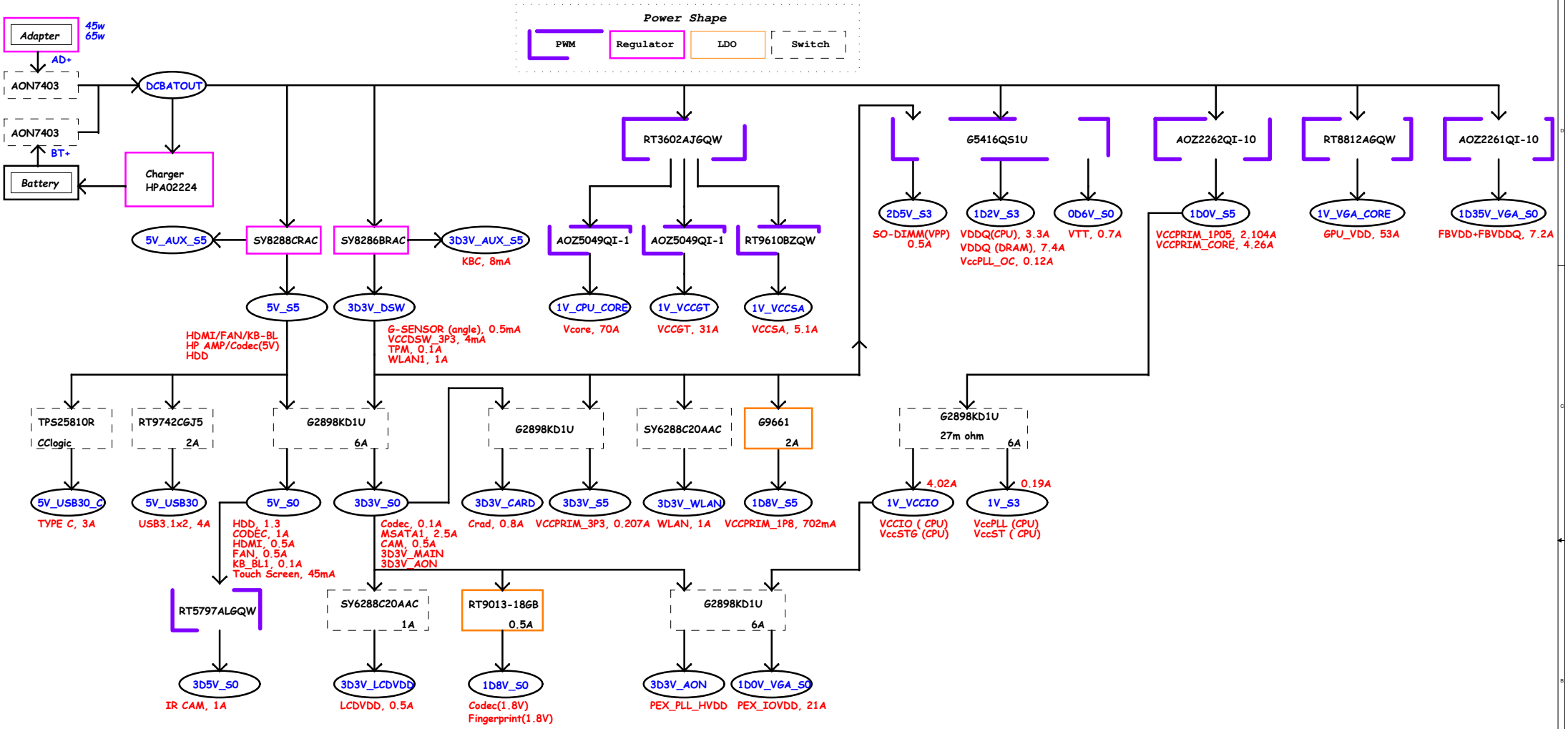

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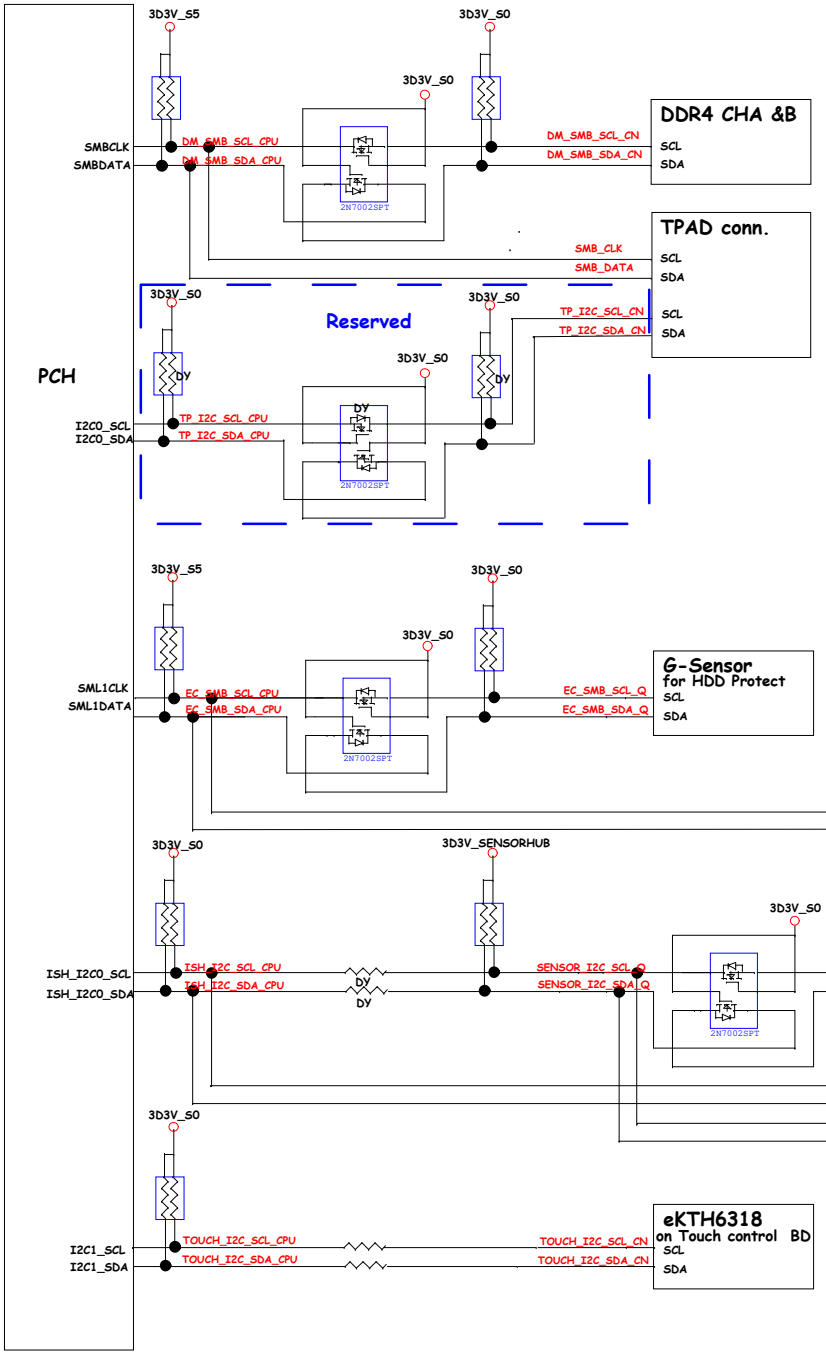
Title: Power Block Diagram

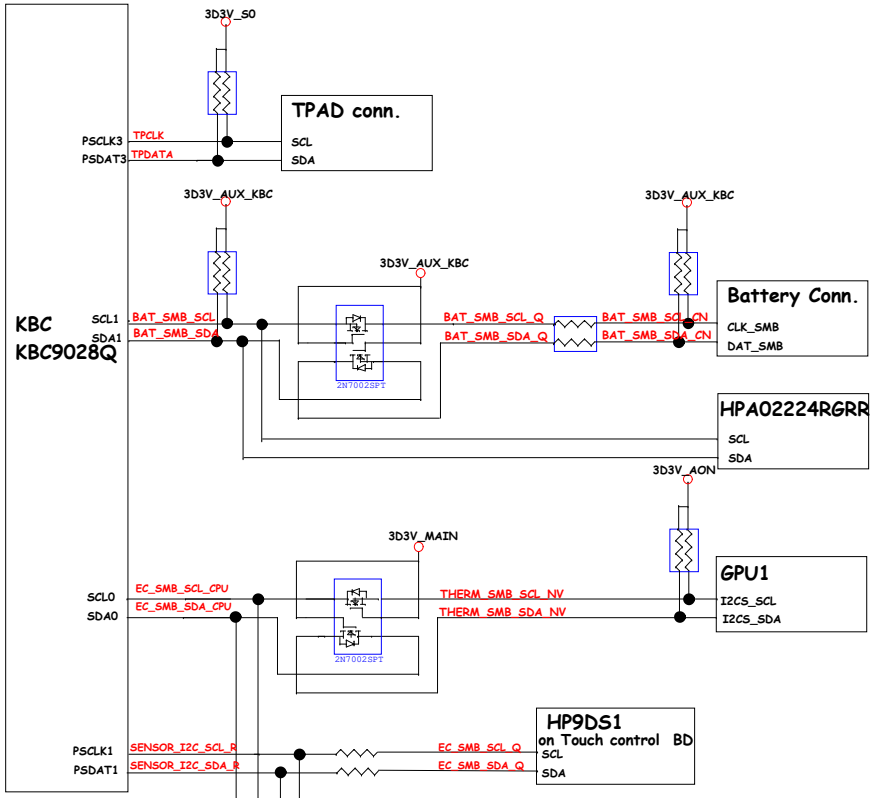
Size	Document Number	Rev
A2	FAROE 14" Pavilion	SA

Date: Monday, August 06, 2018 Sheet 103 of 106

PCH SMBus/ I2C Block Diagram



KBC SMBus/ I2C Block Diagram



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Title: SMBUS/I2C BLOCK DIAGRAM

Size: A2 | Document Number: FAROE 14" Pavilion | Rev: SA

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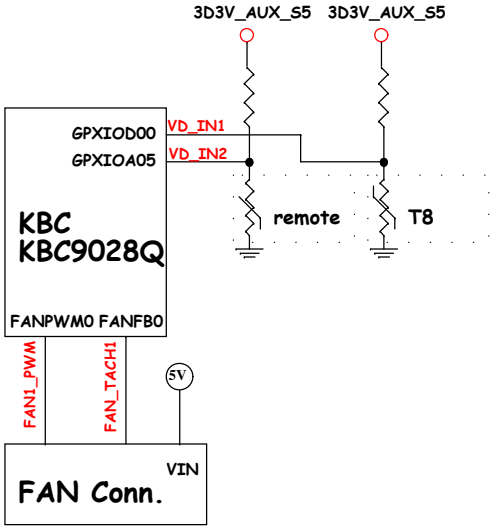
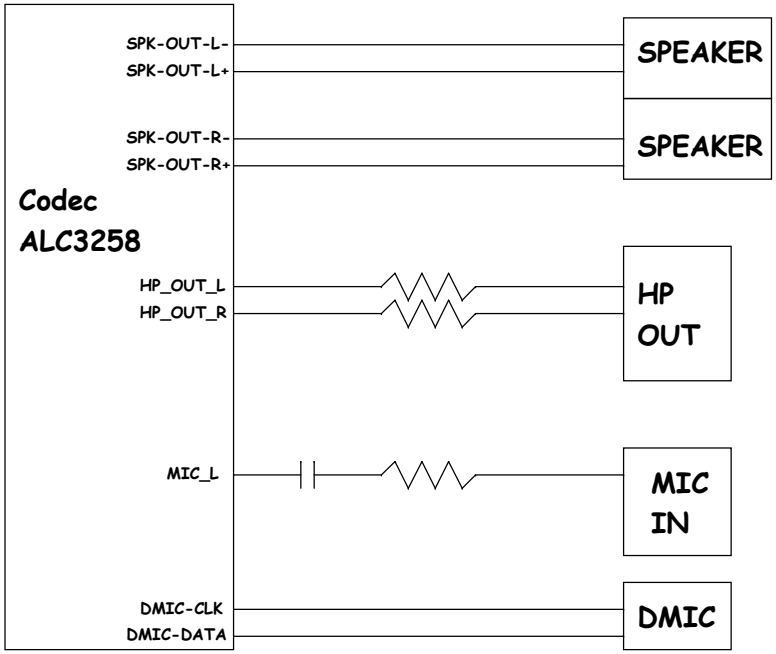
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

Size	Document Number	Rev
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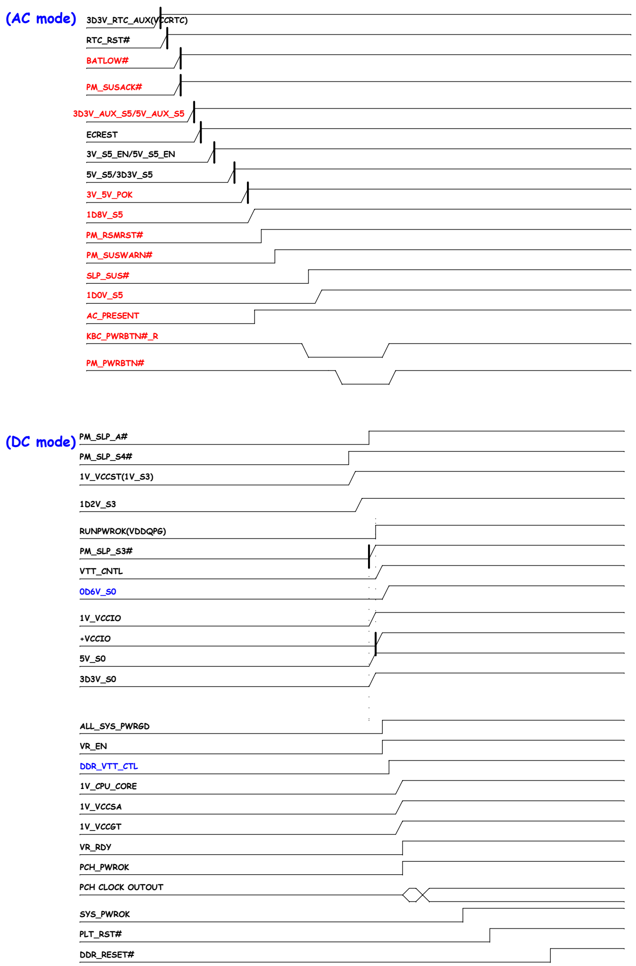
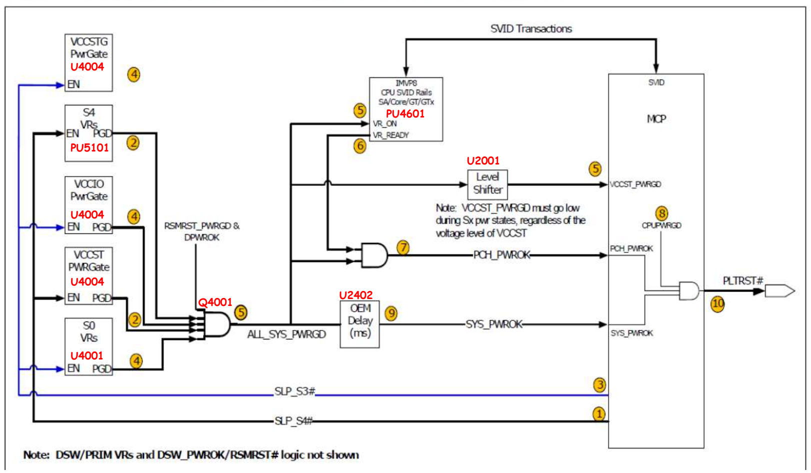
Intel-Power Up Sequence



(AC mode)
3D3V_RTC_AUX(VCCRTC)
RTC_RST#
BATLOW#
PM_SUSACK#
3D3V_AUX_S5/5V_AUX_S5
ECREST
3V_S5_EN/5V_S5_EN
5V_S5/3D3V_S5
3V_5V_POK
1D8V_S5
PM_RSMRST#
PM_SUSWARN#
SLP_SUS#
1D0V_S5
AC_PRESENT
KBC_PWRBTN#_R
PM_PWRBTN#
(DC mode)
PM_SLP_A#
PM_SLP_S4#
1V_VCCST(1V_S3)
1D2V_S3
RUNPWROK(VDDQPG)
PM_SLP_S3#
VTT_CNTL
0D6V_S0
1V_VCCIO
+VCCIO
5V_S0
3D3V_S0
ALL_SYS_PWRGD
VR_EN
DDR_VTT_CTL
1V_CPU_CORE
1V_VCCSA
1V_VCCGT
VR_RDY
PCH_PWROK
PCH CLOCK OUTOUT
SYS_PWROK
PLT_RST#
DDR_RESET#

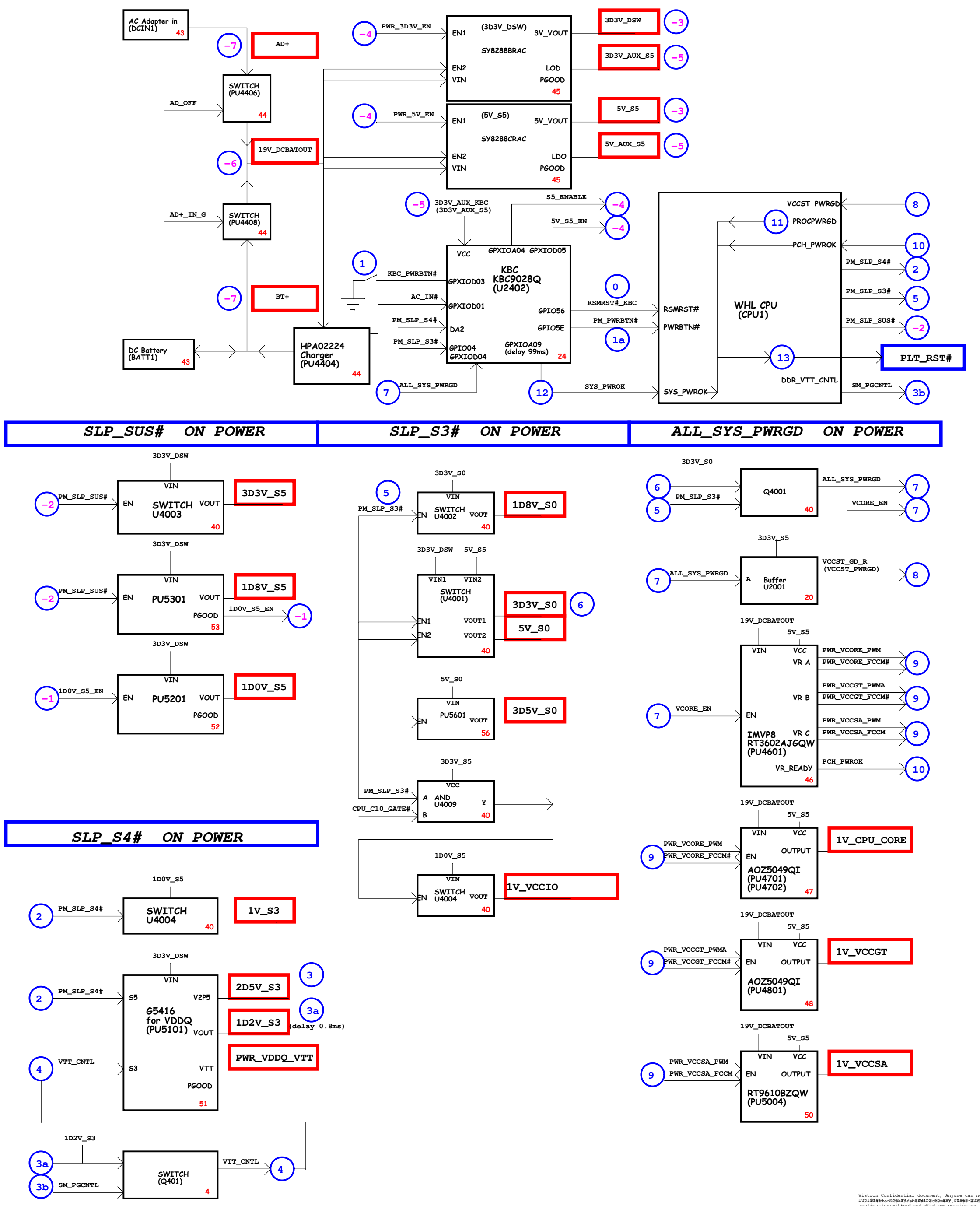
#575412 Rev0.8 P.557

Figure 12-17.WHL U (Volume) PWROK Generation Flow Diagram



SVID Transactions
VCCSTG PwrGate U4004 EN
S4 VRs EN PGD PU5101
VCCIO PwrGate U4004 EN PGD
VCCST PWRGate U4004 EN PGD
S0 VRs U4001 EN PGD
RSMRST_PWRGD & DPWROK
Q4001
ALL_SYS_PWRGD
IMVP8 CPU SVID Rails SA/Core/GT/GTx PU4601 VR_ON VR_READY
U2001 Level Shifter
Note: VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
PCH_PWROK
U2402 OEM Delay (ms)
SYS_PWROK
SVID
MCP
VCCST_PWRGD
CPUPWRGD
PCH_PWROK
SYS_PWROK
PLTRST#
SLP_S3#
SLP_S4#
Note: DSW/PRIM VRs and DSW_PWROK/RSMRST# logic not shown

WHL U POWER UP SEQUENCE DIAGRAM



AC Adapter in (DCIN1)
SWITCH (PU4406)
AD_OFF
AD+
19V_DCBATOUT
SWITCH (PU4408)
AD+_IN_G
BT+
DC Battery (BATT1)
HPA02224 Charger (PU4404)
(3D3V_DSW) SY8288BRAC
PWR_3D3V_EN
3D3V_DSW
3D3V_AUX_S5
(5V_S5) SY8288CRAC
PWR_5V_EN
5V_S5
5V_AUX_S5
3D3V_AUX_KBC (3D3V_AUX_S5)
S5_ENABLE
5V_S5_EN
KBC KBC9028Q (U2402)
KBC_PWRBTN#
AC_IN#
PM_SLP_S4#
PM_SLP_S3#
ALL_SYS_PWRGD
RSMRST#_KBC
PM_PWRBTN#
SYS_PWROK
WHL CPU (CPU1)
VCCST_PWRGD
PROCPWRGD
PCH_PWROK
PM_SLP_S4#
PM_SLP_S3#
PM_SLP_SUS#
PLT_RST#
DDR_VTT_CNTL
SM_PGCNTL
SLP_SUS# ON POWER
SLP_S3# ON POWER
ALL_SYS_PWRGD ON POWER
SWITCH U4003
3D3V_S5
PU5301
1D8V_S5
1D0V_S5_EN
PU5201
1D0V_S5
SWITCH U4002
1D8V_S0
SWITCH (U4001)
3D3V_S0
5V_S0
PU5601
3D5V_S0
AND U4009
CPU_C10_GATE#
SWITCH U4004
1V_VCCIO
Q4001
VCORE_EN
Buffer U2001
VCCST_GD_R (VCCST_PWRGD)
IMVP8 RT3602AJGQW (PU4601)
PWR_VCORE_PWM
PWR_VCORE_FCCM#
PWR_VCCGT_PWMA
PWR_VCCGT_FCCM#
PWR_VCCSA_PWM
PWR_VCCSA_FCCM
PCH_PWROK
VR_READY
AOZ5049QI (PU4701) (PU4702)
1V_CPU_CORE
AOZ5049QI (PU4801)
1V_VCCGT
RT9610BZQW (PU5004)
1V_VCCSA
SLP_S4# ON POWER
SWITCH U4004
1V_S3
G5416 for VDDQ (PU5101)
2D5V_S3
1D2V_S3
(delay 0.8ms)
PWR_VDDQ_VTT
VTT_CNTL
SWITCH (Q401)
SM_PGCNTL

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Title: **Power Sequence**

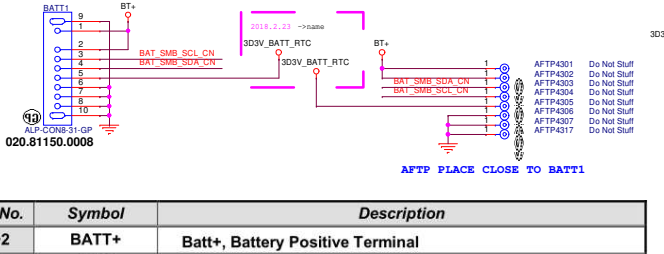
Document Number: **FAROE 14" Pavilion**

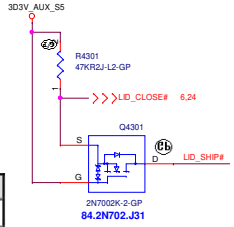
Rev: SA

Size: A1

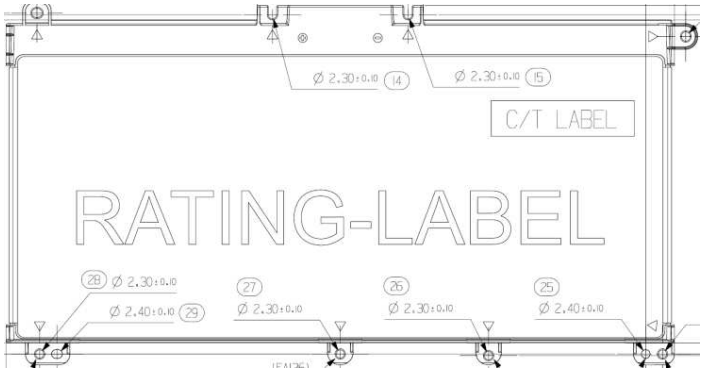
Date: Monday, August 06, 2018 Sheet 102 of 106

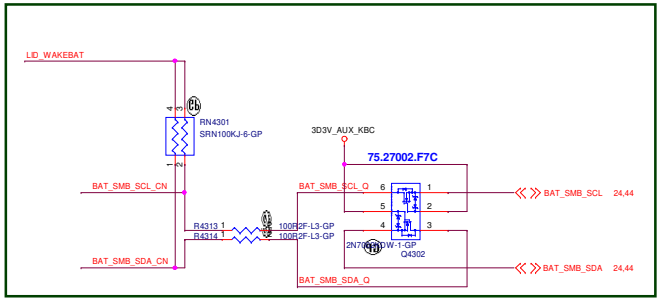
Battery Connector

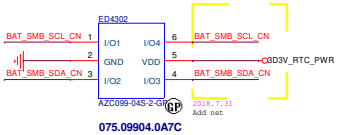


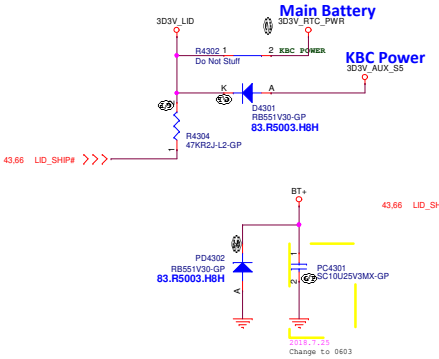


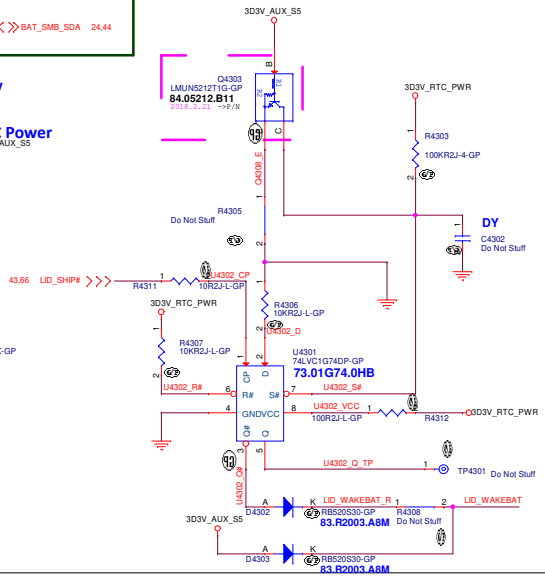
Pin No.	Symbol	Description
1~2	BATT+	Batt+, Battery Positive Terminal
3	SMC	SMBus clock interface I/O pin
4	SMD	SMBus data interface I/O pin
5	RTC	LDO – 3.3V
6	B/I	Connected to GND
7~8	GND	Batt-, Battery Negative Terminal



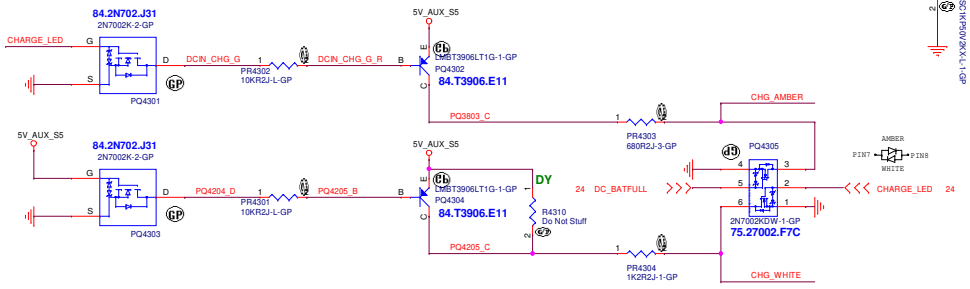


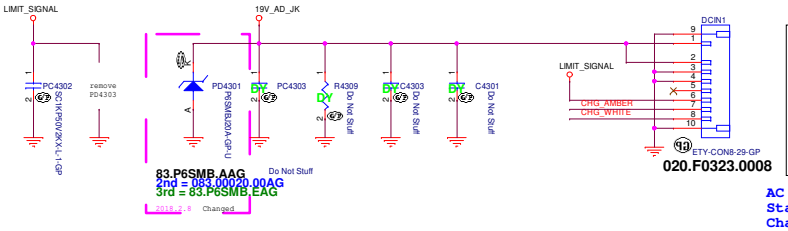


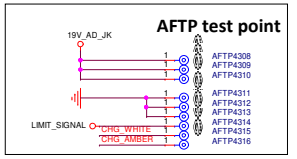




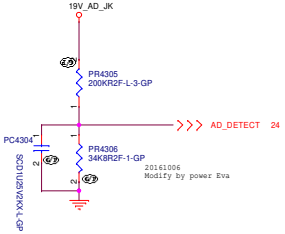
DCIN JACK

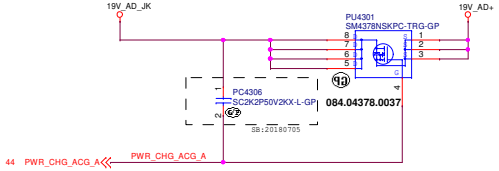






AC Present = White
Standby = White pulsing
Charging = Amber
*LED's are off if no AC jack pluged in





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Title: INT IO (ATX/ DC/ BATT Conn)

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24,43 BAT_SMB_CK — PG4408 Do Not Stuff — PWR_CHG_CLK
24,43 BAT_SMB_DA — PG4410 Do Not Stuff — PWR_CHG_DATA
24 BT_IA — PG418 Do Not Stuff — PWR_CHG_IDCHG
24 AD_IA — PR4413 Do Not Stuff — PWR_CHG_IADP
43 PWR_CHG_ACG_A — PWR_CHG_ACG_A
22,24,44,46 PROCHOT#_CPU — PR4444 Do Not Stuff — PWR_CHG_PROCHOT#
22,24,44,46 PROCHOT#_CPU — PR4445 Do Not Stuff — PROCHOT#_BAT
24 AC_IN# — PR4448 Do Not Stuff — PWR_AC_IN#
24 CHG_ON# — PR4449 Do Not Stuff — PWR_CHG_ON#

PMON : Total system power

46 PWR_VCORE_PSYS — PG4412 Do Not Stuff — PWR_CHG_PMON

AC_IN — PG4414 Do Not Stuff — PWR_CHG_ACOK

SSID = Charger

19V_AD+ → PU4401 SM3317NSQAC-TRG-GP (084.03317.0A37) → AD+_TO_SYS
SB:Change to 0.1uF(20180706)
PC4407 SCD1U25V2KX-L-GP
PWR_CHG_ACG → PR4421 4K02R2F-GP → PWR_CHG_ACG_A

AD+_TO_SYS → PR4404 D01R3217F-GP-U → 19V_DCBATOUT
PG4401 Do Not Stuff
PG4402 Do Not Stuff
DY
PR4409 Do Not Stuff
PC4403 SCD1U25V2KX-L-GP
PWR_CHG_ACP
PWR_CHG_ACN
PC4402 SCD1U25V2KX-L-GP
PC4404 SCD1U25V2KX-L-GP
CHG_AGND

PU4402 SM3317NSQAC-TRG-GP (084.03317.0A37) → BT+_R
2018.7.20 Change to dual N MOS
PWR_CHG_BTG_A → PR4411 4K02R2F-GP → PWR_CHG_BTG

19V_DCBATOUT
PC4405 SC2D2U10V3KX-L-GP
PC4425 SC2D2U10V3KX-L-GP

3D3V_AUX_S5
PR4427 100KR2F-L3-GP
PR4430 100KR2F-L3-GP
PWR_CHG_ILIM
AC_IN
PWR_AC_IN#
PWR_CHG_ON#
PQ4406 SSM6N7002KFU-GP
075.67002.007C
2ND = 075.27002.0E7C
3rd = 75.27002.F7C

3D3V_AUX_KBC
DY
PR4434 Do Not Stuff
PR4416 Do Not Stuff
PWR_CHG_DATA
PWR_CHG_CLK

19V_AD_JK
PD4404 RB520S30-GP
PD4405 RB520S30-GP
BT+
PWR_CHG_VCC_R
PR4415 20R5J-GP
PWR_CHG_VCC
PC4401 SC1U25V3KX-1-GP
CHG_AGND
83.R2003.A8M
2nd = 083.52030.008F

PR4414 10R2F-L-GP
PC4417 SCD047U25V2KX-GP
PWR_CHG_BOOT_A
PR4408 Do Not Stuff
PC4409 SC2D2U10V3KX-L-GP
PWR_CHG_REGN

PQ4403 AON7934-GP
Cyntec 6.8mm × 7.3mm × 3.0mm
DCR: 28.0m~33.0mOhm
Idc : 5.5 A , Isat : 6.5A
PL4401 VCHL-4D71H-33-GP
68.4R71A.20H
2nd = 068.4R710.1301
BT+_R
PR4417 D01R3721F-GP-U
PG4403 Do Not Stuff
PG4404 Do Not Stuff
PC4420 SC10U25V3MX-GP
PC4421 SC10U25V3MX-GP
PC4422 SC10U25V3MX-GP
PC4423 SC10U25V3MX-GP
DY
2018.7.25 Change to 0603
BT+

3D3V_S5
PD4407 RB520S30-GP
PR4450 100KR2F-L3-GP
PWR_CHG_ACDET_B
PR4406 316KR2F-GP
PWR_CHG_ACDET_A
19V_AD_JK
PD4406 RB520S30-GP
83.R2003.A8M
2nd = 083.52030.008F

PR4410 52K3R2F-L-GP
PC4410 SCD1U25V2KX-L-GP
PR4429 100KR2J-4-GP
PR4433 120KR2J-L-GP
PWR_CHG_ACOK
PWR_CHG_REGN
CHG_AGND

PU4403 BQ24781RUYR-GP (074.24781.0073)
SB:Change to BQ24781(20180621)
VCC
ACN
ACP
CMSRC
ACDRV
ACDET
SDA
SCL
ACOK
IADP
IDCHG
PMON
PROCHOT#
NC#13
NC#14
ILIM
REGN
BATDRV
BATSRC
BTST
HIDRV
PHASE
LODRV
GND
SRP
SRN
TB_STAT#
BATPRES#
THERMAL_PAD

PWR_CHG_ACN
PWR_CHG_ACP
PWR_CHG_CMSRC
PWR_CHG_ACG
PWR_CHG_ACDET
PWR_CHG_DATA
PWR_CHG_CLK
PWR_CHG_IADP
PWR_CHG_IDCHG
PWR_CHG_PMON
PROCHOT#_BAT
PWR_CHG_CMPIN
PWR_CHG_CMPOUT
PWR_CHG_ILIM
PWR_CHG_BTST
PWR_CHG_HG
PWR_CHG_PH
PWR_CHG_LG
PWR_CHG_SRP
PWR_CHG_SRN
PWR_CHG_BM#
PWR_CHG_BATPRES#
PWR_CHG_BATSRC

PC4411 SC100P50V2JN-L-GP
PR4428 Do Not Stuff
PC4408 SC100P50V2JN-1-GP
2018.7.23 delet
PR4432 Do Not Stuff
PR4413 Do Not Stuff
PR4425 10R2F-L1-GP
PR4426 10R2F-L1-GP
PC4419 SCD1U25V2KX-L-GP
PC4416 SCD1U25V2KX-L-GP
PC4412 SCD1U25V2KX-L-GP
PR4405 10KR2F-L1-GP
PR4451 10R2F-L1-GP
PWR_CHG_SRP_A
PWR_CHG_SRN_A

IADP : AC adapter detect current :
IADP : 20 or 40 x (Vacp - Vacn) / 10mohm
IDCHG : Dischange detect current :
= 8 or 16 x (Vsrn - Vsrp)

Total Power Setting

PR4407 45W 73.2K ADT PROTECT 110%
PR4407 45W 105K ADT PROTECT 130%
PR4407 65W 150K ADT PROTECT 110%
PR4407 65W 196K ADT PROTECT 130%

PWR_CHG_REGN
PR4431 Do Not Stuff DY
PWR_CHG_CMPOUT
PR4402 Do Not Stuff DY
PWR_CHG_IADP
PR4407 Do Not Stuff DY
R1
PWR_CHG_CMPIN
R2
PR4401 Do Not Stuff
CHG_AGND

PR4401 100K for BQ24780S
PR4401 0 ohm for BQ24781

PQ4408 上件 for BQ24780S
PQ4408 DY for BQ24781
PWR_CHG_PROCHOT#
PQ4408 Do Not Stuff
2ND = 084.27002.0N31
3rd = 084.27002.0L31
DY
PWR_CHG_CMPOUT
PC4426 Do Not Stuff DY

	Stat	PM_SLP_A#	Adaptor Current	AC_Protect protect	AC_Protect Current	PR4404 Sense resistor	0x12H_Bit4 IADP GAIN	0x3BH_Bit 7 CM_VREF	Current to Voltage	R1 PR4407	R2 PR4401
40W	AC + Battery	High	2.1	102%	2.142	20	40	1.2 V	1.7136	41.2	100
45W	AC + Battery	High	2.37	102%	2.4174	20	40	1.2 V	1.93392	60.4	100
65W	AC + Battery	High	3.42	102%	3.4884	10	40	1.2 V	1.39536	16.2	100
90W	AC + Battery	High	4.74	102%	4.8348	10	40	1.2 V	1.93392	60.4	100
120W	AC + Battery	High	6.31	102%	6.4362	10	40	1.2 V	2.57448	113	100
135W	AC + Battery	High	7.1	102%	7.242	10	40	1.2 V	2.8968	140	100

CAL				
Vcomp	Vsense	R1	R2	
1.213598	1.7136	41.2	100	
1.205686	1.93392	60.4	100	
1.200826	1.39536	16.2	100	
1.205686	1.93392	60.4	100	
1.208676	2.57448	113	100	
1.207	2.8968	140	100	

UMA

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Title: 044_Power (Charger_BQ24780S)
Size: Custom | Document Number: FAROE 14" Pavilion | Rev: SB
Date: Monday, August 06, 2018 | Sheet 44 of 106

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24 S5_ENABLE — PR4515 Do Not Stuff — PWR_3D3V_EN

24 5V_S5_EN — PR4551 Do Not Stuff — PWR_5V_EN

IDC : 6A
OCP : 8A

Vin Operating range : 4~23V
Vin_Max : 25V

Ilimt : 8A

EN rating 25V
EN Rising Threshold : 0.8V
EN Falling Threshold : 0.4V

PU4501 SY8288BRAC-GP 074.08288.0A43

Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A

PL4501 IND-1D5UH-23-GP-U 68.1R510.10K

17.8.25 update

22uF	PCS
Suggestion	4

PC4513 PC4509 PC4510 PC4511 PC4525 PC4512 — SC22U6D3V3MX-L1-GP

PWR_3D3V_VOUT — Trace used 10 mil

PC4526 SC1KP50V2KX-L-1-GP

PR4506 1KR2F-3-GP

PR4501 Do Not Stuff — PC4506 SCD1U25V2KX-L-GP

PR4514 1MR2J-1-GP

PR4503 D5R2F-1-GP — PC4507 SC4D7U6D3V3KX-L-GP

PR4509 499KR2F-1-GP (2018.2.26 1K->499K)

PR4508 499KR2F-1-GP (2018.2.26 200K->499K; 2018.3.1 ->Stuff)

PR4505 Do Not Stuff

R4501 Do Not Stuff — PCH_DPWROK 20,24,89

R4502 Do Not Stuff (2018.1.11 ->pad)

PU4551 SY8288CRAC-GP 074.08288.0B43

Cyntec. 6.86 x 6.47 x 3.0mm
DCR: 9~10mOhm
Idc : 11A , Isat : 22A

IDC:8A

17.8.25 update

22uF	PCS
Suggestion	5

PL4502 IND-1D5UH-23-GP-U 68.1R510.10K

PWR_5V_VOUT — Trace used 10 mil

PC4556 PC4557 PC4558 PC4559 PC4560 PC4561 — SC22U6D3V3MX-L1-GP

PC4562 SC2D2U10V3KX-L-GP

PR4560 499KR2F-1-GP (2018.2.26 Added) — PC4564 Do Not Stuff

PR4556 1MR2J-1-GP

PR4555 1KR2F-3-GP — PC4563 SC1KP50V2KX-L-1-GP

PC4551 SC4D7U25V5KX-L2-GP — PR4565 Do Not Stuff

PC4552 PC4554 PC4555 — SC4D7U25V5KX-L2-GP

PR4552 Do Not Stuff — PC4553 SCD1U25V2KX-L-GP — PR4554 Do Not Stuff

PG4562 Do Not Stuff

EN rating 25V
EN Rising Threshold : 0.8V

Ilimt : 8A

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (SY8286B/SY8288C_3V/5V)

Size: Custom | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2018 | Sheet 45 of 106

Main Func = CPU_CORE

OFFPAGE

22,24,44 PROCHOT#_CPU
7 SVID_ALERT#_CPU
7 SVID_CLK_CPU
7 SVID_DATA_CPU
26,40 VCORE_PWRGD
40 VCORE_EN
7 VSSCORE_SENSE
7 VCCCORE_SENSE
8 VCCGT_SENSE
8 VSSGT_SENSE
8 VSSSA_SENSE
8 VCCSA_SENSE
44 PWR_VCORE_PSYS

PR4602 Do Not Stuff 1 2 PWR_CPU_PROCHOT#
PR4603 Do Not Stuff 1 2 PWR_VCORE_ALERT#
PR4607 Do Not Stuff 1 2 VIDSCK_CPU_R
PR4608 Do Not Stuff 1 2 VIDSOUT_CPU_R
PR4612 Do Not Stuff 1 2 PWR_IMVP_PWRGD
PR4616 Do Not Stuff 1 2 PWR_VR_EN
PR4617 Do Not Stuff 2 1 PWR_VCORE_RTN
PC4627 Not Stuff 2 1 PWR_VCORE_VSEN
PR4623 Do Not Stuff 1 2 PWR_VCCGT_VSEN
PR4625 Do Not Stuff 1 2 PWR_VCCGT_RTN
PR4631 Do Not Stuff 2 1 PWR_VCCSA_RTN
PR4634 Not Stuff 2 1 PWR_VCCSA_FB2

2018.1.17 updated

1V_S3
PR4609 45K3R2F-L-GP
PR4610 100R2F-L-GP
PC4602 SCD1U25V2KX-L-GP
DY
VIDSOUT_CPU_R
PWR_VCORE_ALERT#
VIDSCK_CPU_R

PWR_VREF
PR4604 4K22R2F-GP
PR4605 9K53R2F-GP
PR4606 35K7R3F-GP
PR4613 226R2F-GP
PR4614 Do Not Stuff
PR4615 392R2F-GP
PR4620 4K22R2F-GP
PR4621 9K1R2F-1-GP
PR4622 18K2R2F-L-GP
PR4629 95D3R2F-GP
PR4630 143R2F-1-GP
PR4626 130R2F-1-GP
PWR_VCORE_SET1
PWR_VCORE_SET2
PWR_VCORE_SET3
PWR_VCORE_SET1_B
PWR_VCORE_SET2_B
PWR_VCORE_SET3_B

1V_S3
PR4619 Do Not Stuff
PR4601 100R2F-L3-GP
DY
PWR_CPU_PROCHOT
PWR_VCORE_VRHOT#

2018.05.28 Delete

PWR_VREF
19V_DCBATOUT
PR4628 2D2R3F-L-GP
PC4606 SCD22U25V3KX-GP
PR4624 41K2R2F-GP
PC4608 Do Not Stuff
DY

5V_S5
PR4618 8D2R3F-GP
PC4603 SCD7U6D3V3KX-L-GP

PR4647 71K5R2F-1-GP
UMA
PR4646 Do Not Stuff
DIS
PWR_VCORE_PSYS

PR4635 48.7K->49.9K 49K3R2F-L-GP
PC4610 Do Not Stuff
DY
3D3V_S0
PR4636 10KR2F-L1-GP
VIDSCK_CPU_R PR4638 49D9R2F-L1-GP
VIDSOUT_CPU_R PR4639 10R2F-L1-GP
PWR_IMVP_PWRGD
PWR_VCORE_VRRDY#
PWR_VCORE_SCLK
PWR_VCORE_SDIO
PWR_VCORE_ALERT#

PR4640 38K3R2F-GP
PWR_VCORE_IMON_A
PR4642 41K2R2F-GP
PR4678 NTC-100K-12-GP-U
PWR_VCORE_IMON_B
B = 4250
PR4641 13K7R2F-GP
PC4612 Do Not Stuff
DY

PU4601
PSYS
VCC
SET1
SET2
SET3
VIN
VREF06/PSET
IMON_AUXI
IMON_MAIN
IMON_SA
VR_READY
VR_HOT#
VCLK
VDIO
ALERT#
EN
VSEN_AUXI
COMP_AUXI
FB_AUXI
RGND_AUXI
DRVEN_SET
COMP_MAIN
FB_MAIN
RGND_MAIN
VSEN_MAIN
COMP_SA
FB_SA
RGND_SA
NC#14
NC#15
NC#19
NC#20
NC#21
RT3602AJSQW-GP
074.03602.0A73
PWM_SA
ISENP_SA
ISENN_SA
PWM_AUXI
ISENP_AUXI
ISENN_AUXI
PWM2_MAIN
ISEN1P_MAIN
ISEN1N_MAIN
PWM1_MAIN
ISEN2P_MAIN
ISEN2N_MAIN
DRVEN
TSEN_AUXI
TSEN_MAIN
GND

PWR_VCORE_PSYS
PWR_VCORE_VCC
PWR_VCORE_SET1
PWR_VCORE_SET2
PWR_VCORE_SET3
PWR_VCORE_VIN
PWR_VREF
PWR_VCCGT_IMON
PWR_VCORE_IMON
PWR_VCCSA_IMON
PWR_VR_EN
PWR_VCCGT_VSEN
PWR_VCCGT_COMP
PWR_VCCGT_FB
PWR_VCCGT_RTN
PWR_VCORE_DRVEN_SET
PWR_VCORE_COMP
PWR_VCORE_FB
PWR_VCORE_RTN
PWR_VCORE_VSEN
PWR_VCCSA_COMP
PWR_VCCSA_FB
PWR_VCCSA_RTN

PWR_VCCSA_PWM 50
PWR_VCCSA_ISUMP 50
PWR_VCCSA_ISUMN 50
PC4601 Do Not Stuff
PC4605 SCD1U25V2KX-L-GP
PWR_VCCGT_PWM 48
PWR_VCCGT_ISUMP 48
PWR_VCCGT_ISUMN 48
PC4607 Do Not Stuff
PC4609 SCD1U25V2KX-L-GP
PWR_VCORE_PWMB 47
PWR_VCORE_ISUMP_A 47
PWR_VCORE_ISUMN_A 47
PR4683 1R2F-GP
PC4611 Do Not Stuff
PC4613 SCD1U25V2KX-L-GP
PWR_VCORE_PWMA 47
PWR_VCORE_ISUMP_B 47
PWR_VCORE_ISUMN_B 47
PR4684 2 1 1R2F-GP
PWR_VCORE_FCCM# 47,48,50
PC4615 SCD1U25V2KX-L-GP
PWR_VCCGT_TSEN
PWR_VCORE_TSEN

PR4676 NTC-100K-12-GP-U
69.60011.221
B = 4250
PR4664 110KR2F-L-GP
PR4681 NTC-100K-12-GP-U
69.60011.221
B = 4250
PR4677 110KR2F-L-GP
PWR_VCCGT_TSEN_A
PWR_VCORE_TSEN_A

PWR_VREF
PR4654 12KR2F-L-GP
PR4655 15K8R2F-GP
PWR_VCCGT_TSEN_B
PWR_VCORE_TSEN_B
PR4661 845R2F-GP
PR4662 174R2F-GP
PR4670 22K6R2F-1-GP
PR4671 16K9R2F-GP
PWR_VCCGT_TSEN_C
PWR_VCORE_TSEN_C
PR4674 432R2F-GP
PR4675 143R2F-1-GP

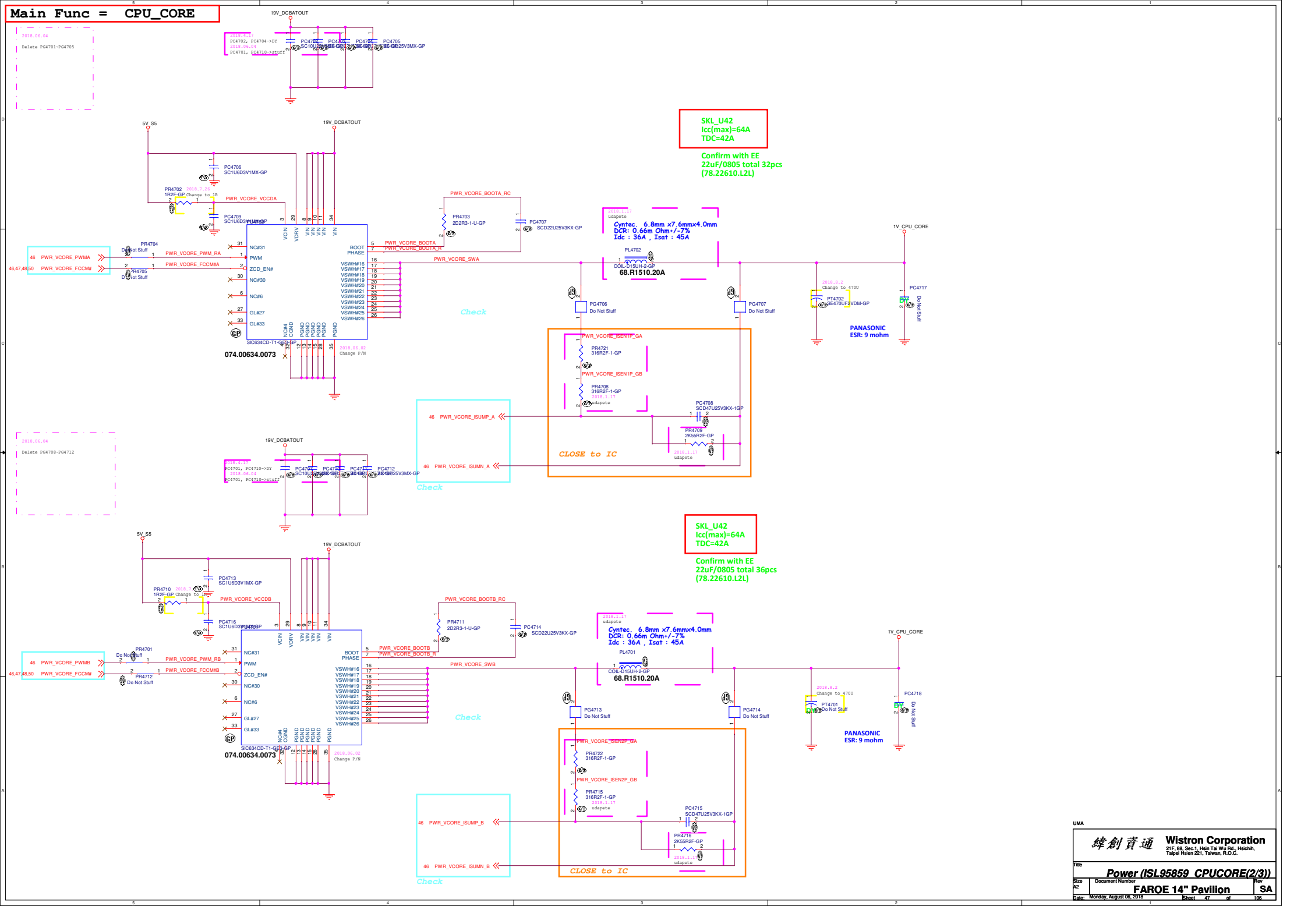
PWR_VCCGT_VSEN
PR4648 10KR2F-L1-GP
PWR_VCCGT_COMP_B
PR4649 Do Not Stuff
PC4616 150pF->220pF SC220P50V2KX-3GP
PC4618 Do Not Stuff
PWR_VCCGT_FB_A
PR4653 Do Not Stuff
DY
PR4650 19.6K->21.5k 21K5R2F
PWR_VCCGT_COMP_A
PR4651 Do Not Stuff
PC4617 82pF->68pF SC68P50V2JN-1GP
5V_S5
PR4645 Do Not Stuff

PWR_VCORE_VSEN
PR4657 10KR2F-L1-GP
PWR_VCORE_COMP_B
PR4658 Do Not Stuff
PC4619 150pF->330pF SC330P50V2KX-3GP
PC4621 Do Not Stuff
PWR_VCORE_FB_A
DY
PR4659 46.4k->64.9k 64K9R2F-1-GP
PWR_VCORE_COMP_A
PR4660 Do Not Stuff
PC4620 82pF->68pF SC68P50V2JN-1GP

PWR_VCCSA_FB2
PR4666 10KR2F-L1-GP
PWR_VCCSA_COMP_B
PR4667 Do Not Stuff
PC4622 330P->470P SC470P50V2KX-L-GP
PC4624 Do Not Stuff
PWR_VCCSA_FB_A
PR4673 Do Not Stuff
DY
PR4668 57K6R2F-GP
PWR_VCCSA_COMP_A
PR4669 Do Not Stuff
PC4623 SC68P50V2JN-1GP

UMA
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: Power (ISL95859 CPUCORE(1/3))
Size: Custom
Document Number: FAROE 14" Pavilion
Rev: SA
Date: Monday, August 06, 2018
Sheet 46 of 106

Main Func = CPU_CORE



UMA

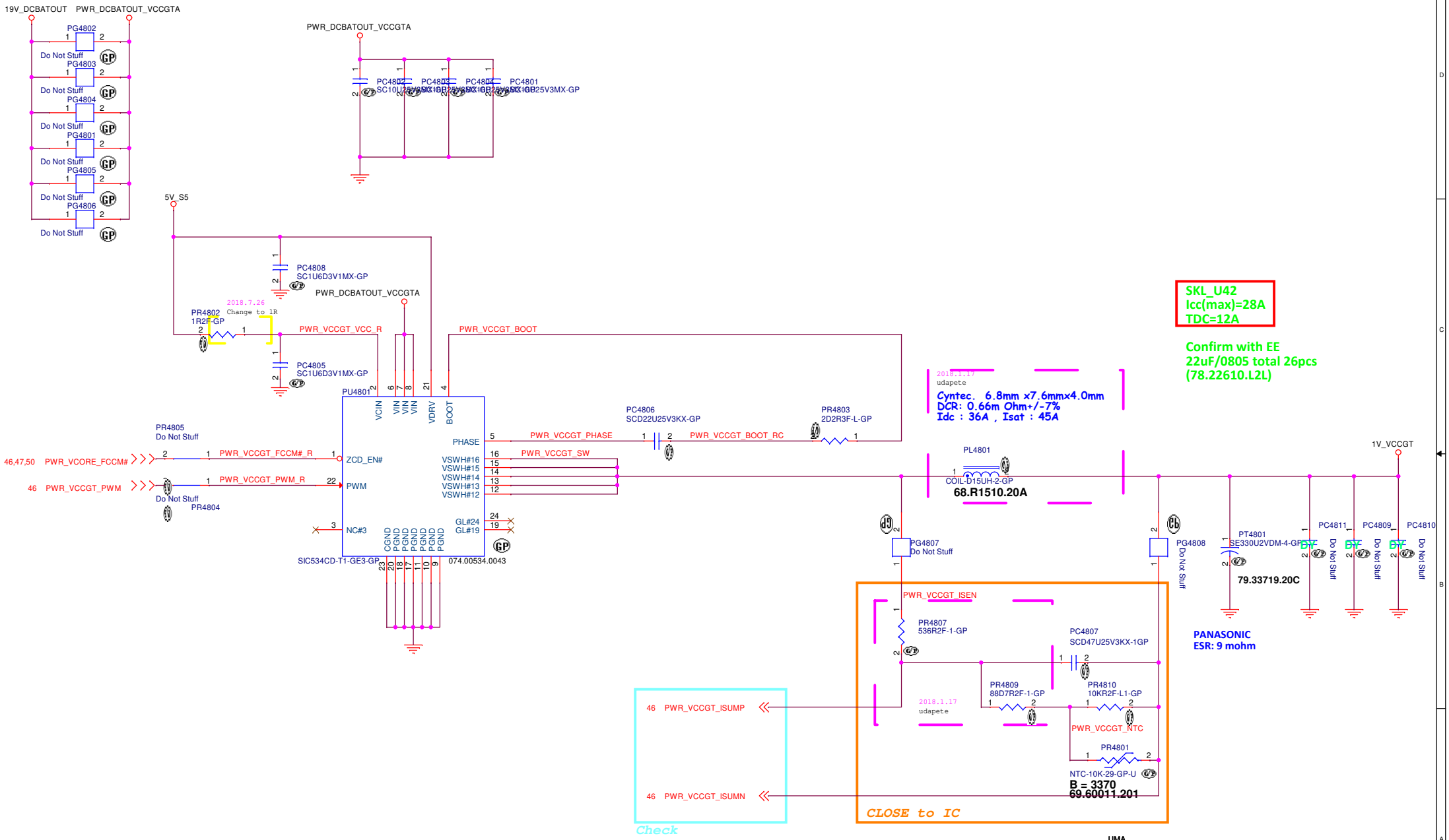
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (ISL95859 CPUCORE(2/3))

Size	Document Number	Rev
A2	FAROE 14" Pavilion	SA

Date: Monday, August 06, 2018 Sheet 47 of 106

Main Func = CPU_CORE

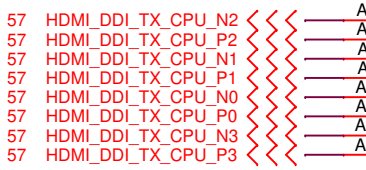


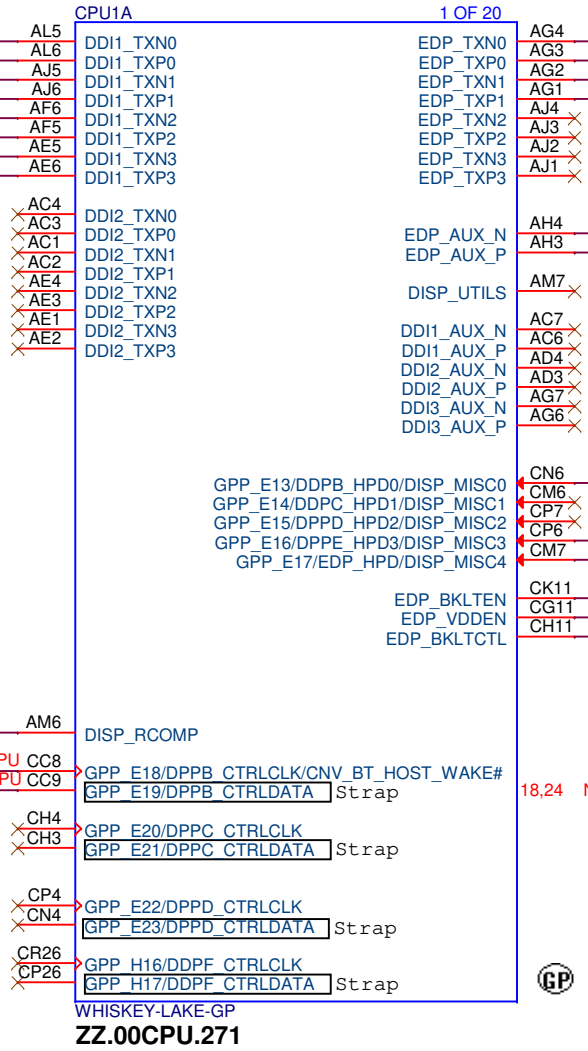
UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Power (ISL95859_CPUCORE(3/3))		
Size: A3	Document Number: FAROE 14" Pavilion	Rev: SA
Date: Monday, August 06, 2018	Sheet 48 of 106	

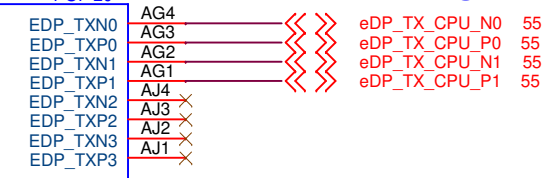
Main Func = CPU

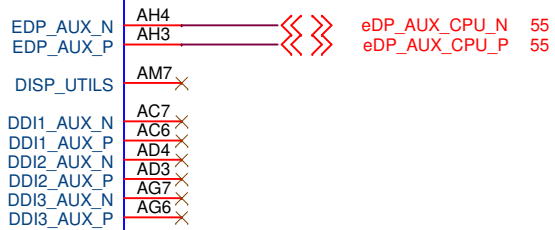
HDMI

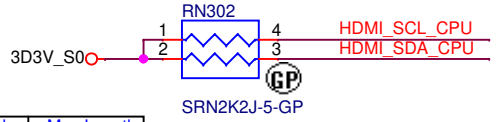


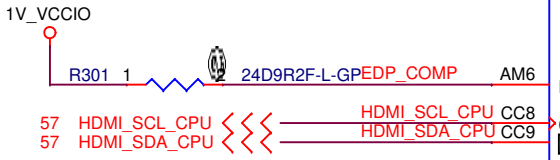


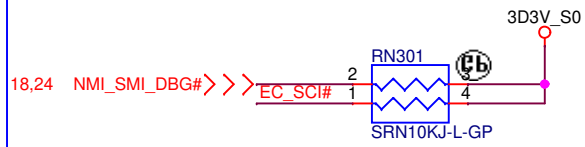
eDP











2018.1.11 updated

#575412 eDP RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length
eDP_RCOMP	5 mils	25 mils	24.9 Ω ±1%	600 mils

2018.1.11 updated

PCH strap pin:

Display Port B Detected	
GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Low = Not detected (Default) High= Detected* This signal has a weak internal PD

PCH strap pin:

Display Port C Detected	
GPP_E21 / DDPC_CTRLDATA	Low = Not detected (Default)* High= Detected This signal has a weak internal PD

PCH strap pin:

Display Port D Detected	
GPP_E23 / DDPD_CTRLDATA	Low = Not detected (Default)* High= Detected This signal has a weak internal PD

PCH strap pin:

(EDS Reserved)	
GPP_H17	Low = TBD High= TBD This signal has a weak internal PD*

This strap should sample LOW.

2018.1.11 updated

#575412 DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	NC
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	NC
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	NC

ZZ.00CPU.271

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDI/EDP)

Size: A4 | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2018 | Sheet 3 of 106

Main Func = CPU

DDR4 Channel A ball type:Non Interleaved Type

Notes:

1. DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel
2. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (DDR_CHA)***

Size: B | Document Number: **FAROE 14" Pavilion** | Rev: **SA**

Date: Monday, August 06, 2018 | Sheet 4 of 106

Main Func = CPU

DDR4 Channel B ball type:Non Interleaved Type

Signal	Trace Width	Trace Spacing	Resistor Value(Ω ±1%)	Max Length
DDR_RCOMP[2:0]	15 mils	20-25 mils	121/80.6/100	500 mils

Notes:

1. DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel
2. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

UMA

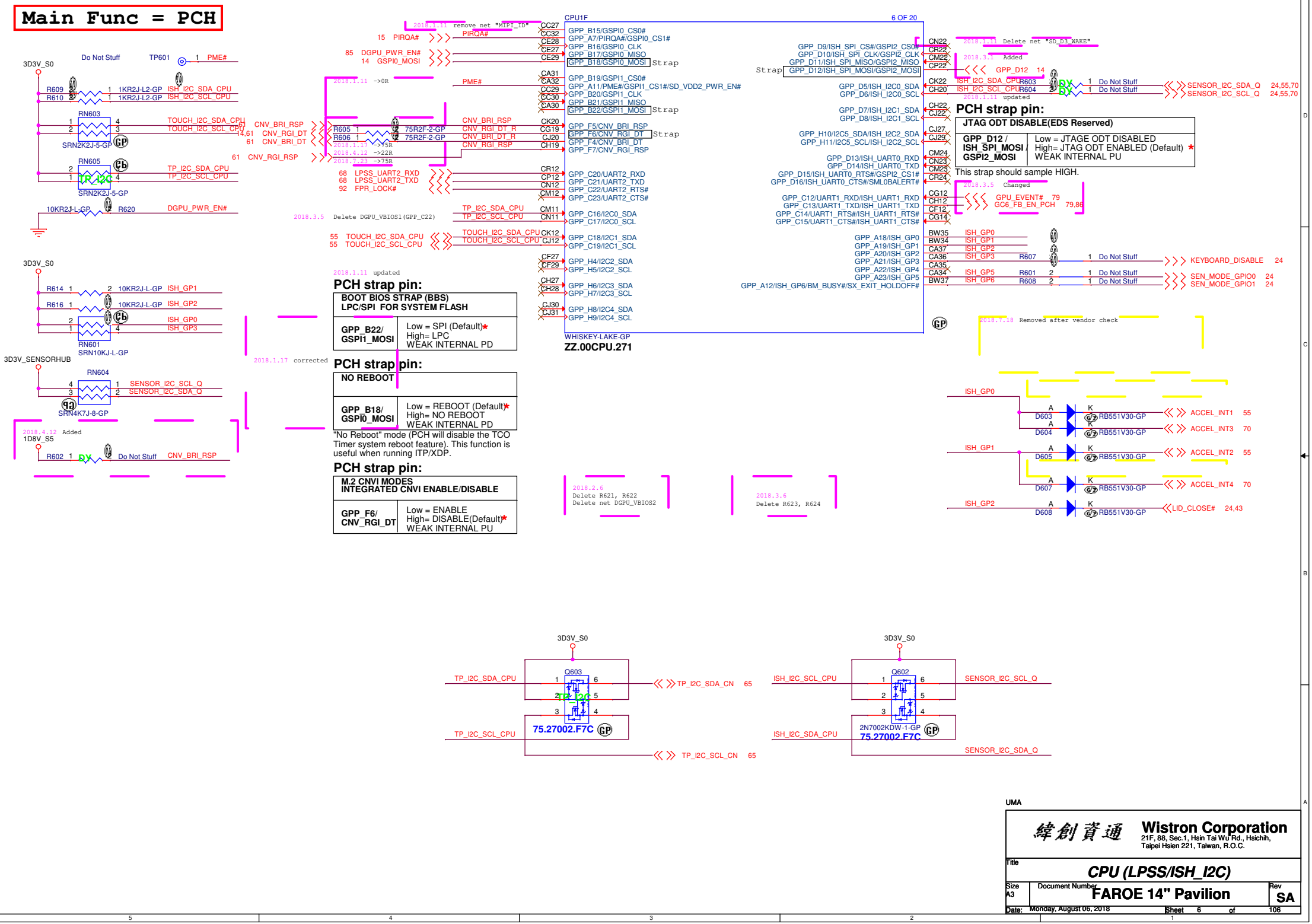
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (DDR_CHB)**

Size: B | Document Number: **FAROE 14" Pavilion** | Rev: **SA**

Date: Monday, August 06, 2018 | Sheet 5 of 106

Main Func = PCH



UMA

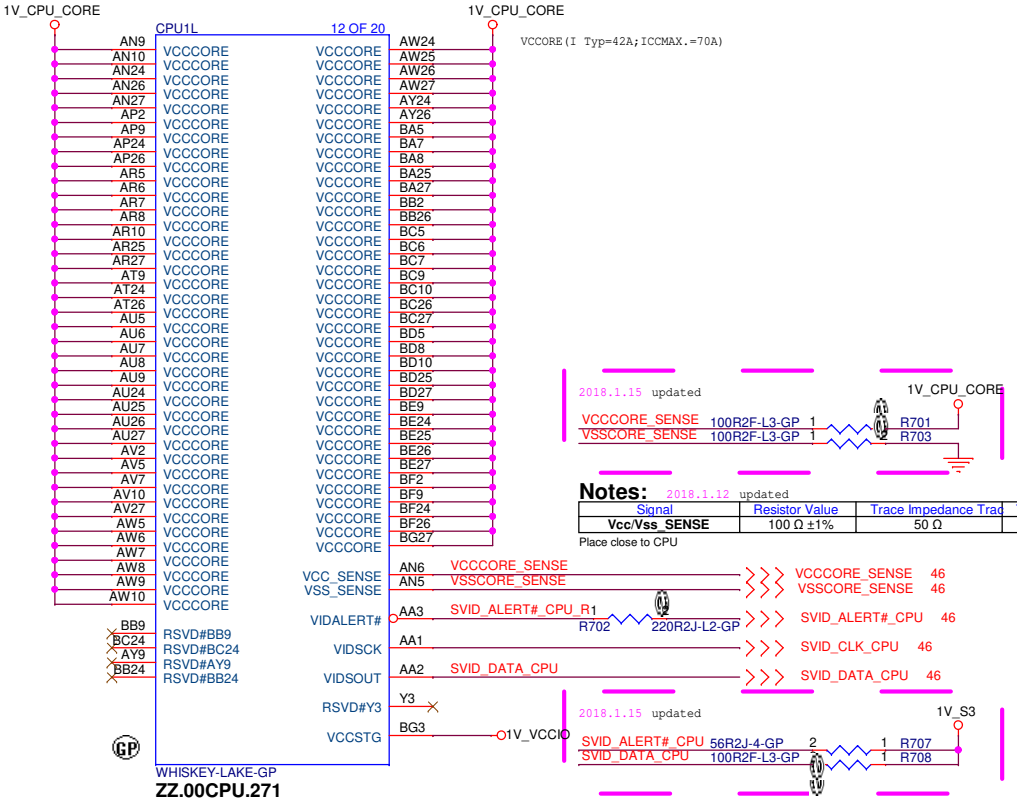
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (LPSS/ISH_I2C)

Size	Document Number	Rev
A3	FAROE 14" Pavilion	SA

Date: Monday, August 06, 2018 Sheet 6 of 106

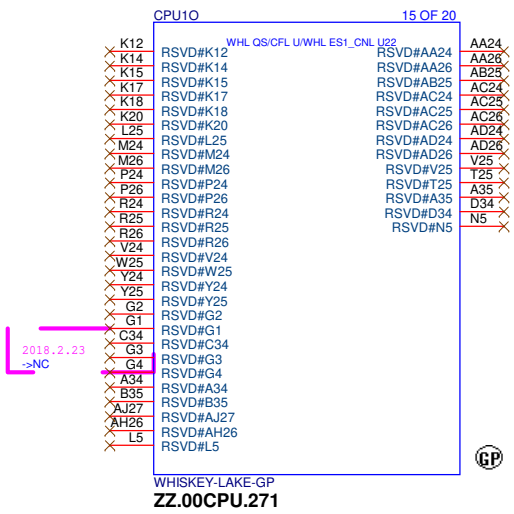
Main Func = CPU



Notes: 2018.1.12 updated

Signal	Resistor Value	Trace Impedance Trac	Trace Length Match
Vcc/Vss_SENSE	100 Ω ±1%	50 Ω	<25mils

Place close to CPU



#575412_PDG rev.0.7 2018.1.15 updated

Figure 7-19. Routing Illustration for SVID Topology

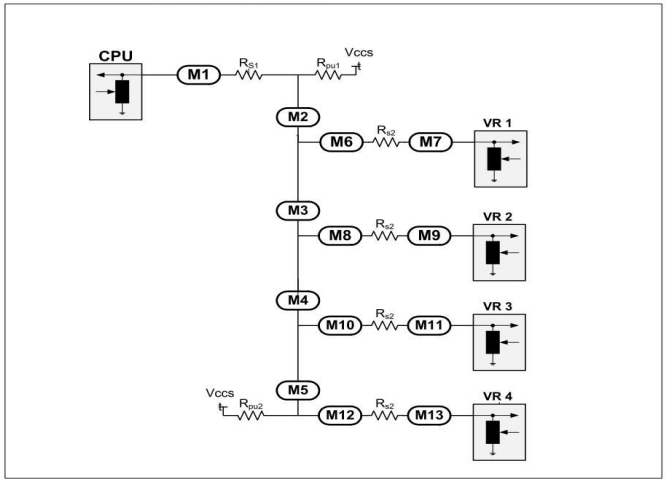


Figure above demonstrates Routing Illustration for SVID Topology, each trace from CPU to VR represents 3 signals: VIDSOUT, VIDSCK, VIDSALERT#.

Table 7-18. SVID Routing Guidelines (Sheet 1 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS		76	76	2992.13	2992.13
Segment	**Tline Type**	**Reference**	**Via Count**	**Max Length, mm**		**Max Length, Mils**	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11
Topology Guidelines							
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#						
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω						
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω						
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω						
Platform resistors tolerances	± 5%						
Route ordering	When routing at minimum spacing route Alert between Data and Clock						
Length Matching Rules							
Length Matching between VIDSOUT and VIDSCK	± 100mils						

UMA

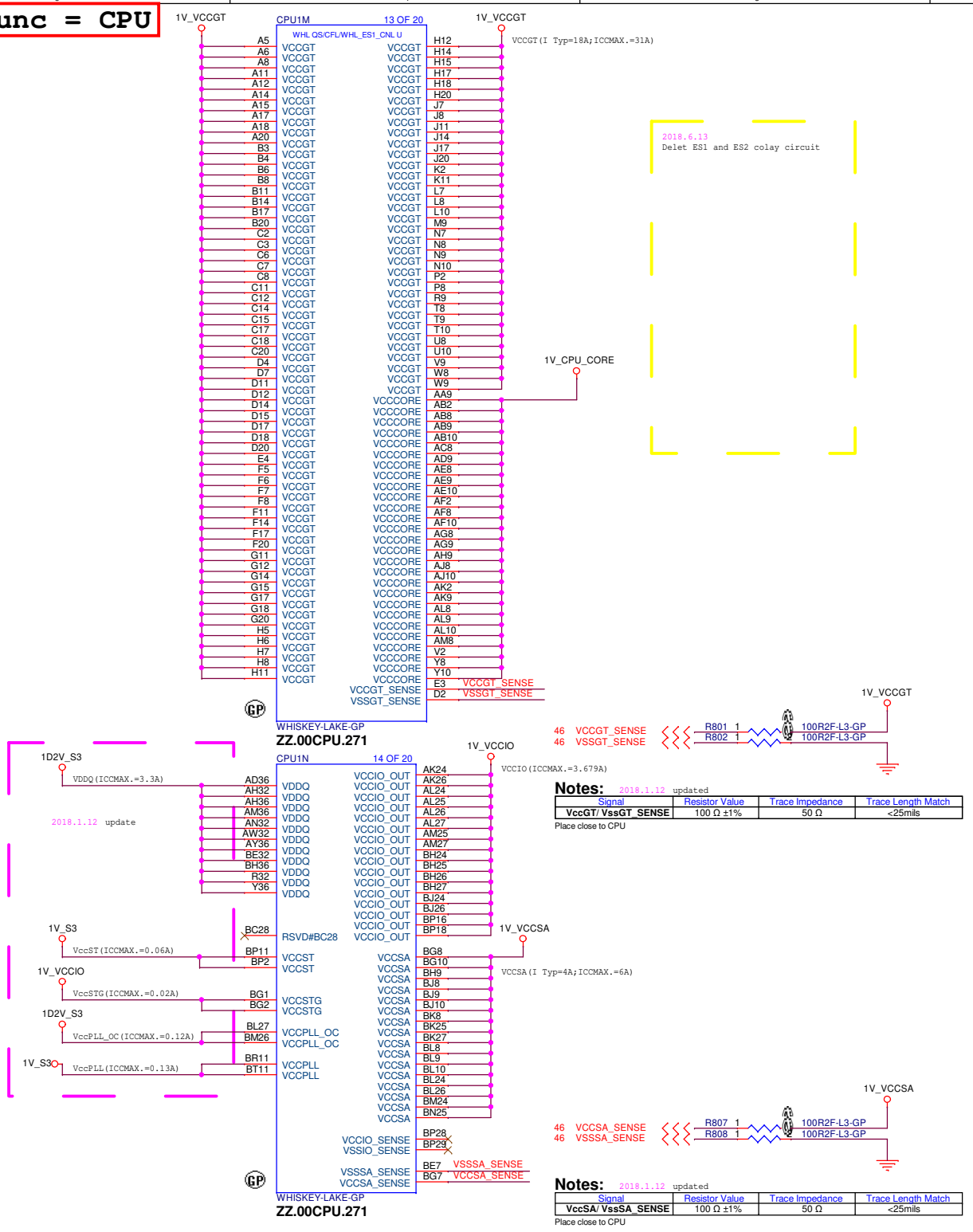
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (POWER1)**

Size: B | Document Number: **FAROE 14" Pavilion** | Rev: **SA**

Date: Monday, August 06, 2018 | Sheet 7 of 106

Main Func = CPU



2018.6.13
Delet ES1 and ES2 colay circuit

2018.1.12 update

46 VCCGT_SENSE
46 VSSGT_SENSE
R801 1 2 100R2F-L3-GP
R802 1 2 100R2F-L3-GP
1V_VCCGT

Notes: 2018.1.12 updated

Signal	Resistor Value	Trace Impedance	Trace Length Match
VccGT/ VssGT_SENSE	100 Ω ±1%	50 Ω	<25mils

Place close to CPU

46 VCCSA_SENSE
46 VSSSA_SENSE
R807 1 2 100R2F-L3-GP
R808 1 2 100R2F-L3-GP
1V_VCCSA

Notes: 2018.1.12 updated

Signal	Resistor Value	Trace Impedance	Trace Length Match
VccSA/ VssSA_SENSE	100 Ω ±1%	50 Ω	<25mils

Place close to CPU

2018.1.12 updated
#575376

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE

UMA

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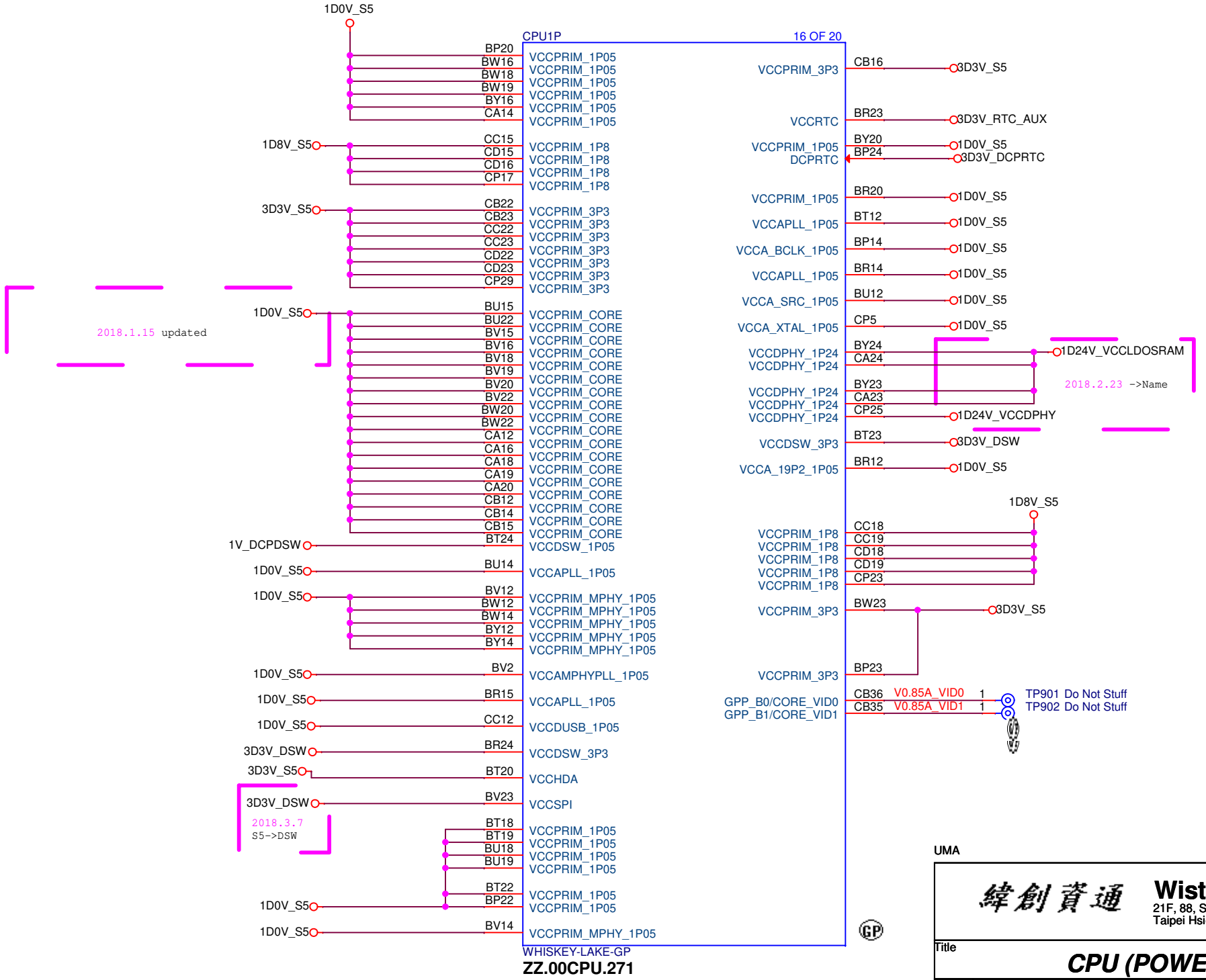
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER2)

Size: A3 | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2018 | Sheet 8 of 106



UMA

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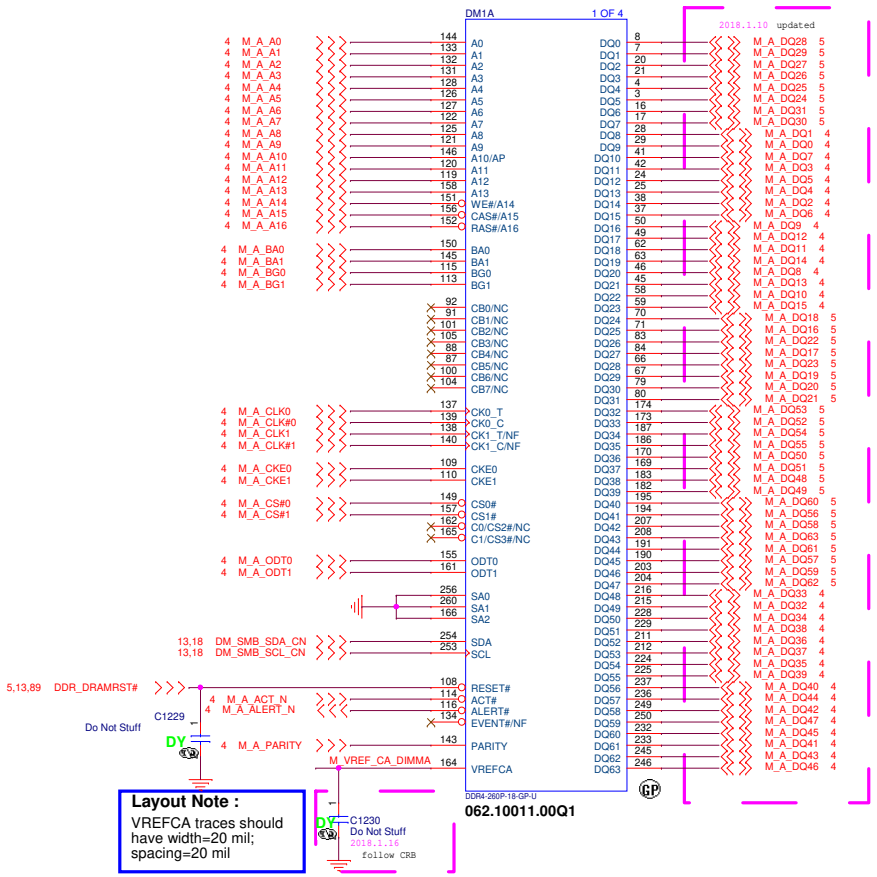
Title: ***CPU (POWER3)***

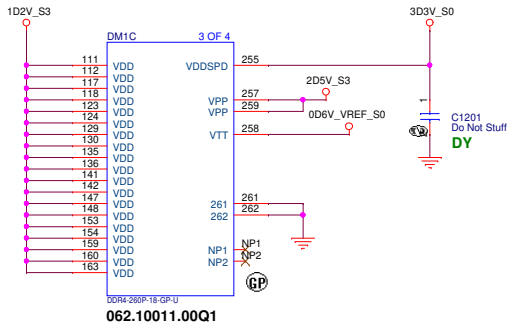
Size	Document Number	Rev
A4	**FAROE 14" Pavilion**	SA

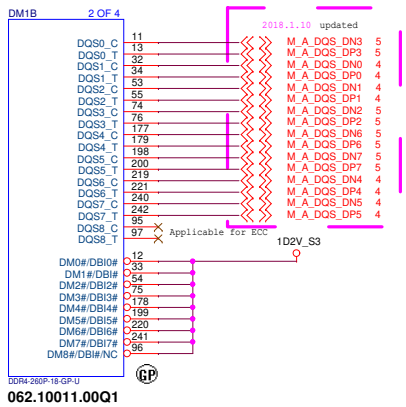
Date: Monday, August 06, 2018 Sheet 9 of 106

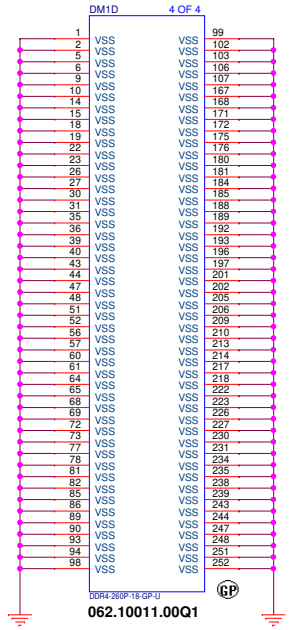
Main Func = DDR SODIMM

DDR4 Reverse Type





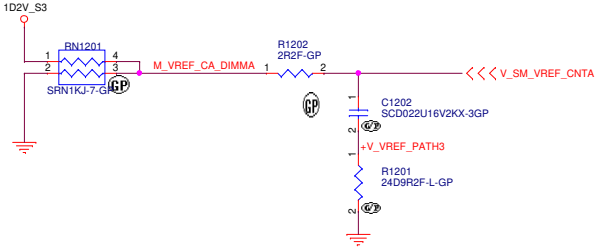




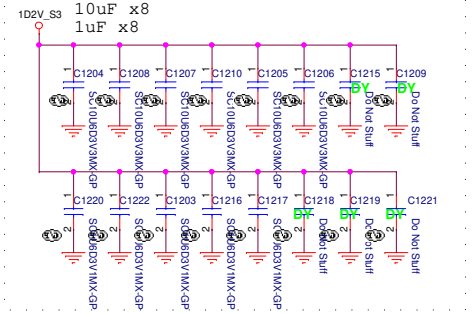
SPD Address of DIMMA

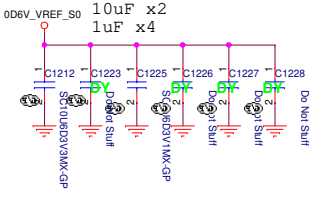
SPD SA2	0
SPD SA1	0
SPD SA0	0

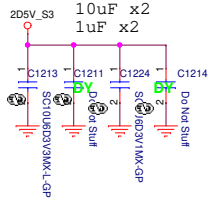
SA_DIMM_VREFDQ



Layout Note :
Place these Caps near DIM1







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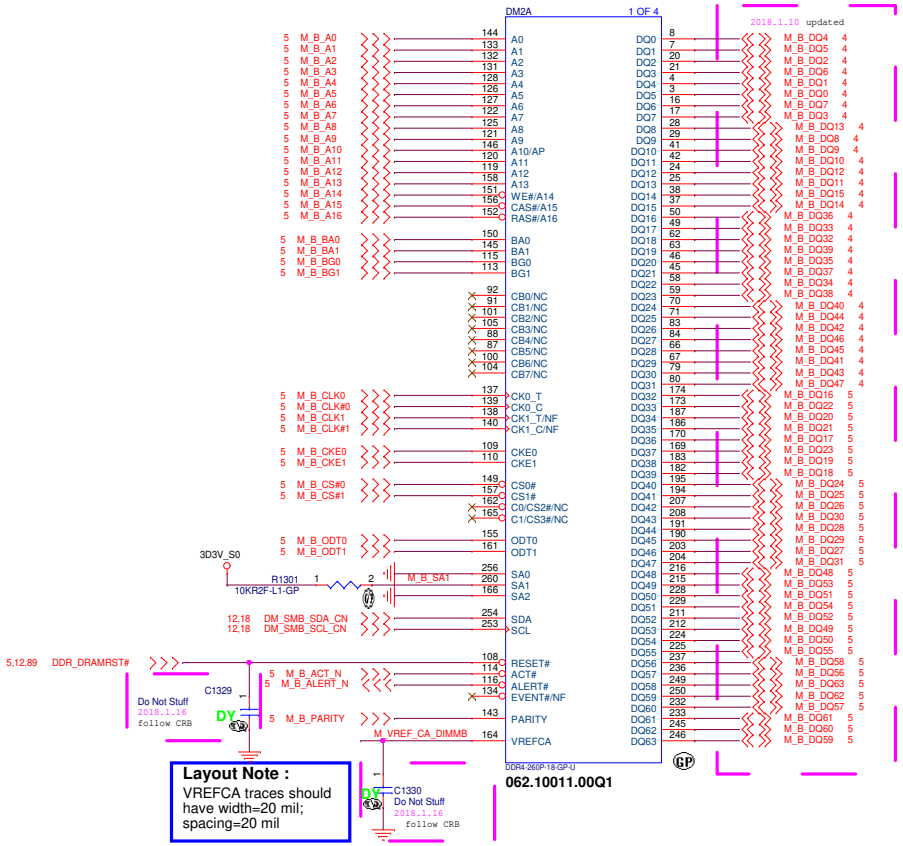
Title: 012_DDR (DDR4-CHA)

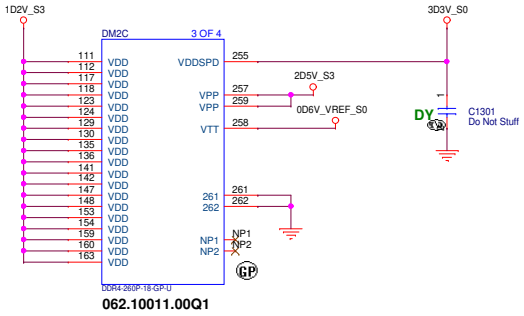
Size: Custom | Document Number: FAROE 14" Pavilion | Rev: SA

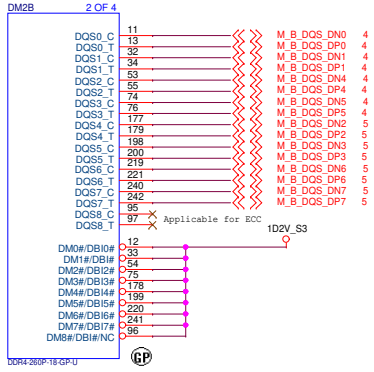
Date: Monday, August 06, 2018 | Sheet 12 of 106

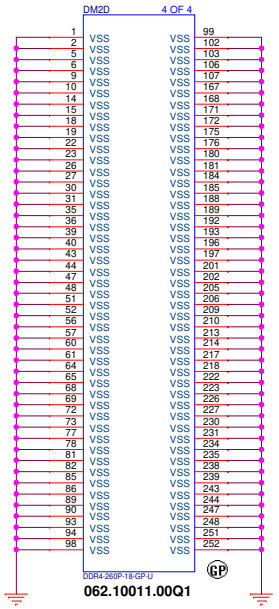
Main Func = DDR SODIMM

DDR4 Reverse Type





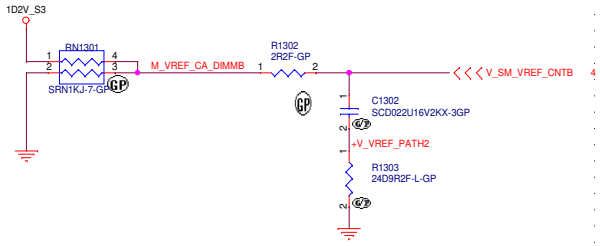




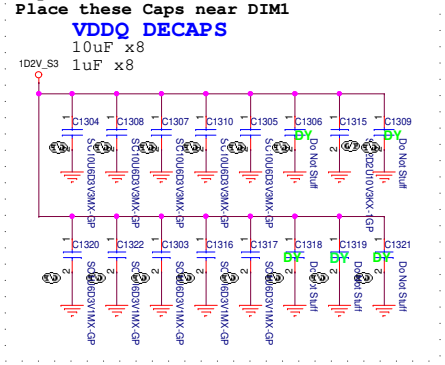
SPD Address of DIMMB

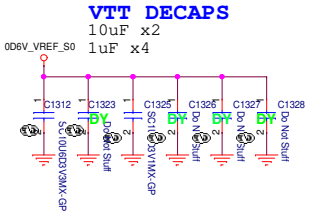
SPD SA2	0
SPD SA1	1
SPD SA0	0

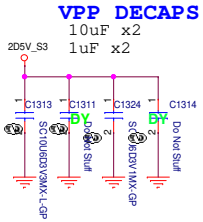
SA_DIMM_VREFDQ



Layout Note :
Place these Caps near DIM1







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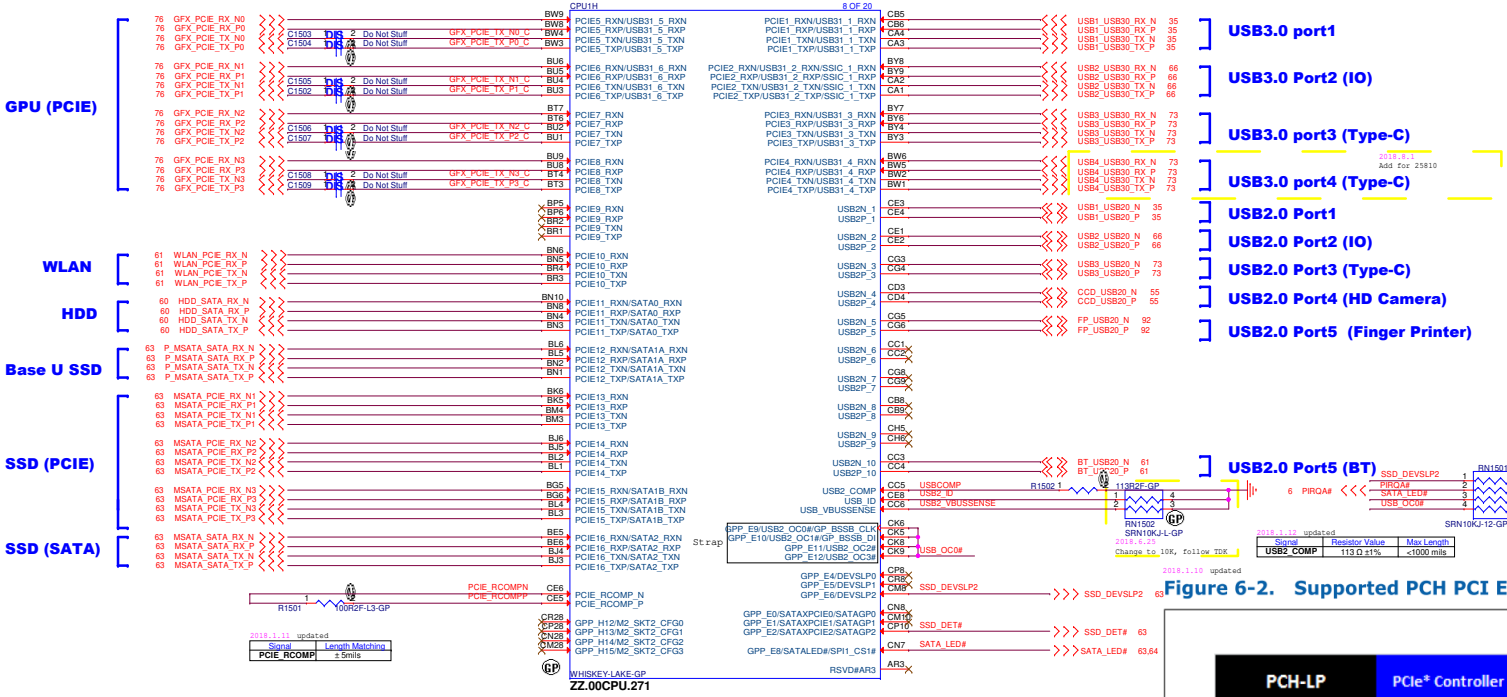
Taipei Hsien 221, Taiwan, R.O.C.

Title: 013_DDR (DDR4-CHB)

Size: Custom | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2018 | Sheet 13 of 106

Main Func = PCH



PCH strap pin:

RING OSCILLATOR BYPASS (QUALIFIED BY DFXTESTMODE)	
GPP_E9/ USB2_OC0#/ GP_BSSB_CLK	Low = RING OSCILLATOR High= BYPASS MODE ENABLED ★ NO INTERNAL PU/PD

PCH strap pin:

XTAL INPUT FREQUENCY [1:0] (QUALIFIED BY DFXTESTMODE)		
GPP_E10/ USB2_OC1#	00-24MHZ 01-25MHZ 10-250MHZ 11-100MHZ ★	HVM ONLY
GPP_E11/ USB2_OC2#		

PCH strap pin:

XTAL INPUT MODE (QUALIFIED BY DFXTESTMODE)	HVM ONLY
GPP_E12/ USB2_OC3#	Low = XTAL INPUT IS SINGLE ENDED High= XTAL INPUT IS DIFFERENTIAL ★ NO INTERNAL PU/PD

THIS IS NOT APPLICABLE FOR CNL

Figure 6-2. Supported PCH PCI Express* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3 Cycle Router #2				PCIe* Controller #4 Cycle Router #3			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9		RP16	RP15	RP13	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

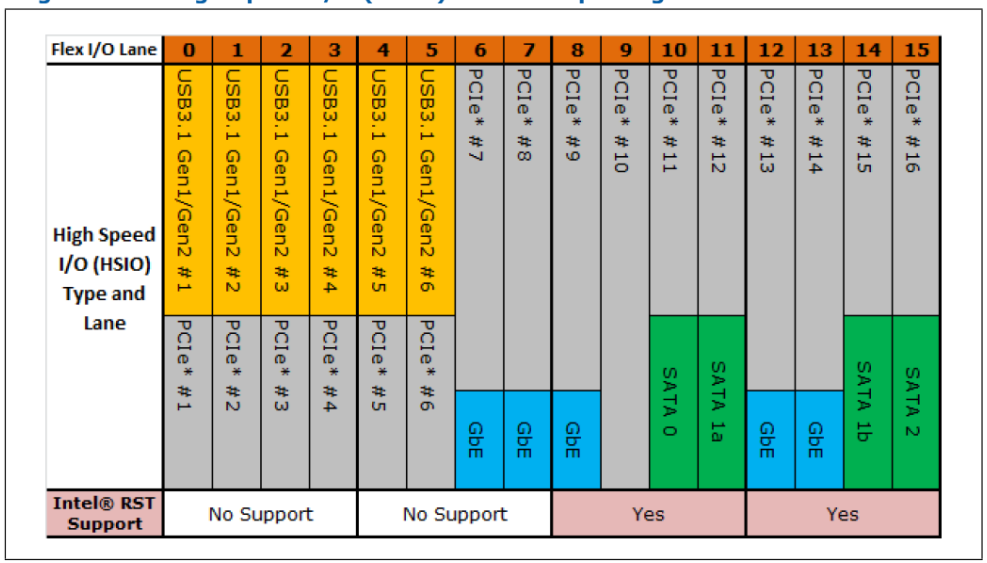


Table 6-15. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[1]	None[2]	None[3]

Notes:

1. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
2. For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
3. For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Use a non-interleaved breakout to isolate Tx and Rx.

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Wistron Corporation
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Title: PCH (PCIE,SATA,USB3,USB2)

Size: A2 | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2018 | Sheet 15 of 106

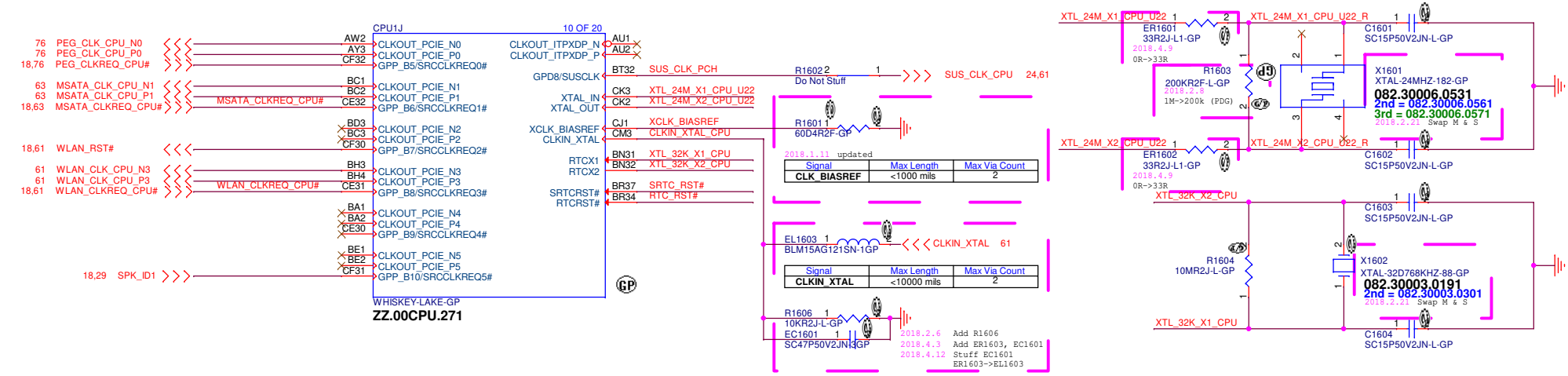
Main Func = PCH

GPU PEG BUS

SSD

WLAN

CARD



2018.1.10 updated

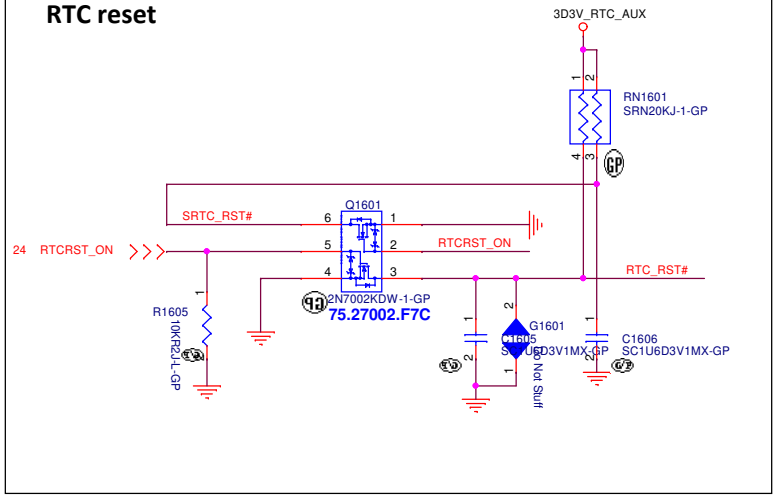
Table 7-1. Platform Clocks and Associated Signal Details and Descriptions

Signal Name	Type	SSC Capable	Description
CLKOUT_ITPXDP_P CLKOUT_ITPXDP_N	O	Yes	**Differential ITP Debug Clock:** 100 MHz differential output to processor XDP/ ITP connector on the platform
CNL U PCH-LP: • CLKOUT_PCIE_P[5:0] • CLKOUT_PCIE_N[5:0]	O	Yes	**PCI Express* Clock Output:** Serial Reference 100 MHz PCIe* 3.0 specification compliant differential output clocks to PCIe* devices
CLKOUT_LPC[1:0]	O	No	**Low Pin Count (LPC) Clock Outputs:** Single-Ended 24-MHz output to various single load connectors/devices
SRCCLKREQ#[5:0]	I/O		**Clock Request:** Serial Reference Clock request signals for PCIe* 100 MHz differential clocks
XTAL_IN	I		**Crystal Input:** Input connection for 24MHz crystal to PCH
XTAL_OUT	O		**Crystal Output:** Output connection for 24 MHz crystal to PCH
XCLK_BIASREF	I/O		**Differential Clock Bias Reference:** Used to set BIAS reference for differential clocks
CLKIN_XTAL	I		**XTAL Clock Input:** Single ended integrated CNV (Connectivity) XTAL clock input

Note:
1. SSC = Spread Spectrum Clocking
2. The SRCCLKREQ# signals can be configured to map to any of the PCH PCI Express* Root Ports while using any of the CLKOUT_PCIE_P/N differential pairs

—

RTC reset



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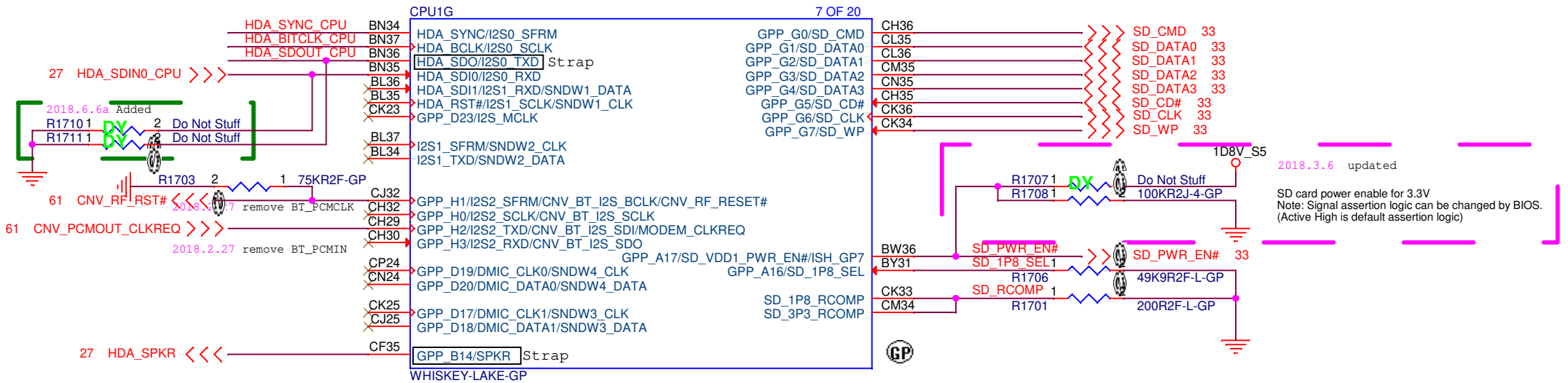
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (CLK/RTC)

Size: A3 | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2018 | Sheet 16 of 106

Main Func = PCH



ZZ.00CPU.271

2018.1.11 updated

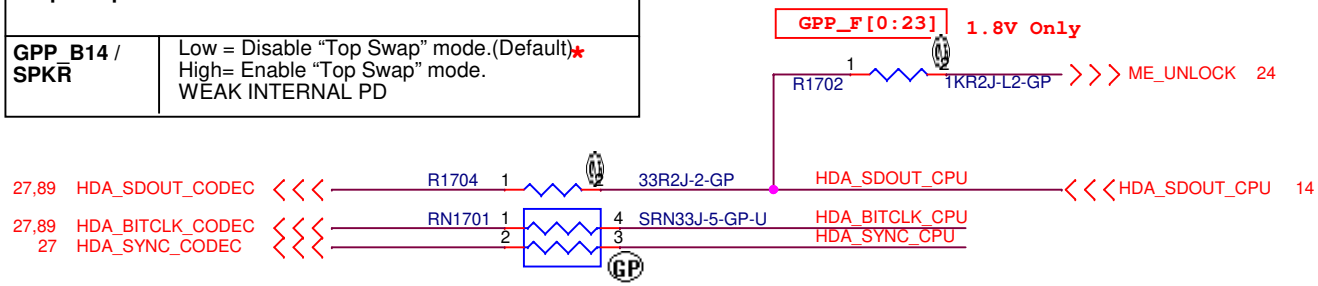
PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDO/ I2S0_TXD	Low = Security measures not override(Default)* High= Overriden WEAK INTERNAL PD

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

Top Swap Override	
GPP_B14 / SPKR	Low = Disable “Top Swap” mode.(Default)* High= Enable “Top Swap” mode. WEAK INTERNAL PD



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (AUDIO/SDIO/SDXC)

Size	Document Number	Rev
A4	FAROE 14" Pavilion	SA

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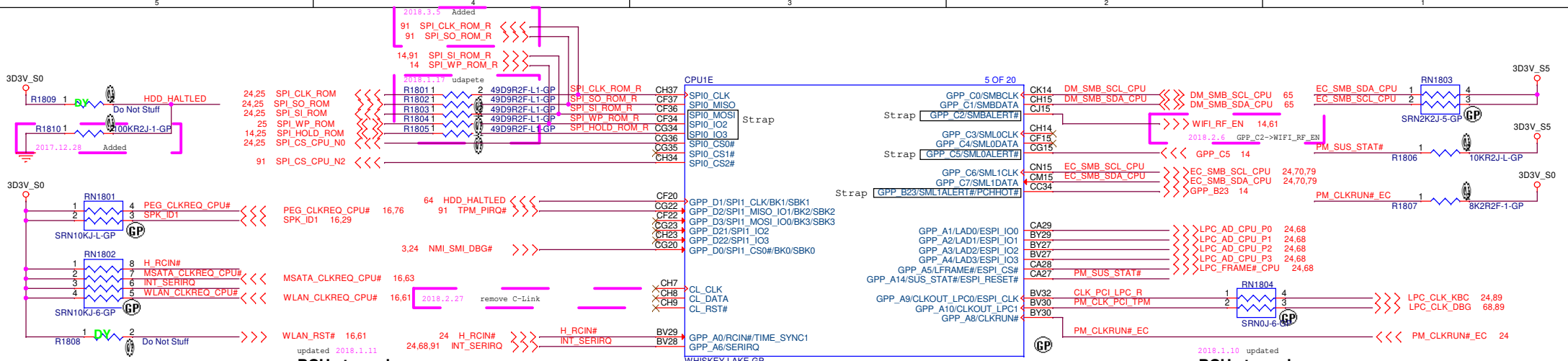

PCH strap pin:

BOOT HALT(EDS Reserved)	
SPI0_MOSI	Low = Enable High= Disable(Default)★ WEAK INTERNAL PU

This strap should sample HIGH.

PCH strap pin:

CONSENT STRAP(EDS Reserved)	
SPI0_IO2	Low = Enable High= Disable(Default)★ WEAK INTERNAL PU

This strap should sample HIGH.

PCH strap pin:

A0 PERSONALITY STRAP(EDS Reserved)	
SPI0_IO3	Low = Enable High= Disable(Default)★ WEAK INTERNAL PU

This strap should sample HIGH.

PCH strap pin:

TLS CONFIDENTIALITY Intel ME Crypto Transport Layer Security	
GPP_C2 / SMBALERT#	Low = Disable(Default)★ High= Enable WEAK INTERNAL PD

PCH strap pin:

eSPI or LPC is selected for EC	
GPP_C5 / SML0ALERT#	Low = LPC(Default) ★ High= eSPI WEAK INTERNAL PD

PCH strap pin:

EXI BOOT STALL BYPASS	
GPP_B23 / SML1ALERT# / PCHHOT#	Low = DIABLED (BSSB 4 WIRE)(Default) ★ High= ENABLED (BSSB 2+2) WEAK INTERNAL PD

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

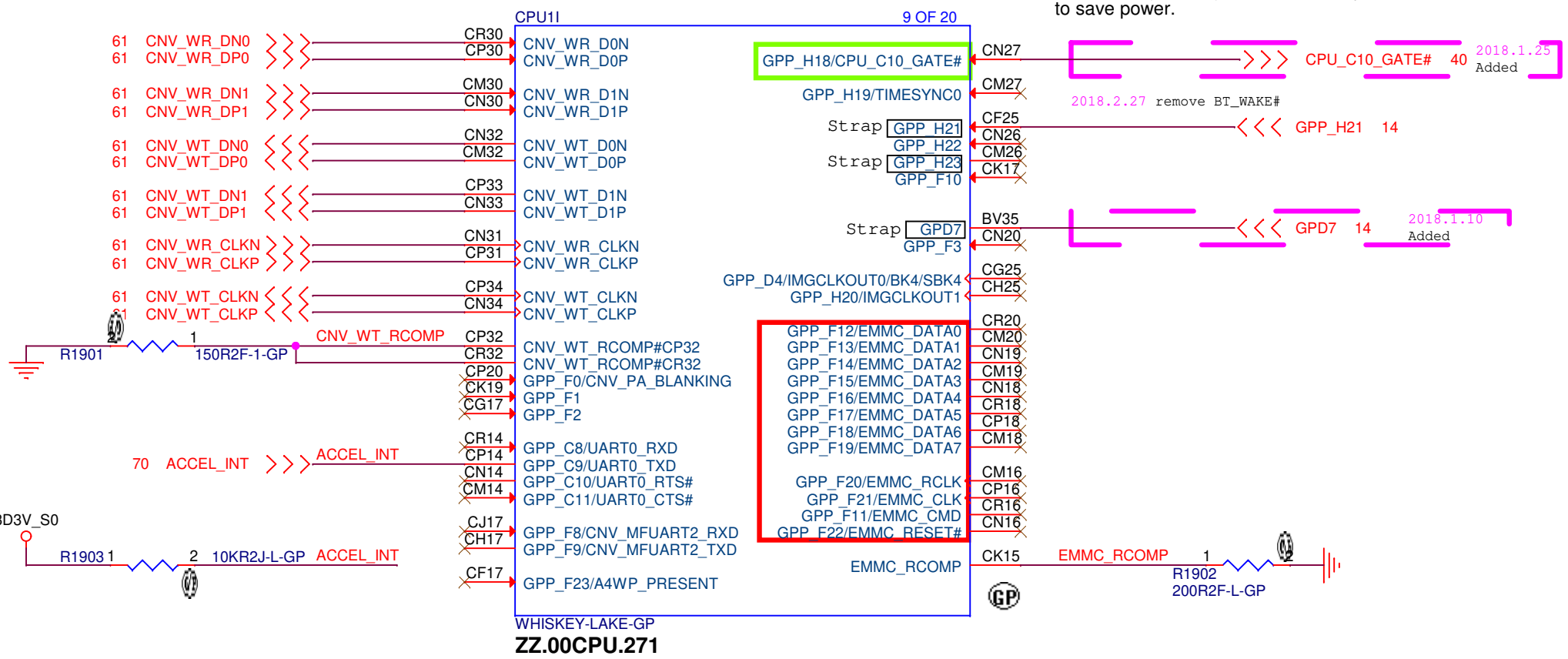
Title: ***PCH (LPC/SPI/SMBUS/CLINK)***

Size: A3 | Document Number: **FAROE 14" Pavilion** | Rev: **SA**

Date: Monday, August 06, 2018 | Sheet 18 of 106

Main Func = PCH

2018.1.12 updated
CPU_C10_GATE# is a new signal from the Whiskey Lake SoC that can be used for gating off VccSTG, VccPLL_OC and VccIO (WHL-U) in the S0/C10 system state in order to save power.



ZZ.00CPU.271

2018.1.10 updated

PCH strap pin:

XTAL INPUT MODE	HVM ONLY
GPP_H21	Low = 38.4/19.2MHZ (DEFAULT) High= 24MHZ*

2018.1.10 updated

PCH strap pin:

MAF/SAF STRAP	
GPP_H23	Low = MAF ENABLE(Default) * High= SAF ENABLE WEAK INTERNAL PD

2018.1.11 updated

PCH strap pin:

XTAL INPUT MODE(EDS Reserved)	HVM ONLY
GPD7	Low = XTAL INPUT IS SINGLE ENDED * High= XTAL IS ATTACHED WEAK INTERNAL PD?

UMA

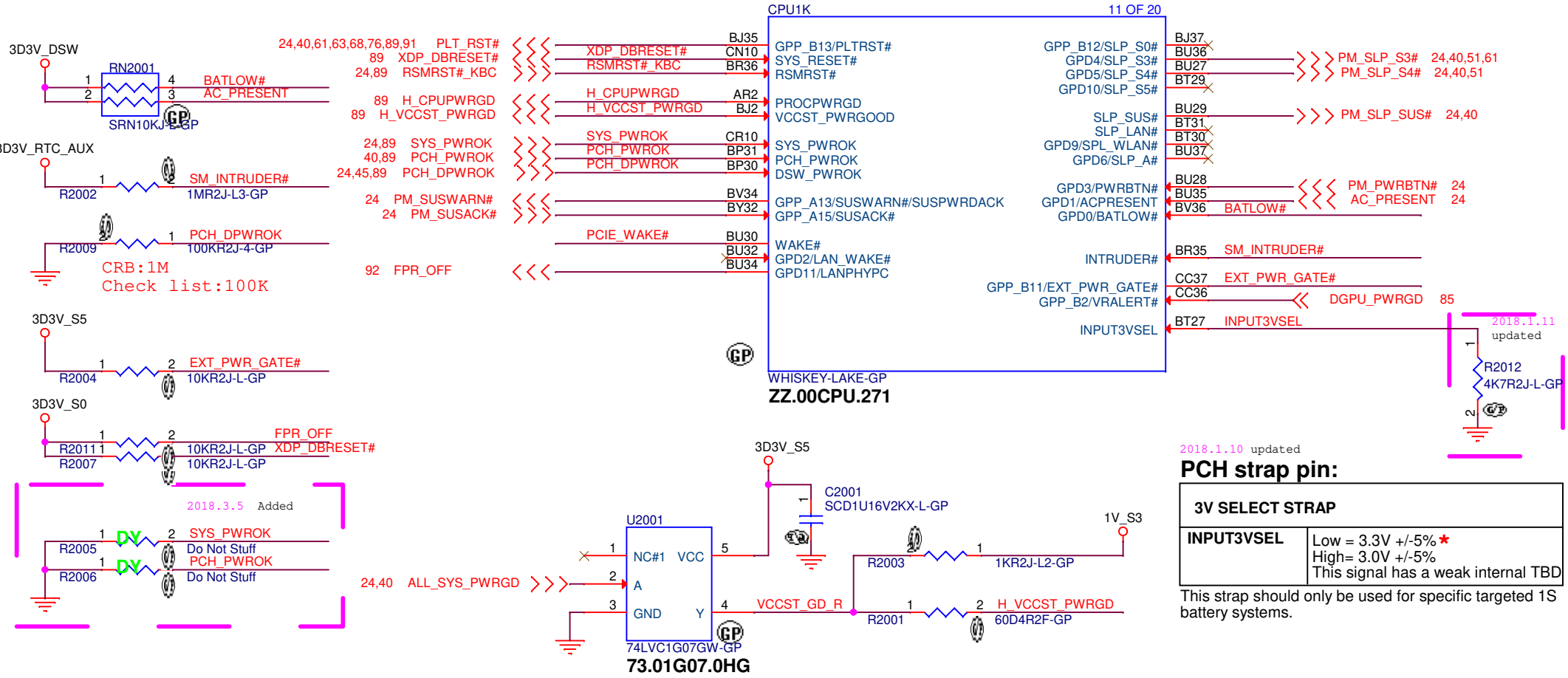
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (CSI2/EMMC)

Size: A | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2018 | Sheet 19 of 106

Main Func = PCH

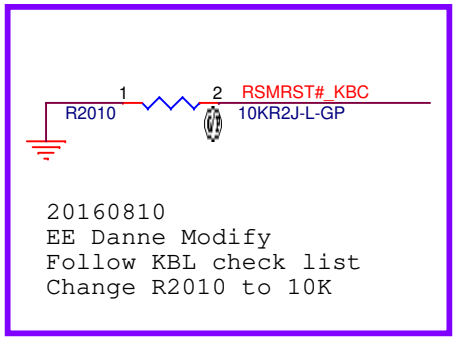


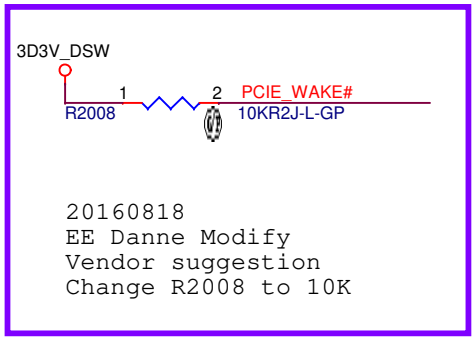
2018.1.10 updated

PCH strap pin:

3V SELECT STRAP	
INPUT3VSEL	Low = 3.3V +/-5% * High= 3.0V +/-5% This signal has a weak internal TBD

This strap should only be used for specific targeted 1S battery systems.





UMA

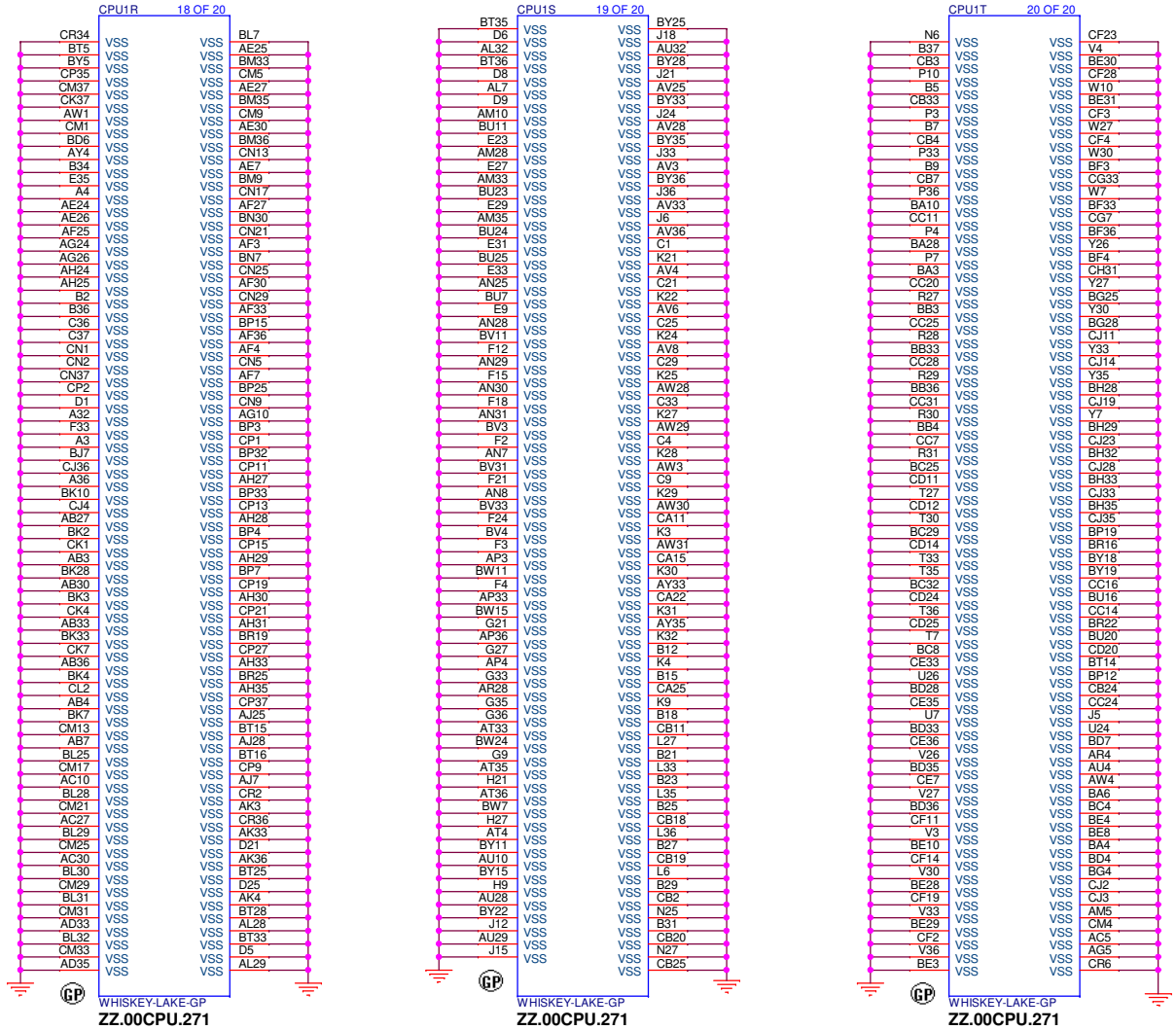
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (SYS POWER MANAGEMENT)***

Size	Document Number	Rev
A4	**FAROE 14" Pavilion**	SA

Date: Monday, August 06, 2018 Sheet 20 of 106

Main Func = PCH

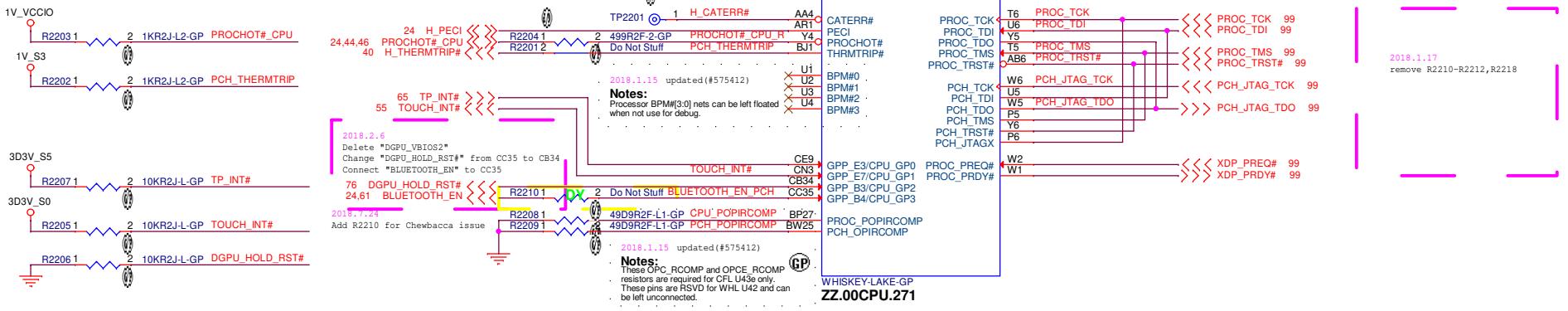


UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***PCH (VSS)***	
Size A3	Document Number **FAROE 14" Pavilion**	Rev **SA**
Date: Monday, August 06, 2018	Sheet 21 of 106	

Main Func = CPU



2018.1.15 updated

#575412 PDG rev.0.7

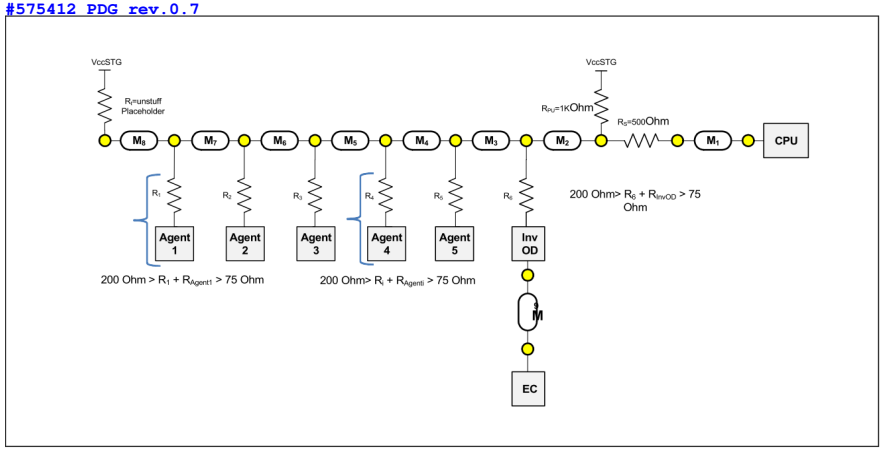


Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1496.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254	254	10000	10000
Topology Guidelines							
Platform resistors values	Rpu=1KΩ, Rs=500Ω, Ri+Ragent=75-200Ω, R6+Rinvod=75-200Ω						
Platform resistors tolerances	± 5%						

Table 7-11. PROCHOT# Routing Guidelines (Sheet 2 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
Agent's series resistor	If an Agent's internal pulldown resistance is >75Ω then additional series platform resistor is not needed						

2018.1.15 updated

#575412 PDG rev.0.7

Figure 7-16. Routing Illustration for THERMTRIP# Topology

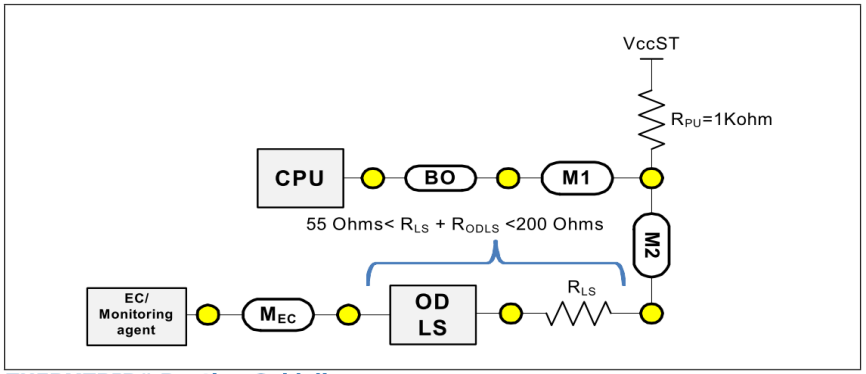


Table 7-15. THERMTRIP# Routing Guidelines

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
BO	MS/SL/DSL	VSS	1	13	775	511.81	30511.8
M1	MS/SL/DSL	VSS	2	254		10000	
M2	MS/SL/DSL	VSS	2	254		10000	
M3	MS/SL/DSL	VSS	2	254		10000	
Topology Guidelines							
Platform resistors values	Rpu=1KΩ, Rls+Rodls=55-200Ω						
Platform resistors tolerances	± 5%						
EC/monitoring Agent	THERMTRIP# should be connected to EC or any other monitoring agent.						

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (JTAG/CPU SIDE BAND)**

Size: A3 | Document Number: **FAROE 14" Pavilion** | Rev: **SA**

Date: Monday, August 06, 2018 | Sheet 22 of 106

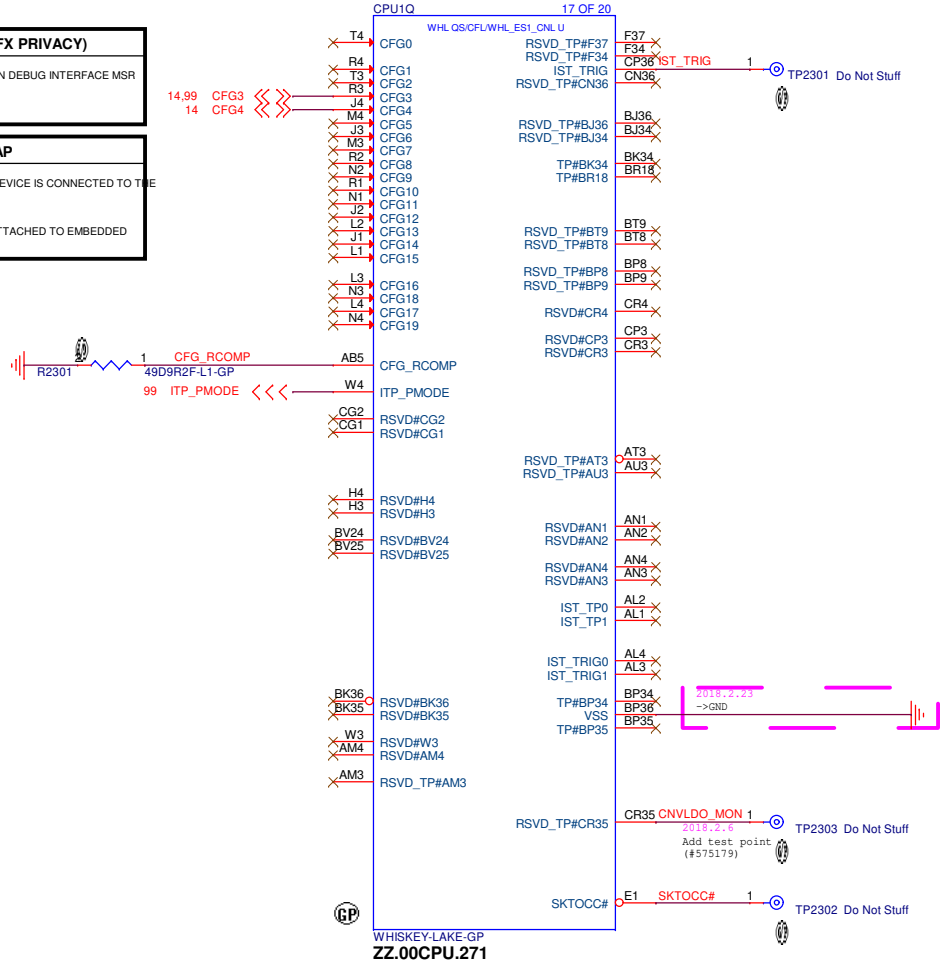
Main Func = CPU

2018.1.12 updated

CPU strap pin:

PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG3	Low = ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR High= DISABLED*

DISPLAY PORT PRESENCE STRAP	
CFG4	Low = ENABLED* AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT High= DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT



2018.1.15 updated

#575962 RVP Rev0.5 P.32~33

Description

```
CFG[0]:EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED
    1 : (DEFAULT) NORMAL OPERATION; NO STALL
    0 : STALL

CFG[1]:PCH/ PCH LESS MODE SELECTION
    1 : (DEFAULT) NORMAL OPERATION
    0 :  PCH-LESS MODE

CFG[2]:PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS
    1 : (DEFAULT)NORMAL OPERATION;
    0 : LANE REVERSAL

CFG[3]:PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)
    0 : ENABLED
    SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
    1 : DISABLED

CFG[4]:DISPLAY PORT PRESENCE STRAP
    0 :  ENABLED
    AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED
    DISPLAY PORT
    1 :  DISABLED
    NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

CFG[6:5]:PCIE PORT BIFURCATION STRAPS
    11 : DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED
    10 : DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED
    01 : DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED
    00 : DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED

CFG[7]:PEG DEFER TRAINING
    1 : (DEFAULT) PEG TRAIN IMMEDIATELY
    FOLLOWING XXRESETB DE ASSERTION
    0 : PEG WAIT FOR BIOS FOR TRAINING

CFG[8]:ALLOW THE USE OF NOA ON LOCKED UNITS
    1 : DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN
        LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS
    0 : ENABLED; NOA WILL BE AVAILABLE REGARDLESS
        OF THE LOCKING OF THE UNIT

CFG[9]:NO SVID PROTOCOL CAPABLE VR CONNECTED
    1 : VRS SUPPORTING SVID PROTOCOL ARE PRESENT
    0 : NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE
        (OR RESPOND TO) SVID ACTIVITY

CFG[10]:SAFE MODE BOOT
    1 : POWER FEATURES ACTIVATED DURING RESET
    0 : POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

CFG[11]:DMI AC COUPLING - JUST A PLACE HOLDER. NOT APPLICABLE FOR
ULX-ULT
    1 : (DEFULT)DMI WILL BE CONFIGURED AS HALF SWING DC COUPLED
    0 : DMI WILL BE CONFIGURED AS FULL SWING AC COUPLED

CFG[12]:PM SYNC LEGACY
THIS STRAP IS NEW IN SKL. IT TELL THE CPU THAT IT IS CONNECTED TO
PCH SUPPORTING OLDER VERSION OF PMSYNC PROTOCOL IN LEGACY MORE CPU
DOESN'T WAIT FOR EPOC MESSAGE FROM THE PCH
    1 : (DEFAULT)  PMSYNC 2.0
    0 : LEGACY

CFG[13]:PMSYNC AYNC MODE- PM SYNC
    1 : (DEFAULT)SYNCHCRONOUS (1 24 MHZ CYCLE PER BIT)
    0 : ASYNC - 4-24MHZ CYCLES PER BIT
```

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Title	CPU (RESERVED,CFG)	
Size A3	Document Number FAROE 14" Pavilion	Rev SA
Date: Monday, August 06, 2018	Sheet 23 of 106	

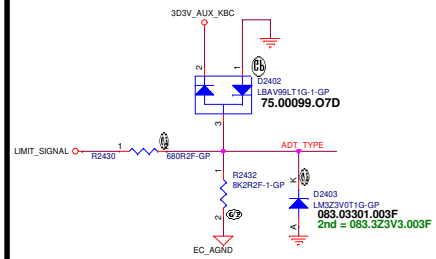
SSID = KBC

KBC9028Q

CONFIRM EC THIS PIN PM_PWRBTN# PIN HI OUPUT

S0_PWR_GOOD ==DELAY 99ms

HP Limit Signal Detect



		RID	RP	RS	
	v	k ohm	k ohm	k ohm	ADT_TYPE_AD(V)
45w	19.5	499	0.68	8.2	0.3148
65w	19.5	383	0.68	8.2	0.4080
90w	19.5	294	0.68	8.2	0.5279
120w	19.5	221	0.68	8.2	0.6956
135w	19.5	169	0.68	8.2	0.8989
150w	19.5	130	0.68	8.2	1.1514
180w	19.5	100	0.68	8.2	1.4686
200w	19.5	85.207	0.68	8.2	1.6995
230w	19.5	72.752	0.68	8.2	1.9588
reserve	19.5	64.9	0.68	8.2	2.1673
reserve	19.5	57.6	0.68	8.2	2.4052
330w	19.5	42.2	0.68	8.2	3.1304

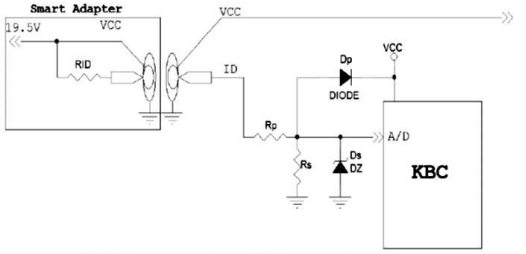
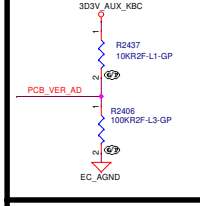


FIGURE 3. Smart Adapter EC Detection Schematic

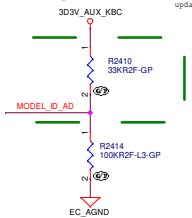
R2410
10.0K ---> 64.10025.L0L (UMA U42
20.0K ---> 64.20025.L0L (4G U42
33.0K ---> 64.33025.6DL (2G U42
47.0K ---> 64.47025.6DL (UMA U22
64.9K ---> 64.64925.6DL (4G U22
76.8K ---> 64.76825.6DL (2G U22

PCB VERSION : SA



PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.524 V	< 1.126 V

MODEL ID



MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	ECRAM 0x67
14" Intel WHL-U42 UMA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	0x01
14" Intel WHL-U42 DIS N16S x16	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V 0x02
14" Intel WHL-U42 DIS N16S x32	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V 0x03
14" Intel WHL-U22 UMA	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V 0x04
14" Intel WHL-U22 DIS N16S x16	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V 0x05
14" Intel WHL-U22 DIS N16S x32	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V 0x06
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.958 V	< 1.126 V
Reserved for project use	100.0 K	280.0 K	0.868 V	0.881 V	>= 0.809 V	< 0.958 V
Reserved for project use	100.0 K	340.0 K	0.750 V	0.762 V	>= 0.664 V	< 0.809 V
Reserved for project use	100.0 K	470.0 K	0.579 V	0.589 V	>= 0.519 V	< 0.664 V
Reserved for project use	100.0 K	620.0 K	0.458 V	0.466 V	>= 0.229 V	< 0.519 V

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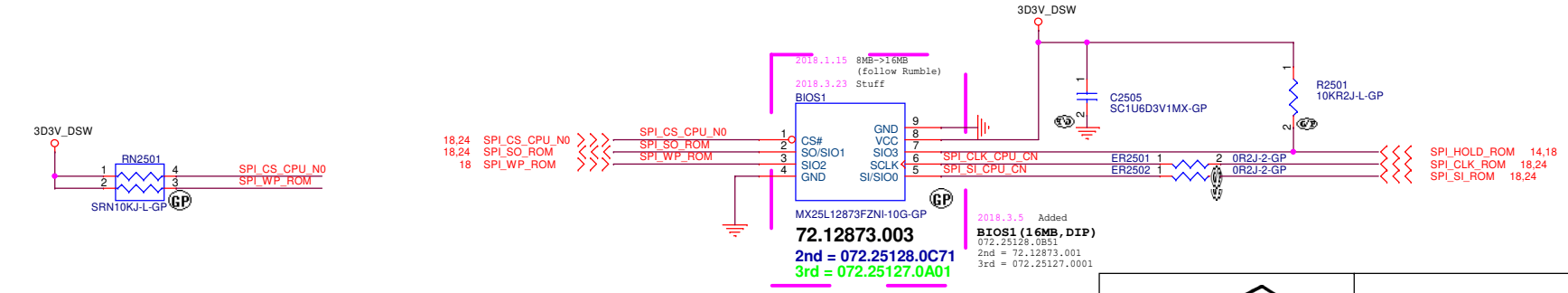
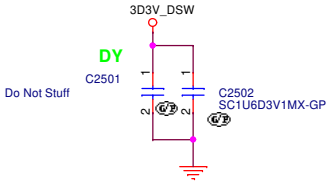
Title: ECIO(ENE KB9028)

Size: A2 | Document Number: FAROE 14" Pavilion | Rev: SA

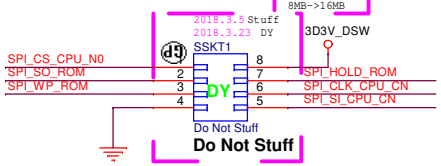
Date: Monday, August 06, 2018 | Sheet 24 of 106

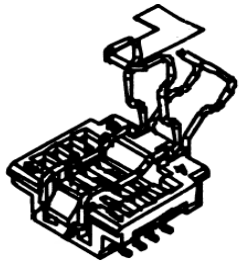
SSID = Flash.ROM



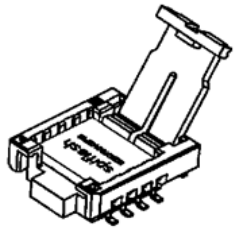


SPI FLASH ROM 16M byte





62.10089.011

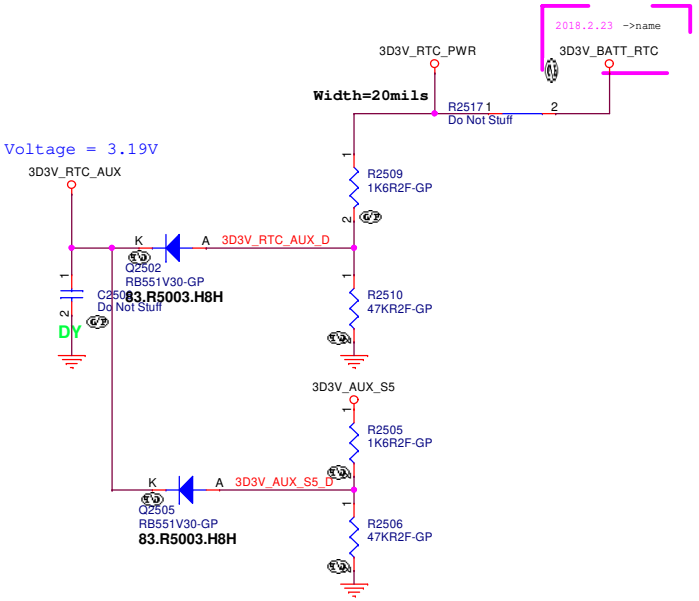


062.10029.0001

V

Co-lay with BIOS1

SSID = RBAT



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Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size	Document Number	Rev
A3	FAROE 14" Pavilion	SA

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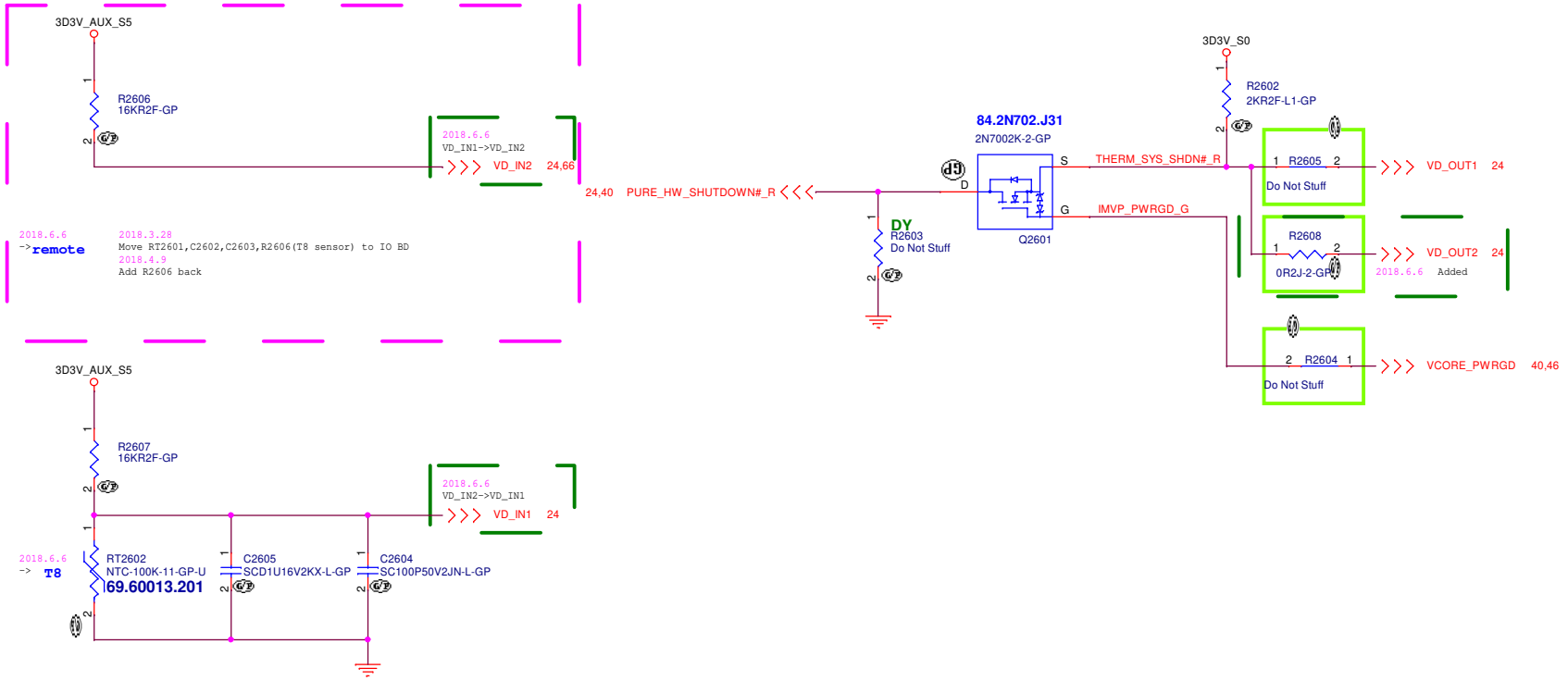
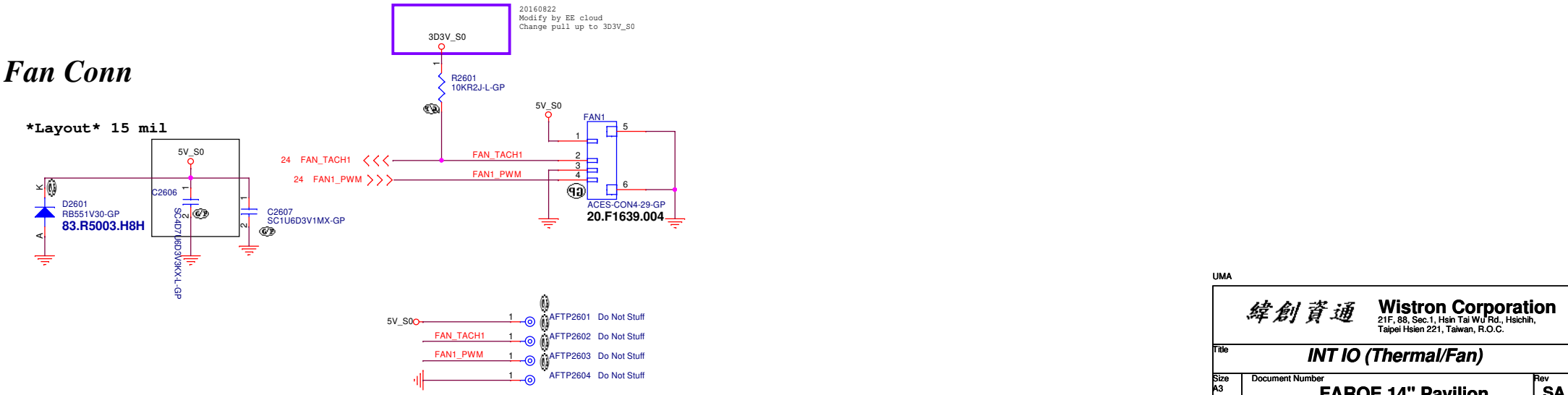
SSID = Thermal

Thermal sensor NCT 7718W



Fan Conn



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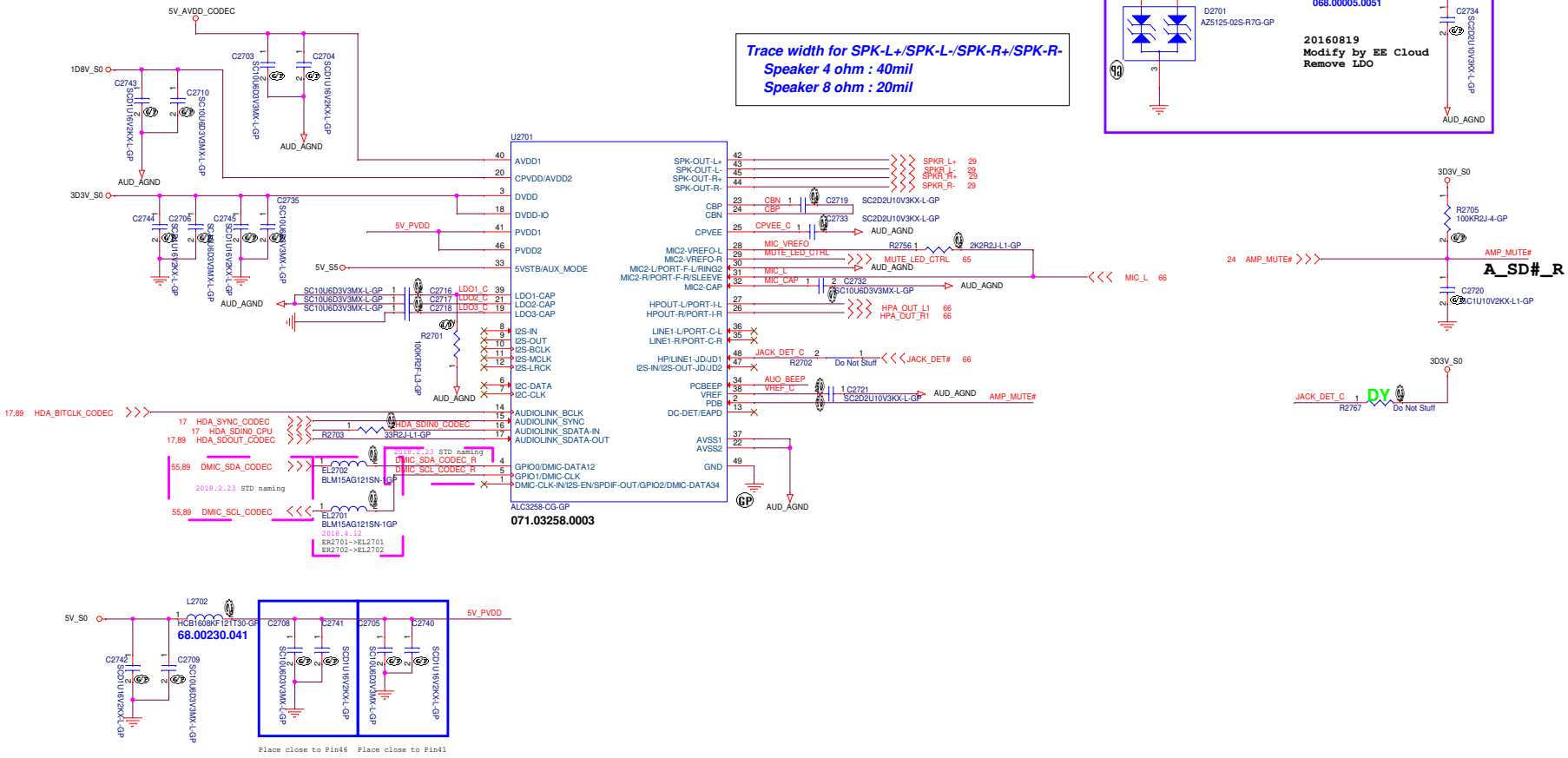
Taipei Hsien 221, Taiwan, R.O.C.

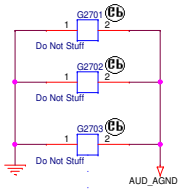
Title	***INT IO (Thermal/Fan)***	
Size A3	Document Number **FAROE 14" Pavilion**	Rev **SA**
Date: Monday, August 06, 2018	Sheet 26 of 106	



AMP. for Headphone

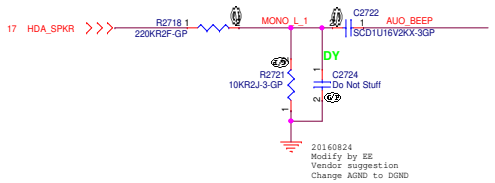
Digital GND & AUD_AGND

Tie Analog GND and Digital GND under codec by a single point



audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

PC BEEP



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Taipei Hsien 221, Taiwan, R.O.C.

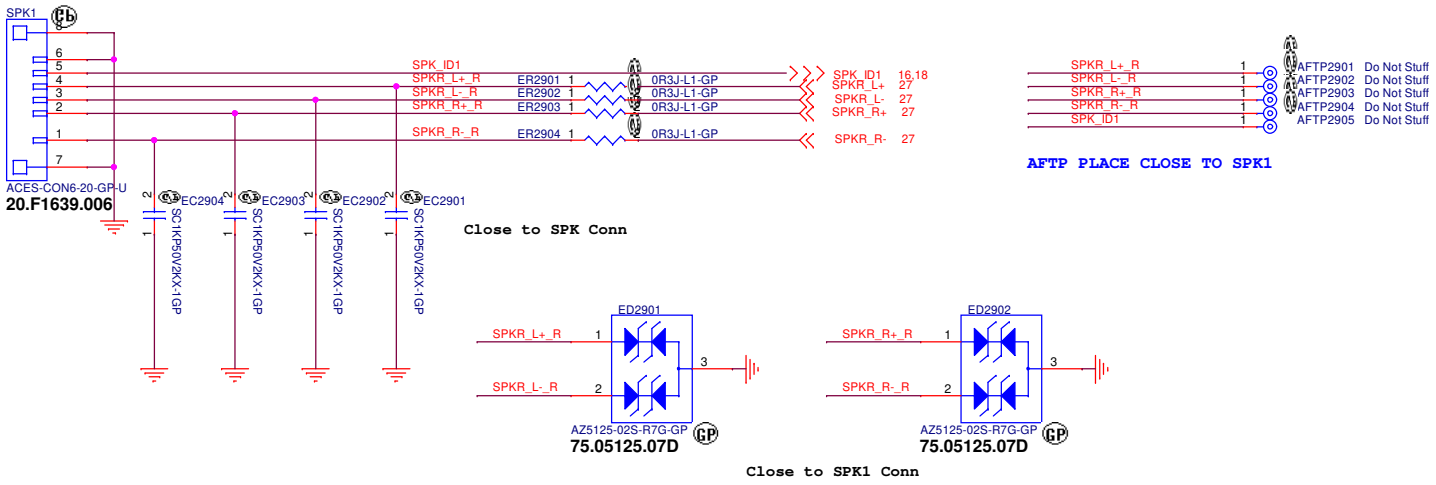
Title: **Audio (Codec ALC3258)**

Size	Document Number	Rev
C	FAROE 14" Pavilion	SA

Date: Monday, August 06, 2018 Sheet 27 of 106

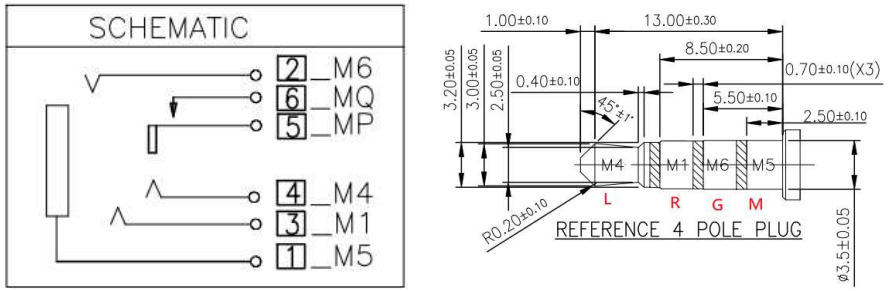
Audio_Speaker

Speaker vendor	FG	Sable
SPK_ID (0 or 1)	1	0



Audio_Jack

Combo-Jack (Headphone & MIC)



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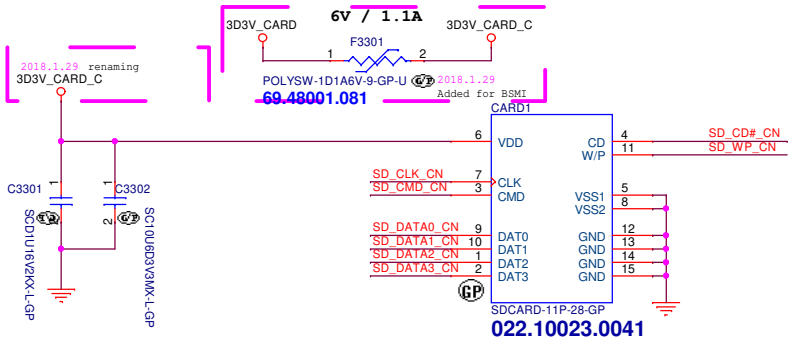
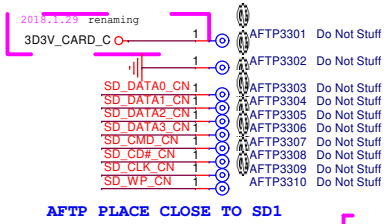
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Audio (HP/SPK/MIC Jack)		
Size A3	Document Number FAROE 14" Pavilion	Rev SA
Date: Monday, August 06, 2018	Sheet 29 of 106	

Cardreader IC & Cardreader Connector

SSID = CardReader



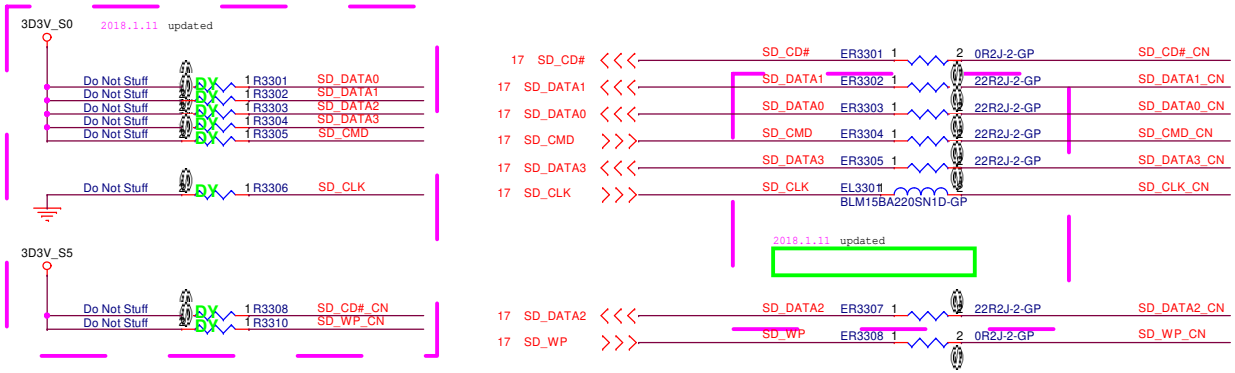


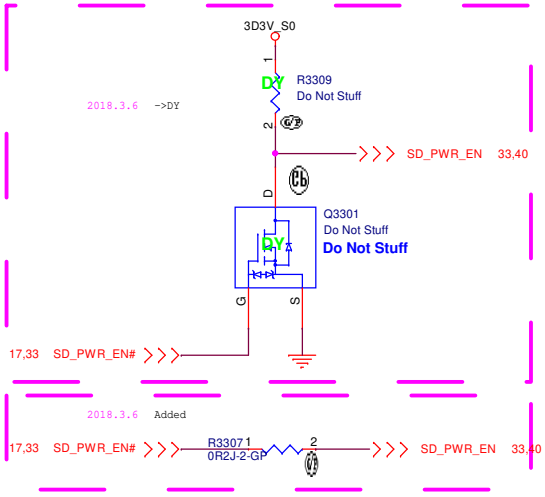
AFTP PLACE CLOSE TO SD1

with out card	CD — CD WP — WP
inserted card (unlock)	CD — CD WP — WP
inserted card(lock)	CD — CD WP — WP

Pin Define

Connector Pin No.	SD Card Pin No.	Pin Define
P1	P9	DAT2
P2	P1	DAT3
P3	P2	CMD
P4		CD
P5	P3	VSS1
P6	P4	VDD
P7	P5	CLK
P8	P6	VSS2
P9	P7	DATO
P10	P8	DAT1
P11		W/P
P12		GND
P13		GND
P14		GND
P15		GND





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Taipei Hsien 221, Taiwan, R.O.C.

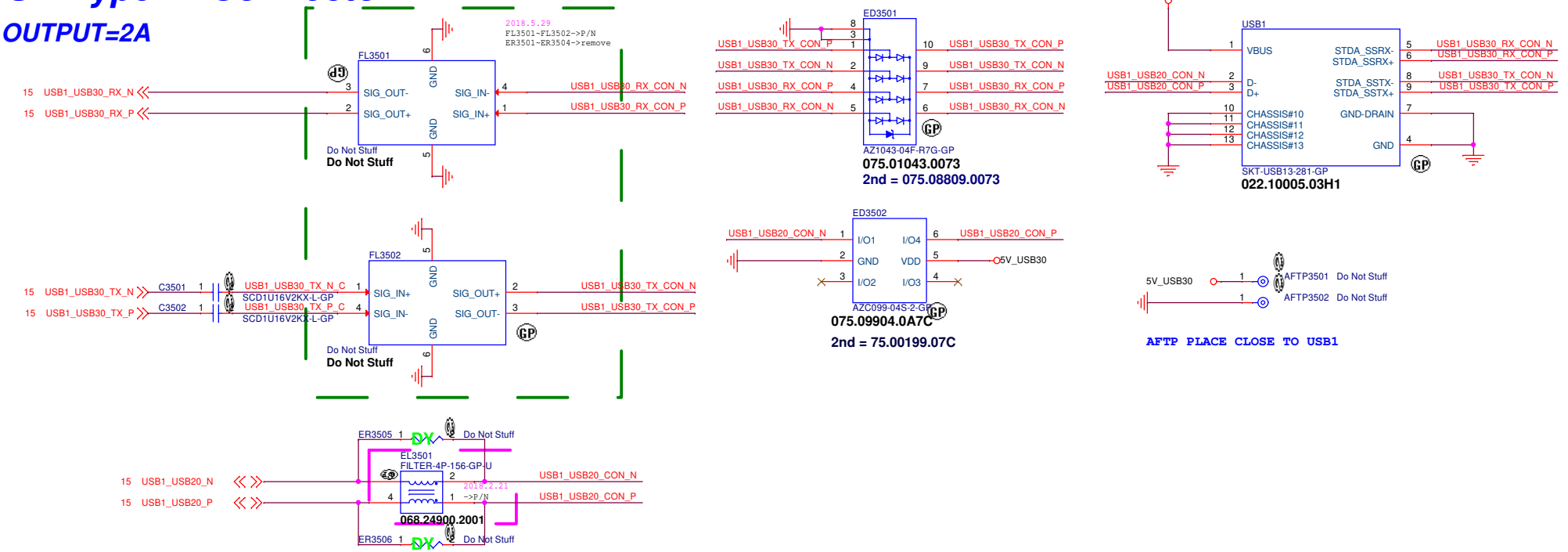
Title: ***CARDREADER (SDIO/SD Conn)***

Size	Document Number	Rev
A3	**FAROE 14" Pavilion**	SA

Date: Monday, August 06, 2018 Sheet 33 of 106

USB Type A Connector

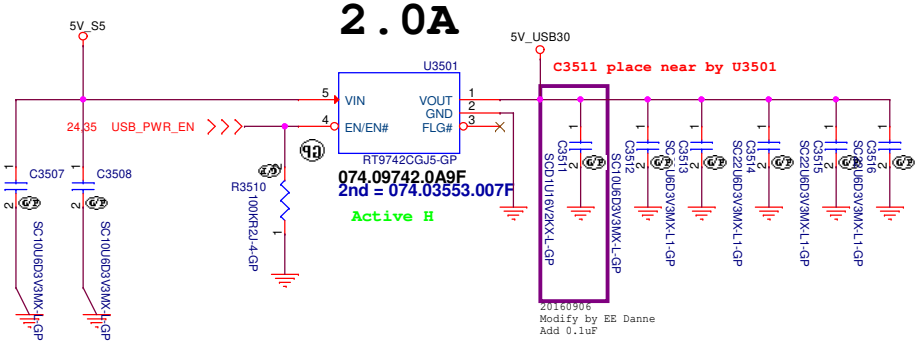
OUTPUT=2A



USB3 Power Switch

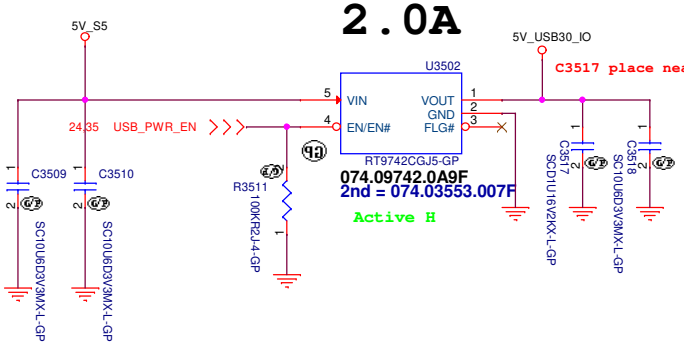
U3501 place close to USB1

2.0A



U3502 place close to IO1

2.0A



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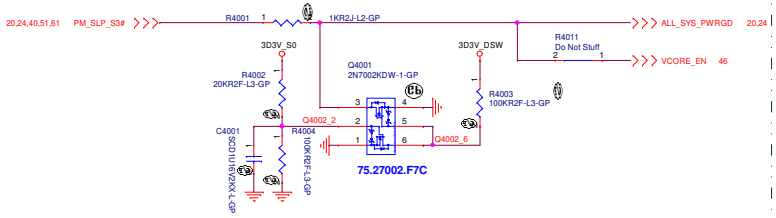
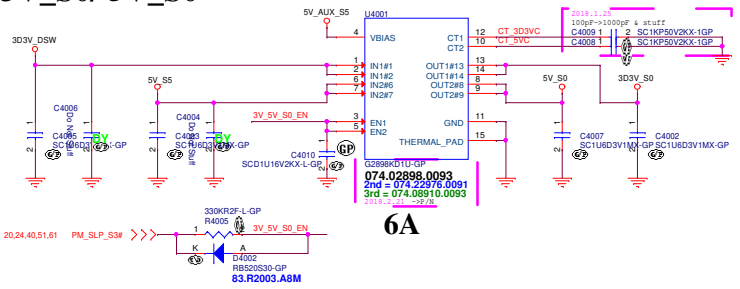
Title: USB (USB3.0 Conn)		
Size: A3	Document Number: FAROE 14" Pavilion	Rev: SA
Date: Monday, August 06, 2018	Sheet 35 of 106	

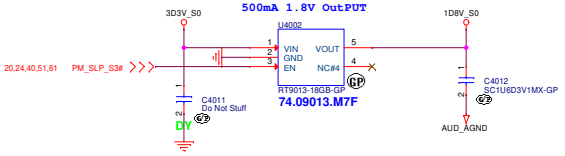
ALLSYSPWRGO/ VCORE ENABLE



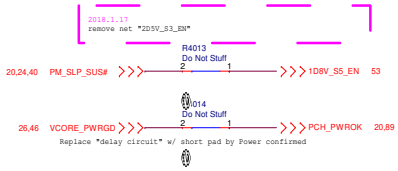
3D3V_S0/ 5V_S0



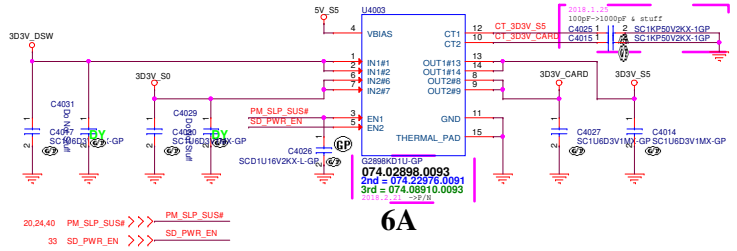
1D8V_S0



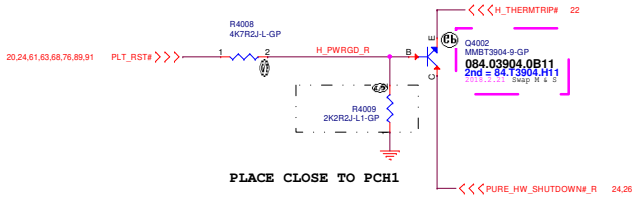
Power Sequence



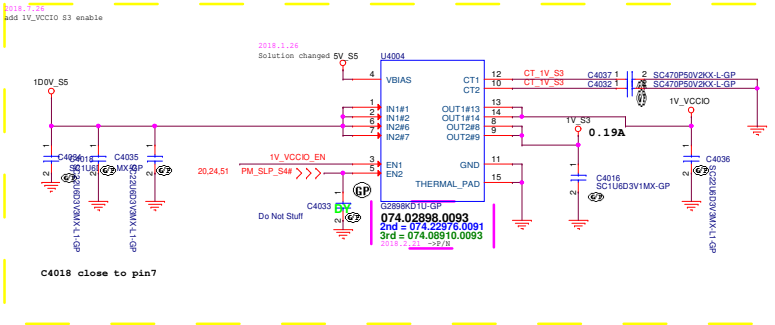
3D3V_S5/ 3D3V_CARD



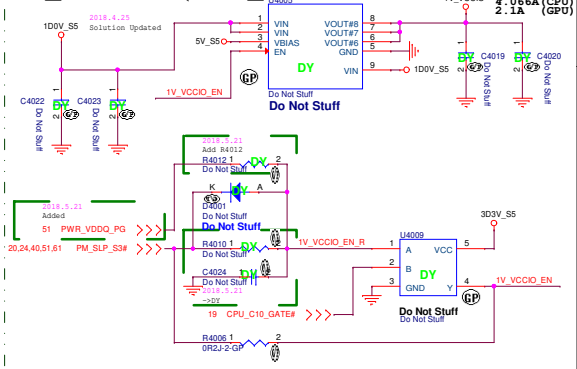
HW_SHUTDOWN



1V_S3/1V_VCCIO (S3 Enable)



1V_VCCIO (G10_GATE ENABLE)



UMA

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Title: Sequence (Power Plane Enable)		
Size: A2	Document Number: FAROE 14" Pavilion	Rev: SA
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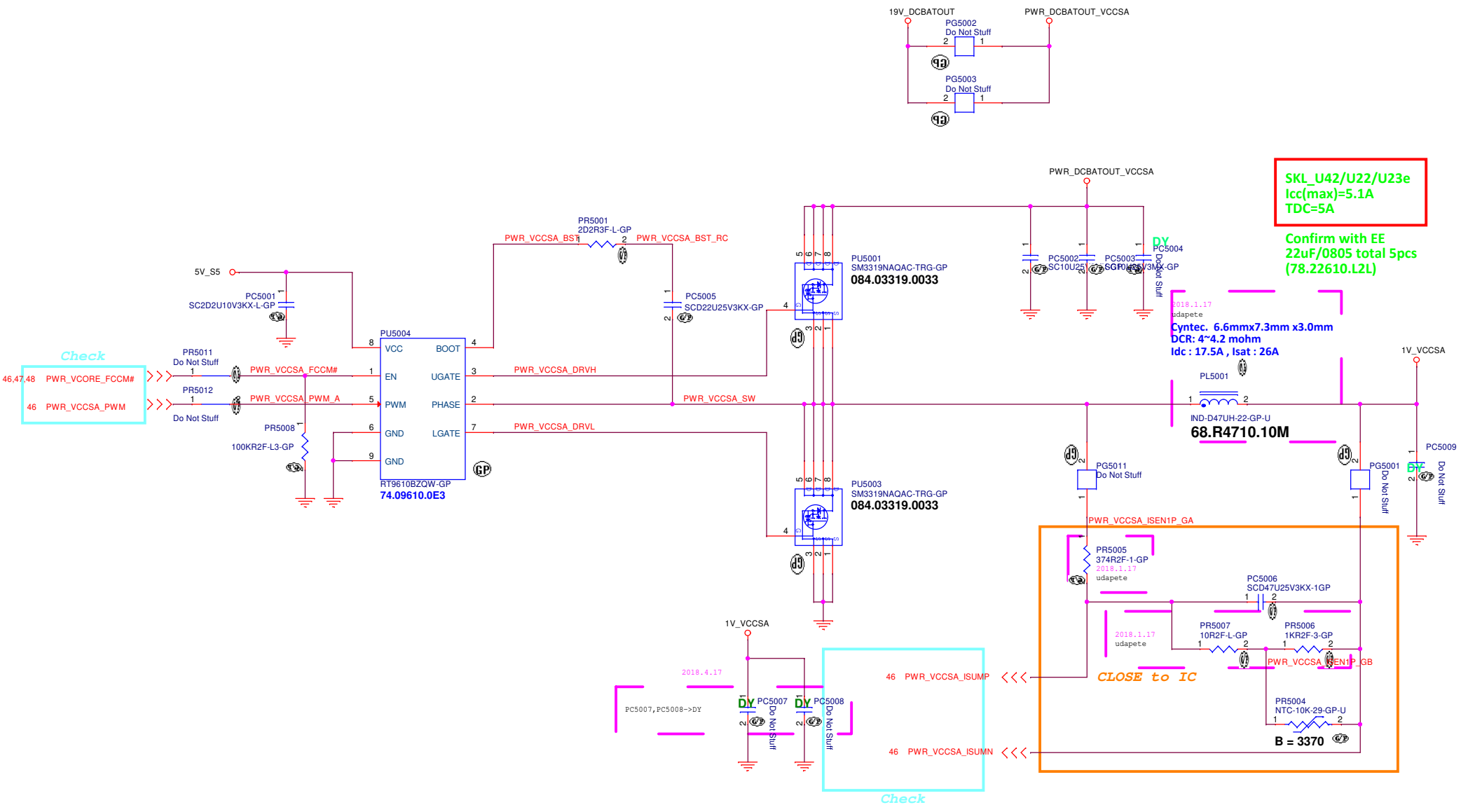
Main Func = CPU_CORE



UMA

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Title: Power (ISL95808_CPU_VCCSA)		
Size: A3	Document Number: FAROE 14" Pavilion	Rev: SA
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OFFPAGE

S5

20,24,40 PM_SLP_S4# — R5102 0R2J-L-GP — PWR_VDDQ_EN

DY

C5116 Do Not Stuff

S3

4 VTT_CNTL — R5103 0R2J-L-GP — PWR_VTT_EN

20,24,40,61 PM_SLP_S3# — R5101 SB 20151020 EE Do Not Stuff

DY

PH on EE Side

40 PWR_VDDQ_PG — PWR_VDDQ_PG

OFFPAGE_GAP

19V_DCBATOUT — PG5101 Do Not Stuff — PWR_DCBATOUT_VDDQ

PG5102 Do Not Stuff

PG5103 Do Not Stuff

1D2V_S3 — PG5105 Do Not Stuff — PWR_VDDQ

PG5106 Do Not Stuff

PG5107 Do Not Stuff

PG5108 Do Not Stuff

PG5109 Do Not Stuff

PG5110 Do Not Stuff

PG5112 Do Not Stuff

PG5114 Do Not Stuff

1D2V_S3 — PG5115 Do Not Stuff — PWR_VDDQ_VLDOIN

0D6V_VREF_S0 — PG5111 Do Not Stuff — PWR_VDDQ_VTT

3D3V_S5 — PG5119 Do Not Stuff — PWR_VDDQ_V3V

2D5V_S3 — PG5118 Do Not Stuff — PWR_VDDQ_V2P5

PC5104因為layout關係所以直接下PGND即可
獨立下地並遠離NOISE

DY PC5102 Do Not Stuff

If 5V has droop
Please mount it

5V_S5 — PR5101 10R2J-L-GP — PWR_VDDQ_PH — PR5108 620KR2F-GP

PC5104 SC10U6D3V3MX-L-GP — PWR_VDDQ_V3V

DDR_AGND

3D3V_S5 — PR5104 Do Not Stuff — DY

PC5117 SC10U6D3V3MX-L-GP

PU5101 G5416QS1U-GP

TON, VCC, GND, V3V, S3, S5, PGOOD, VLODIN, VTT, VTTGND, VTTSNS, VTTREF, VDDQSNS, VDDQSET, BST, LX#12, LX#11, LX#10, LX#9, LX#32, V2P5, PGND

PWR_VDDQ_TON, PWR_VDDQ_VCC, PWR_VTT_EN, PWR_VDDQ_EN, PWR_VDDQ_PG, PWR_VDDQ_VLDOIN, PWR_VDDQ_VTT, PWR_VDDQ_VTTSNS, PWR_VDDQ_VTTREF, PWR_DCBATOUT_VDDQ, PWR_VDDQ_BOOT, PWR_VDDQ_BOOTA, PWR_VDDQ_PH, PWR_VDDQ_V2P5

PR5111 Do Not Stuff — PC5110 SCD1U25V2KX-L-GP — DY — PC5108 — PC5101 SC10U25V3MX-GP — PC5105 SC10U25V3MX-GP

2018.7.25 Change to 0603

PWR_DCBATOUT_VDDQ

TDC : 8A

Cyntec. 7 x 7 x 3.0 mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A

PL5101 COIL-1UH-34-GP-U1

PC5116 SC22U6D3V3MX-L-GP

PR5110 Do Not Stuff — DY

PC5115 — PWR_VDDQ_SNS — PR5113 — PG5104 Do Not Stuff

Close to PC5113

PC5106 — PC5107 — PC5109 — PC5113

SC22U6D3V3MX-L-GP
SC22U6D3V3MX-L-GP
SC22U6D3V3MX-L-GP
SC22U6D3V3MX-L-GP

PWR_VDDQ_VDDQSET_A

R1 PR5105 6K2R2F-GP — PC5124 Do Not Stuff — DY

R2 PR5106 10K2R2F-GP

DDR_AGND

PC5118 SC10U6D3V3MX-L-GP

PC5111 — PC5112 — DY — Do Not Stuff SC10U6D3V3MX-L-GP

PC5114 SCD1U16V2KX-L-GP — DDR_AGND

PG5120 Do Not Stuff — DDR_AGND

PWR_VDDQ_VTT — PR5112 Do Not Stuff

PWR_VDDQ_VDDQSNS

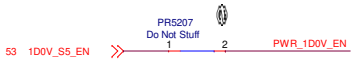
PWR_VDDQ_VDDQSET

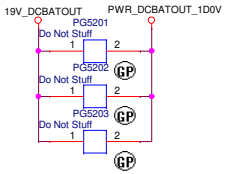
Vout= 0.75*(1+R1/R2) = 1.2

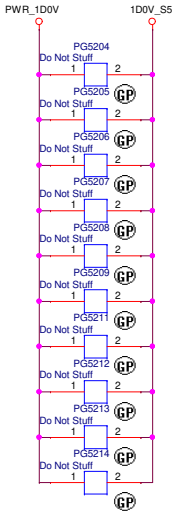
UMA

Title	<Title>	
Size A2	Document Number FAROE 14" Pavilion	Rev <RevCode>
Date: Monday, August 06, 2018	Sheet 51 of 106	

OFFPAGE



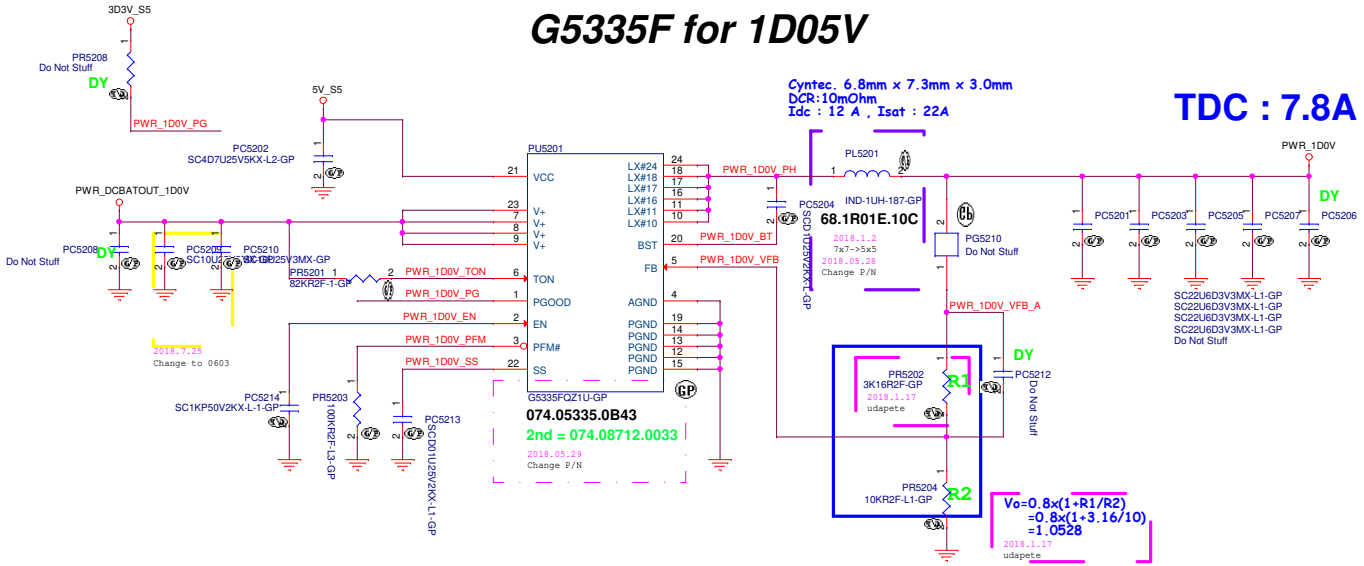




IC / COM	AOZ2262(10A) 074.02262.0043	AOZ2261(8A) 074.02261.0A73	AOZ2260(6A) 074.02260.0043
Chock	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1

SSID = PWR.Plane.Regulator_1p0v

G5335F for 1D05V



TDC : 7.8A

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (AOZ2262QI_1D0V)

Size: Custom | Document Number: FAROE 14" Pavilion | Rev: SA

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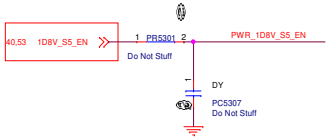
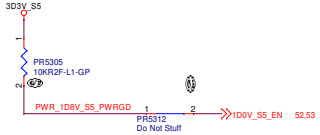
1D8V_S5 POWER GOOD

52,53 1D0V_S5_EN

1D8V_S5 ENABLE

40,53 1D8V_S5_EN





1D8V_S5

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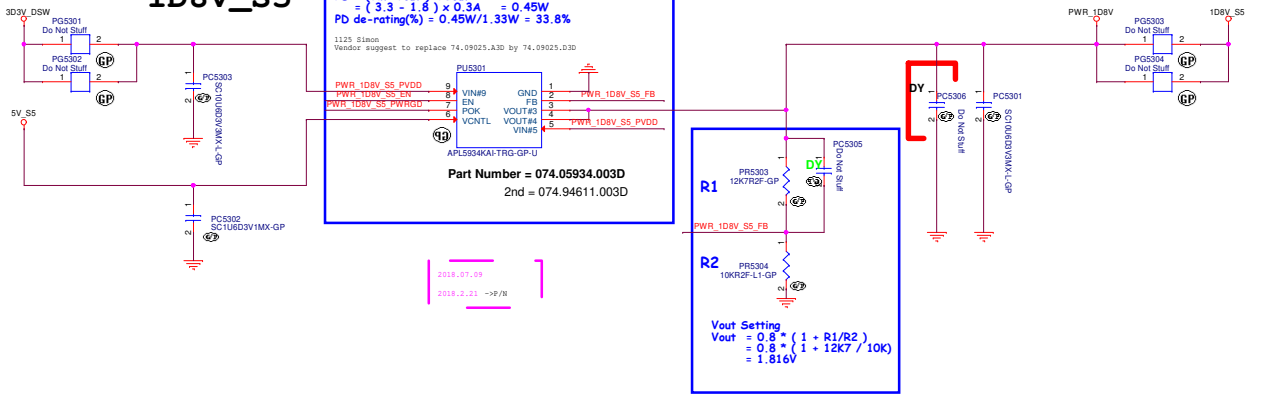

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power (RT9025_1D8V)**

Size	Document Number	Rev
A2	FAROE 14" Pavilion	SA

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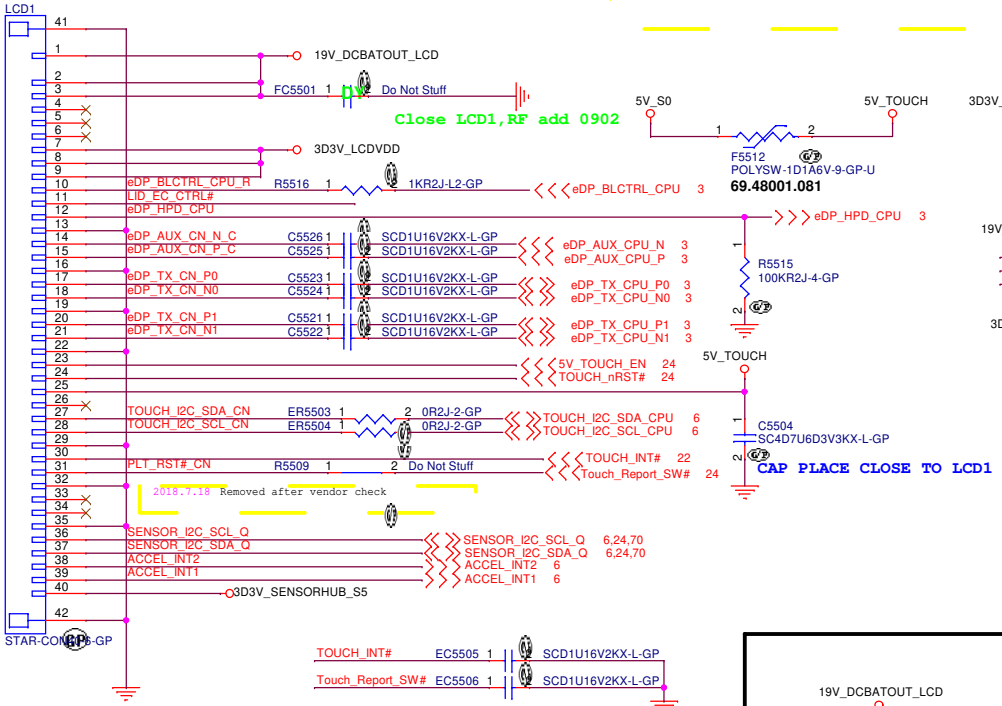
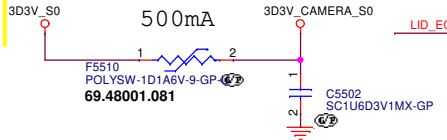
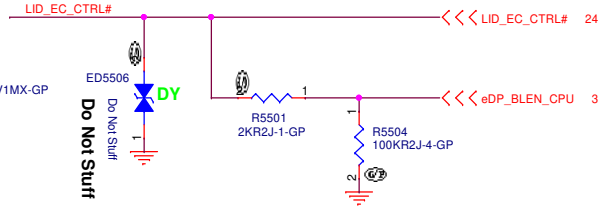
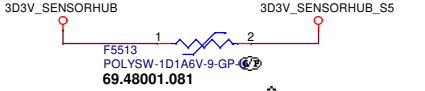
eDP + G-sensor + Touch Connector

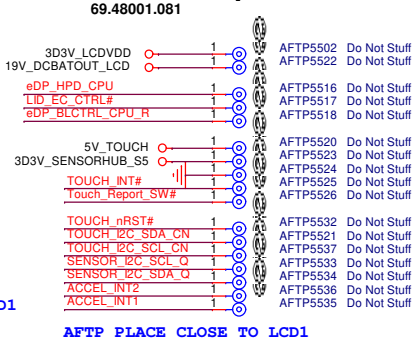


2018.7.19 Removed IR

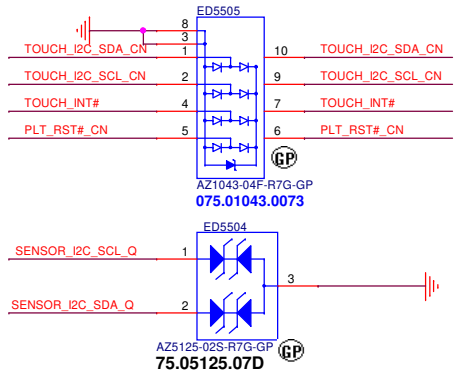




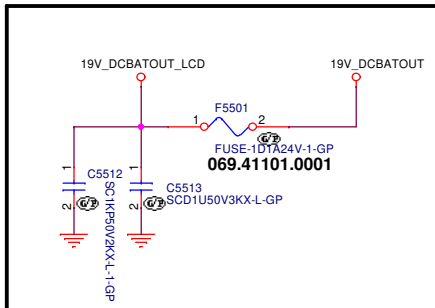


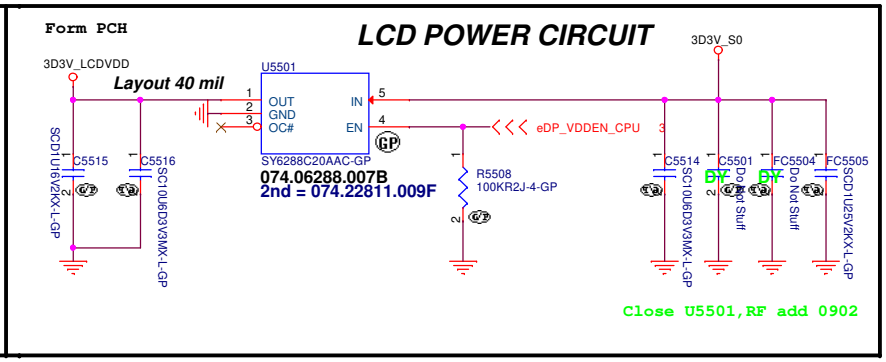


AFTP PLACE CLOSE TO LCD1

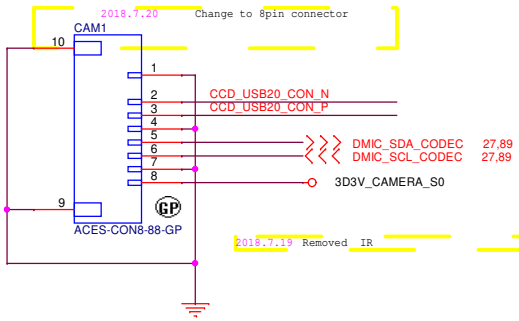


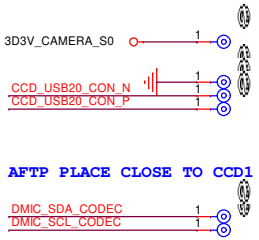
2018.7.20 Delet TOUCH POWER



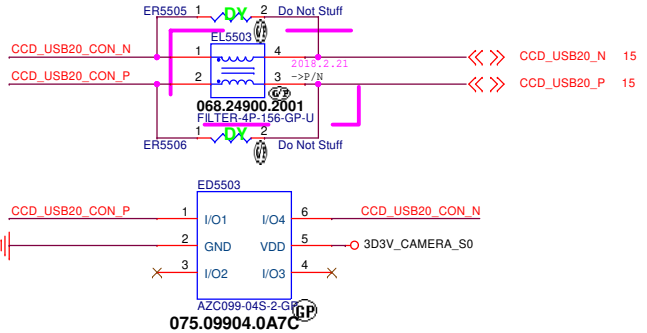


CCD





AFTP PLACE CLOSE TO CCD1



UMA

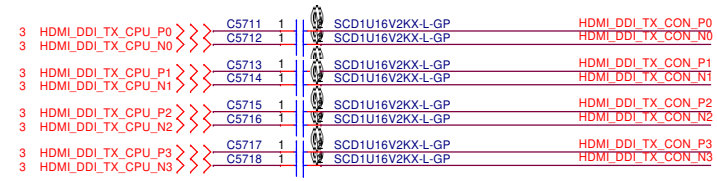
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

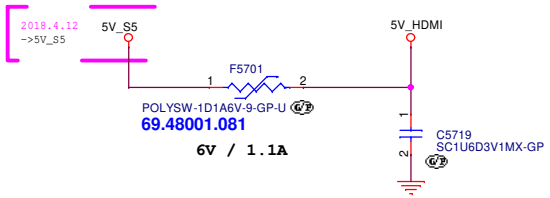
Title: Display (LCD/Inverter)

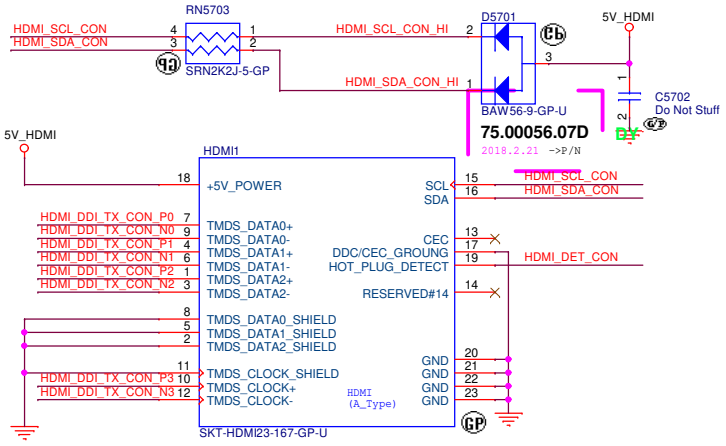
Size: A3 | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2018 | Sheet 55 of 106

HDMI PORT







2018.1.16 updated

#575412 PDG rev.0.7

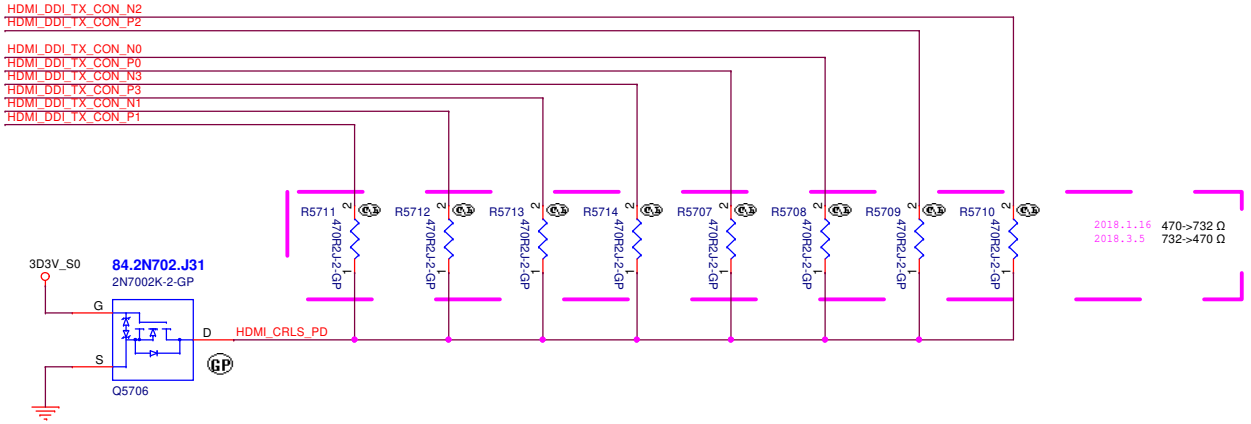


Figure 5-20. HDMI* Cost-Reduced-Level-Shifter (CRLS) Topology

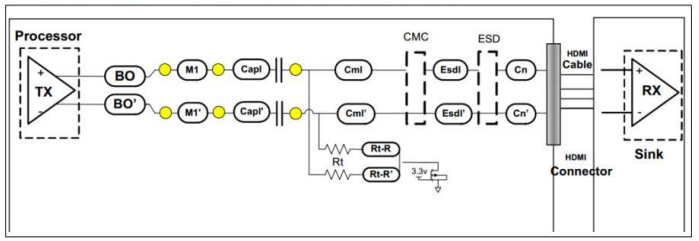
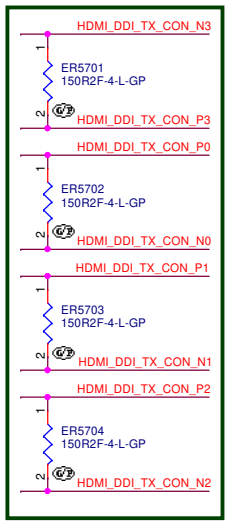
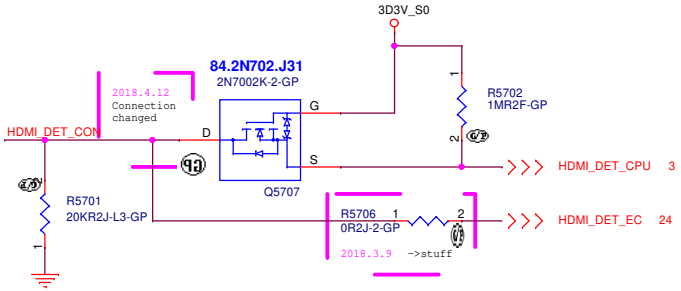


Table 5-26. HDMI* Cost-Reduced-Level-Shifter (CRLS) Topology Guidelines for Max Data rate of 1.65 GT/s

Segment	Stack-up	Via Count[1]	Max Length [mils]	Max Length [mm]
Max Data Rate			1.65 GT/s	2.97 GT/s
B0	MS/SL	Max 3 Vias are allowed.	500	500
M1	MS/SL/DSL		6000	2400
Capl	MS		100	100
Cml	MS		100	100
Esdl	MS		100	100
Cn	MS		300	300
Rt-R	MS		500	100
Total Length			**6500**	**2500**





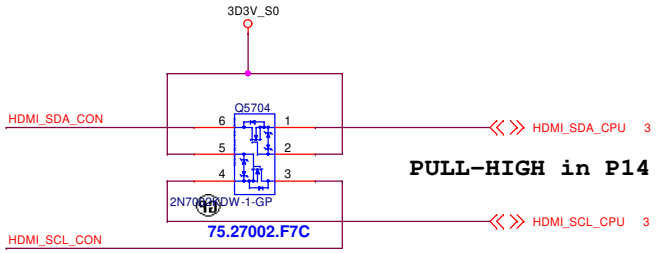


Table 5-26. HDMI* Cost-Reduced-Level-Shifter (CRLS) Topology Guidelines for Max Data rate of 1.65 GT/s

Segment	Stack-up	Via Count[1]	Max Length [mils]	Max Length [mm]
Max Data Rate			1.65 GT/s	2.97 GT/s

Notes:

1. CRLS at 2.97 GT/s supports only Stripline stack-up (no microstrip) for B0 and M1 Segments.
2. 12 mils PTPS for main route sections
3. ESD is recommended. CMC is optional
4. Resistor (Rt) Value = 740 ohm +/-5%
5. Max nFET Ron = 3 ohm
6. The 3.3V supply should be core rail which will turn off in sleep states.

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

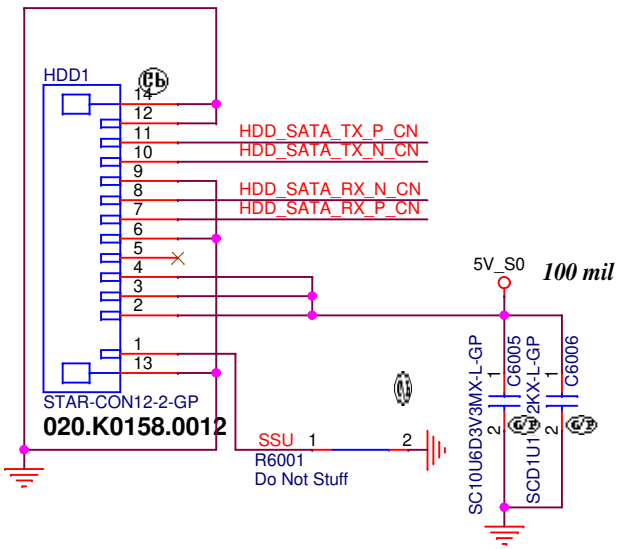
Title: **Display (HDMI Level Shifter/Conn)**

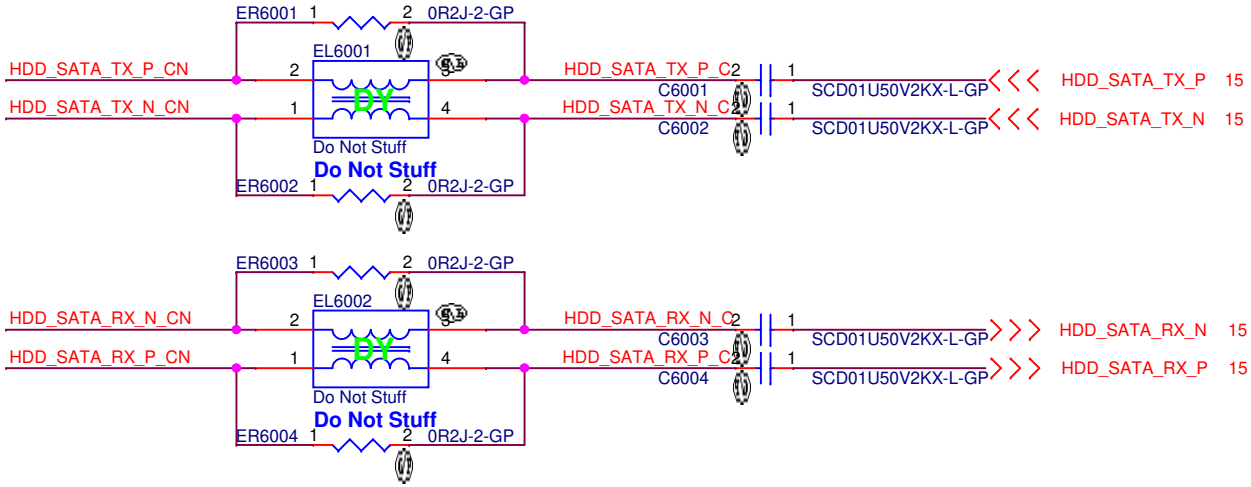
Size: A3 | Document Number: **FAROE 14" Pavilion** | Rev: **SA**

Date: Monday, August 06, 2018 | Sheet 57 of 106

SSID = SATA

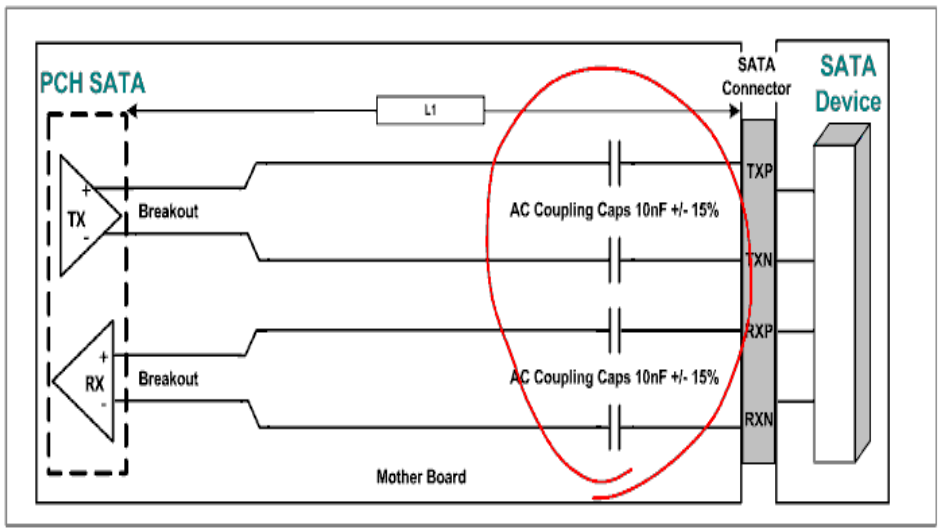
SATA HDD Connector

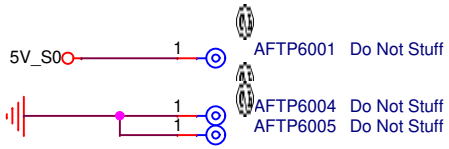




2018.7.19 Removed

need checkTX/RX mapping





AFTP PLACE CLOSE TO HDD1

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

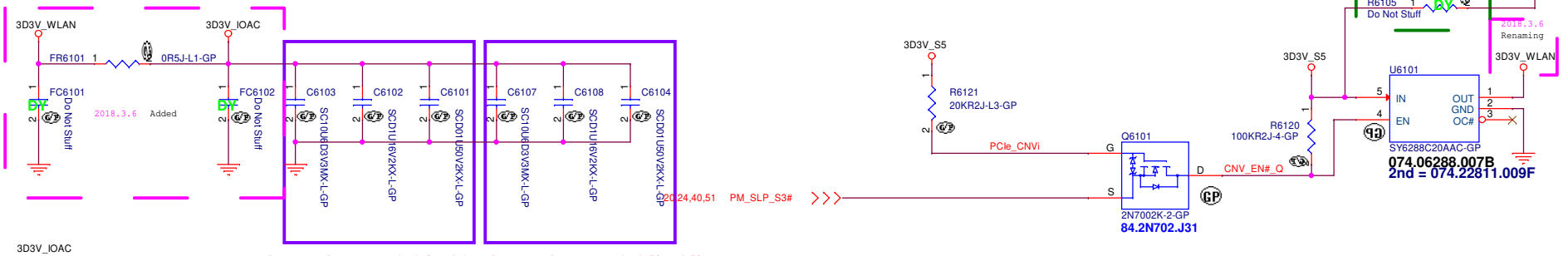
Title: INT IO (HDD/ODD)

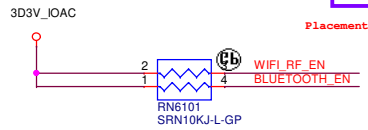
Size: A4 | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2018 | Sheet 60 of 106

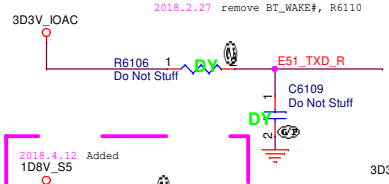
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



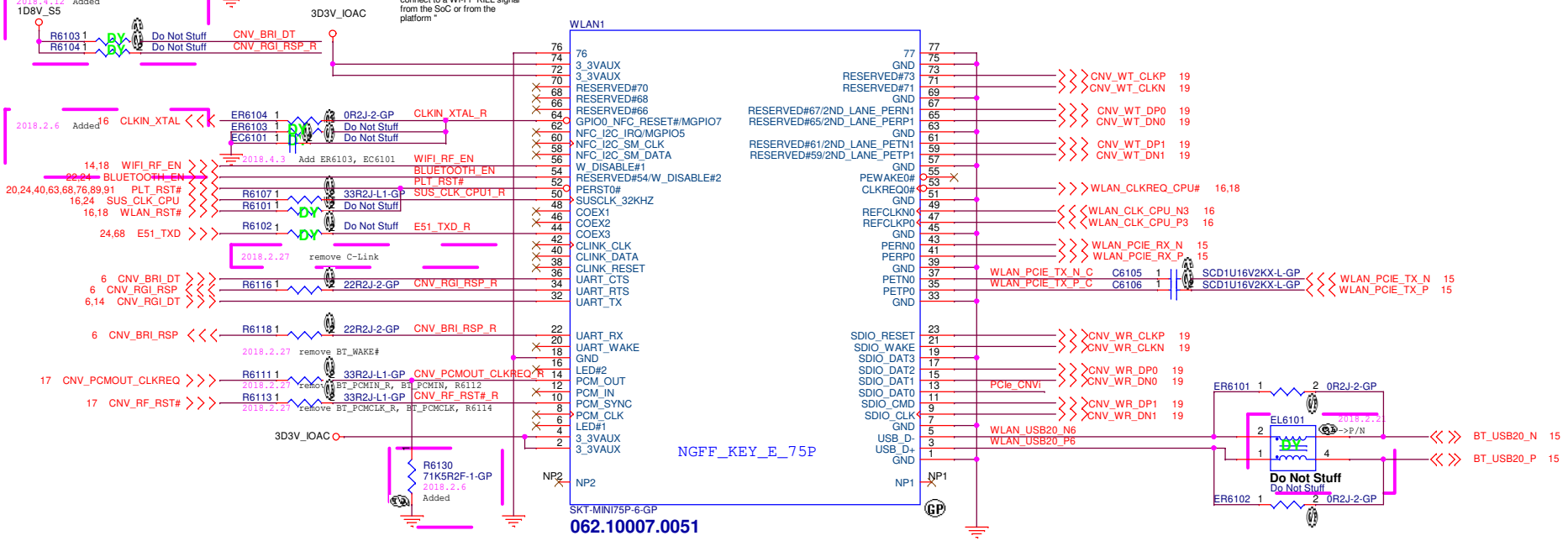


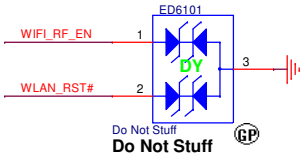
2018.2.27 remove BT_WAKE#, R6110



BLUETOOTH_EN(Pin 54)
"BT_KILL input. Optional to connect to a Bluetooth KILL signal from the SoC or from the platform "

WIFI_RF_EN(Pin 56)
"WLAN_KILL"input. Optional to connect to a Wi-Fi" KILL signal from the SoC or from the platform "





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Title: INT IO (WLAN M.2)

Size: A3 | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2018 | Sheet 61 of 106

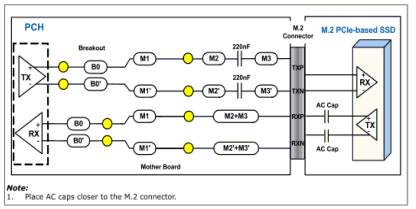
NGFF Connector

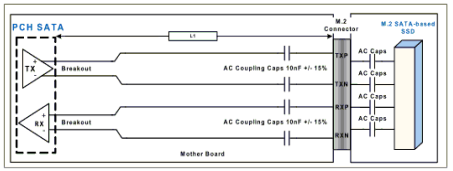
SSD slot C key M 2280-S3

SSD_DET#	
1	SATA
0	PCIe

20150713 Add Truth Table and modify direction

8	N/C	N/C
10	LED1#	Device Active Signal
12	3.3V	3.3V source





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place close to MSATA1

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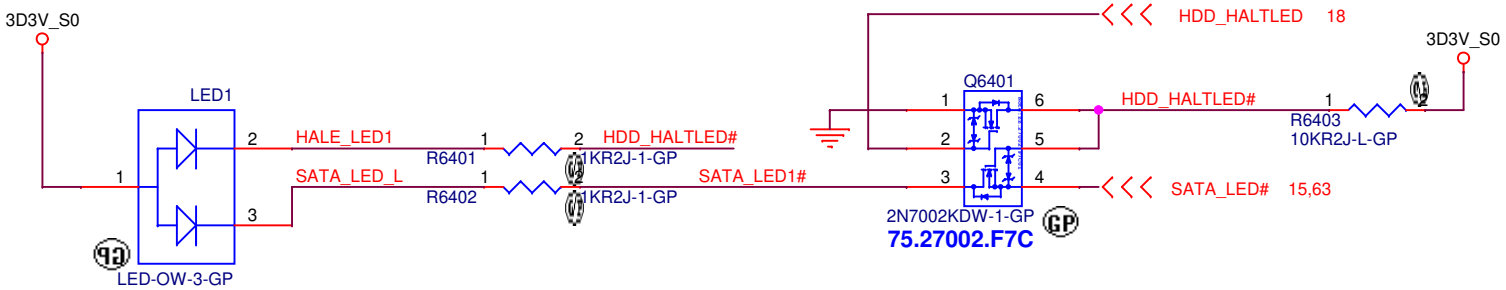
Title	INT IO (SSD M.2/ eMMC)
Size A3	Document Number FAROE 14" Pavilion
Rev	SA
Date: Monday, August 06, 2018	Sheet 63 of 106

HDD LED



Vol Up,Down BTN

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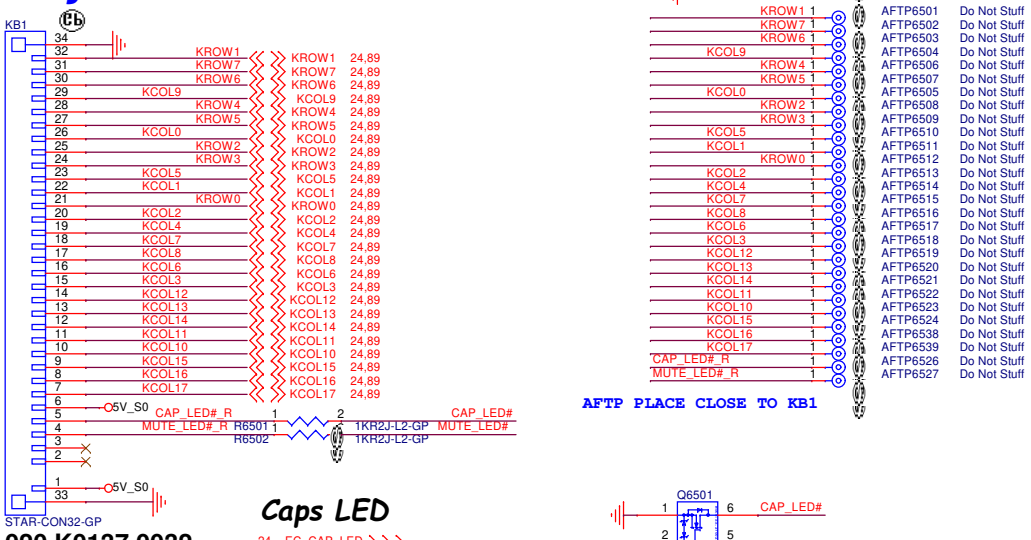
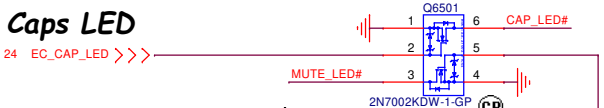
Title: LED / Button / Power Button		
Size: A4	Document Number: FAROE 14" Pavilion	Rev: SA
Date: Monday, August 06, 2018	Sheet 64 of 106	

SSID = Key Board CN & TP CN

Key Board conn.

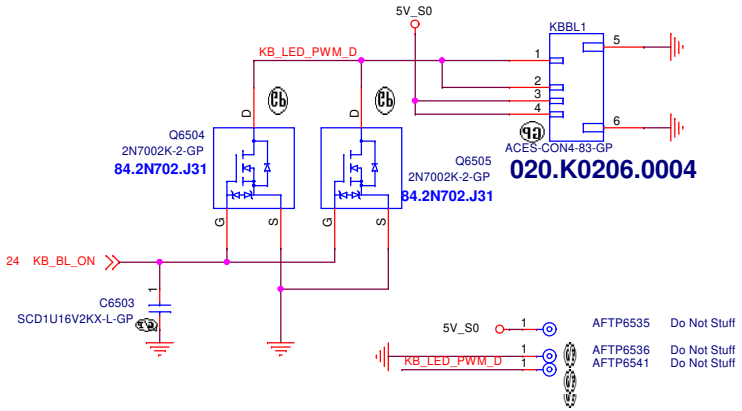


Caps LED

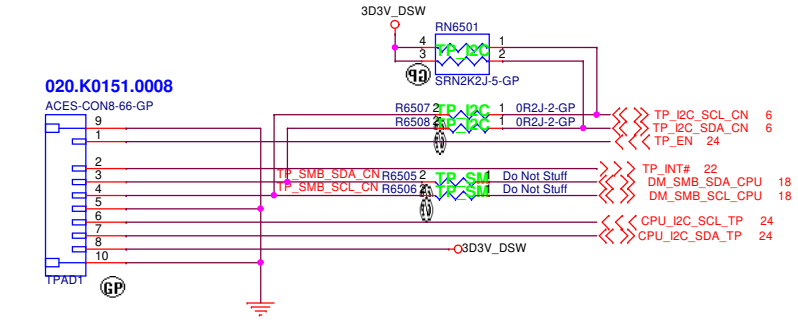


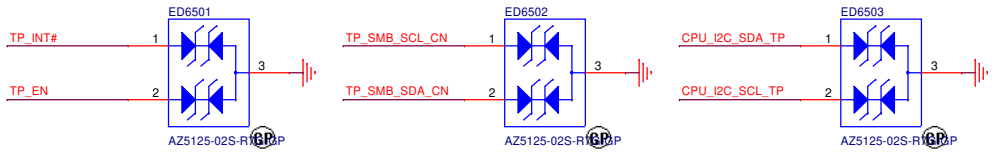
MUTE LED

Keyboard backlight conn.



Touch Pad conn.





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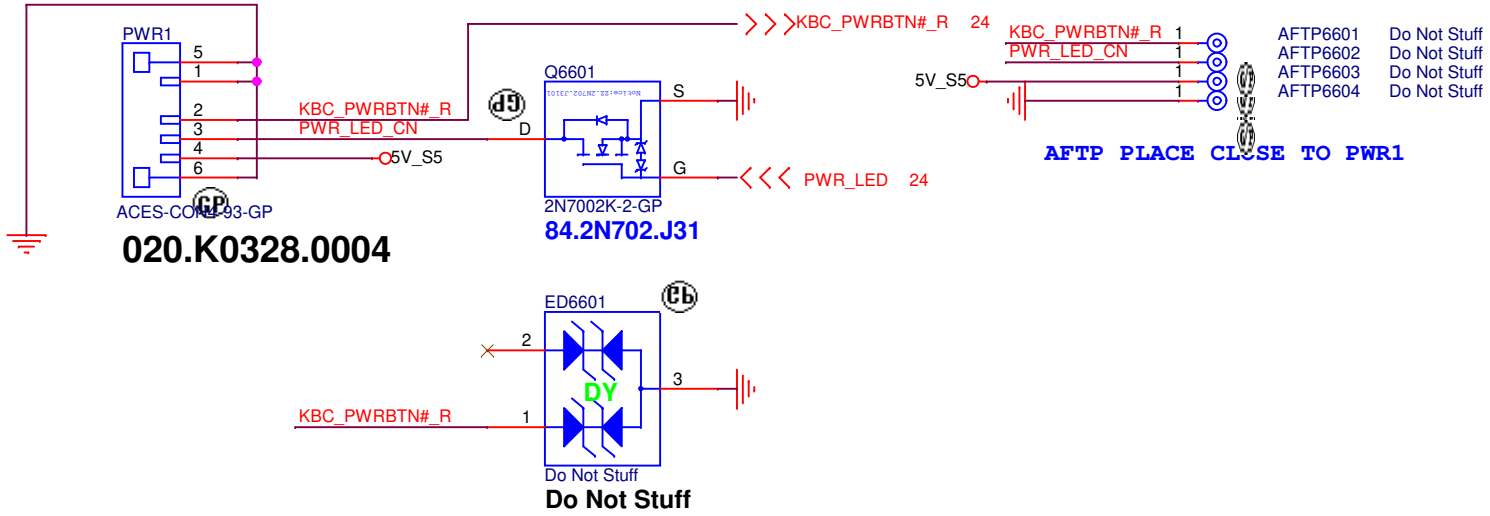
Title: INT IO (KB/TP)

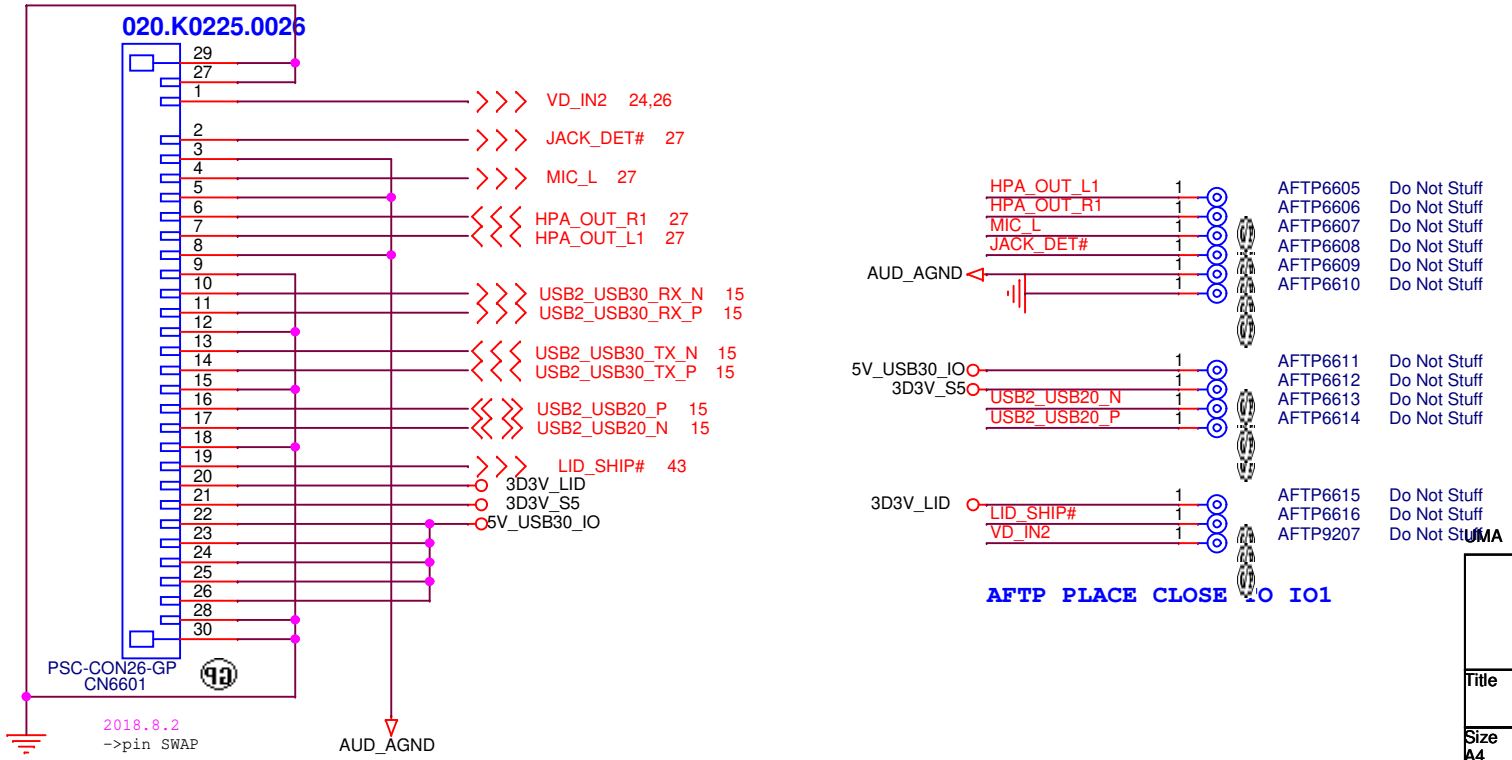
Size: A3 | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2018 | Sheet 65 of 106

PWBD Conn.



IO Board Conn.



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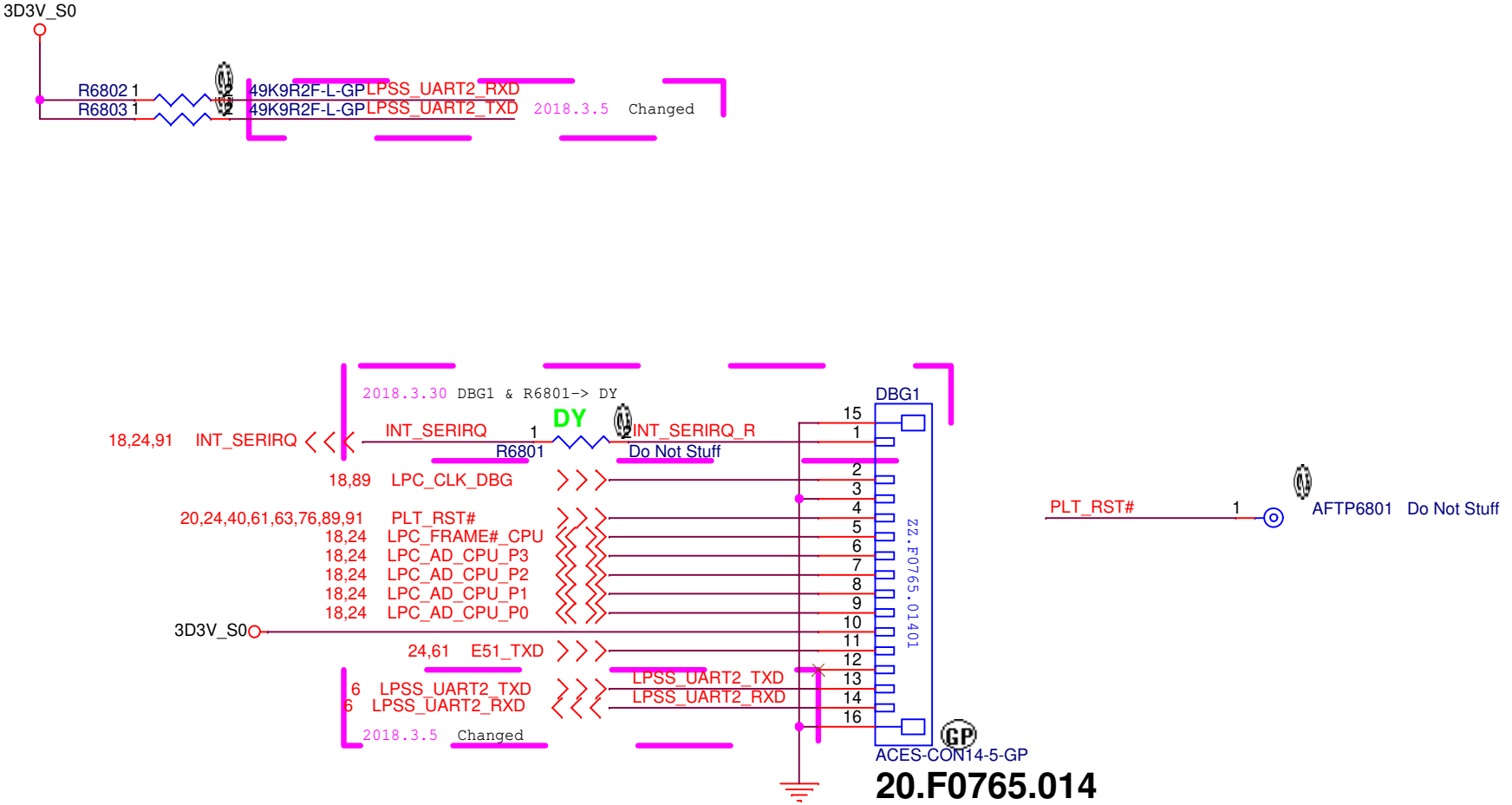
Title	IO Board Conn (USB/AUDIO/CR..etc)	
Size A4	Document Number FAROE 14" Pavilion	Rev SA
Date: Monday, August 06, 2018	Sheet 66 of 106	



20.F0765.014

DB,SI,PV: 20.F0765.014
MV: ZZ.F0765.01401

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Title: ***Debug (LPC debug)***

Size	Document Number	Rev
A	**FAROE 14" Pavilion**	**SA**

Date: Monday, August 06, 2018 Sheet 68 of 106

G-SENSOR

To KBC for HDD Protect

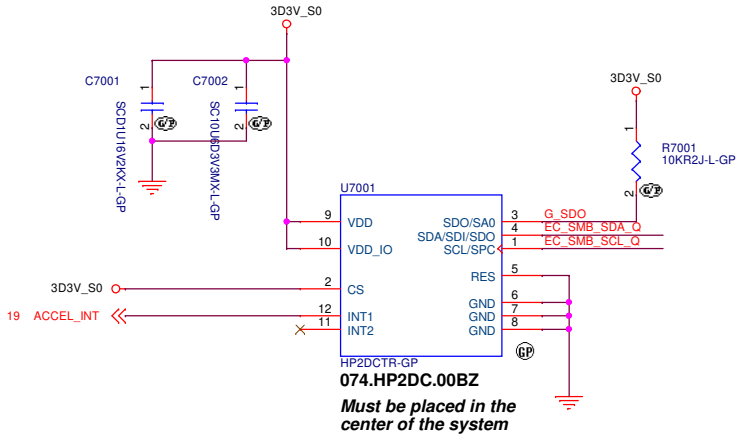
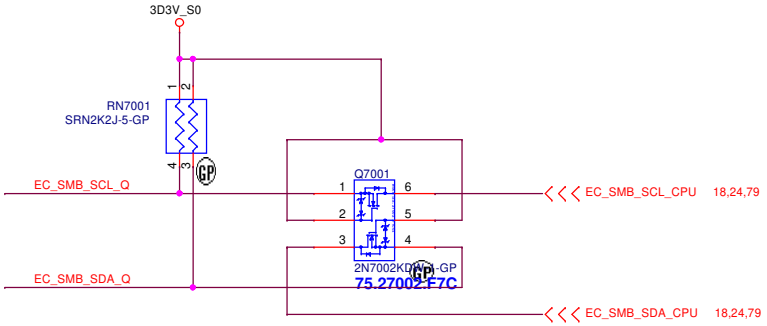


Table 13. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)



To Sensor HUB for LCD angle

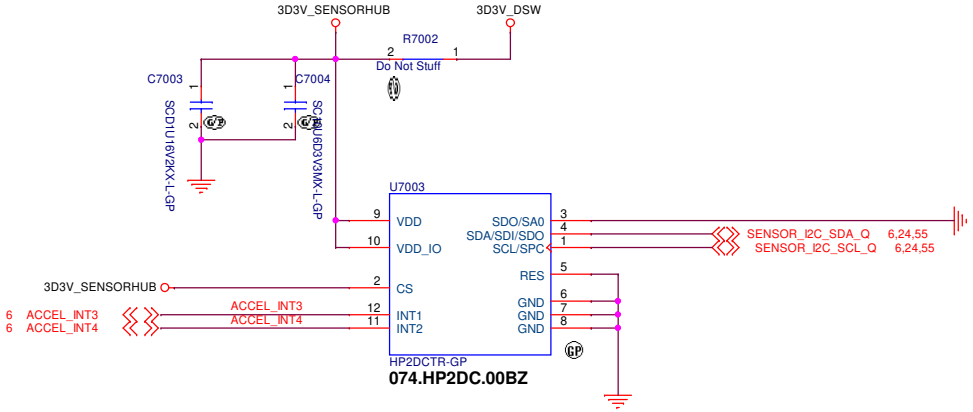


Table 13. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

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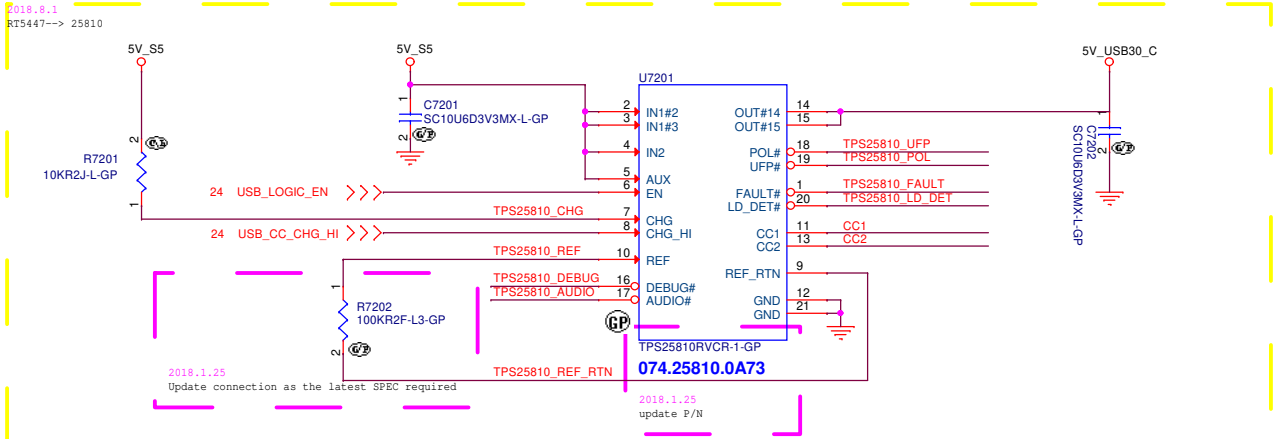
Title: Sensor (G-sensor)

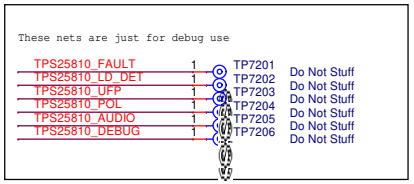
Size: A3 | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2018 | Sheet 70 of 106

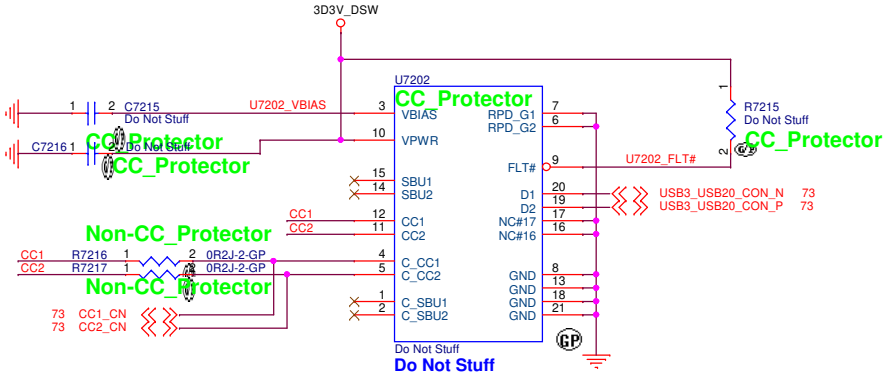
USB 3.0 TYPE C Controller OUTPUT=3A



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A



USB 3.0 TYPE C Port Protector



Do Not Stuff

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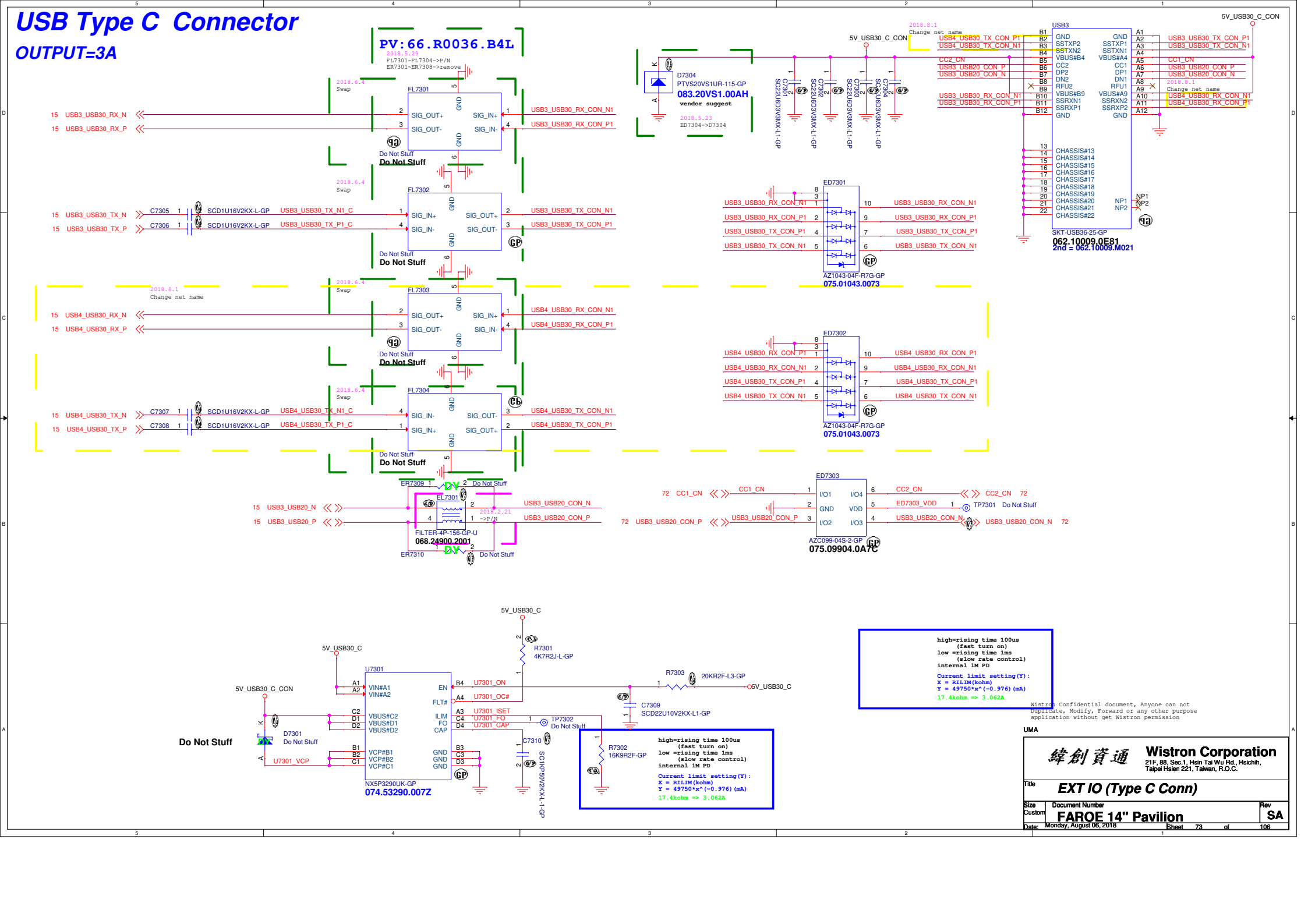
Title: ***EXT IO (Type C CC Logic)***

Size	Document Number	Rev
A3	**FAROE 14" Pavilion**	SA

Date: Monday, August 06, 2018 Sheet 72 of 106

USB Type C Connector

OUTPUT=3A



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Title: EXT IO (Type C Conn)

Size: Custom | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2018 | Sheet 73 of 106

Main Func = dGPU

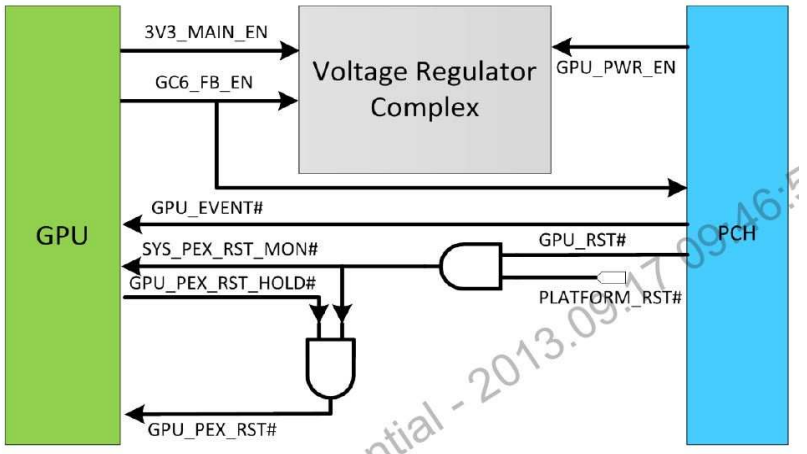


Figure 18-11. GC6 2.0 High-level Signal Connection Concept

dGPU Reset

1.05V +/- 30mV
3.3A

20161214 N17

20161215 N17

Under GPU

Near GPU

Between GPU and PS

3.3V +/- 5%
210mA

20161228 N17

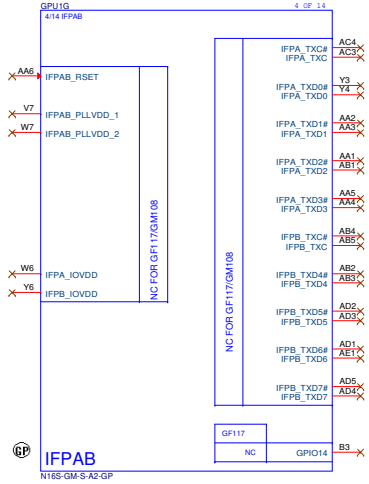
POWER IC

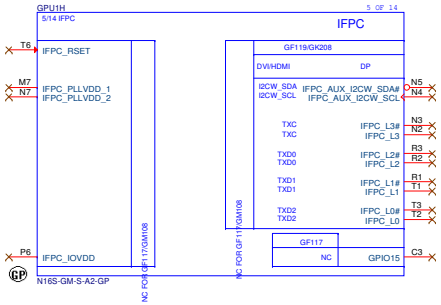
<DUMMY>

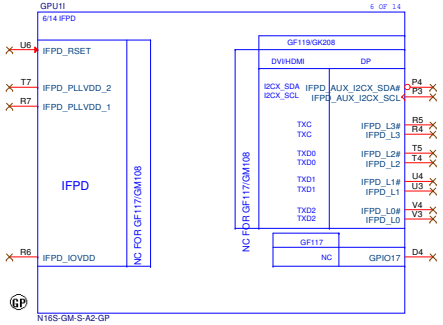
UMA

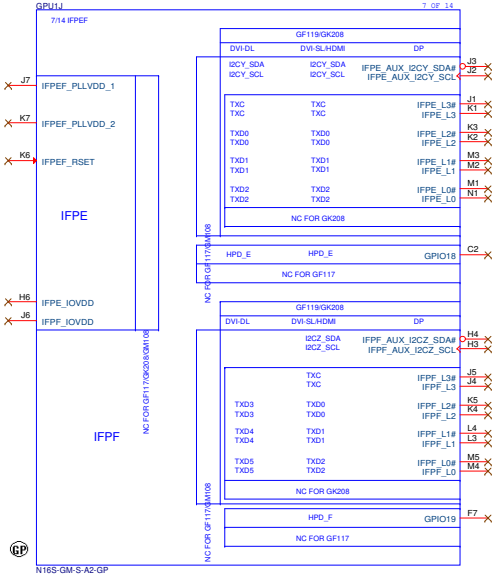
Wistron Corporation		
Title: GPU_PEG (1/5)		
Size: A2	Document Number: FAROE 14" Pavilion	Rev: SA
Date: Monday, August 06, 2018	Sheet 76 of 106	

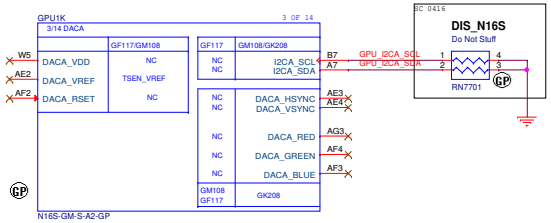
Main Func = dGPU











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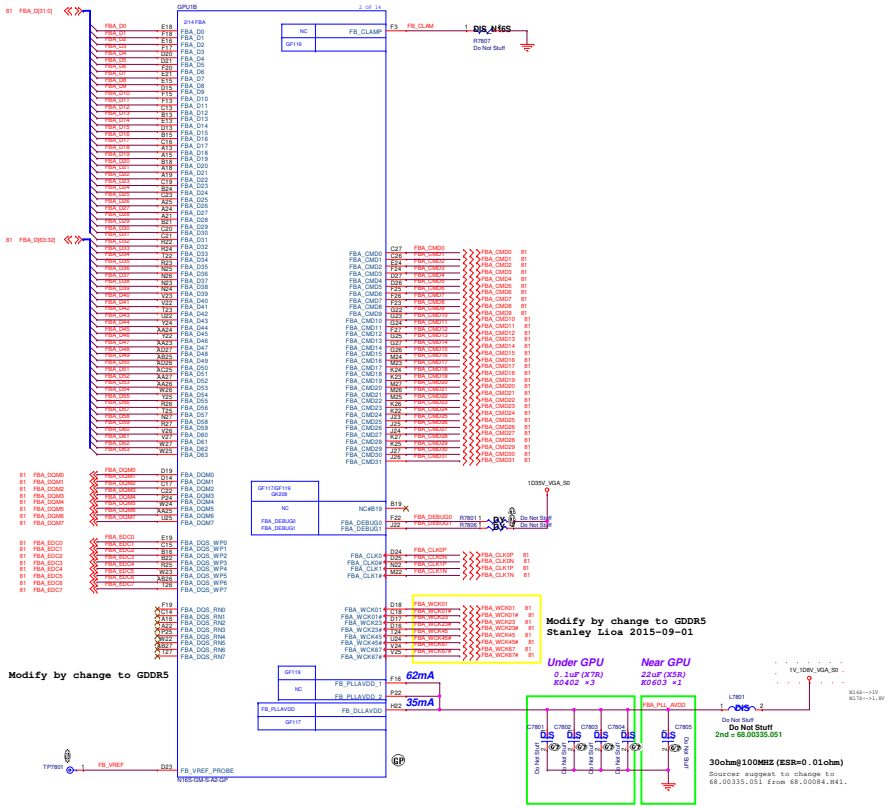
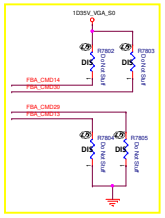
Title: *GPU DIGITALOUT (2/5)*		
Size: A2	Document Number: FAROE 14" Pavilion	Rev: SA
Date: Monday, August 06, 2018	Sheet 77 of 106	

Main Func = dGPU





Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

LMA

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Title: GPU_VRAM I/F (3/5)

Size: A3 | Document Number: FAROE 14" Pavilion | Rev: SA

Date: Monday, August 06, 2012 | Sheet 78 of 105

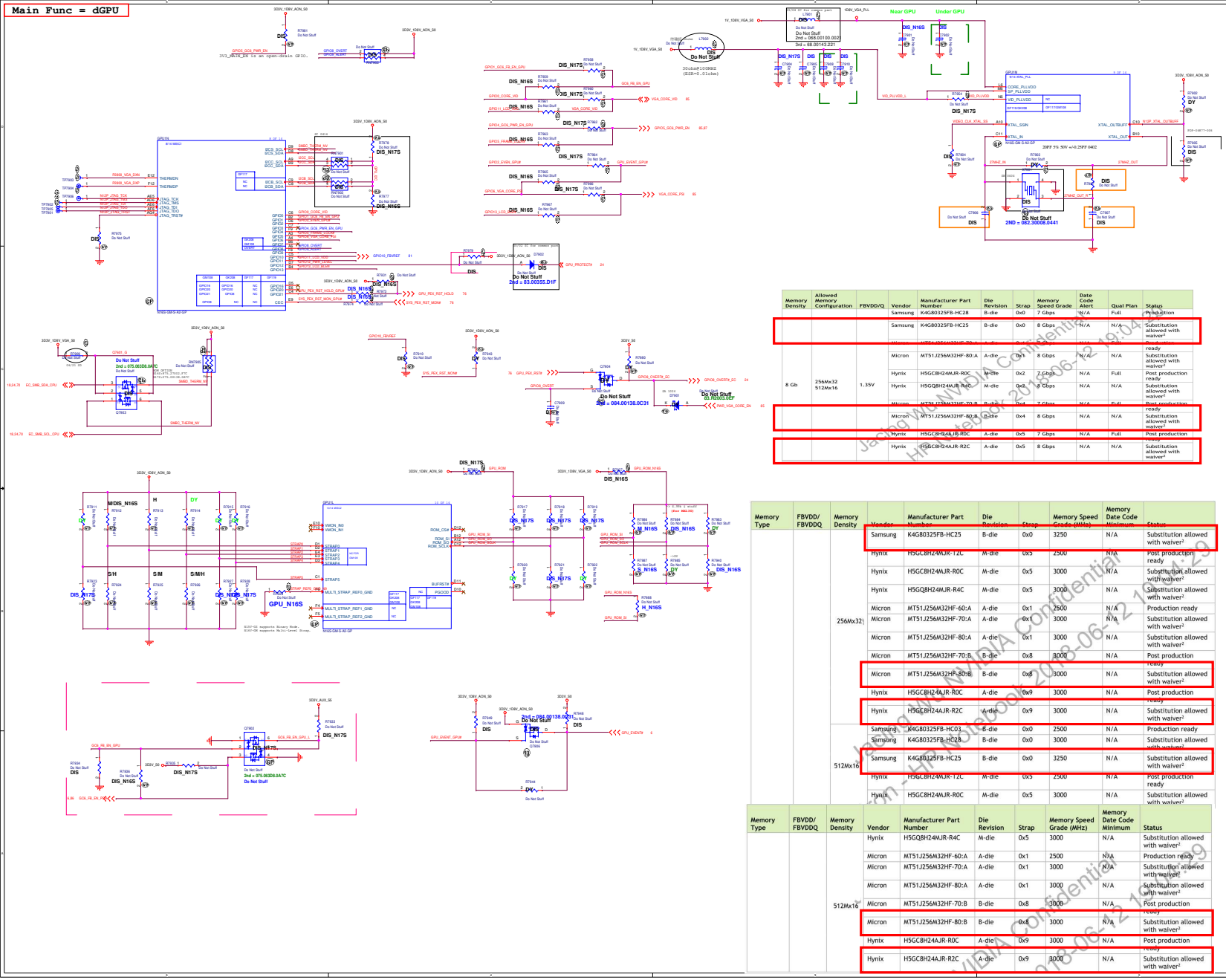

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
			Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-70:B	B-die	0x4	7 Gbps	N/A	Full	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x4	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24AJR-R0C	A-die	0x5	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x5	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
			Samsung	K4G80325FB-HC25	B-die	0x0	3250	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24MJR-T2C	M-die	0x5	2500	N/A	Post production ready
			Hynix	H5GC8H24MJR-R0C	M-die	0x5	3000	N/A	Substitution allowed with waiver[2]
			Hynix	H5GQ8H24MJR-R4C	M-die	0x5	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready
		256Mx32	Micron	MT51J256M32HF-70:A	A-die	0x1	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-80:A	A-die	0x1	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:B	B-die	0x8	3000	N/A	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x8	3000	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24AJR-R0C	A-die	0x9	3000	N/A	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x9	3000	N/A	Substitution allowed with waiver[2]
			Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
			Samsung	K4G80325FB-HC28	B-die	0x0	3000	N/A	Substitution allowed with waiver[2]
		512Mx16	Samsung	K4G80325FB-HC25	B-die	0x0	3250	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24MJR-T2C	M-die	0x5	2500	N/A	Post production ready
			Hynix	H5GC8H24MJR-R0C	M-die	0x5	3000	N/A	Substitution allowed with waiver[2]

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
			Hynix	H5GQ8H24MJR-R4C	M-die	0x5	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready
			Micron	MT51J256M32HF-70:A	A-die	0x1	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-80:A	A-die	0x1	3000	N/A	Substitution allowed with waiver[2]
		512Mx16	Micron	MT51J256M32HF-70:B	B-die	0x8	3000	N/A	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x8	3000	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24AJR-R0C	A-die	0x9	3000	N/A	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x9	3000	N/A	Substitution allowed with waiver[2]

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

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GPU_GPIO/STRAP (4/5)
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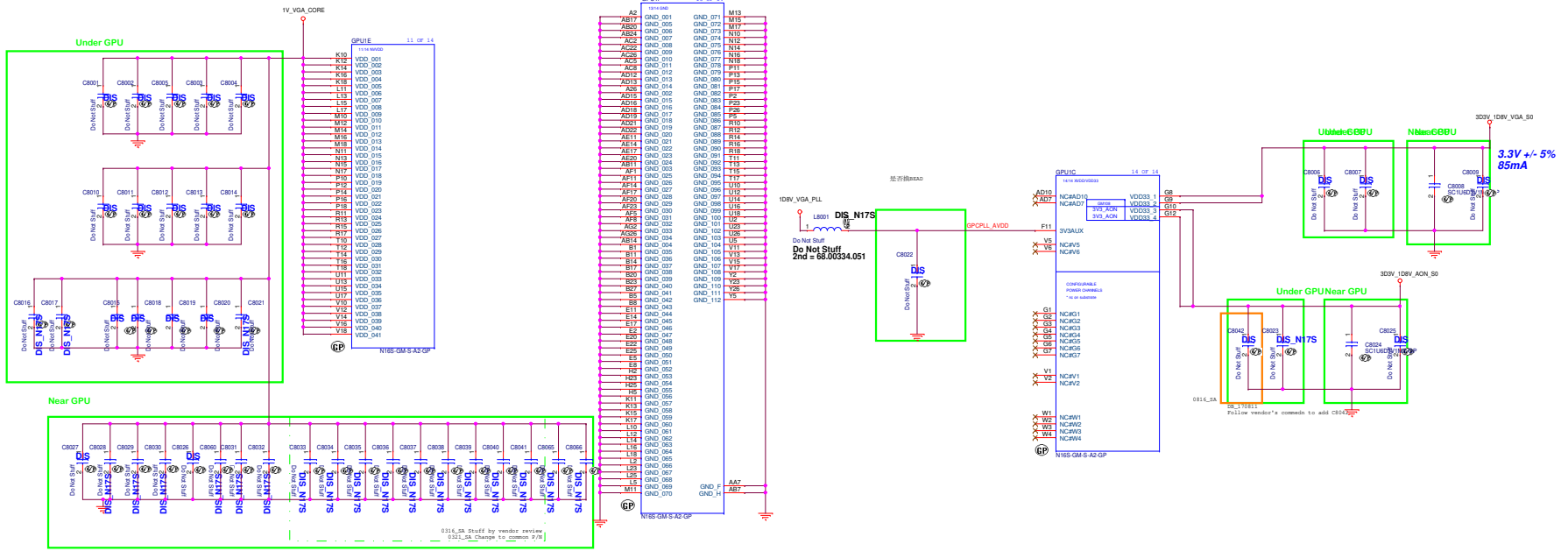

Table 3. NVVDD Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
NVVDD Supply Net					
GB2B-64, GB2C-64	4.7 µF	X6S 0603	10	12	Under GPU
	1 µF	X6S 0402	4	5	Under GPU
	47 µF	X5R 0805	1	-	Near GPU
	10 µF	X7R 0805	-	11	Near GPU
	22 µF	X5R 0805	1	4	Near GPU
	4.7 µF	X5R 0805	1	4	Near GPU
	330 µF	POS 7343	1	2	Near GPU

Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R 0402	2	0	Under GPU
	1 µF	X7R 0603	2	8	Under GPU
	4.7 µF	X6S 0603	2	0	Under GPU
	10 µF	X6S 0603	0	2	Under GPU
	10 µF	X6S 0603	1	1	Near GPU
	22 µF	X6S 0603W	1	3	Near GPU

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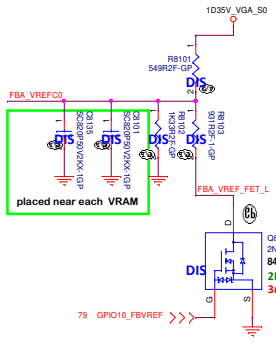
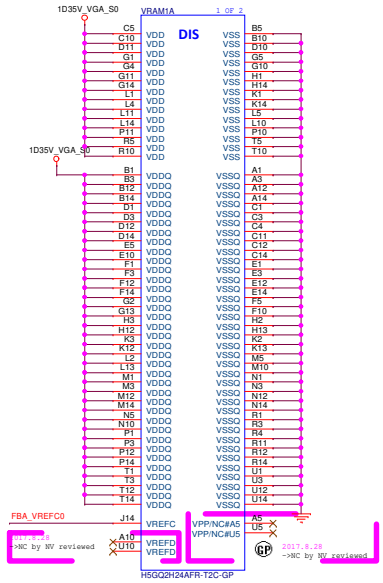
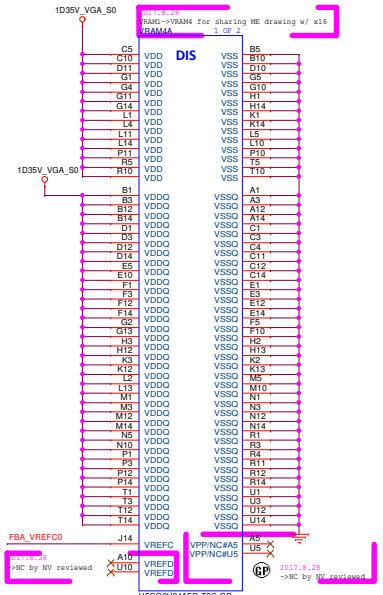
Frame Buffer Patition



FBVREF Termination

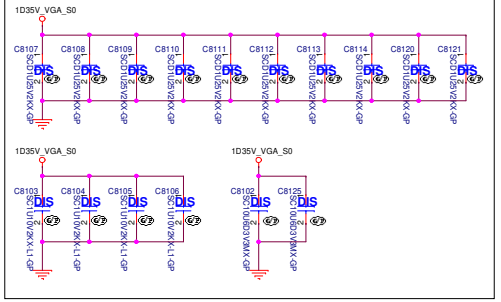
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low





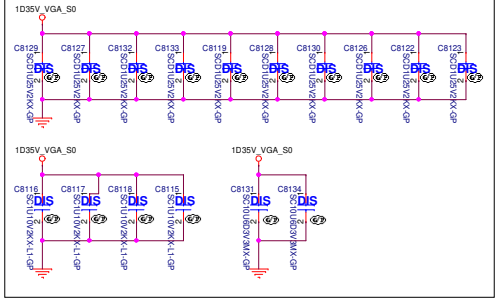
DECOUPLING FOR VRAM1 DEVICE

Place close VDD ball



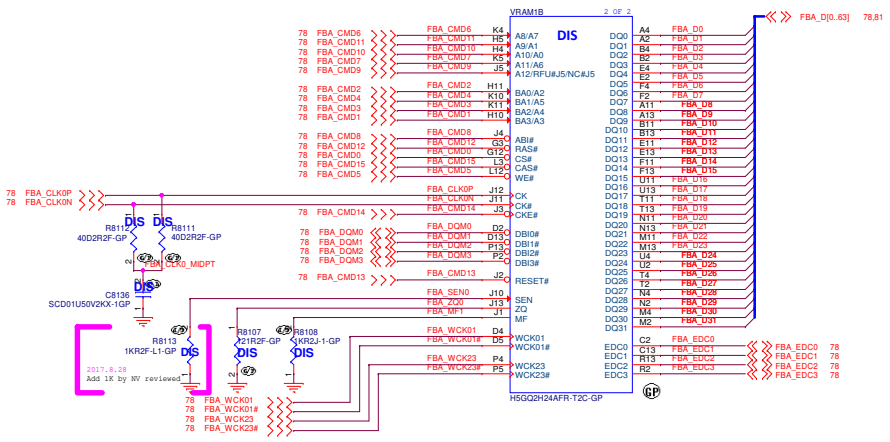
DECOUPLING FOR VRAM2 DEVICE

Place close VDD ball



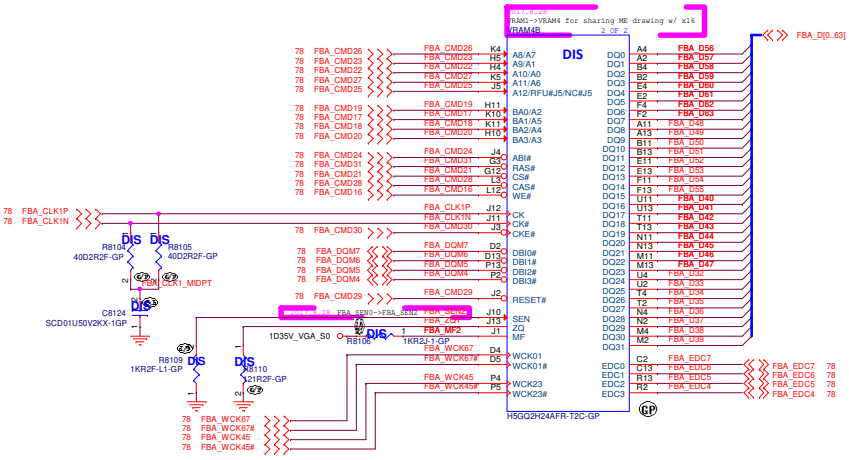
Frame Buffer Patition 0..31

Normal(MF=0)



Frame Buffer Patition 32..63

Mirrored(MF=1)



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Title: 081_GPU (VRAM1,2 1/4)

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Main Func = dGFX_CORE

need EE Check

Table 1	
Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

Figure 8.8 GC6 2.1 Voltage Regulator Complex Signal Connection

dGPU Power Discharge Circuit

1D0V_VGA_S0

1V_VGA_CORE

1D8V_AON_S0

1D35V_VGA_S0

Discharge schematic change (solution different)
2010915 Alden chiang modify

1D8V_VGA_S0

For tuning VGA_CORE sequence.

N17S-G1
EDP-Continuous : 30 A
EDP-Peak : 60.1 A

Item	Location	N16		N17	
1	PU8514	RT8812AGQW	74.08812.073	RT8816AGQW	074.08816.0A73
2	PR8511	20K	64.20025.6DL	6.19K	64.61915.6DL
3	PR8510	20K	64.20025.6DL	20.5K	64.20525.6DL
4	PR8512	2K	64.20015.6DL	4.32k	64.43215.6DL
5	PR8514	18K	64.18025.6DL	16.5K	64.16525.6DL
6	PR8561	0R	63.R0034.1DL	309R	64.30905.6DL
7	PC8519	2700p	78.27224.2FLDL	4700p	078.47222.02FD
8	PR8525	0R	63.R0034.1DL	DY	
9	PR8526	0R	63.R0034.1DL	DY	
10	PR8527	DY		0R	63.R0034.1DL
11	PR8576	DY		0R	63.R0034.1DL
12	PR8577	DY		160K	64.16035.6DL
13	PR8508	15.4K	64.15425.6DL	DY	
14	PR8504	348K	64.34835.6DL	499K	64.49935.6DL

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GPU_VGA_CORE_RT8812A

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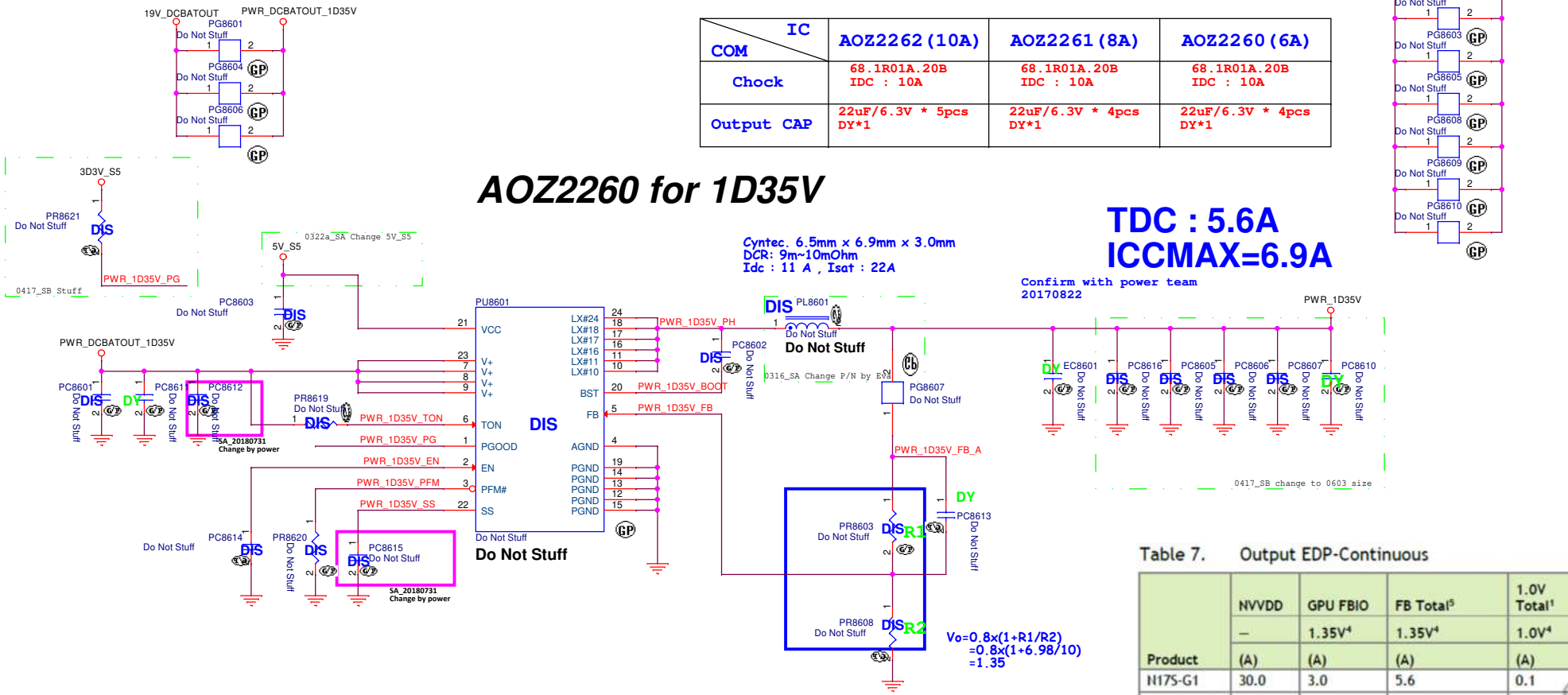
SSID = PWR.Plane.Regulator_1p35v

AOZ2260 for 1D35V

IC / COM	AOZ2262 (10A)	AOZ2261 (8A)	AOZ2260 (6A)
Chock	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1



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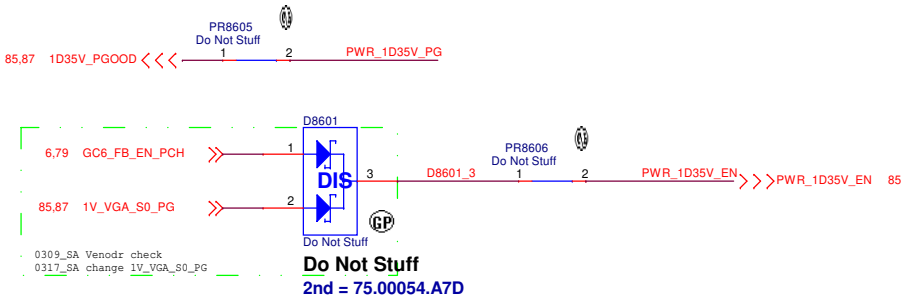

Table 7. Output EDP-Continuous

Product	NVVDD –	GPU FBIO 1.35V[4]	FB Total[5] 1.35V[4]	1.0V Total[1] 1.0V[4]	1.8V Total[2] 1.8V[4]
	(A)	(A)	(A)	(A)	(A)
N17S-G1	30.0	3.0	5.6	0.1	0.3
N17S-LG	15.4	2.5	5.0	0.1	0.2

Table 8. Output EDP-Peak

Product	NVVDD –	GPU FBIO 1.35V[3]	FB TOTAL[4] 1.35V[3]	1.0V Total[1] 1.0V[3]
	(A)	(A)	(A)	(A)
N17S-G1	60.1	3.4	6.9	0.2
N17S-LG	48.3	2.8	5.8	0.2

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A3	FAROE 14" Pavilion	SA

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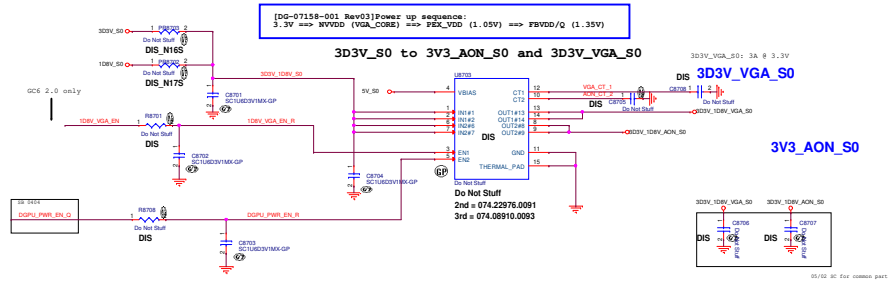
Main Func = dGPU

G5516 for 1.8V_AON_S0



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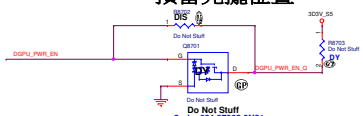
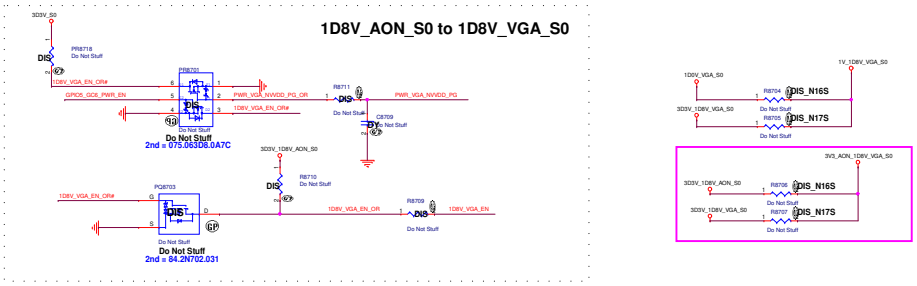
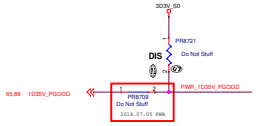
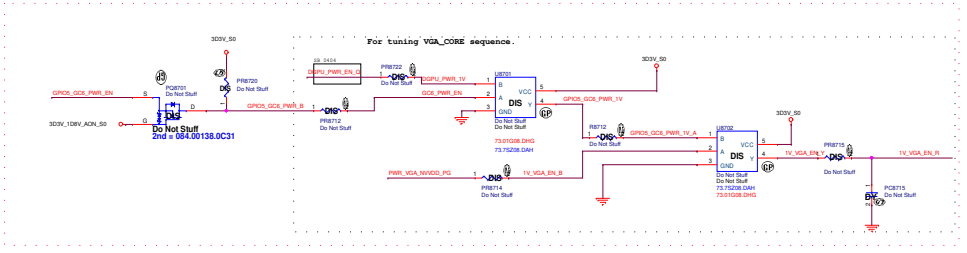


PARAMETER	MIN	MAX	UNITS
VIN1,2 Input voltage range	0.8	V_{BIAS}	V
VBIAS Bias voltage range	2.5	5.5	V
EN1,2 ON voltage range	0	5.5	V
VOUT1,2 Output voltage range	---	VIN1,2	V
VIH High-level input voltage, EN1, EN2	1.2	5.5	V
VIL Low-level input voltage, EN1, EN2	---	0.5	V
CT1,2 Input Capacitor	1	---	µF

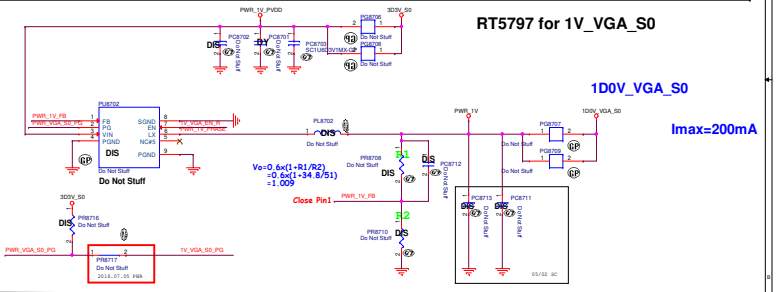
1D8V_AON_S0 to 1D8V_VGA_S0







RT5797 for 1V_VGA_S0



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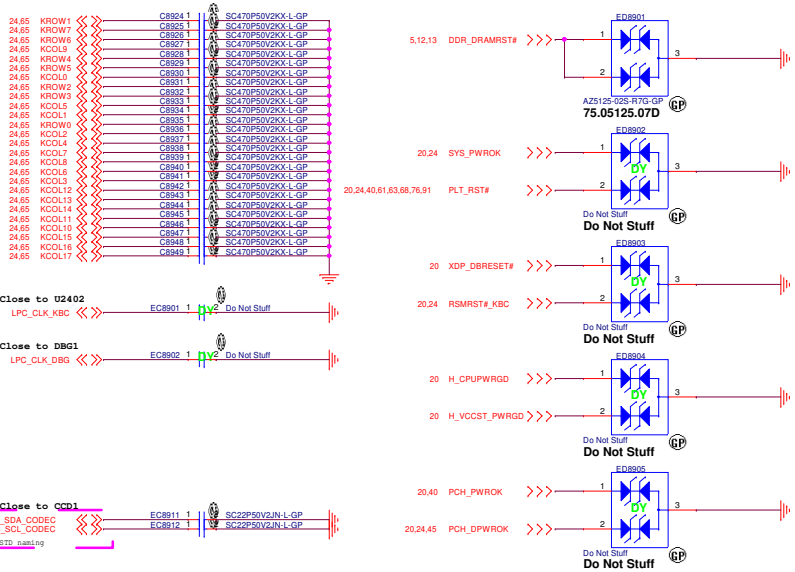
EMI



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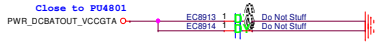
Close to DBG1

Close to CCD1

Close to PU4801



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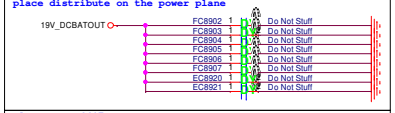
Close to PR4402

Close to PU4408

RF

Close to PU4406

place distribute on the power plane



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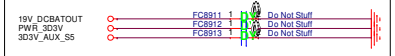

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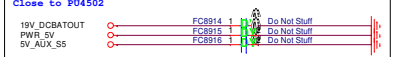

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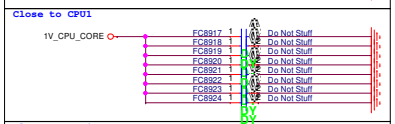
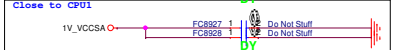


Close to CPU1

Close to CPU1



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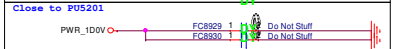

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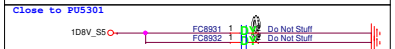

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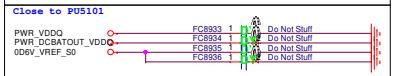

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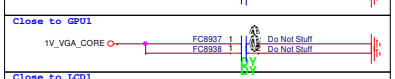

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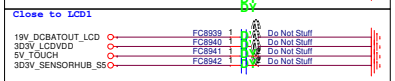

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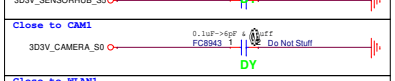

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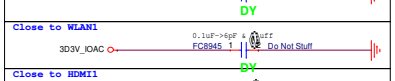
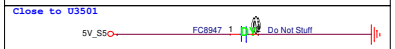


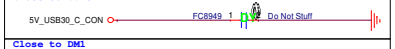
Close to HDMI1

Close to U3501



Close to USB2

Close to USB3



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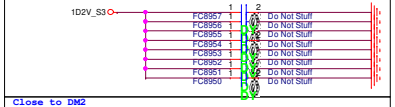

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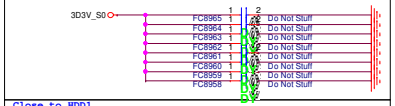

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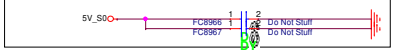
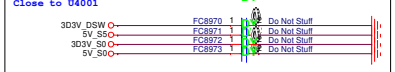


Close to MSATA1

Close to U4001



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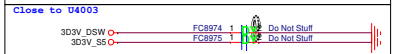

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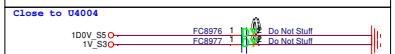

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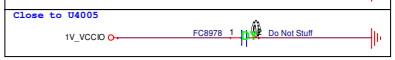
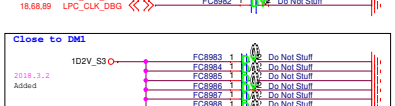


Close to RN1704

Close to RN1705

Close to RN1804

Close to DM1



Close to DM2

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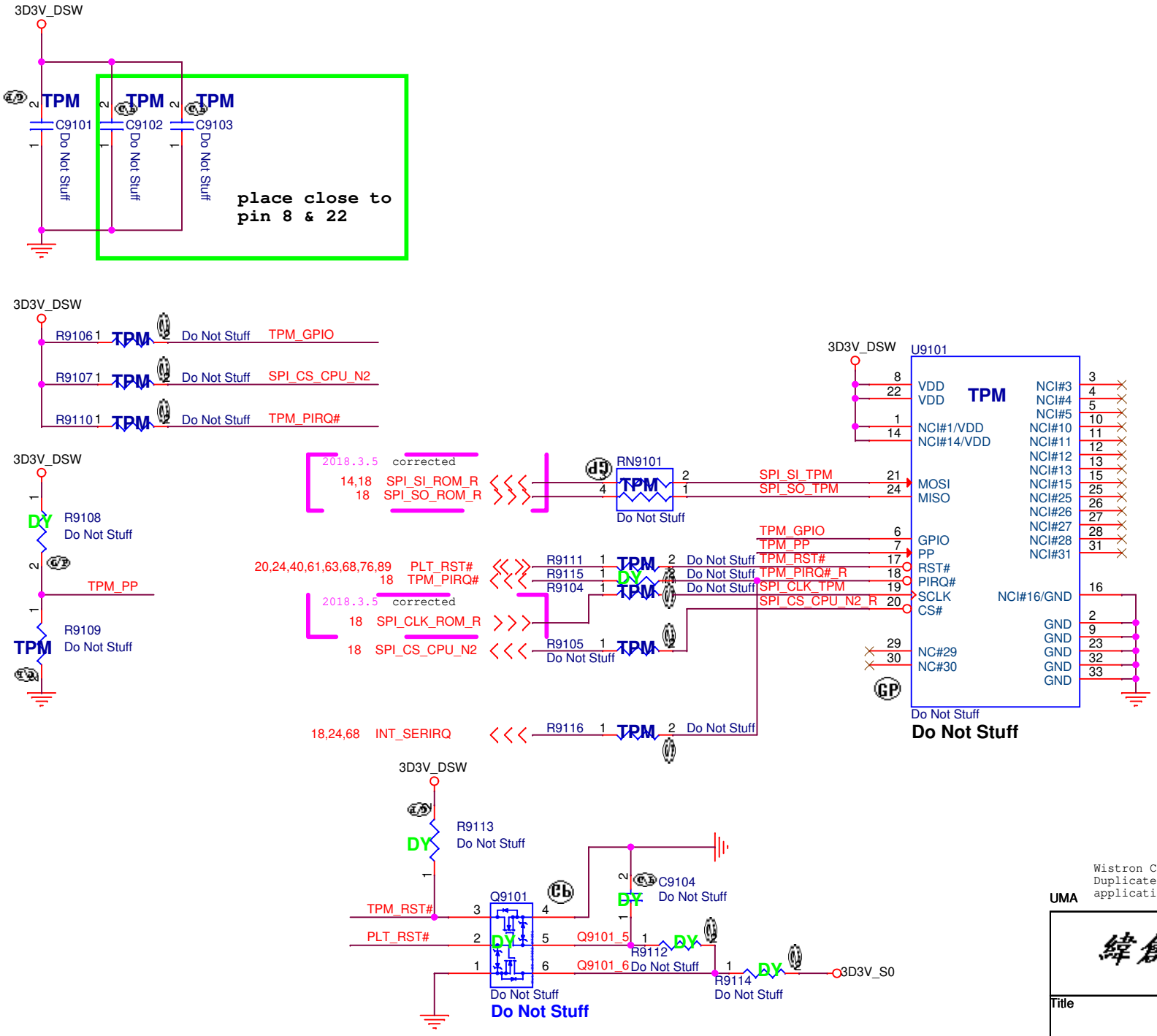

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (TPM)

Size	Document Number	Rev
A4	FAROE 14" Pavilion	SA

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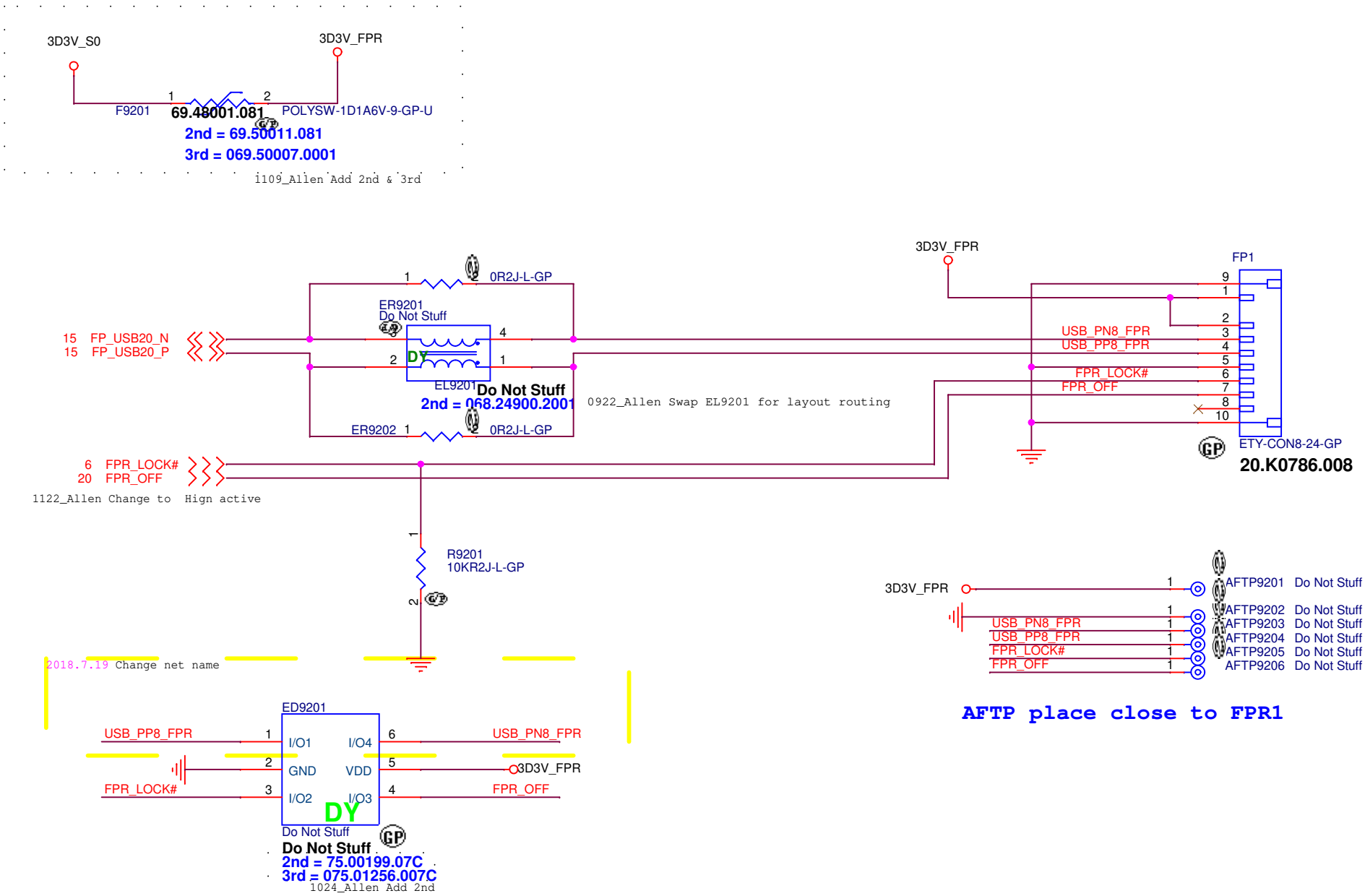

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***INT IO (Finger Print)***	
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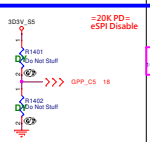
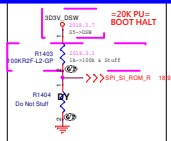
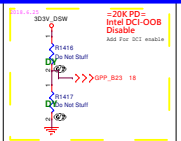
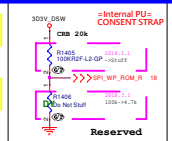
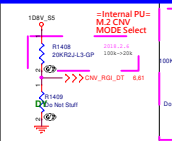
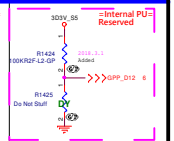
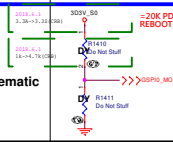
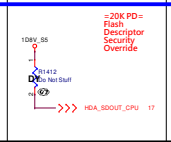
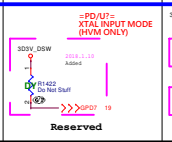
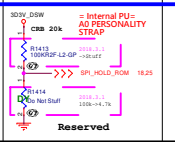
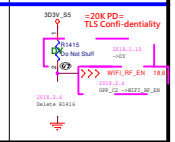
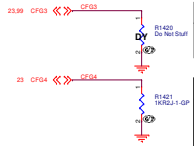
PCH Strap Pin

GPIO	GPP_C5/SML0ALERT#	SPI0_MOSI	GPP_E6	GPP_B23	SPI0_IO2	CNV_BRI_DT	GPP_F6 / CNV_RGI_DT	GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI
Schematic			Reserved (ICL)			Reserved (ICL)		
Description	0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.	This strap should sample HIGH External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.	This strap should sample HIGH.	Intel DCI-OOB	This strap should sample HIGH External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.	XTAL Frequency Selection	An external pull-up or pull-down is required.	This strap should sample HIGH External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
High	eSPI	Disable =default=	Reserved	Enable IntelR DCI-OOB	DISABLED =default=	24M	INTEGRATED CNVI DISABLE	3.3V
Low	LPC =default=	Enable	Reserved	Disable IntelR DCI-OOB =default=	ENABLED	38.4 MHz =default=	INTEGRATED CNVI ENABLE	1.8V

GPIO	GPP_B18/GSPI0_MOSI	HDA_SDO / I2S0_TXD	TBT LSX #0	TBT LSX #1	TBT LSX #2	GPD7	SPI0_IO3	GPP_C2
Schematic			Reserved (ICL)	Reserved (ICL)	Reserved (ICL)			
Description	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode	Flash Descriptor Security Override	DDP1 I2C /TBT LSX #0 / BSSB-LS #0 pins VCC configuration	DDP2 I2C/TBT LSX #1/ BSSB-LS #1 pins VCC configuration	DDP3 I2C/TBT LSX #2/BSSB-LS #2 pins VCC configuration	This strap should sample HIGH External pull-up is required. Recommend 100K.	This strap should sample HIGH External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.	Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
High	No Reboot	Disable	3.3V	3.3V	3.3V	XTAL IS ATTACHED	DISABLED =default=	Enable
Low	Reboot =default=	Enable =default=	1.8V	1.8V	1.8V	XTAL INPUT IS SINGLE ENDED	Enable	Disable =default=

GPIO	GPP_H2	ITP_PMODE	GPP_H21	GPP_H23				
Schematic	=20K PD= eSPI Flash Sharing Mode Reserved (ICL)	=Internal PU= DFXTESTMODE Reserved Add TP on p99		=Internal PD= eSPI Flash Sharing Mode Reserved				
Description	eSPI Flash Sharing Mode	Reserved	An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.	This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled)				
High	1 = Slave Attached Flash Sharing (SAFS) is enabled.	DFXTESTMODE DISABLED =default=	24MHZ	SAF ENABLE				
Low	0 = Master Attached Flash Sharing (MAFS) is enabled. (Default)	DFXTESTMODE ENABLED	38.4/19.2MHZ =default=	MAF ENABLE =default=				

CPU Strap Pin



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

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Title: CPU (STRAP)

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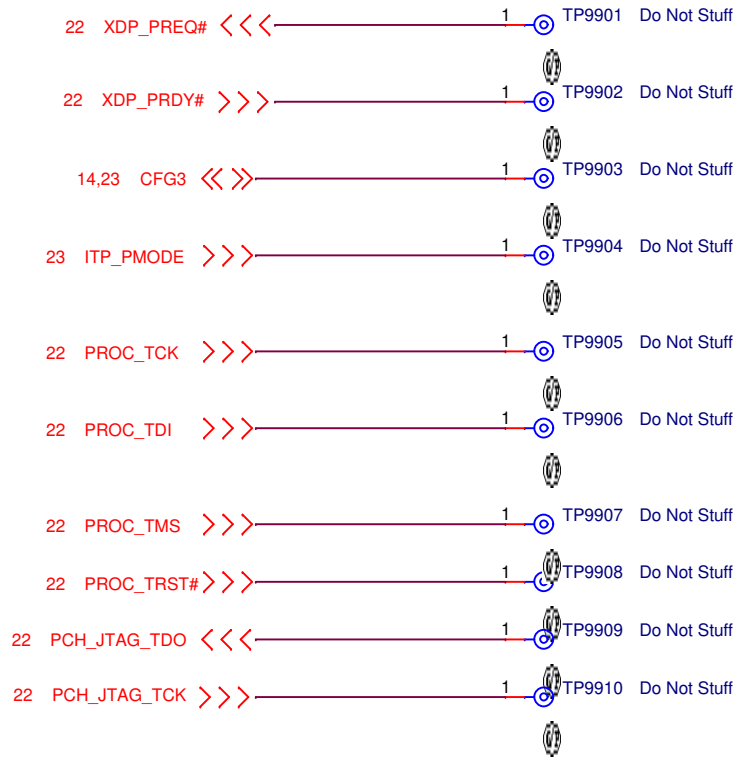

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Title: ***Debug (HDT debug)***

Size	Document Number	Rev
A4	**FAROE 14" Pavilion**	**SA**

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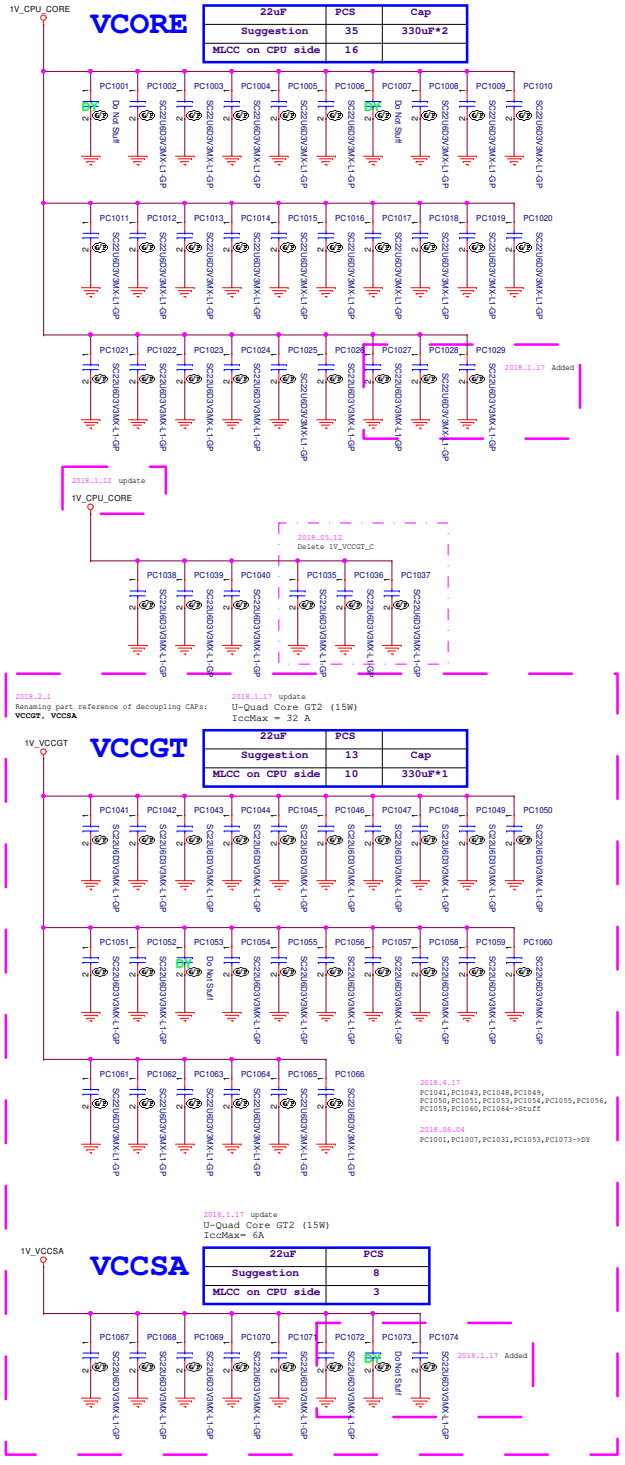
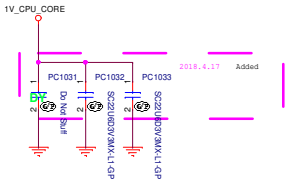
Main Func = CPU





2018.1.12 updated
#575412 PDG rev.0.7

Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
$V_{CC_{CORE}}$		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.

Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
$V_{CC_{GT}}$	15x 22uF 0603		Place underneath the package
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
$V_{CC_{SA}}$		*4x 0402*	*Placeholder only.*
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805		*Placeholder Only*
V_{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
$V_{CC_{IO}}$	4x 1uF 0201		Place underneath the package
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		*Placeholder Only*
$V_{CC_{PLL\_OC}}$	1x 1uF 0402		Do not merge $V_{CC_{PLL}}$, $V_{CC_{PLL\_OC}}$ and $V_{CC_{ST}}$ to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
$V_{CC_{PLL}}$	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		*Placeholder Only.* Can be placed on as either Primary or back side cap.
$V_{CC_{ST}}$	1x 1uF 0402		
$V_{CC_{STG}}$	1x 1uF 0402		

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps >Power source.

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Title: ***CPU (Power CAP1)***

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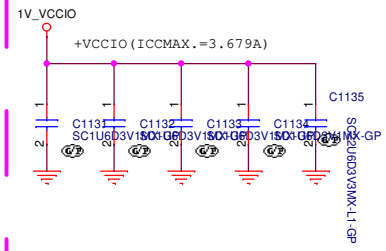
Main Func = CPU

VCCIO

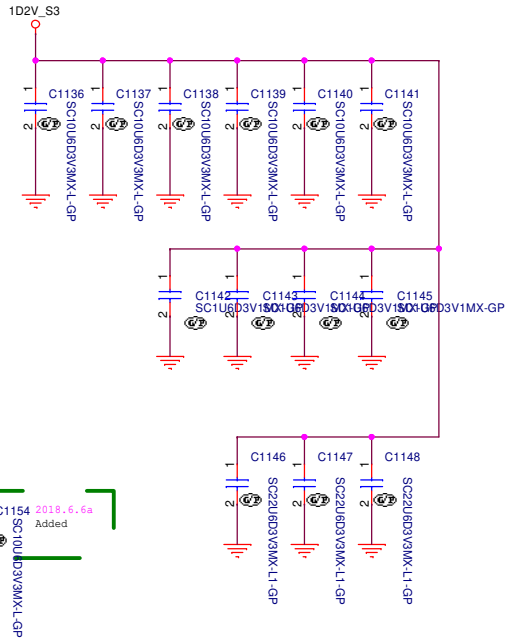


2018.2.1
Renaming part reference of decoupling CAPs:
VCCIO, VDDQ, VccST, VccSG, VccPLL_OC, VCCPLL

Place as close to the CPU as possible

VDDQ

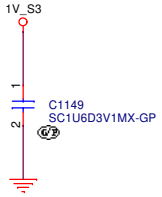
U-Quad Core GT2 (15W)
Imax = 3.3A



2018.1.12 update

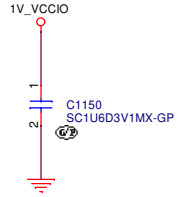
VccST

IccMax = 0.06A



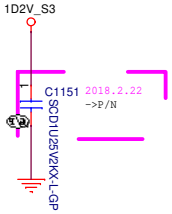
VccSTG

IccMax = 0.02 A



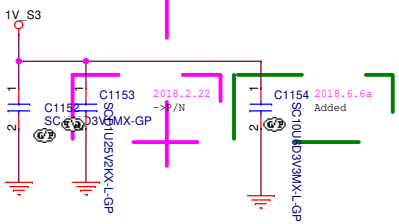
VccPLL_OC

IccMax = 0.12 A



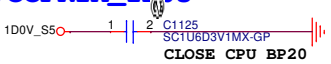
VCCPLL

IccMax = 0.13 A



CLOSE CPU BP11,BP2 CLOSE CPU BG1,BG2 CLOSE CPU BL27,BM26 CLOSE CPU BR11,BT11

VCCPRIM_1P05



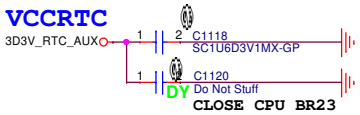
1uF*1

CLOSE CPU BP20

VCCDPHY_1P24

N/A

VCCRTC



1uF*1
0.1uF*1(DY)

CLOSE CPU BR23

VCCPRIM_CORE

1uF*1(DY)

CLOSE CPU BU15

VCCDPHY_EC_1P24

4.7uFx1

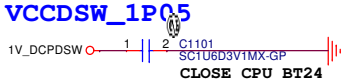
CLOSE CPU CP25

DCPRTC

0.1uF*1(DY)

CLOSE CPU BP24

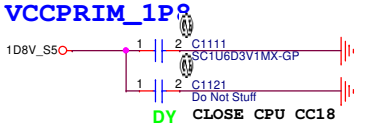
VCCDSW_1P05



1uF*1

CLOSE CPU BT24

VCCPRIM_1P8



1uF*1
1uF*1(DY)

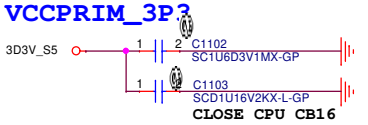
CLOSE CPU CC18

VCCPRIM_MPHY_1P05

22uF*1

CLOSE CPU BV12

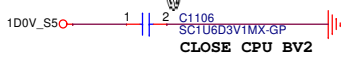
VCCPRIM_3P3



1uF*1(DY)
0.1uF*1(DY)

CLOSE CPU CB16

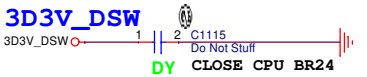
VCCAMPHYPLL_1P05



1uF*1
47uF*1(DY)

CLOSE CPU BV2

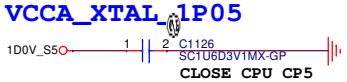
3D3V_DSW



1uF*1(DY)

CLOSE CPU BR24

VCCA_XTAL_1P05



1uF*1
47uF*1(DY)

CLOSE CPU CP5

VCCHDA

N/A

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Title	*CPU (Power CAP2)*	
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2018.7.20 Change P/N

H1 Do Not Stuff
H2 Do Not Stuff
H3 Do Not Stuff
H4 Do Not Stuff
H5 Do Not Stuff

Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff

2018.2.22 ->P/N

H6 Do Not Stuff
H7 Do Not Stuff
H8 Do Not Stuff
H9 Do Not Stuff

Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff

2018.4.3 ->P/N(ZZ.00PAD.5S1->ZZ.00PAD.VK1)

H10 Do Not Stuff
H11 Do Not Stuff
H12 Do Not Stuff
H13 Do Not Stuff

Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff

2018.7.20 ADD

HS1
STF237R113H86-GP
434.07K0E.0001

HS2
STF237R113H86-GP
434.07K0E.0001

CLIP10 SPRING-166-GP
CLIP1 SPRING-166-GP
CLIP2 SPRING-166-GP
CLIP3 SPRING-166-GP
CLIP4 SPRING-166-GP
CLIP5 SPRING-166-GP
CLIP6 SPRING-166-GP
CLIP7 SPRING-166-GP

34.41L50.001 34.41L50.001 34.41L50.001 34.41L50.001 34.41L50.001 34.41L50.001 34.41L50.001 34.41L50.001

CLIP8 SPRING-166-GP
CLIP9 SPRING-166-GP

34.41L50.001 34.41L50.001

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CLIP12 SPRING-166-GP
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CLIP14 SUL-1315A1M-GP
CLIP15 SUL-1315A1M-GP
CLIP16 SUL-1315A1M-GP

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SPR2 SPRING-U4-GP
34.40U07.001
RV2
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2nd = 83.10603.BA0
SPR2_GND

SPR3 SPRING-U4-GP
34.40U07.001
RV3
SFI0603-240E2R5PP-LF-GP
83.60324.0A0
2nd = 83.10603.BA0
SPR3_GND

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Title: UNUSED PARTS (ME part)

Size: A3 | Document Number: FAROE 14" Pavilion | Rev: SA

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