GENERAL DESCRIPTION

OB2736x is a high frequency Quasi-Resonant(QR) controller with 650V GaN FET intergrated. It is optimized for high performance, low EMI, low standby power consumption and wide output voltage range PD adapter solutions, together with PD secondary controller, such as OB2613. The controller is as well compatible with cost effective offline flyback converter applications covering a wide output range.

With On-Bright proprietary technology, OB2736x operates in QR Valley lockout operation in high line input voltage at normal load condition. To minimize switching loss, the maximum average switching frequency in QR mode is internally limited to 225KHz. As the load decreases, at light load, it operates in Fast frequency decreasing mode with lower frequency for high power conversion efficiency. When the load is very small, the IC operates in 'Extended Burst Mode' to minimize the standby power loss. Additionally, in the low line input voltage, the IC operates in fixed frequency (100KHz) CCM mode at the heavy loading. As a result, high conversion efficiency can be achieved in the whole loading range.

High voltage startup is implemented in OB2736x, which features with short startup time and low standby power loss.

OB2736x offers complete protection including brownout protection, cycle-by-cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP), output short protection (SCP), output and VDD over voltage protection. Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 22KHz is minimized to avoid audio noise during operation.

OB2736x is offered in SOP8 package.

FEATURES

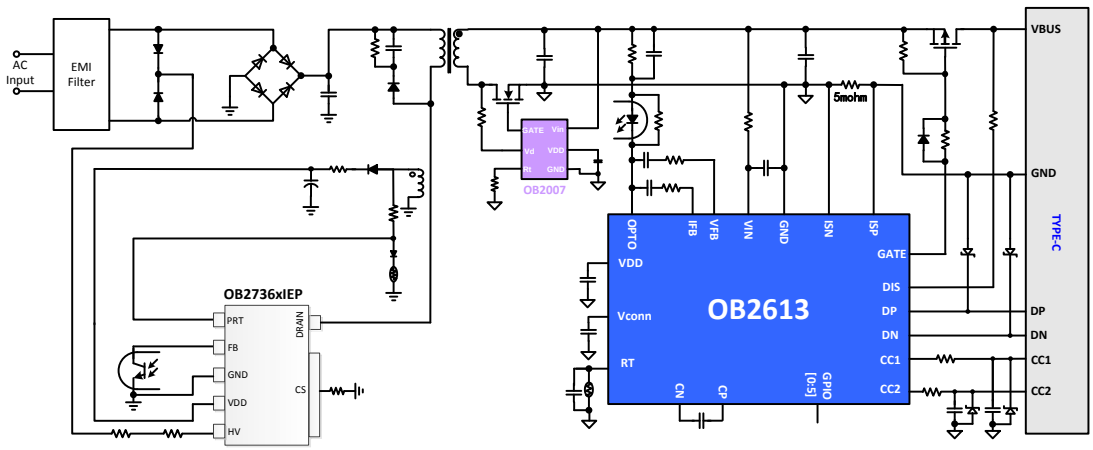
- Multi-Mode Operation
  - 225KHz max. average frequency in QR mode @ high line
  - 100KHz min. average frequency in CCM mode @ low line
  - Valley lockout operation @ Green Mode
  - Fast frequency decreasing(FFD) @Light load
  - Burst Mode @ Deep Light Load & No Load
- Adaptive loop gain compensation with load detection
- Extended burst mode control for improved efficiency and low standby power
- Power on soft start reducing MOSFET Vds stress
- Adaptive frequency shuffling for EMI
- Low operating current at no/light load
- Audio noise free operation
- High voltage startup integrating intelligent brownout detection, AC off detection with X-CAP discharge function
- Comprehensive auto-recovery protection
  - VDD under voltage lockout with hysteresis (UVLO)
  - Cycle-by-cycle over current protection (OCP)
  - Overload protection (OLP)
  - Over temperature protection (OTP)
  - VDD over voltage protection
  - Output over voltage protection
  - Output short protection (SCP)
  - Brownout protection
  - Output diode short protection

APPLICATIONS

Offline AC/DC flyback converter for

- High power density GaN FETs PD adapters

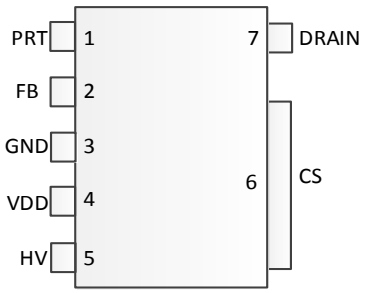
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The OB2736x is offered in LSOP8-7 package, shown as below.



Ordering Information

Part Number	Description
OB2736RIEP-H	LSOP8-7, Halogen-free, Tube
OB2736RIEPA-H	LSOP8-7,Halogen-free, T&R
OB2736VIEP-H	LSOP8-7, Halogen-free, Tube
OB2736VIEPA-H	LSOP8-7,Halogen-free, T&R
OB2736WIEP-H	LSOP8-7, Halogen-free, Tube
OB2736WIEPA-H	LSOP8-7,Halogen-free, T&R

Package Dissipation Rating

Package	RθJA(℃/W)
LSOP8-7	80

Recommended operating condition

Symbol	Parameter	Range
VDD	VDD Supply Voltage	10 to 50V

Absolute Maximum Ratings

Parameter	Value
DRAIN Voltage	-0.3 to 650V
Transient DRAIN Voltage	-0.3 to 750V Note2
VDD DC Supply Voltage	54V
High-Voltage Pin, HV	-0.3 to 700 V
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
PRT Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature TJ	-40 to 150 ℃
Min/Max Storage Temperature Tstg	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Note2: The transient DRAIN voltage is relaxed to 750V for surge ratings during non-repetitive events that are<200us and repetitive events that are<100ns.

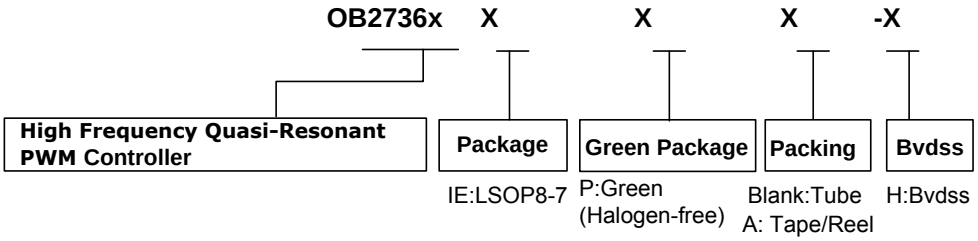
Note3: The negative voltage spike amplitude is relaxed to -1V under the condition that spike duty cycle is in less than 5%, or its equivalent average current is in less than 1mA.

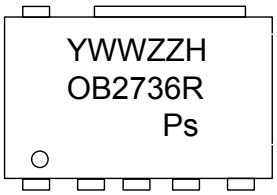
Output Power Table

Product	230VAC±15%	85-265VAC
	Adapter[1]	Adapter[1]
OB2736RIEP	38	33
OB2736VIEP	50	45
OB2736WIEP	70	65

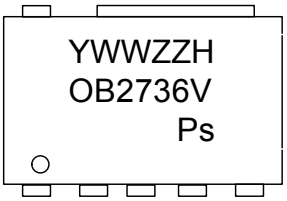
Note: Maximum practical continuous power in an adapter design with sufficient drain pattern as a heat sink, at 40℃ ambient.

Marking Information

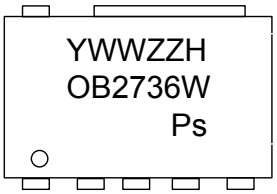




Y:Year Code
WW:Week Code(01-52)
ZZ:Lot Code
H:Bvdss
R:Mos code
P:Character Code
s:Internal Code(Optional)



Y:Year Code
WW:Week Code(01-52)
ZZ:Lot Code
H:Bvdss
V:Mos code
P:Green Package(Halogen-free)
s:Internal Code(Optional)



Y:Year Code
WW:Week Code(01-52)
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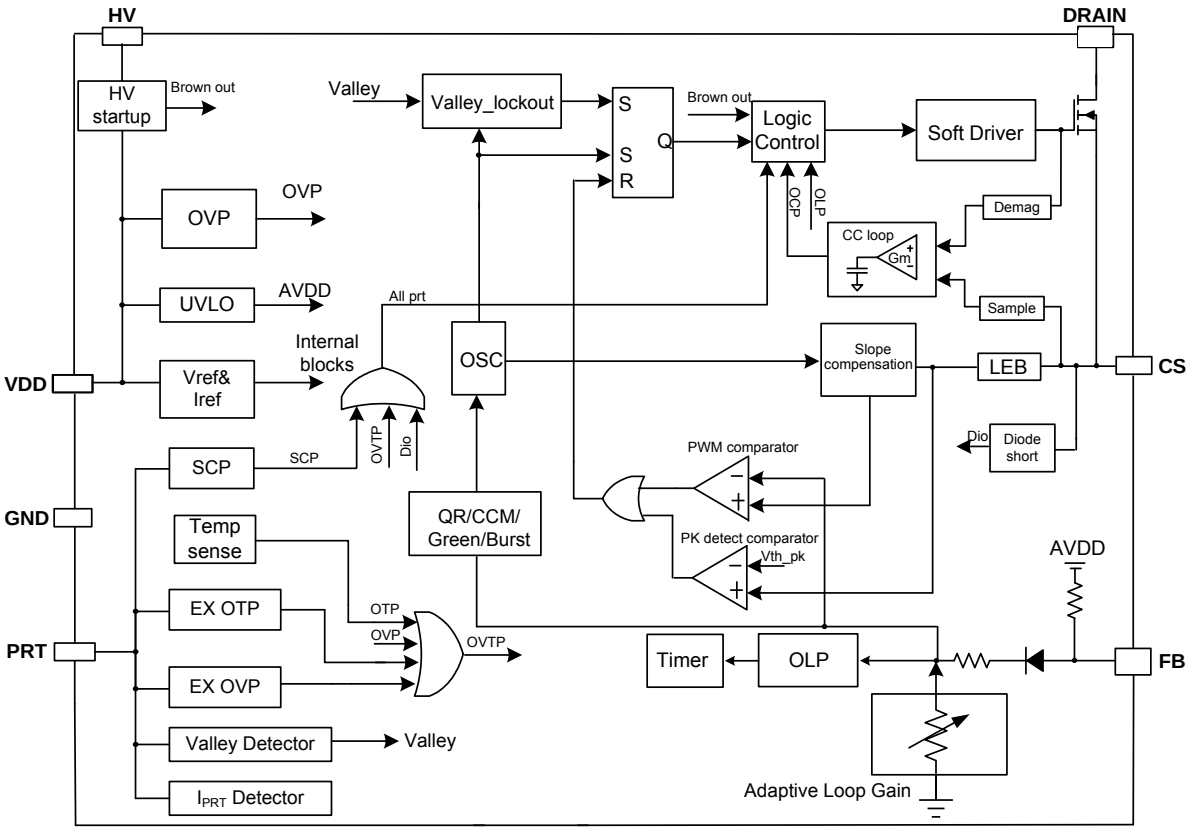
H:Bvdss
W:Mos code
P:Green Package(Halogen-free)
s:Internal Code(Optional)

TERMINAL ASSIGNMENTS

Pin NO.	Pin Name	I/O	Description
1	PRT	I	Multiple functions pin. Connecting a NTC resistor to ground for OTP detection. Connecting a resistor from Vaux can adjust IOVP/ISCP trigger current and detect transformer core demagnetization. If both OTP and OVP/SCP are needed, a diode should be connected between PRT pin and the NTC resistor.
2	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at CS pin
3	GND	P	Ground
4	VDD	P	Power Supply
5	HV	P	Connected to the line input via resistors and diodes for startup and x-cap discharge, this PIN allows the brownout detection as well.
6	DRAIN	I	GaN FET Drain pin.
7	CS	I	Current sense input

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(T_A = 25℃, VDD=18V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
HV Startup						
IHV1	Supply current from HV pin @VDD>1V	VDD=13.5V, HV=120V	1	2	5	mA
IHV2	Supply current from HV pin @VDD<1V	VDD=0.5V,HV=120V	0.3	0.57	0.85	mA
leakage	HV pin leakage current after startup	VDD=18V, HV=500V		15	30	uA
Supply Voltage (VDD)						
I startup	VDD Start up Current	VDD=UVLO(OFF)-1V, measure leakage current into VDD		5	10	uA
I_VDD_Operation	Normal Operation Current	V_{FB}=3V, CL=1nF		3	4	mA
I_VDD_Burst	Burst Operation Current	V_{FB}=0.5V, CL=1nF		0.65	0.85	mA
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		13.8	14.8	15.8	V
UVLO(HOLD)	VDD Holdup Enter Voltage to Turn on Gate	V_{FB}=0.5V	7.5	8	8.5	V
UVLO(ON)_PRE	PRE VDD Under Voltage Lockout Enter to Turn off Gate	V_{FB}=3V	6.9	7.4	7.9	V
UVLO(ON)	VDD Under Voltage Lockout Enter		6.5	7	7.5	V
VOVP	Over voltage protection voltage	FB=3V Ramp up VDD until gate clock is off	51	52.5	54	V
T_D_rst	Restart time for OLP/ SCP protection occurs			1.4		s
Feedback Input Section(FB Pin)						
V_{FB}_Open	V_{FB} Open Loop Voltage		4.6	5.1	5.6	V
Avcs	PWM input gain ΔVFB/ΔVCS	FB>1.45V & with Hysteresis under Iprt>127uA		5		V/V
		FB<1.35V with Hysteresis under Iprt>127uA		3		V/V
		FB>1.45V with Hysteresis under 65uA<Iprt<121uA		6.1		V/V
		FB<1.35V with Hysteresis under 65uA<Iprt<121uA		3.6		V/V
		Iprt<60uA		4.5		V/V
Ton_max	Max Ton time @ VDD=18V, VFB=3V,VCS=0V		6.2	7.7	9.2	us
Vref_green	The threshold enter green mode		2.05	2.25	2.45	V
Vref_FFD_L	The threshold entering Fast Freq.	Iprt>65uA		1.35		V

	decreasing(FFD) mode					
Vref_FFD_H	The threshold exiting Fast Freq. decreasing mode	Iprt>65uA		1.5		V
Vref_burst_H	The threshold exit burst mode	Iprt>65uA	0.75	0.90	1.05	V
		Iprt≦60uA	0.70	0.85	1.00	V
Vref_burst_L	The threshold enter burst mode	Iprt>65uA	0.65	0.80	0.95	V
		Iprt≦60uA	0.60	0.75	0.90	V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current	290	380	470	uA
Z_{FB}_IN	Input Impedance			15		KΩ
V_{TH}_Openloop	The open loop FB Threshold Voltage		4.1	4.5	4.9	V
T_D_ Openloop	The open loop protection debounce Time		50	60	70	ms
Current Sense Input(CS Pin)						
SST_CS	Soft start time of CS threshold			4		ms
T_blanking	Leading edge blanking time		160	220	280	ns
T_D_OC	Over Current Detection and Control Delay	From Over Current Occurs till the gate driver output starts to turn off		80		ns
Vth_ocp	Internal OCP protection threshold		0.248	0.268	0.288	V
Vth_PK	Internal current limiting threshold	HV=300V	0.495	0.525	0.555	V
		HV=120V	0.57	0.60	0.63	V
ΔVmax_CS_shuffling	Max CS jittering of QR mode	FB > 1.65V & under Iprt>127uA		45		mV
F_shuffling_CS	CS Shuffling frequency of QR mode	FB > 1.65V & under Iprt>127uA		4		KHz
Oscillator						
F_QR_inc	Average switching frequency for increasing valley in QR mode	FB > 2.25V		225		KHz
F_QR_dec	Average switching frequency for decreasing valley in QR mode	FB > 2.25V		148		KHz
Td_valley	Valley increased or decreased debounce time			400		cycles
F_CCM_low line	Minimum clamp oscillation frequency in CCM mode @ low line	FB > 2.25V	90	100	110	KHz
Fmin_QR_high line	Frequency low clamp in QR mode @ high line	FB > 2.25V		25		KHz
F_FFD_in	Switching frequency entering Fast Freq.	FB =1.3V		45		KHz

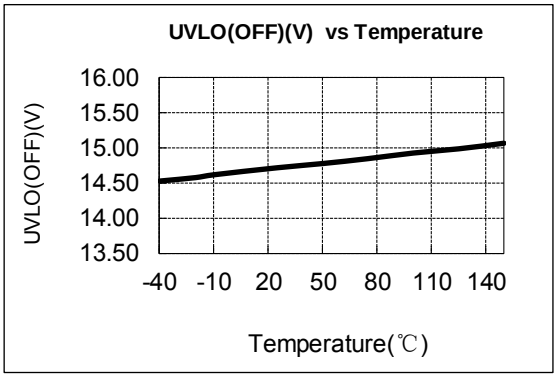
	decreasing(FFD) mode					
Δf_OSC_CCM	Frequency jittering of clamp fmin_CCM			±4		%
F_shuffling_CCM	Shuffling frequency clamp fmin_CCM	FB > 1.65V & under Iprt>127uA		4		KHz
F_burst	Burst mode frequency			25		KHz
PRT pin						
Ibias	Output bias current expect during OVP detection			20		uA
IRT	Output current for external OTP detection		93	100	107	uA
VOTP	Threshold voltage for external OTP		0.93	1.00	1.07	V
Td_ex_OTP	EX OTP debounce time			50		cycles
I_ovp	Current threshold for adjustable output OVP		215	240	265	uA
Td_ ovp/scp	OVP /SCP debounce time			8		cycles
I_scp	SCP threshold		11	16	21	uA
Td_scp	SCP detect after startup			15		ms
Tsp	Output voltage Sampling Blanking Time	FB>2.25V		1.3		us
		FB<1.35V		1.0		us
On Chip OTP						
OTP Level				155		℃
OTP exit				125		℃

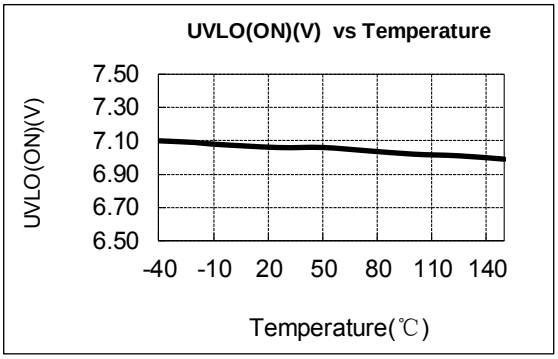
Parameter / Product	Max VDS(V) GaN FET Max Drain-Source Voltage			Rds,on(Ω) On resistance		
	Min	Typ.	Max	Min	Typ.	Max
OB2736RIEP-H			650[note]		0.62	
OB2736VIEP-H			650[note]		0.37	
OB2736WIEP-H			650[note]		0.18	

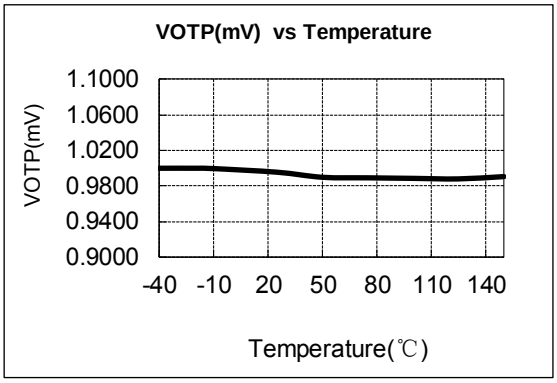
Note: The transient VDS voltage is relaxed to 750V for surge ratings during non-repetitive events that are<200us and repetitive events that are<100ns.

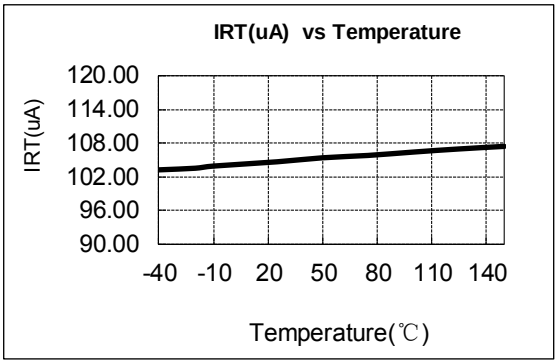
CHARACTERIZATION PLOTS

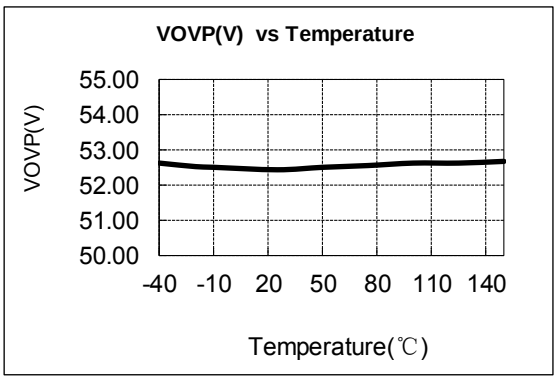
VDD = 18V, TA = 25℃ condition applies if not otherwise noted.

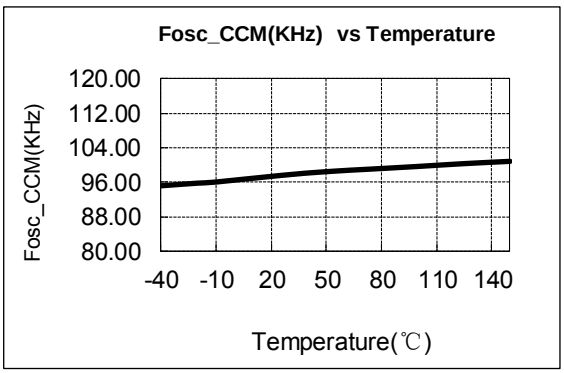


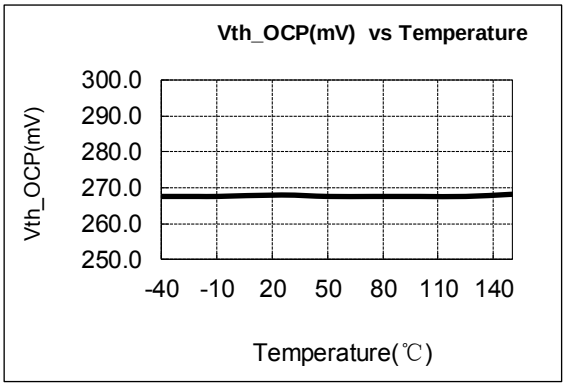


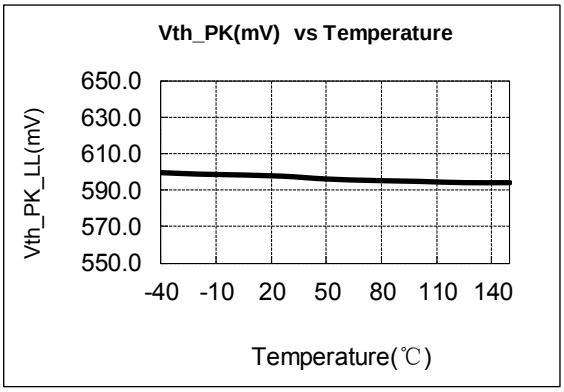












OPERATION DESCRIPTION

Quasi-Resonant (QR) converter typically features lower EMI and higher power conversion efficiency compared to conventional hard-switched converter with a fixed switching frequency. OB2736x is a highly integrated high frequency Quasi-Resonant (QR) controller with adaptive multi-mode regulation, optimized for high power density GaN FETs PD adapter solutions, together with PD secondary controller, such as OB2613. The controller is as well compatible with cost effective offline flyback converter applications covering a wide output range. The 'Extended burst mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Internal High Voltage Startup and Under Voltage Lockout (UVLO)

OB2736x integrates HV startup circuit, and provides about 2mA current to charge VDD pin during power on state from HV pin. When VDD voltage is higher than UVLO(OFF), the charge current is switched off. At this moment, the VDD capacitor provides current to OB2736x until the auxiliary winding of the main transformer starts to provide the operation current.

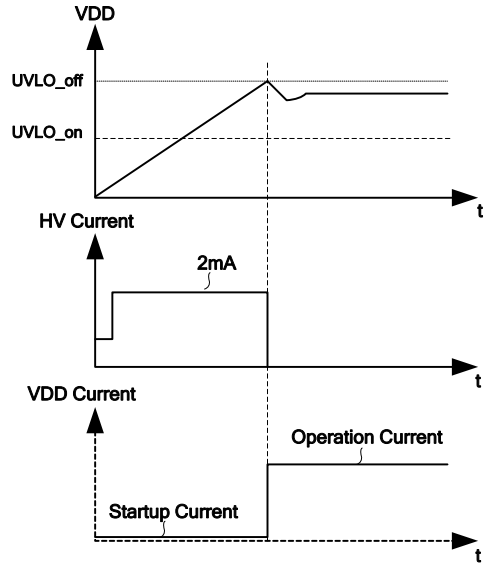


Fig.1 Startup current timing

Operating Current

The Operating current of OB2736x is low at 3mA (typical). Good efficiency is achieved with OB2736x low operation current together with the 'extended burst mode' control features.

Soft Start

OB2736x features an internal 4ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the CS peak voltage is gradually increased from 0 V to the maximum level. Every restart up is followed by a soft start.

Adaptive Loop Gain Compensation

With On-Bright proprietary technology, an adaptive loop compensation is implemented to ensure the system loop stability for wide output voltage range according to FB voltage and PRT current detection.

Frequency shuffling for EMI improvement

In OB2736x, Adaptive frequency shuffling (switching frequency modulation) is implemented over the universal input voltage and load range. When the fixed frequency CCM mode is reached, the triangular frequency shuffling will be automatically added to the system to improve the EMI performance. When the system exits fixed frequency CCM mode and enters in the QR mode, a random CS shuffling (ΔV_CS_shuffling) will be automatically added to system to adjust the turn-on time and demagnetization time. In addition, a triangular jittering of valley conduction pulse is supplemented in the Quasi-Resonant mode to regulate the gate turn-on point. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Extended Burst Mode Operation

At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below Vref_burst_L (the threshold enter burst mode) and device enters Burst Mode control. The Gate drive output switches when FB input rises back to Vref_burst_H (the threshold exit burst mode). Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to greatest extend.

Multi-Mode Operation for High Efficiency

OB2736x is a multi-mode PWM controller, integrating the QR, CCM, green and burst mode. The controller changes the operation mode

according to line voltage, output voltage and load conditions.

At normal full load conditions (VFB> 2.25V, Fig. 2), when the system input is in low line input range, the IC operates in fixed 100KHz frequency CCM mode. When the system input is in high line input range, the IC operates in QR mode, in which average maximum frequency is clamped at 225KHz. With On-Bright proprietary technology, OB2736x implements a valley lockout circuitry to avoid valley skipping when it enters in QR mode. As is shown in Fig. 2, once n valley is selected, the controller keeps the locked valley until the output power varies significantly. When the output load is decreased, the CS peak is reduced and the switching frequency is increased. When the operation frequency is higher than F_QR_inc after 400 PWM cycles (typical) debounce time, the operating n valley is added by one (n+1). Otherwise, when the output load is increased, the CS peak is rised and the switching frequency is decreased. Once the operation frequency is forced equal to F_QR_dec after 400 PWM cycles debounce time, the operating valley is reduced by one. In addition, an intermediate state in which n/n+1 adjacent valleys coexisting is implemented in OB2736x to improve the valley locked stability, based on On-Bright proprietary technology. Thus switching frequency is optimized to a tight range under a fixed loading. In this way, high power conversion efficiency can be achieved in the universal input range when system is at heavy loading conditions. The efficiency and system cost is controlled at an optimal level.

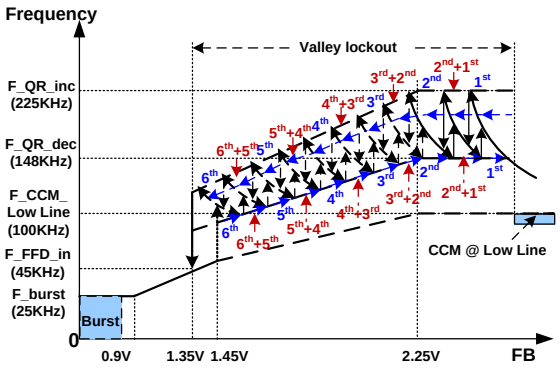


Fig. 2 Frequency vs Feedback voltage

At green mode conditions (2.25V>VFB>1.35V, Fig.2), the system operates in PFM (pulse frequency modulation) green mode for high power conversion efficiency. Generally, in flyback converter, the decreasing of load results in voltage level decreasing at FB pin. The controller monitors the voltage level at FB and control the switching frequency. However, the valley switching characteristic is still preserved in PFM mode. OB2736x automatically operates in maximum 6th valley locked conduction to achieve the frequency decreasing in the PFM green mode. At light load conditions(1.35V>VFB>0.9V), When FB voltage decreases below the 1.35V after 1ms debounce time, OB2736x enters the frequency fast decreasing mode. The operating state skips from high frequency(typical 100KHz) of 6th valley switching to forced low frequency(typical 45KHz) of no valley switching. In such way, a smooth frequency fold-back is realized and high power conversion efficiency is achieved.

At no load or very light load conditions (VFB<0.9V), the system operates in On-Bright's proprietary "extended burst mode". In the extended burst mode, the switching frequency at below 22KHz is minimized to avoid audio noise during operation.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2736x current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense voltage and the FB voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Demagnetization Detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through PRT pin. This voltage features a flyback polarity. After the on time (determined by the CS voltage and FB voltage), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately $1/2\pi\sqrt{L_p C_d}$, where L_p is the primary self inductance of primary winding of the transformer and C_d is the capacitance on the drain node.

The typical detection level is fixed at 85mV(typical) at the PRT pin. Demagnetization is recognized by detection of a possible "valley" when the voltage at PRT is below 85mV in falling edge.

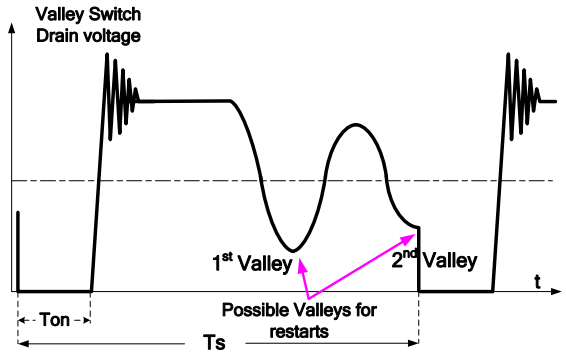


Fig. 3 Valley detection

Programmable OCP and Peak output Current Controls

In order to meet peak current output requirement, OB2736x sets up two levels output current protection thresholds. The two thresholds correspond to the normal OCP protection and peak power protection respectively. When output current exceeds the OCP threshold for 60ms (typical), OCP protection occurs. The OCP loop ensures the output OCP has a very tight range and is only related with turns ratio and Rsense. The specification for output OCP protection voltage threshold, Vocp_ref, is 0.268V (typical).

$$I_{out} = \frac{1}{T_s}\int_0^{Tdem} n \cdot \frac{V_{cs\_peak}}{2Rsense} = n \cdot \frac{T_{dem}}{T_s} \cdot \frac{V_{cs\_peak}}{2Rsense}$$

$$I_{ocp} = n \cdot \frac{Vocp\_ref}{2Rsense}$$

Where V_{cs_peak} / 2Rsense is the primary average current during the on-time, Tdem is the demagnization period, Ts is the Switching period, n is the turns ratio of the primary winding and secondary winding. Rsense is the current sensing resistance and Vocp_ref is OCP threshold reference.

The calculated Iout is compared with Iocp, when Iout>Iocp, the OCP occurs. To simplify,

If $\frac{T_{dem} \cdot V_{cs\_peak}}{T_s} > V_{ocp\_ref}$,

Then, the OCP occurs.

Fig.4 is the realization method of the OCP calculation. S1 is CS peak point sampling switch. At S1 shut down time, the voltage of C1 capacitor is the V_{cs_peak}, S2 is integral of current in the Tdem time. Therefore, the real OCP point is related to the rising/falling edge due to its influence on the peak point sampling.

OB2736x also provides a cycle-by-cycle CS peak limiting. The maximum cycle-by-cycle CS peak threshold voltage Vth_PK is 0.525V(typical) in the high line voltage, and in the low line voltage, the Vth_PK is 0.6V(typical).

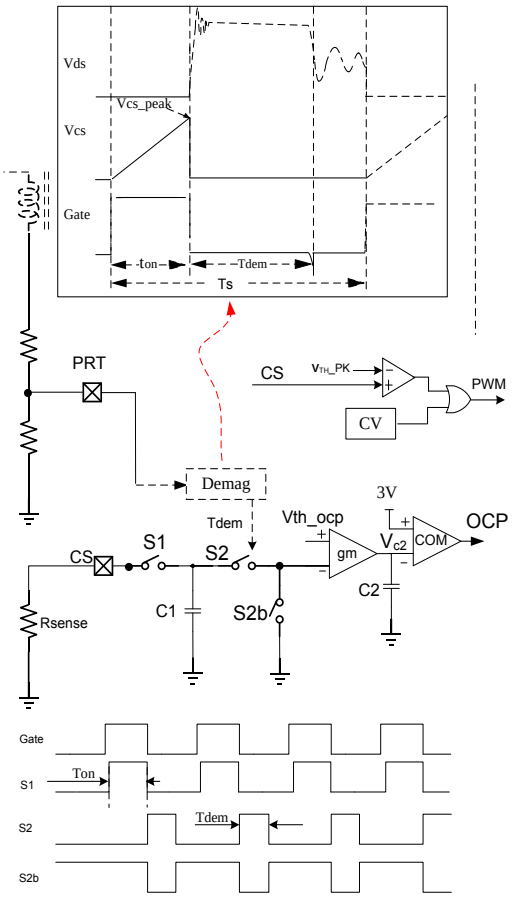
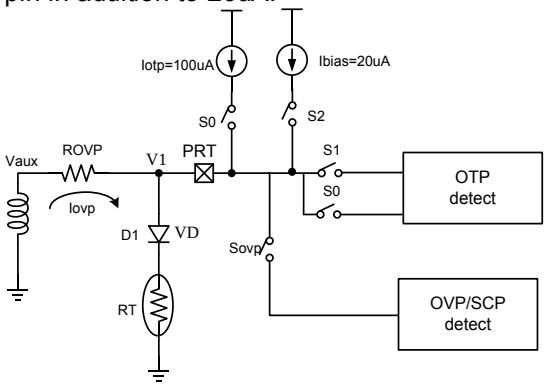


Fig.4 OCP circuit diagram

Dual Function of External OTP and Output OVP/SCP

On-Bright proprietary dual function of external OTP and output OVP provides feasible and accurate detection of external OTP through NTC resistor and output OVP. The dual function is realized through time-division technology as shown in the Fig. 5.

There is a 20uA(typical) bias current outflow when S2=1, that's S0= "1" or S1= "1". For external OTP detection, when switch control signal S1= "1", the 20uA (typical) current flows out from PRT pin. When switch control signal S0= "1", another 100uA (typical IRT) current flows out from PRT pin in addition to 20uA.



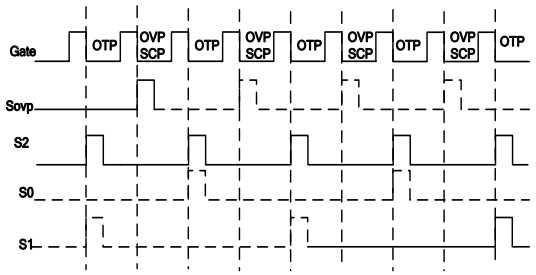


Fig. 5 PRT Pin protection timing

So the PRT pin voltage V1(s1) at phase S1="1" is:

$$V1(S1) = \frac{ROVP \cdot VD + RT \cdot Vaux + RT \cdot ROVP \times 20uA}{ROVP + RT}$$

The PRT pin voltage V1(s0) at phase S0="1" is

$$V1(S0) = \frac{ROVP \cdot VD + RT \cdot Vaux + RT \cdot ROVP(20uA + 100uA)}{ROVP + RT}$$

Vaux is the auxiliary winding demagnetization voltage.
VD is D1 forward voltage.
ROVP and RT are shown in Fig. 5.
Voltage difference of ΔVotp at phase S0 and S1 phase is

$$\Delta V_{otp} = V1(S0) - V1(S1) = \frac{RT \cdot ROVP}{ROVP + RT} \times 100uA$$

This voltage difference cancels the effect of D1 diode forward voltage.
When ΔVotp< VOTP (1.0V typical), external OTP auto-recovery protection is triggered after 50 (typical) PWM cycles debounce.
For output OVP detection, when Sovp= "1", Iovp is equal to (Naux/Nsec)*(Vout+Vdiode)/ROVP. If Iovp is larger than 240uA (typical Ioutput_ovp), output OVP is triggered. The output OVP voltage is calculated as

$$V_{outovp} = \frac{I_{output\_ovp} \times N_{sec} \times RPRT}{N_{aux}} - V_{diode}$$

Nsec is transformer secondary winding turns, Naux is transformer auxiliary winding turns, Vdiode is the secondary output diode forward voltage.
OVP auto-recovery protection is triggered after 8 Gate cycles debounce. By selecting proper Rovp resistance, output OVP level can be programmed.
For output SCP detection, when Sovp= "1", Iscp is equal to (Naux/Nsec)*(Vout+Vdiode)/ROVP. During the 15ms after the IC startup, if Iscp is less than 16uA (typical Iscp), SCP is triggered. The output SCP voltage calculation method is the same as output OVP detection.
SCP auto-recovery protection is triggered after 8 Gate cycles debounce. By selecting proper Rovp resistance, output SCP level can be programmed.

Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including OCP, output short protection, Under Voltage Lockout on VDD (UVLO) and over load protection, Over Temperature Protection (OTP), VDD and output Over Voltage Protection (OVP).
With On-Bright proprietary technology, the OCP is line voltage compensated to achieve constant output OCP limit over the universal input voltage range and its dependency on primary inductance and frequency is removed.
At overload condition when FB input voltage exceeds power limit threshold value for more than Td_OLP, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit.

Intelligent Brown-in and Brown-out protection, AC off detection with X-CAP discharge function

A precise brown-in and brown-out detection is implemented by monitoring the rectified AC voltage on HV pin.
The HV pin is also used for AC off detection. When AC is off, the AC off state can be detected through HV pin. Then IC will provide a discharge path from HV pin to GND for the X-CAP discharge. OB2736x meets IEC62368-1 requirements.

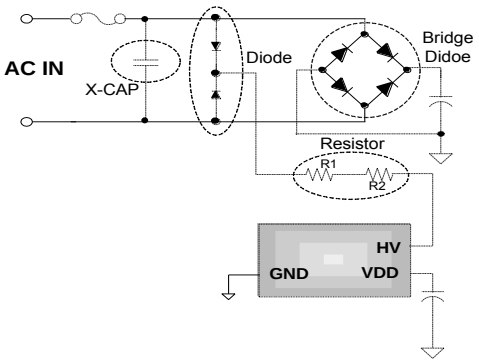


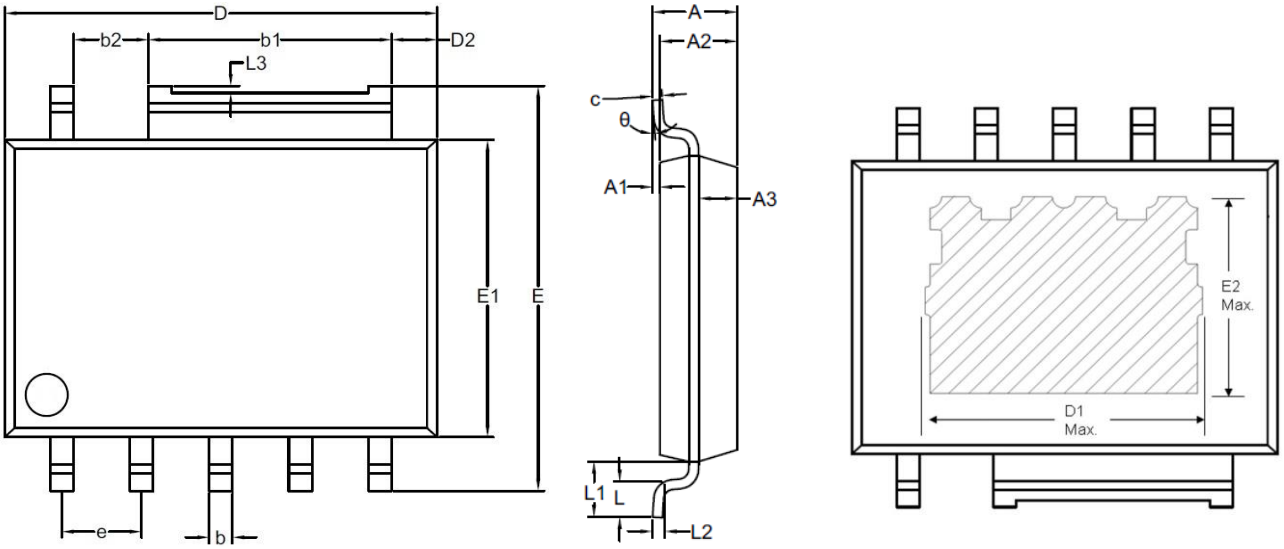
Fig.6 X-CAP discharge circuit

Discharge circuit main components selection

Components	Voltage/Current Stress Range
Bridge Diode	600-1000V, 0.5-20A.
Diode	1000V,1A
Resistor(R1,R2)	2K-20Kohm, 1/4W, SMD1206
X-CAP	0.1uF – 2.04uF

Note: R2 is recommended to be placed close to the HV PIN.

PACKAGE MECHANICAL DATA



TOP VIEW SIDE VIEW BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.60	1.95	0.063	0.077
A1	0.05	0.15	0.002	0.006
A2	1.50	1.70	0.059	0.067
A3	0.75	0.85	0.030	0.033
b	0.48	0.56	0.019	0.022
b1	5.18	5.26	0.204	0.207
b2	1.57	-	0.062	-
c	0.18	0.25	0.007	0.010
D	9.15	9.35	0.360	0.368
D1*	-	5.60	-	0.220
D2	0.865	1.085	0.034	0.043
E	8.55	8.75	0.337	0.344
E1	6.25	6.45	0.246	0.254
E2*	-	3.85	-	0.152
e	1.70 (BSC)		0.067 (BSC)	
L	0.69	0.79	0.027	0.031
L1	1.15 (REF)		0.045 (REF)	
L2	0.25 (REF)		0.010 (REF)	
L3	-	0.15	-	0.006
θ	0°	8°	0°	8°

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