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User's Guide

INTECH®

ITM-1601A™ LCM

16 Characters X 1 lines
with 5 X 8 dots format

(Liquid Crystal Display Module)

Contents

CHAPTER 1

Introduction to ITM-1601A LCM

ITM-1601A is a dot matrix character LCD module which is fabricated by low power COMS technology ,It can display 16 characters * 1 lines with 5*8 dots format. It interfaces with 4-bit or 8-bit MPU.

Features

- Display format: 16 characters * 1 lines
- STN yellow-green mode
- Easy interface with 4-bit or 8-bit MPU
- Low power consumption
- LED back-light
- Translucent light method
- Viewing angle: 6 O'clock
- Multiplex level: 1/16 duty, 1/5 bias
- LCD driver IC: KS0066
- Connector: Zebra

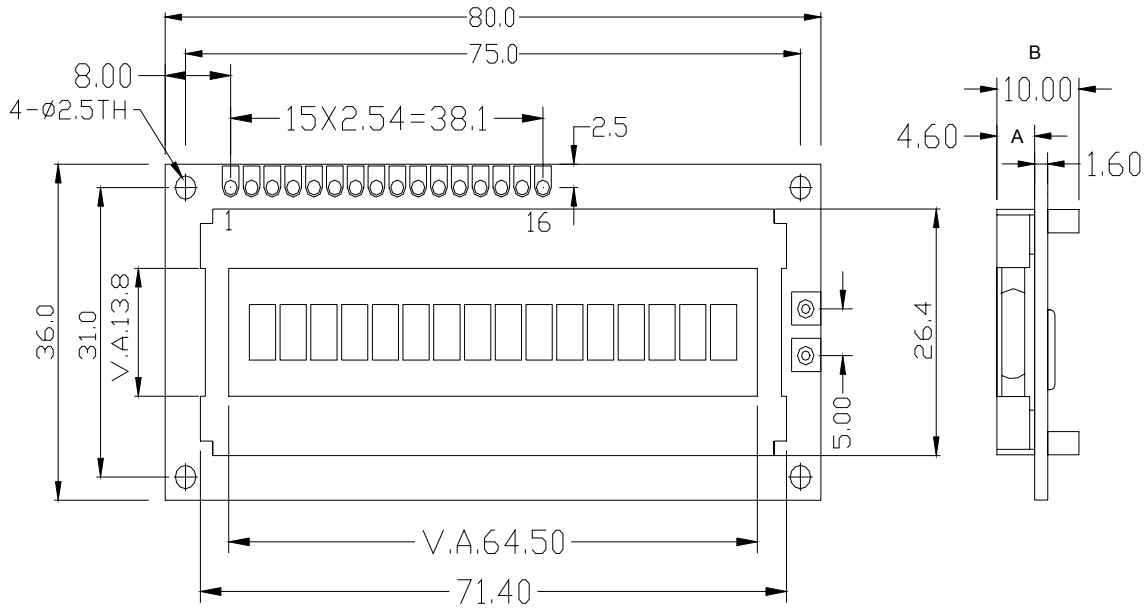
Mechanical Specifications

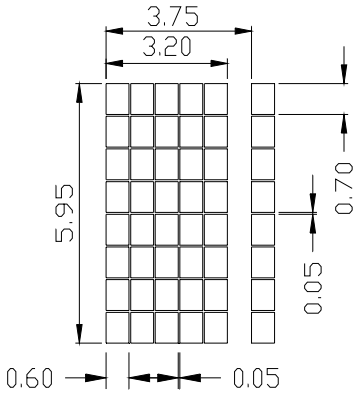
Item	Dimension	Unit
Module Size With LED B/L(W*H*T)	80.0*36.0*13.0	mm
Module Size(W*H*T)	80.0*36.0*10.0	mm
Viewing Area(W*H)	64.5*13.8	mm
Dot Size(W*H)	0.6*0.7	mm
Dot Pitch(W*H)	0.65*0.75	mm
Character Pitch	3.75*5.95	mm
Character Size(W*H)	3.20*5.95	mm
Character Font	5*8 dots	-

Temperature Characteristics

Parameter	Symbol	Rating	Unit
Operating temperature	Topr	0 ~ +50	℃
Storage temperature	Tstg	-20 ~ +70	℃

Figure 1. External Dimensions





	A	B
LOW	4.6	10.0
HIGH	7.6	13.0

*Note

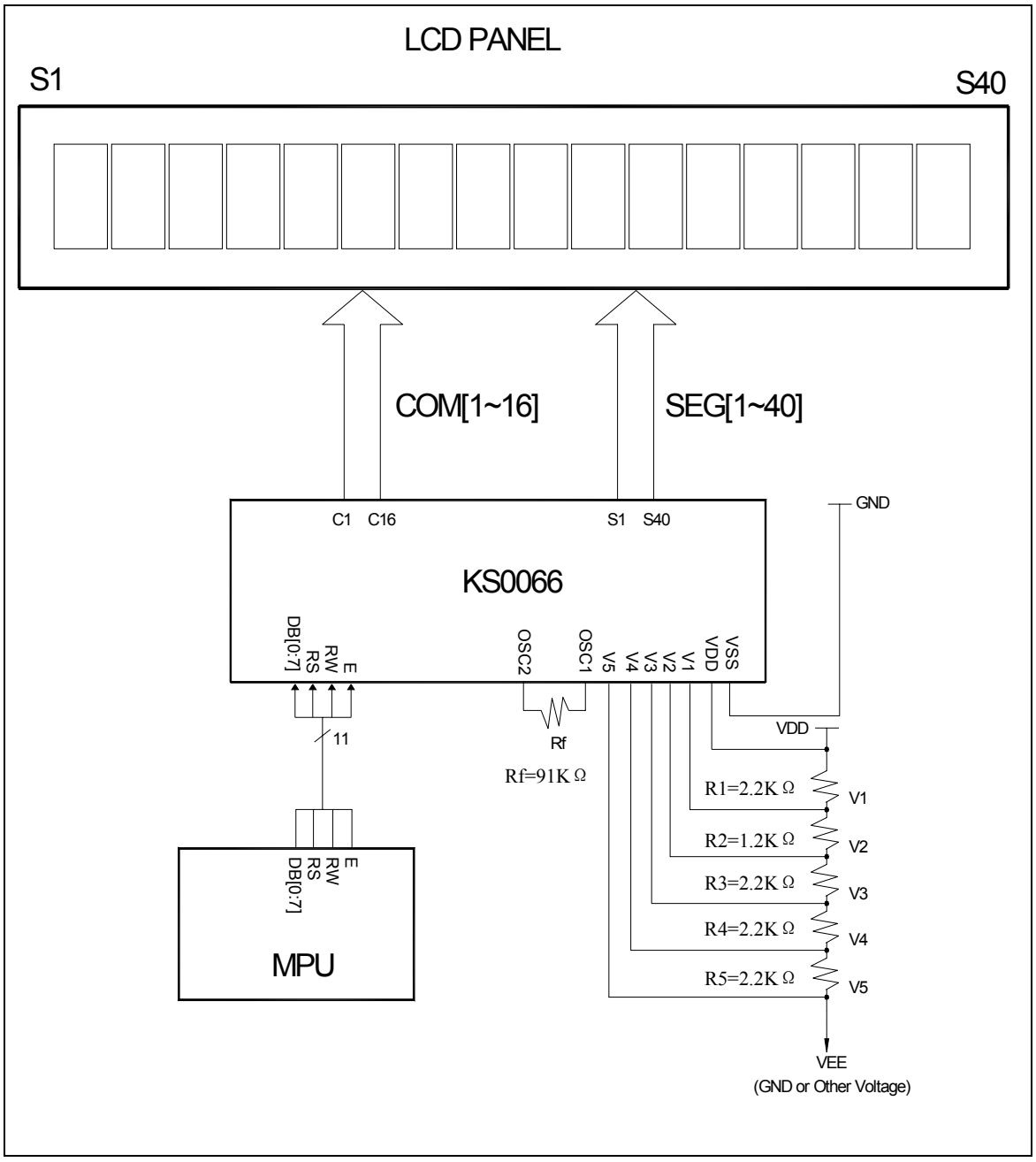
High is a module with LED back-light.

CONNECTION

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
VSS	VDD	VEE	RS	RW	E	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	A	K

Dimensions in Milimeters

Figure 2. Application Diagram



***Note**

1/16 duty, 1/5 bias

$V1 = V_{DD} - V_{LCD}/5$
$V2 = V_{DD} - 2V_{LCD}/5$
$V3 = V_{DD} - 3V_{LCD}/5$
$V4 = V_{DD} - 4V_{LCD}/5$
$V5 = V_{DD} - V_{LCD}$

Electro-Optical characteristics

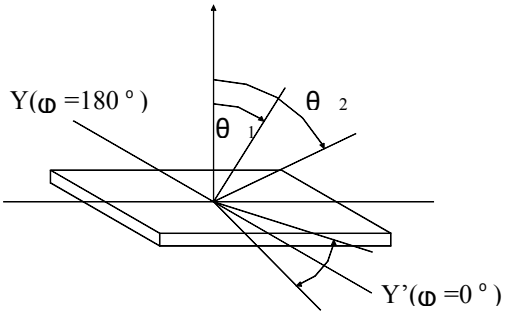
TN Type (Twisted Nematic)

Item	Symbol	Min.	Typ.	Max.	Unit	Condition	Note
Viewing Angle	$\frac{\theta_2 - \theta_1}{\phi}$	40	-	-	deg.	Cr = 2.0	1,2
Contrast Ratio	Cr	-	4	-	-	$\theta = 20^\circ$ $\phi = 0^\circ$	3
Response Time (rise)	t_R	-	110	-	ms	$\theta = 20^\circ$ $\phi = 0^\circ$	4
Response Time (fall)	t_F	-	110	-	ms	$\theta = 20^\circ$ $\phi = 0^\circ$	4

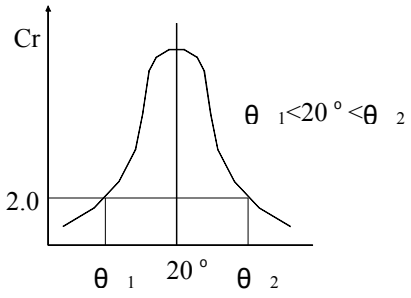
STN Type (Super Twisted Nematic)

Item	Symbol	Min.	Typ.	Max.	Unit	Condition	Note
Viewing Angle	$\frac{\theta_2 - \theta_1}{\phi}$	70 -90	-	+90	deg.	Cr = 2.0	1,2
Contrast Ratio	Cr	-	4	-	-	$\theta = 20^\circ$ $\phi = 0^\circ$	3
Response Time (rise)	t_R	-	110	-	ms	$\theta = 20^\circ$ $\phi = 0^\circ$	4
Response Time (fall)	t_F	-	110	-	ms	$\theta = 20^\circ$ $\phi = 0^\circ$	4

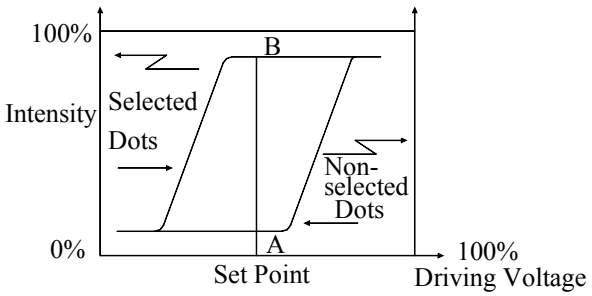
1. Definition of angle θ & φ



2. Definition of viewing angle θ 1 & φ 2



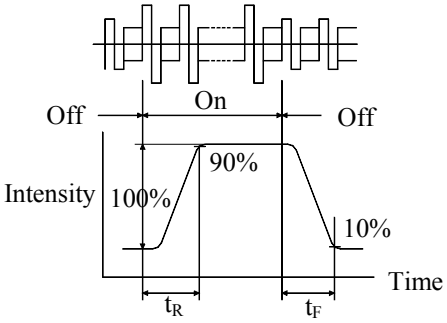
3. Definition of contrast Cr



$Cr = (A / B)^P$ Negative : P = -1

Positive : P = +1

4. Definition of optical response



Interface Pin Connections

Pin No.	Symbol	Name	Description
1	VSS	Power supply	0V (GND)
2	VDD	Power supply	Power supply for logic circuit and LCD (+4.5V~+5.5V)
3	VEE	LCD Supply Voltage	Bias voltage level for LCD driving
4	RS	Register select	Register select input. When RS= "High", data register is selected. When RS= "Low", instruction register is selected.
5	RW	Read/Write	Read/Write selection input. When RW= "High", read operation. When RW= "Low", write operation.
6	E	Read Write enable	Start enable signal to read or write the data
7	DB0	Data bus 0-7	DB0-DB3, in 8-bit bus mode, used as low order bi-directional data bus. During 4-bit bus mode, open these pins
8	DB1		
9	DB2		
10	DB3		
11	DB4		DB4-DB7, in 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order.
12	DB5		
13	DB6		
14	DB7		DB7 used for Busy Flag output
15	A		back-light anode
16	K		back-light cathode

Maximum Absolute Rate

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	-0.3 to +7.0	V
LCD Supply Voltage	V_{LCD}	V_{DD}-13.5 to V_{DD}+0.3	V
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V

*Note: Voltage greater than above may damage to the circuit. ($V_{DD} \geqslant V1 \geqslant V2 \geqslant V3 \geqslant V4 \geqslant V5$)

DC Electrical Characteristics

(V_{DD}=+4.5v~5.5v, V_{SS}=0v, Ta=-20℃ to +75℃)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	-	4.5	-	5.5	V
Operating Circuit (*1)	I_{DD1}	Ceramic resonator fosc=250KHz	-	0.55	0.8	mA
	I_{DD2}	Resistor oscillation external clock operation fosc=270kHz	-	0.35	0.6	
Input Voltage 1 (E,DB0-DB7,R/W,RS)	V_{IH1}	-	2.2	-	V_{DD}	V
	V_{IL1}	-	-0.3	-	0.6	
Input Voltage 2 (OSC1)	V_{IH2}		V_{DD} -1.0	-	V_{DD}	
	V_{IL2}		-0.2	-	1.0	
Output Voltage 1 (DB0-DB7)	V_{OH1}	I_{OH}=-0.205mA	2.4	-	-	
	V_{OL1}	I_{OL}=1.2mA	-	-	0.4	
Output Voltage 2 CLK1,CLK2,M,D	V_{OH2}	I_O=-40μA	0.9V_{DD}	-	-	
	V_{OL2}	I_O=40μA	-	-	0.1V_{DD}	
Voltage Drop COM[1~16],SEG[1~200]	Vd_{COM}	I_O=±0.1mA	-	-	1	
	Vd_{SEG}		-	-	1	
Input Leakage Current	I_{LKG}	V_{IN}=0 or V_{DD}	-1	-	1	μA
Input Low Current	I_{IL}	V_{DD}=5V	-50	-125	-250	
External Clock Frequency	f_{EC}	-	125	250	350	kHz
External Clock Duty	duty	-	45	50	55	%
External Clock Rise time	t_R	-	-	-	0.2	μs
External Clock Fall time	t_F	-	-	-	0.2	
Internal Clock Frequency	fosc1	R_f = 91kΩ ±2%	190	270	350	kHz
Ceramic Resonator Oscillation Frquency	fosc2	-	245	250	255	
LCD Driving Voltage	V_{LCD}	1/5 bias	4.6	-	10.0	V

Note

*1. The supply current value from VDD when the power condition is as follows
V_{DD} = 5V, GND = 0V, V1=3.4V, V2=1.8V, V3=0.2V, V4=-1.4V, V5=-3V.

CHAPTER 2

Driver IC Function Description

KS0066 Driver IC
16com/40seg driver & controller for dot matrix LCD

System Interface

This chip has all two kinds interface type with MPU: 4-bit bus and 8-bit bus.
4-bit bus and 8-bit bus is selected by DL bit in the instruction register.

During read or white operation, two 8-bit registers are used. One is data register(DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.
Hence, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The instruction register(IR) is used only to store instruction code transferred from MPU, MPU can't use it to read instruction data.

To select register, use RS input pin in 4-bit/8-bit bus mode.

Table1. Various kinds of operations according to RS and R/W bits.

RS	R/W	Operation
0	0	Instruction write operation (MPU writes instruction code into IR)
0	1	Read Busy flag(DB7) and address counter (DB0-DB6)
1	0	Data write operation (MPU writes data into DR)
1	1	Data Read operation (MPU reads data from DR)

Busy Flag (BF)

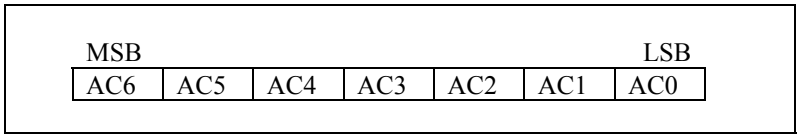
When BF = "High", it indicates the internal operation is being processed. So during this time the next instruction can't be accepted. BF can be read, when RS = Low and R/W = High(Read Instruction Operation), through DB7 port

Before executing the next instruction, be sure that BF is not High.

Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80*8 bits (80 characters).
DDRAM address is set in the address counter (AC) as a hexadecimal number. (refer to Figure 3.)

Figure 3. DDRAM Address



1. 1-line display
   In the case of 1 line display, the address range of DDRAM is 00H ~ 4FH.
2. 2-line display
   In the case of 2 line display , the address range of DDRAM is 00H - 27H, and 40H -67H.

Timing Generation Circuit

Timing generation circuit generates clock signals for the internal operations.

Address Counter (AC)

Address Counter (AC) stores DDRAM/CGRAM address, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = “Low”: and R/W = “High”, AC can be read through DB0 -DB6.

Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF at cursor position.

LCD Driver Circuit

LCD Driver circuit has 16 common and 40 segment signals for LCD driving.

Data from CGRAM/CGRAM is transferred to 40-bit segment latch serially, and then stored to 40-bit shift latch. When each common is selected by 16-bit common register, segment data also output through segment driver from 40-bit segment latch.

In case of 1-line display mode, COM1-COM8 have 1/8 duty or COM1-COM11 have a 1/11 duty. In a 2-line display mode, COM1-COM16 have a 1/16 duty ratio.

CGROM (Character Generation ROM)

CGROM has a 5*8-dot 208 character pattern, and a 5*11-dot 32 character pattern (Refer to Table 3)

CGRAM (Character Generation RAM)

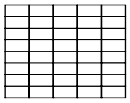
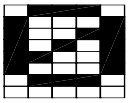
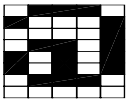
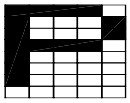
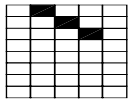
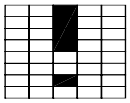
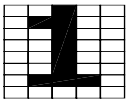
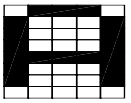
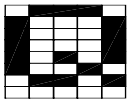
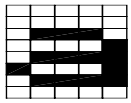
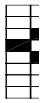
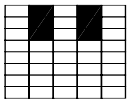
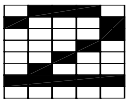
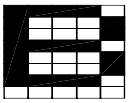
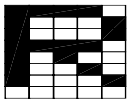
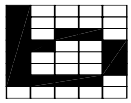
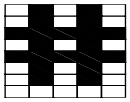
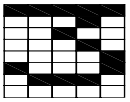
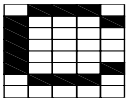
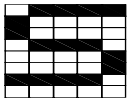
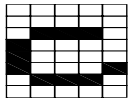
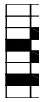
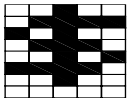
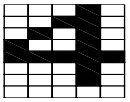
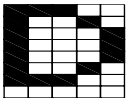
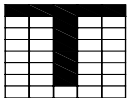
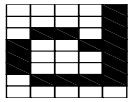
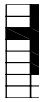
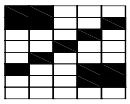
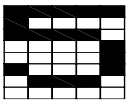
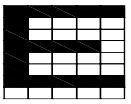
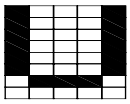
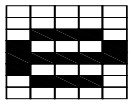
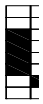
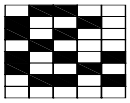
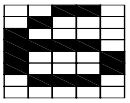
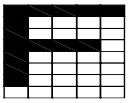
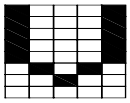
CGRAM has up to 5*8-dot 8 characters. By writing font data to CGRAM, user defined character can be used. (Refer to Table 2)

Table 2. Relationship between character code(DDRAM) and character pattern(CGRAM)

Character Code (DDRAM data)								CGRAM address						CGRAM data								Pattern
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	number
0	0	0	0	X	0	0	0	0	0	0	0	0	0	X	X	X	0	①	①	①	0	pattern 1
											0	0	1				①	0	0	0	①	
											0	1	0				①	0	0	0	0	
											0	1	1				①	①	①	①	①	
											1	0	0				①	0	0	0	①	
											1	0	1				①	0	0	0	①	
											1	1	0				①	0	0	0	①	
											1	1	1				0	0	0	0	0	
				:						:						:						:
0	0	0	0	X	1	1	0	1	1	0	0	0	0	X	X	X	0	①	①	①	0	pattern 7
											0	0	1				①	0	0	0	①	
											0	1	0				①	0	0	0	0	
											0	1	1				①	0	①	①	①	
											1	0	0				①	0	0	0	①	
											1	0	1				①	0	0	0	①	
											1	1	0				0	①	①	①	①	
											1	1	1				0	0	0	0	0	
0	0	0	0	X	1	1	1	1	1	1	0	0	0	X	X	X	①	0	0	0	①	pattern 8
											0	0	1				①	0	0	0	①	
											0	1	0				①	0	0	0	①	
											0	1	1				①	①	①	①	①	
											1	0	0				①	0	0	0	①	
											1	0	1				①	0	0	0	①	
											1	1	0				①	0	0	0	①	
											1	1	1				0	0	0	0	0	

* "X": don't care

Table 3. Character Generator ROM (KS0066-00)

Upper 4bit / Lower 4bit	LLLL	LLHL	LLHH	LHLL	LHLH	LHHL	L
LLLL	CG RAM (1)						
LLLH	(2)						
LLHL	(3)						
LLHH	(4)						
LHLL	(5)						
LHLH	(6)						
LHHL	(7)						
LHHH	(8)						
HLLL	(1)						
HLLH	(2)						
HLHL	(3)						
HLHH	(4)						
HHLL	(5)						
HHLH	(6)						
HHHL	(7)						
HHHH	(8)						

CHAPTER 3

Instruction Description

Outline

To overcome the speed difference between internal clock of KS0066 and MPU clock, KS0066 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. (refer to Table 5) Instructions can be divided largely four kinds:

1. KS0066 function set instructions (set display methods, set data length, etc.)
2. address set instructions to internal RAM
3. data transfer instructions with internal RAM
4. others

The address of internal RAM is automatically increased or decreased by 1.

***Note**
During internal operation, Busy flay(DB7) is read High. Busy Flag check must precede the next instruction. When you make a MPU program with checking the Busy Flag(DB7), it must be necessary 1/2Fosc for executing the next instruction by falling E signal after the Busy Flag(DB7) goes to “Low”.

Table 5. Instruction Set

Instruction	Instruction Code										Description	Execution Time (fosc= 270kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRAM, and set DDRAM address to “00H” from AC.	1.52ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction. I/D=”1”: increment, I/D=”0”: decrement and display shift enable bit. SH=”1”: make entire display shift of all lines during DDRAM write. SH=”0”: display shift disable	37us
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink on/off D=”1”: display on, D=”0”: display off, C=”1”: cursor on, C=”0”: cursor off, B=”1”: blink on, B=”0”: blink off.	37us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	Cursor or display shift, S/C=”1”: display shift, S/C=”0”: cursor shift, R/L=”1”: shift to right, R/L=”0”: shift to left.	37us
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length DL=”1”: 8-bit DL=”0”: 4-bit N=”1”: 2-line display N=”0”: 1-line.display F=”0” 5*7-dot F=”1” 5*10-dot	37us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	37us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	37us
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Can be known whether during internal operation or not by reading BF. The contents of address counter can also be read. BF=”1”: busy state, BF=”0”: ready state.	0us
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43us
Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	43us

***Note:**

1. When an MPU program with Busy Flag(DB7) checking is made, 1/2 fosc is necessary for executing the next instruction by the “E” signal after the Busy Flag (DB7) goes to “Low”.
2. “X” Don’t care.

Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter). Return cursor to the original status, hence, bring the cursor to the left edge on first line of the display. Entry mode is set to increment mode (I/D = “1”)

Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return Home is cursor return home instruction.

Set DDRAM address to “00H” into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1/D	SH

Set the moving direction of cursor and display.
1/D : Increment / decrement of DDRAM address (cursor or blink)
When 1/D = “High”, cursor/blink moves to right and DDRAM address is increased by 1.
When 1/D = “Low”, cursor/blink moves to left and DDRAM address is decreased by 1.
*CGRAM operates the same as DDRAM, when read from or write to CGRAM.

SH: Shift of entire display
When SH = “High”, after DDRAM write, the entire display of all lines is shifted to the right (1/D= “0”) or to the left (1/D = “1”). But it will seem as if the cursor does not move.
When SH = “Low”, or DDRAM read, or CGRAM read/write operation, shift of entire display is not performed.

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D : Display ON/OFF control bit
When D = “High”, entire display is turned on.
When D = “Low”, display is turned off, but display data is remained in DDRAM.

C : Cursor ON/OFF control bit
When C= “High”, cursor is turned on.
When C= “Low’, Cursor is disappeared in current display, but 1/D register remains its data.

B : Cursor Blink ON/OFF control bit
When B = “High”, cursor blink is on, that performs alternate between all the high data and display character at the cursor position. if fosc has 270 kHz frequency, blinking has 370 ms interval.
When B = “Low”, blink is off.

Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	S/C	R/L	-	-

Without writing or reading of display data, shift right/left cursor position or display.
This instruction is used to correct or search display data. (Refer to Table 4)
During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line.
Note that display shift is performed simultaneously in all the line.
When displayed data is shifted repeatedly, each line shifted individually.
When display shift is performed, the contents of address counter are not changed.

Table 6. Shift Patterns According To S/C And R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL : Interface data length control bit
When DL = “High”, it means 8-bit bus mode with MPU.
When DL = “Low”, it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
In 4-bit bus mode, it is required to transfer 4-bit data two times.

N : Display line number control bit
When N = “Low”, it means 1-line display mode.
When N = “High”, 2-line display mode is set.

F: Display font type control bit
When F= “0”, 5*8 dots format display mode.
When F= “1”, 5*11 dots format display mode.

Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM Address to AC.
This instruction makes CGRAM data available from MPU.

Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction makes CGRAM data available from MPU.
In 1-line display mode (N=0) DDRAM address is from “00H” to “4FH”.
In 2-line display mode (N=1), DDRAM address is from “00H” to “27H” in the 1st line, from “40H” to “67H” in the 2nd line.

Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KSOO66 is in internal operation or not. If the resultant BF is High, the internal operation is in progress and you have to wait until BF to be Low. Then the next instruction can be performed. In this instruction you can read the value of address counter.

Write Data To RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, and CGRAM is set by the previous address set instruction : DDRAM address set, and CGRAM address set. RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

Read Data From RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, as the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, the correct RAM data can be from the second, but the first data would be incorrect, as there is no time margin to transfer RAM data. In DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction ; it also transfer RAM data to output data register.

After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

*In case of RAM write operation, AC is increased/decreased by 1 as in read operation after this. In this time, AC indicates the next address position, but you can read only the previous data can only be read by read instruction.

CHAPTER 4

Interface With MPU

KS0066 can transfer data in bus mode (4-bit or 8-bit) with MPU. Hence, both types of 4 or 8-bit MPU can be used.
In case of 4-bit bus mode, data transfer is performed by twice to transfer 1 byte data.

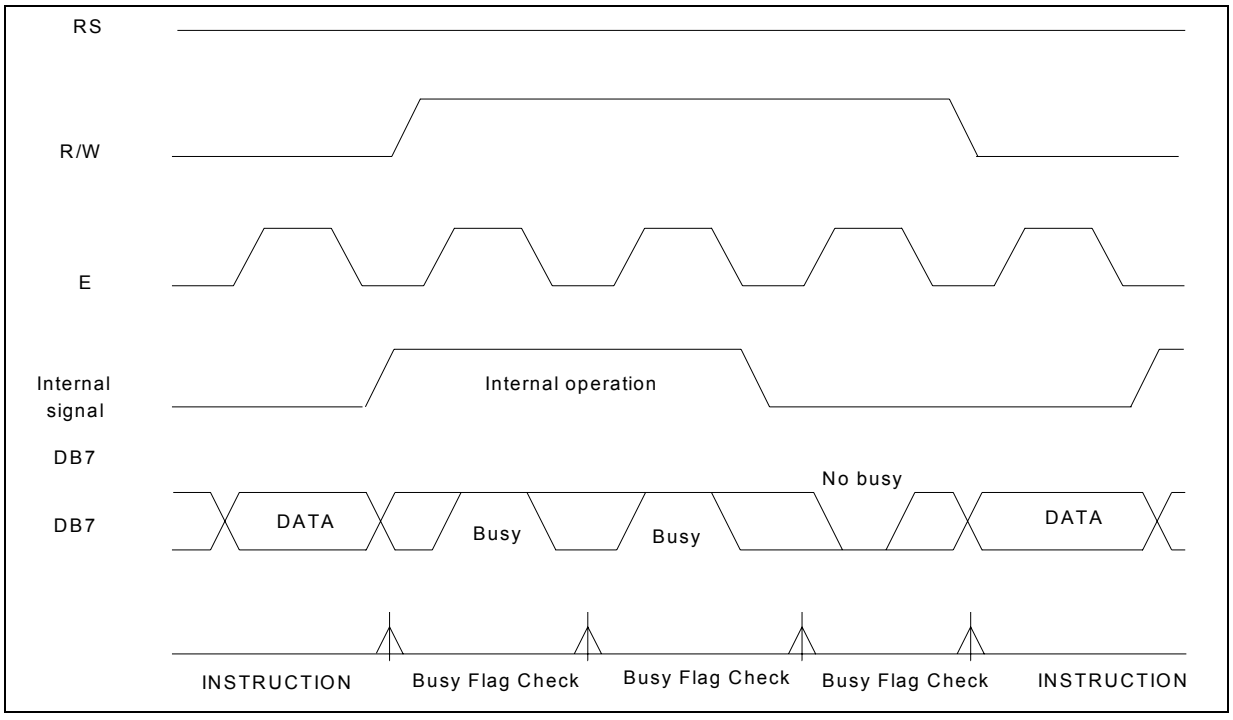
1. When interfacing data length are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus. At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4-DB7) are transferred, and then lower 4-bit(in case of 8-bit bus mode, the contents of DB0-DB3) are transferred. So transfer is performed by twice. Busy Flag outputs “high” after the second transfer is ended.
2. When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.

Interface With 8-bit MPU

If 8-bit MPU is used, transfer is performed all at once through 8 ports, from DB0 to DB7.

Example of timing sequence is shown below.

Figure 4. Example of 8-bit Bus Mode Timing Sequence

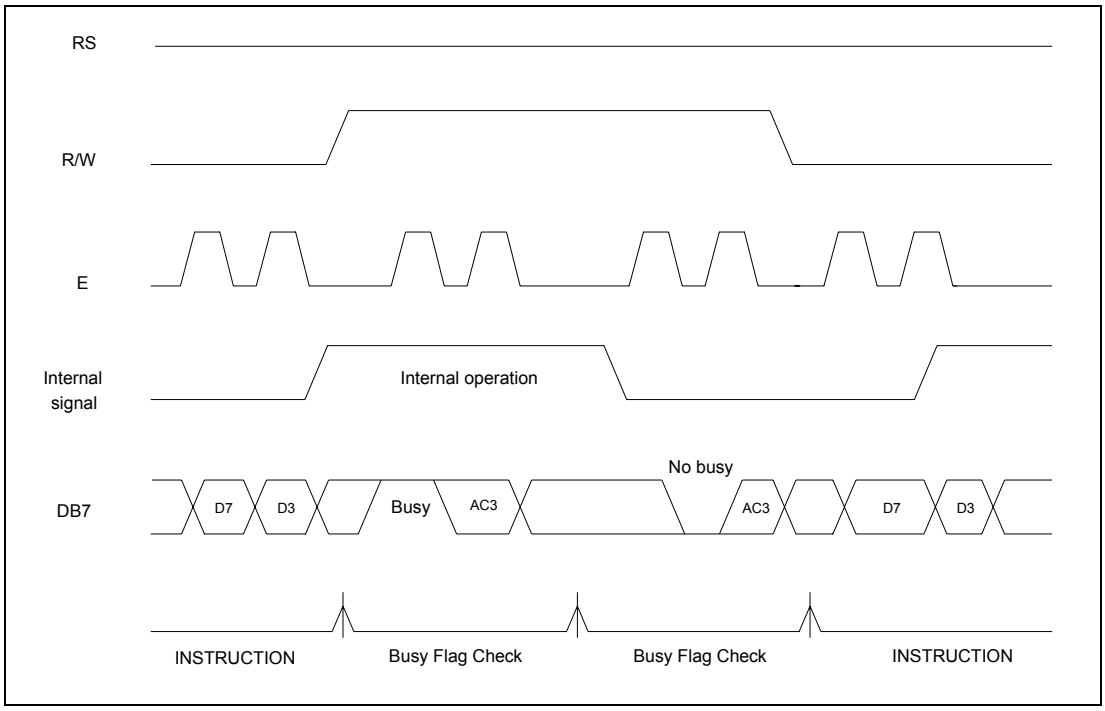


Interface with 4-bit MPU

When interfacing data length are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus. At first, higher 4-bit (in case of 8-bit bus mode, the contents of DB4-DB7) are transferred, and then the lower 4-bit (in case of 8-bit bus mode, the contents of DB0-DB3) are transferred. So transfer is performed in two parts. Busy Flag outputs "1" after the second transfer are ended.

Example of timing sequence is shown below.

Figure 5. Example of 4-bit Bus Mode Timing Sequence



AC ELECTRICAL CHARACTERISTICS

(VDD = +5V±10%, Ta=-30 to +85℃)

Mode	Item	Symbol	Min	Typ	Max	Unit
Write Mode (refer to Fig-6)	E Cycle Time	tc	500	-	-	ns
	E Rise/Fall Time	t_R, t_F	-	-	20	
	E Pulse Width (High, Low)	t_W	230	-	-	
	R/W and RS Setup Time	$t_{su}1$	40	-	-	
	R/W and RS Hold Time	t_H1	10	-	-	
	Data Setup Time	$t_{su}2$	60	-	-	
	Data Hold Time	t_H2	10	-	-	
Read Mode (refer to Fig-7)	E Cycle Time	tc	500	-	-	ns
	E Rise/Fall Time	t_R, t_F	-	-	20	
	E Pulse Width (High, Low)	t_W	230	-	-	
	R/W and RS Setup Time	t_{su}	40	-	-	
	R/W and RS Hold Time	t_H	10	-	-	
	Data Output Delay Time	t_D	-	-	120	
	Data Hold Time	t_{DH}	5	-	-	

Figure 6. Write Mode Timing Diagram

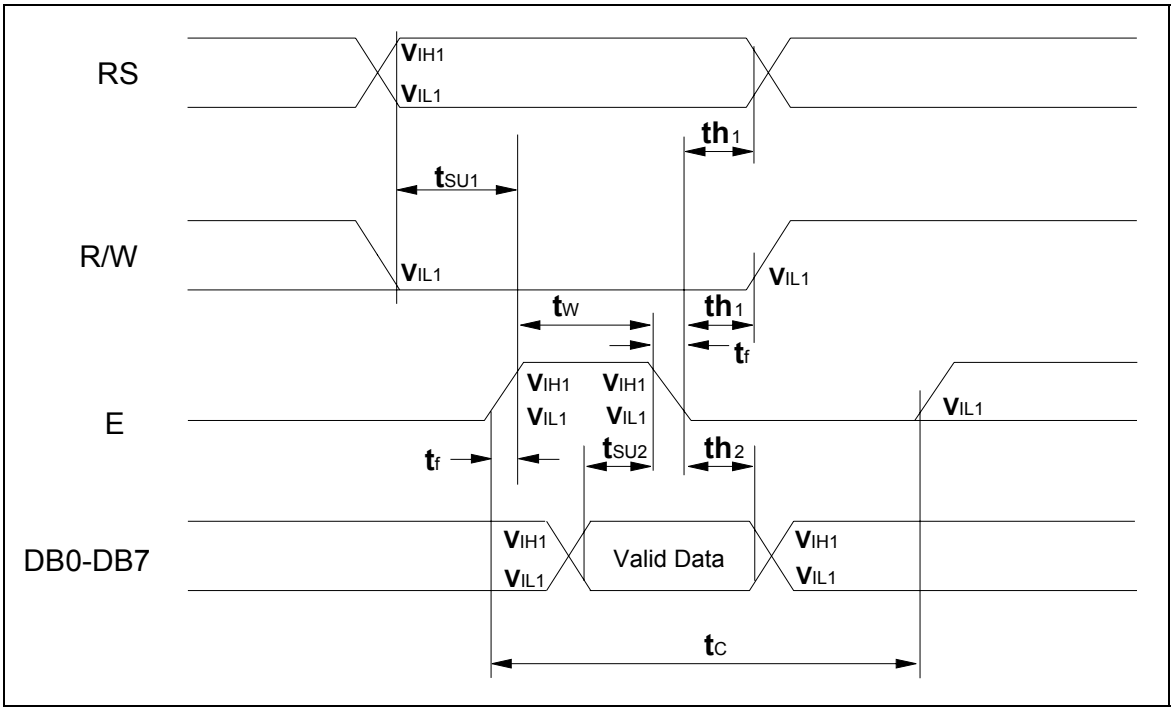


Figure 7. Read Mode Timing Diagram