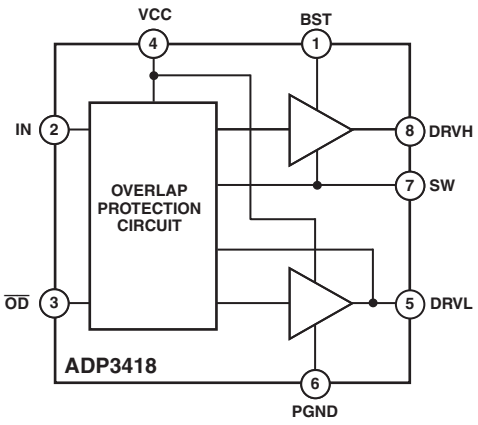
Dual Bootstrapped 12 V MOSFET Driver with Output Disable

ADP3418

FEATURES
All-In-One Synchronous Buck Driver
Bootstrapped High-Side Drive
1 PWM Signal Generates Both Drives
Anticross-Conduction Protection Circuitry
Output Disable Control Turns Off Both MOSFETs to Float Output per Intel® VRM 10 Specification

APPLICATIONS
Multiphase Desktop CPU Supplies
Single-Supply Synchronous Buck Converters

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3418 is a dual high voltage MOSFET driver optimized for driving two N-channel MOSFETs, which are the two switches in a nonisolated synchronous buck power converter. Each of the drivers is capable of driving a 3000 pF load with a 20 ns propagation delay and a 30 ns transition time. One of the drivers can be bootstrapped and is designed to handle the high voltage slew rate associated with floating high-side gate drivers. The ADP3418 includes overlapping drive protection to prevent shoot-through current in the external MOSFETs. The $\overline{OD}$ pin shuts off both the high-side and the low-side MOSFETs to prevent rapid output capacitor discharge during system shutdown.

The ADP3418 is specified over the commercial temperature range of 0°C to 85°C and is available in a thermally enhanced 8-lead SOIC package.

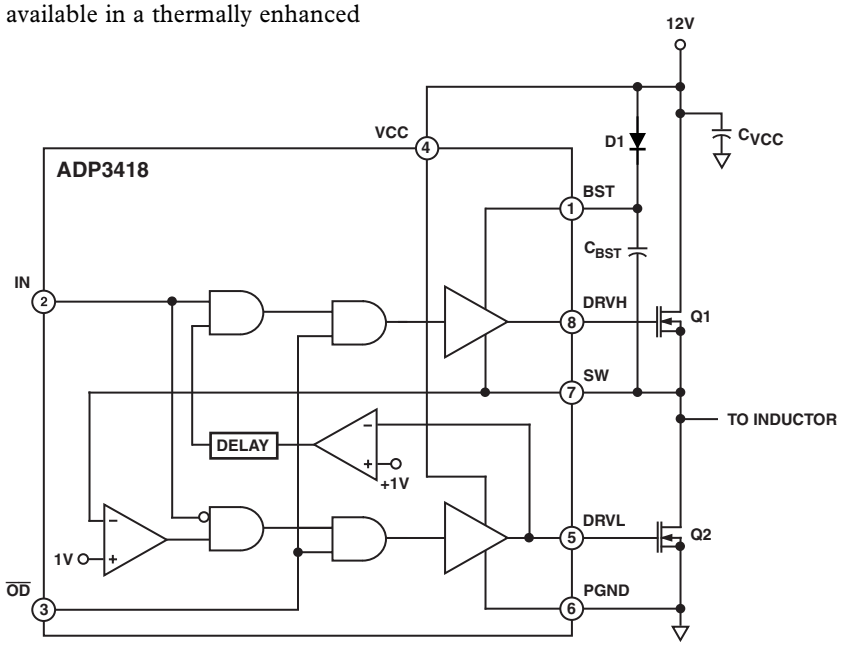


Figure 1. General Application Circuit

REV. 0

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ADP3418–SPECIFICATIONS[1] (VCC = 12 V, BST = 4 V to 26 V, T_A = 0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY						
Supply Voltage Range	V_{CC}		4.15		13.2	V
Supply Current	I_{SYS}	BST = 12 V, IN = 0 V		3	6	mA
$\overline{OD}$ INPUT						
Input Voltage High			2.8			V
Input Voltage Low					0.8	V
Input Current			–1		+1	µA
Propagation Delay Time[2]	$t_{pdl\overline{OD}}$	See Figure 2		15	30	ns
	$t_{pdh\overline{OD}}$	See Figure 2		20	40	ns
PWM INPUT						
Input Voltage High			3.5			V
Input Voltage Low					0.8	V
Input Current			–1		+1	µA
HIGH-SIDE DRIVER						
Output Resistance, Sourcing Current		$V_{BST} - V_{SW}$ = 12 V		1.8	3.0	Ω
Output Resistance, Sinking Current		$V_{BST} - V_{SW}$ = 12 V		1.0	2.5	Ω
Transition Times[2]	t_{rDRVH}	See Figure 3, $V_{BST} - V_{SW}$ = 12 V, C_{LOAD} = 3 nF		35	45	ns
	t_{fDRVH}	See Figure 3, $V_{BST} - V_{SW}$ = 12 V, C_{LOAD} = 3 nF		20	30	ns
Propagation Delay[2, 3]	$t_{pdhDRVH}$	See Figure 3, $V_{BST} - V_{SW}$ = 12 V		40	65	ns
	$t_{pdlDRVH}$	$V_{BST} - V_{SW}$ = 12 V		20	35	ns
LOW-SIDE DRIVER						
Output Resistance, Sourcing Current				1.8	3.0	Ω
Output Resistance, Sinking Current				1.0	2.5	Ω
Transition Times[2]	t_{rDRVL}	See Figure 3, C_{LOAD} = 3 nF		25	35	ns
	t_{fDRVL}	See Figure 3, C_{LOAD} = 3 nF		21	30	ns
Propagation Delay[2, 3]	$t_{pdhDRVL}$	See Figure 3		30	60	ns
	$t_{pdlDRVL}$	See Figure 3		10	20	ns

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).

[2]AC specifications are guaranteed by characterization but not production tested.

[3]For propagation delays, t_{pdh} refers to the specified signal going high, and t_{pdl} refers to it going low.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

VCC . . . . . –0.3 V to +15 V
BST . . . . . –0.3 V to VCC + 15 V
BST to SW . . . . . –0.3 V to +15 V
SW
  DC . . . . . –5 V to +15 V
  <200 ns . . . . . –10 V to +15 V
DRVH . . . . . SW – 0.3 V to BST + 0.3 V
DRVL (<200 ns) . . . . . –2 V to VCC + 0.3 V
All Other Inputs and Outputs . . . . . –0.3 V to VCC + 0.3 V
Operating Ambient Temperature Range . . . . . 0°C to 85°C
Operating Junction Temperature Range . . . . . 0°C to 150°C
Storage Temperature Range . . . . . –65°C to +150°C

Junction-to-Air Thermal Resistance (θ_{JA})
  2-Layer Board . . . . . 123°C/W
  4-Layer Board . . . . . 90°C/W
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

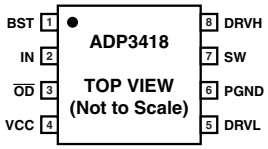
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all voltages are referenced to PGND.

ORDERING GUIDE

Model	Temperature Range	Package Option
ADP3418JR	0°C to 85°C	RN-8 (SOIC-8)

PIN CONFIGURATION

RN-8



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	BST	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between the BST and SW pins holds this bootstrapped voltage for the high-side MOSFET as it is switched. The capacitor should be chosen between 100 nF and 1 µF.
2	IN	Logic Level Input. This pin has primary control of the drive outputs.
3	$\overline{OD}$	Output Disable. When low, this pin disables normal operation, forcing DRVH and DRVL low.
4	VCC	Input Supply. This pin should be bypassed to PGND with ~1 µF ceramic capacitor.
5	DRVL	Synchronous Rectifier Drive. Output drive for the lower (synchronous rectifier) MOSFET.
6	PGND	Power Ground. Should be closely connected to the source of the lower MOSFET.
7	SW	This pin is connected to the buck-switching node, close to the upper MOSFET's source. It is the floating return for the upper MOSFET drive signal. It is also used to monitor the switched voltage to prevent turn-on of the lower MOSFET until the voltage is below ~1 V. Thus, according to operating conditions, the high-low transition delay is determined at this pin.
8	DRVH	Buck Drive. Output drive for the upper (buck) MOSFET.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3418 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended dation or loss of functionality.

TIMING CHARACTERISTICS

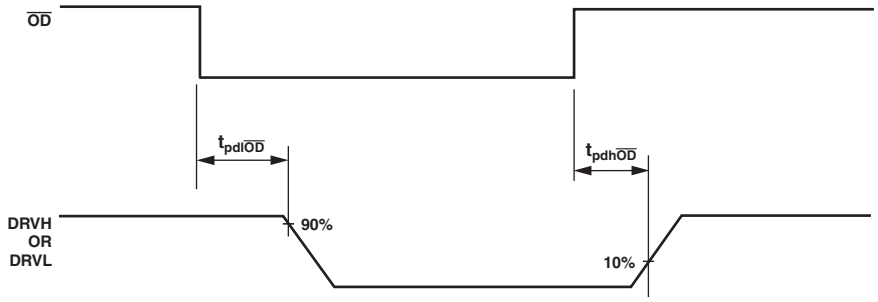


Figure 2. Output Disable Timing Diagram

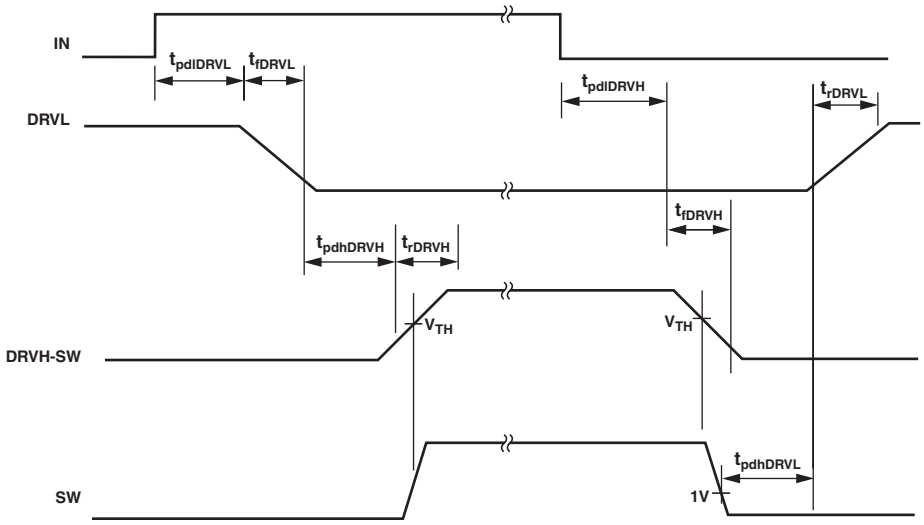
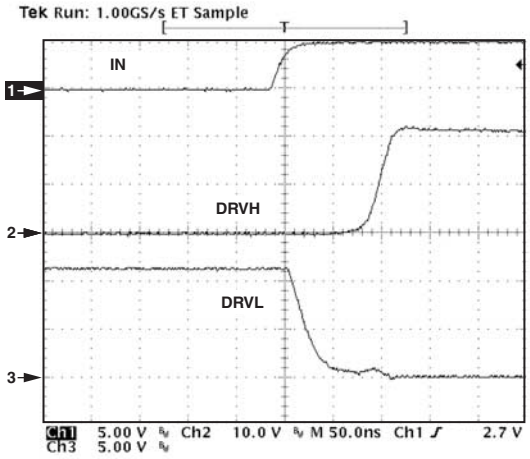
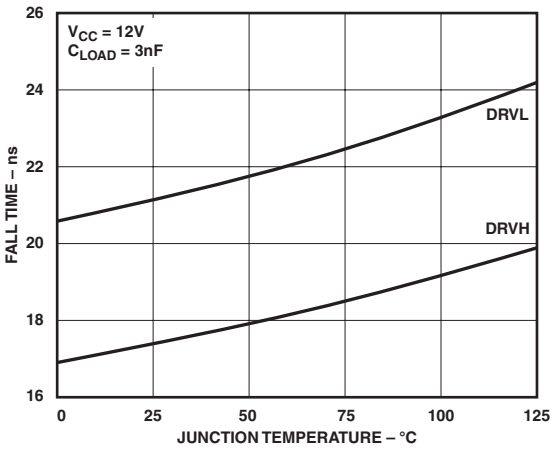


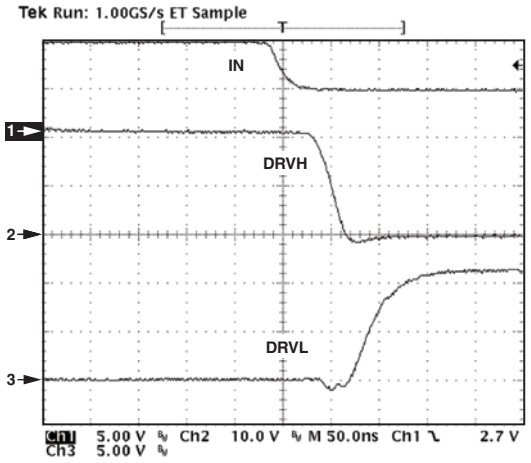
Figure 3. Nonoverlap Timing Diagram (Timing is referenced to the 90% and 10% points, unless otherwise noted.)



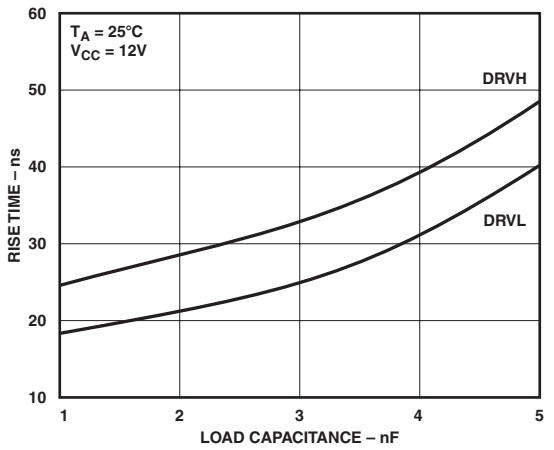
TPC 1. DRVH Rise and DRVL Fall Times



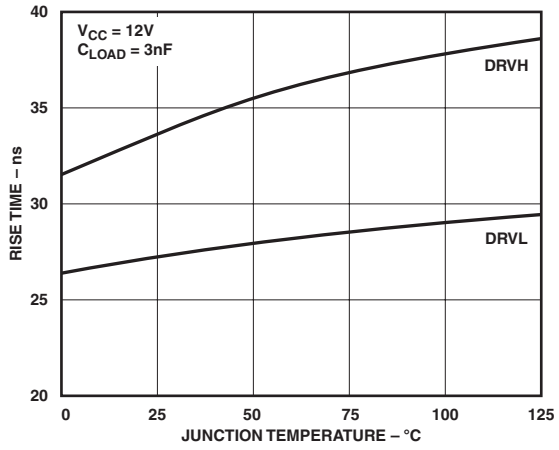
TPC 4. DRVH and DRVL Fall Times vs. Temperature



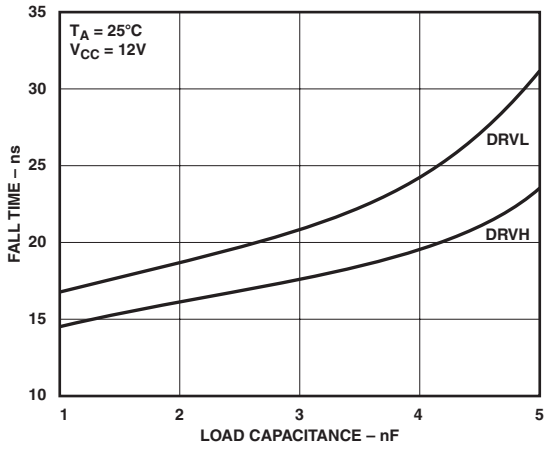
TPC 2. DRVH Fall and DRVL Rise Times



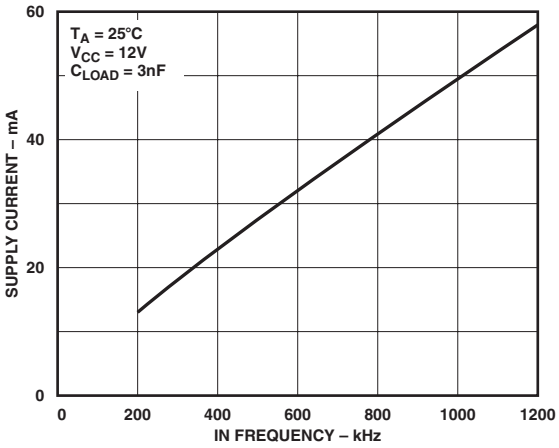
TPC 5. DRVH and DRVL Rise Times vs. Load Capacitance



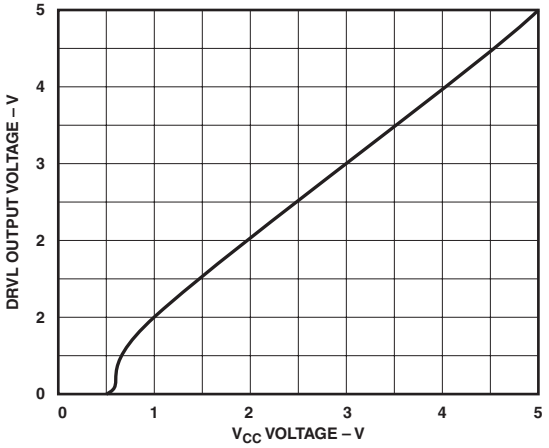
TPC 3. DRVH and DRVL Rise Times vs. Temperature



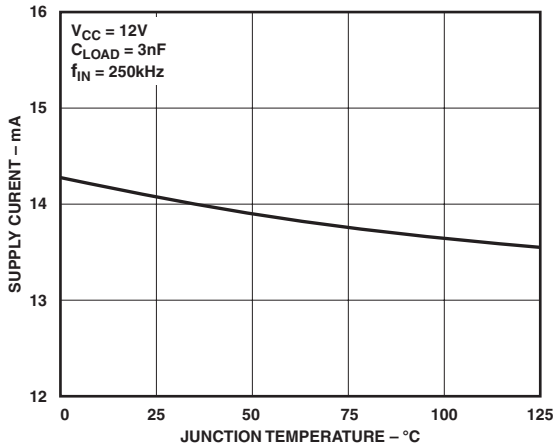
TPC 6. DRVH and DRVL Fall Times vs. Load Capacitance



TPC 7. Supply Current vs. Frequency



TPC 9. DRVL Output Voltage vs. Supply Voltage



TPC 8. Supply Current vs. Temperature

THEORY OF OPERATION

The ADP3418 is a dual MOSFET driver optimized for driving two N-channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each driver is capable of driving a 3 nF load at speeds up to 500 kHz.

A more detailed description of the ADP3418 and its features follows. Refer to the Functional Block Diagram.

Low-Side Driver

The low-side driver is designed to drive a ground-referenced low $R_{DS(ON)}$ N-channel MOSFET. The bias to the low-side driver is internally connected to the VCC supply and PGND.

When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the ADP3418 is disabled, the low-side gate is held low.

High-Side Driver

The high-side driver is designed to drive a floating low $R_{DS(ON)}$ N-channel MOSFET. The bias voltage for the high-side driver is developed by an external bootstrap supply circuit, which is connected between the BST and SW pins.

The bootstrap circuit comprises a diode, D1, and bootstrap capacitor, C_{BST}. When the ADP3418 is starting up, the SW pin is at ground, so the bootstrap capacitor will charge up to VCC through D1. When the PWM input goes high, the high-side driver will begin to turn on the high-side MOSFET, Q1, by pulling charge out of C_{BST}. As Q1 turns on, the SW pin will rise up to V_{IN}, forcing the BST pin to $V_{IN} + V_{C(BST)}$, which is enough gate-to-source voltage to hold Q1 on. To complete the cycle, Q1 is switched off by pulling the gate down to the voltage at the SW pin. When the low-side MOSFET, Q2, turns on, the SW pin is pulled to ground. This allows the bootstrap capacitor to charge up to VCC again.

The high-side driver's output is in phase with the PWM input. When the driver is disabled, the high-side gate is held low.

Overlap Protection Circuit

The overlap protection circuit prevents both of the main power switches, Q1 and Q2, from being on at the same time. This is done to prevent shoot-through currents from flowing through both power switches and the associated losses that can occur during their on-off transitions. The overlap protection circuit accomplishes this by adaptively controlling the delay from Q1's turn-off to Q2's turn-on and by internally setting the delay from Q2's turn-off to Q1's turn-on.

To prevent the overlap of the gate drives during Q1's turn-off and Q2's turn-on, the overlap circuit monitors the voltage at the SW pin. When the PWM input signal goes low, Q1 will begin to turn-off (after a propagation delay), but before Q2 can turn on, the overlap protection circuit waits for the voltage at the SW pin to fall from V_{IN} to 1 V. Once the voltage on the SW pin has fallen to 1 V, Q2 will begin turn-on. By waiting for the voltage on the SW pin to reach 1 V, the overlap protection circuit ensures that Q1 is off before Q2 turns on, regardless of variations in temperature, supply voltage, gate charge, and drive current.

To prevent the overlap of the gate drives during Q2's turn-off and Q1's turn-on, the overlap circuit provides an internal delay that is set to 50 ns. When the PWM input signal goes high, Q2 will begin to turn off (after a propagation delay), but before Q1 can turn on, the overlap protection circuit waits for the voltage at DRVL to drop to around 10% of V_{CC}. Once the voltage at DRVL has reached the 10% point, the overlap protection circuit will wait for a 20 ns typical propagation delay. Once the delay period has expired, Q1 will begin turn-on.

APPLICATION INFORMATION

Supply Capacitor Selection

For the supply input (V_{CC}) of the ADP3418, a local bypass capacitor is recommended to reduce the noise and to supply some of the peak currents drawn. Use a 4.7 µF, low ESR capacitor. Multilayer ceramic chip (MLCC) capacitors provide the best combination of low ESR and small size. Keep the ceramic capacitor as close as possible to the ADP3418.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and a diode, as shown in Figure 1. Selection of these components can be done after the high-side MOSFET has been chosen.

The bootstrap capacitor must have a voltage rating that is able to handle twice the maximum supply voltage. A minimum 50 V rating is recommended. The capacitance is determined using the following equation

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}} \quad (1)$$

where Q_{GATE} is the total gate charge of the high-side MOSFET, and ΔV_{BST} is the voltage droop allowed on the high-side MOSFET drive. For example, an IPD30N06 has a total gate charge of about 20 nC. For an allowed droop of 200 mV, the required bootstrap capacitance is 100 nF. A good quality ceramic capacitor should be used.

A small-signal diode can be used for the bootstrap diode due to the ample gate drive voltage supplied by V_{CC}. The bootstrap diode must have a minimum 15 V rating to withstand the maximum supply voltage. The average forward current can be estimated by

$$I_{F(AVG)} = Q_{GATE} \times f_{MAX} \quad (2)$$

where f_{MAX} is the maximum switching frequency of the controller. The peak surge current rating should be checked in-circuit, since this is dependent on the source impedance of the 12 V supply and the ESR of C_{BST}.

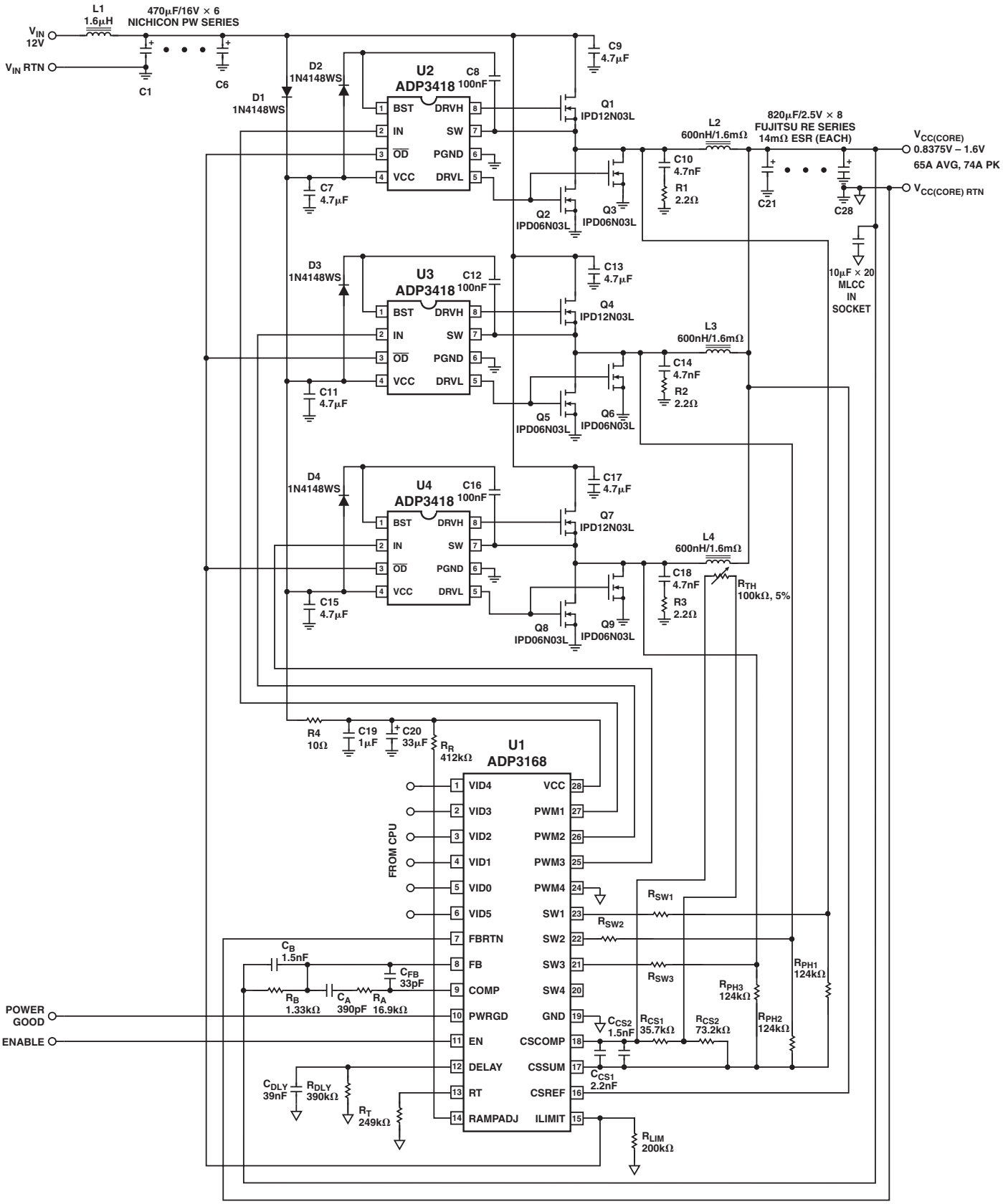


Figure 4. VRD 10 Compliant Intel CPU Supply Circuit

PC BOARD LAYOUT CONSIDERATIONS

Use the following general guidelines when designing printed circuit boards.

1. Trace out the high current paths and use short, wide (>20 mil) traces to make these connections.
2. Connect the PGND pin of the ADP3418 as close as possible to the source of the lower MOSFET.
3. The V_{CC} bypass capacitor should be located as close as possible to the VCC and PGND pins.
4. Use vias to other layers when possible to maximize thermal conduction away from the IC.

The circuit in Figure 4 shows how three drivers can be combined with the ADP3168 to form a total power conversion solution for generating $V_{CC(CORE)}$ for an Intel CPU that is VRD 10 compliant. Figure 5 gives an example of the typical land patterns based on the guidelines given previously. For more detailed layout guidelines for a complete CPU voltage regulator subsystem, refer to the ADP3168 data sheet.

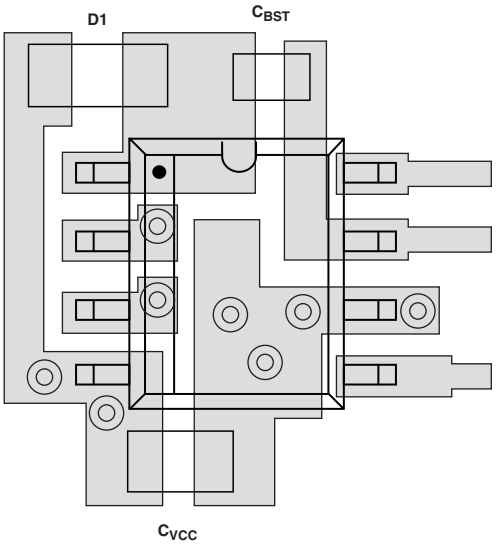
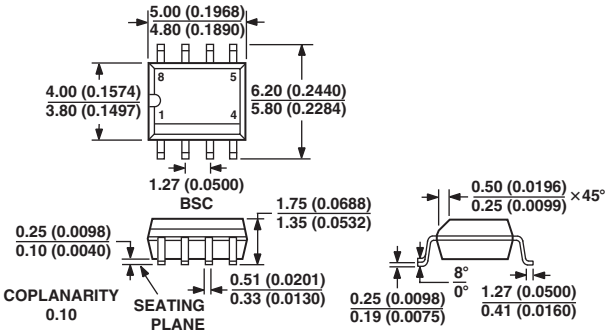


Figure 5. External Component Placement Example for the ADP3418 Driver

OUTLINE DIMENSIONS

8-Lead Standard Small Outline Package [SOIC]
(RN-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN