



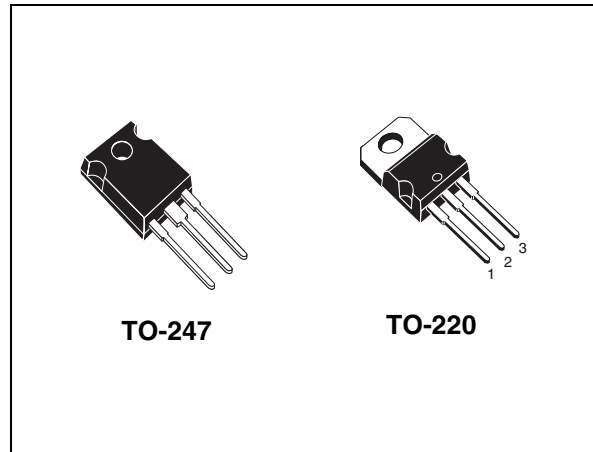
STGP30NC60W STGW30NC60W

N-channel 30A - 600V - TO-247 - TO-220
Ultra fast switching PowerMESH™ IGBT

General features

Type	V _{CES}	V _{CE(sat)} Max @25°C	I _C @100°C
STGW30NC60W	600V	< 2.5V	30A
STGP30NC60W	600V	< 2.5V	30A

- High frequency operation
- Lower C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)
- Very soft ultra fast recovery antiparallel diode
- Short circuit withstand time 10μs



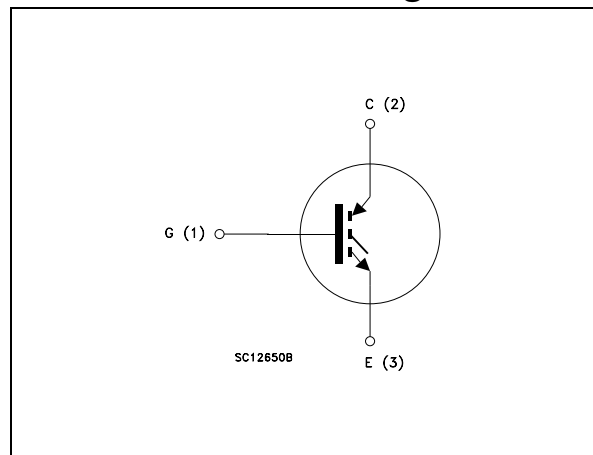
Description

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix "W" identifies a family optimized for very high frequency application.

Applications

- High frequency motor controls, inverters, ups
- HF, SMPS and PFC in both hard switch and resonant topologies

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STGW30NC60W	GW30NC60W	TO-247	Tube
STGP30NC60W	GP30NC60W	TO-220	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GS} = 0$)	600	V
I_C	Collector current (continuous) at 25°C	60	A
I_C	Collector current (continuous) at 100°C	30	A
$I_{CM}^{(1)}$	Collector current (pulsed)	200	A
V_{GE}	Gate-emitter voltage	± 20	V
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	200	W
T_{stg}	Storage temperature	– 55 to 150	°C
T_j	Operating junction temperature		
T_L	Maximum lead temperature for soldering purpose (1.6mm from case, for 10 sec.)	300	°C

1. Pulse width limited by max junction temperature

Table 2. Thermal resistance

			Min.	Typ.	Max.	Unit
Rthj-case	Thermal resistance junction-case				0.625	°C/W
Rthj-amb	Thermal resistance junction-ambient	TO-220 TO-247			62.5 50	°C/W °C/W

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 1\text{mA}$, $V_{GE} = 0$	600			V
$V_{CE(SAT)}$	Collector-emitter saturation voltage	$V_{GE}=15\text{V}$, $I_C= 20\text{A}$, $T_j= 25^{\circ}\text{C}$ $V_{GE}=15\text{V}$, $I_C= 20\text{A}$, $T_j= 125^{\circ}\text{C}$		2.1 1.8	2.5	V V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE}= V_{GE}$, $I_C= 250\mu\text{A}$	3.75		5.75	V
I_{CES}	Collector-emitter leakage current ($V_{CE} = 0$)	$V_{CE} = \text{Max rating}$, $T_c=25^{\circ}\text{C}$ $V_{CE} = \text{Max rating}$, $T_c=125^{\circ}\text{C}$			10 1	μA mA
I_{GES}	Gate-emitter leakage current ($V_{CE} = 0$)	$V_{GE} = \pm 20\text{V}$, $V_{CE} = 0$			± 100	nA
g_{fs}	Forward transconductance	$V_{CE} = 15\text{V}$, $I_C = 20\text{A}$		15		S

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{CE} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GE}=0$		2080 175 52		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	$V_{CE} = 390\text{V}$, $I_C = 20\text{A}$, $V_{GE} = 15\text{V}$, (see Figure 16)		102 17.5 47	140	nC nC nC
I_{CL}	Turn-Off SOA minimum current	$V_{clamp} = 480\text{V}$, $T_j = 150^{\circ}\text{C}$ $R_G = 10\Omega$, $V_{GE}= 15\text{V}$	200			A

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390V, I_C = 20A$		29.5		ns
t_r	Current rise time	$R_G = 10\Omega, V_{GE} = 15V,$		12		ns
$(di/dt)_{on}$	Turn-on current slope	$T_J = 25^\circ C$ (see Figure 15)		1640		A/ μs
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390V, I_C = 20A$		29		ns
t_r	Current rise time	$R_G = 10\Omega, V_{GE} = 15V,$		13.5		ns
$(di/dt)_{on}$	Turn-on current slope	$T_J = 125^\circ C$ (see Figure 15)		1600		A/ μs
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 390V, I_C = 20A,$		19.5		ns
$t_{d(off)}$	Turn-off delay time	$R_{GE} = 10\Omega, V_{GE} = 15V$		118		ns
t_f	Current fall time	$T_J = 25^\circ C$ (see Figure 17)		27		ns
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 390V, I_C = 20A,$		46		ns
$t_{d(off)}$	Turn-off delay time	$R_{GE} = 10\Omega, V_{GE} = 15V,$		151		ns
t_f	Current fall time	$T_J = 125^\circ C$ (see Figure 17)		38		ns

Table 6. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390V, I_C = 20A$		116		μJ
$E_{off}^{(2)}$	Turn-off switching losses	$R_G = 10\Omega, V_{GE} = 15V,$		181		μJ
E_{ts}	Total switching losses	$T_J = 25^\circ C$ (see Figure 17)		297		μJ
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390V, I_C = 20A$		239		μJ
$E_{off}^{(2)}$	Turn-off switching losses	$R_G = 10\Omega, V_{GE} = 15V,$		355		μJ
E_{ts}	Total switching losses	$T_J = 125^\circ C$ (see Figure 17)		594		μJ

1. E_{on} is the turn-on losses when a typical diode is used in the test circuit in figure 2. If the IGBT is offered in a package with a co-pak diode, the co-pak diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C)
2. Turn-off losses include also the tail of the collector current

2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

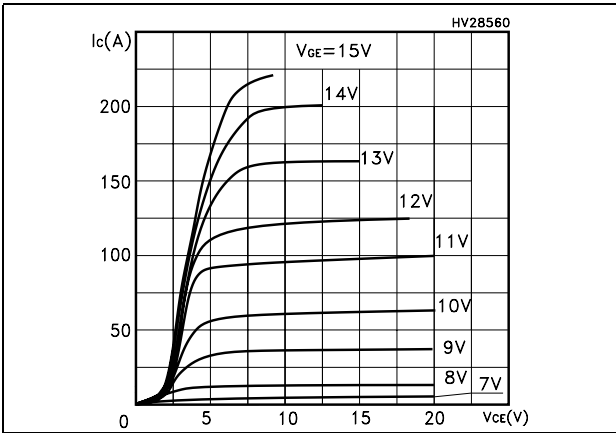


Figure 2. Transfer characteristics

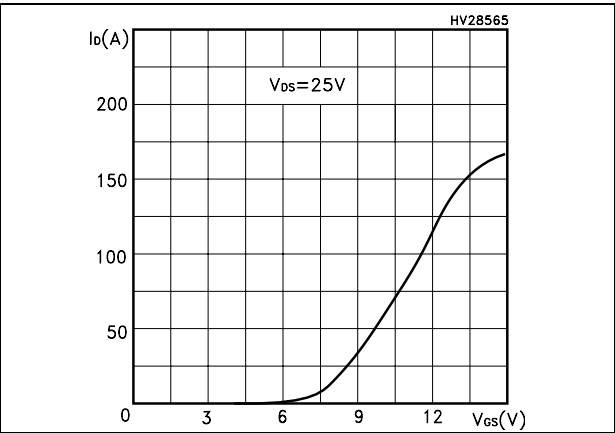


Figure 3. Transconductance

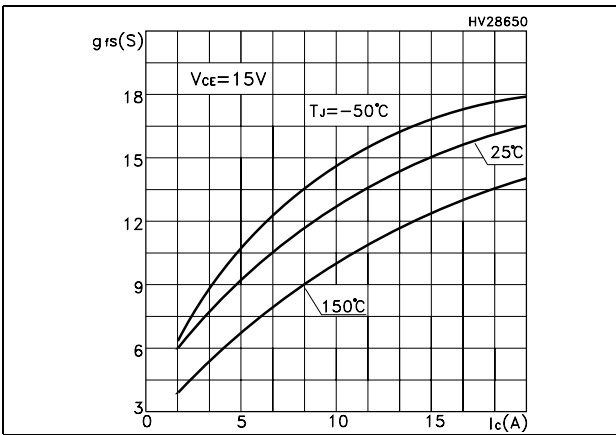


Figure 4. Collector-emitter on voltage vs temperature

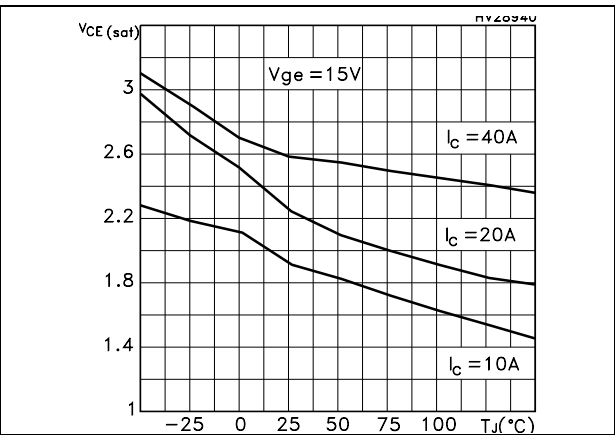


Figure 5. Gate charge vs gate-source voltage

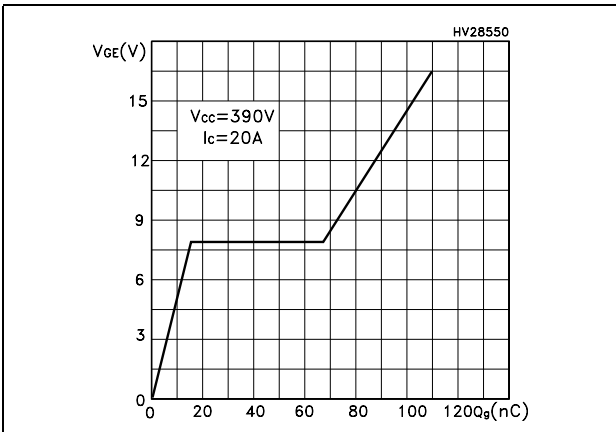


Figure 6. Capacitance variations

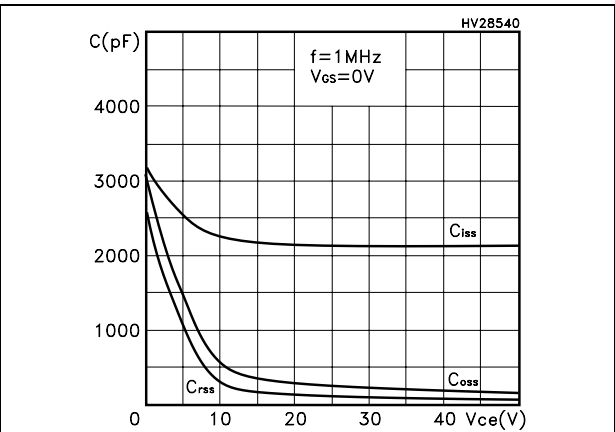


Figure 7. Normalized gate threshold voltage vs temperature

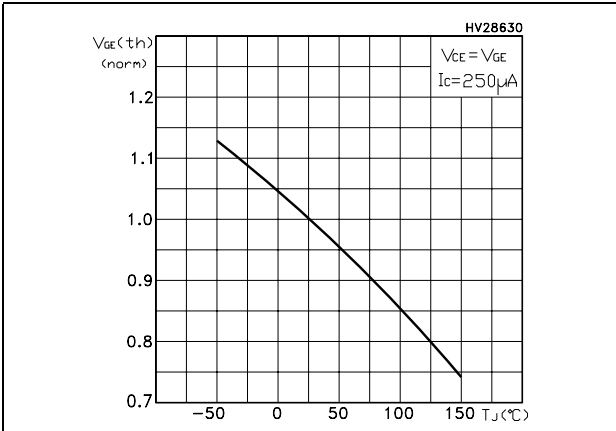


Figure 8. Collector-emitter on voltage vs collector current

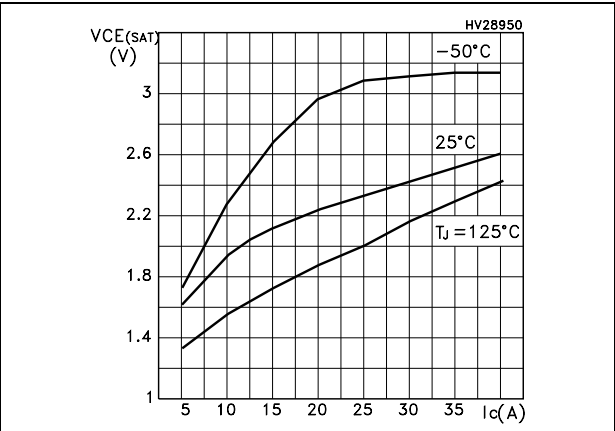


Figure 9. Normalized breakdown voltage vs temperature

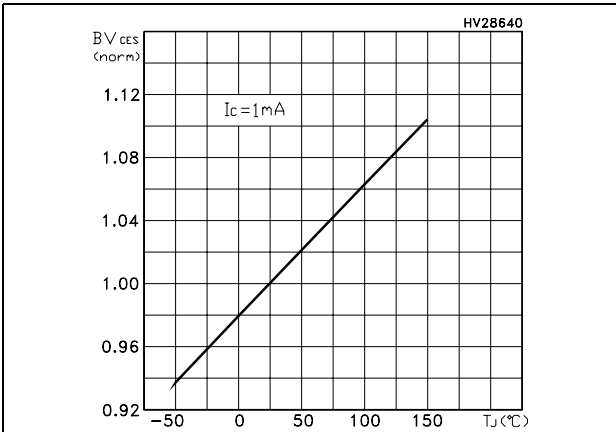


Figure 10. Switching losses vs temperature

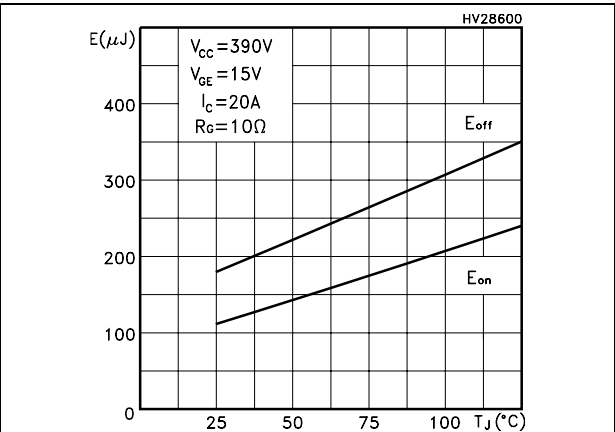


Figure 11. Switching losses vs gate resistance

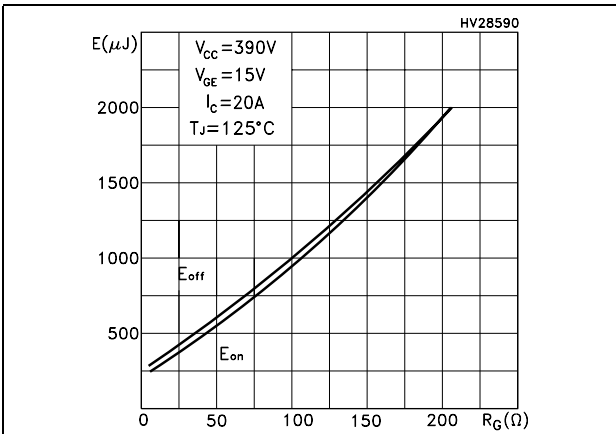


Figure 12. Switching losses vs collector current

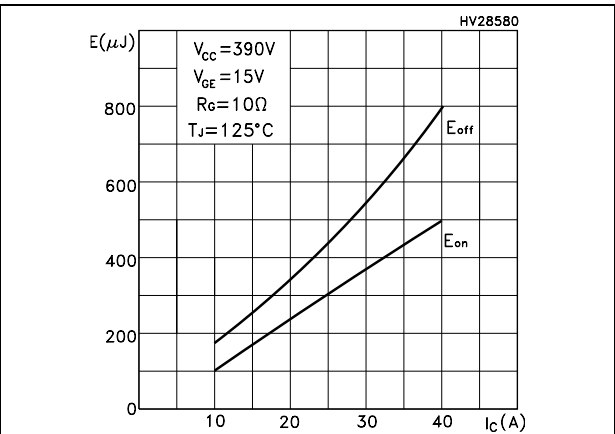


Figure 13. Thermal impedance

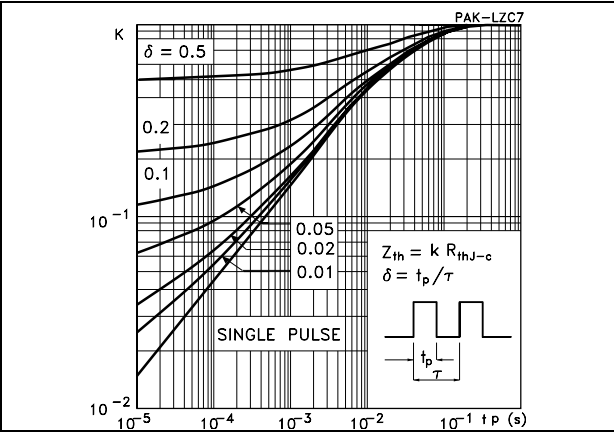
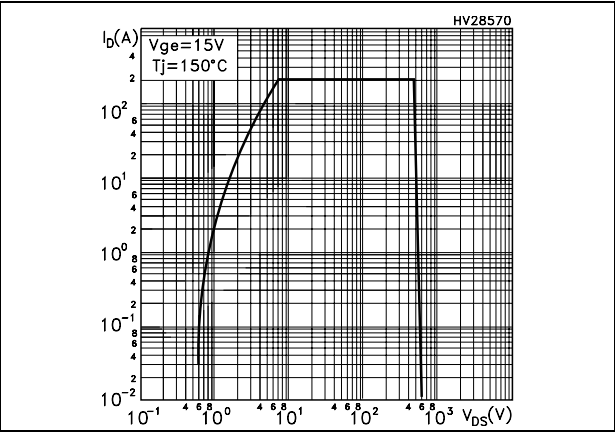


Figure 14. Turn-off SOA



3 Test circuit

Figure 15. Test circuit for inductive load switching

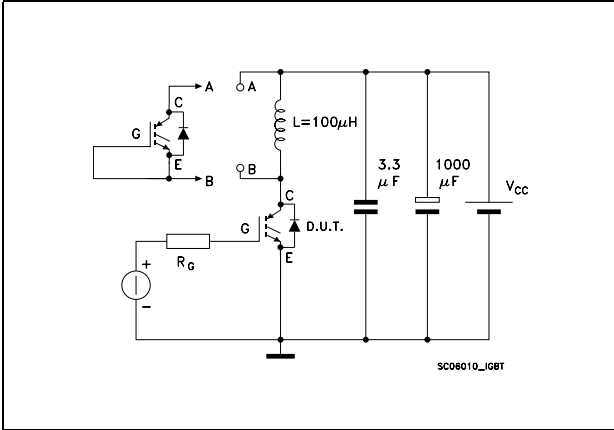


Figure 16. Gate charge test circuit

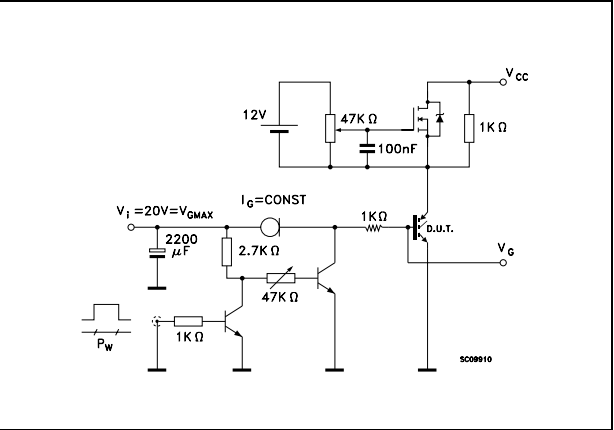


Figure 17. Switching waveform

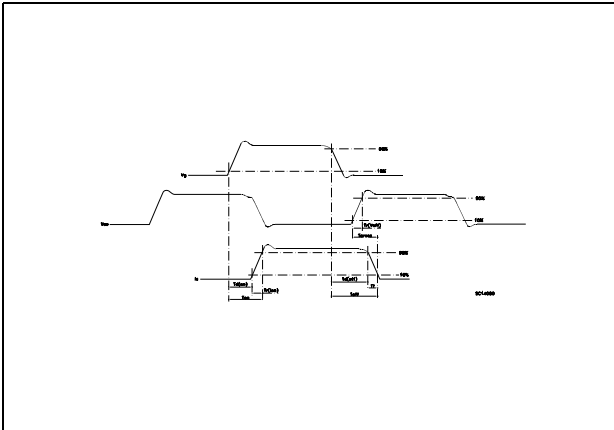
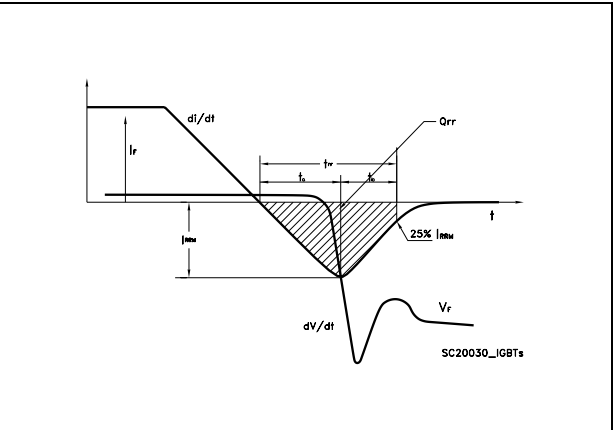


Figure 18. Diode recovery time waveform

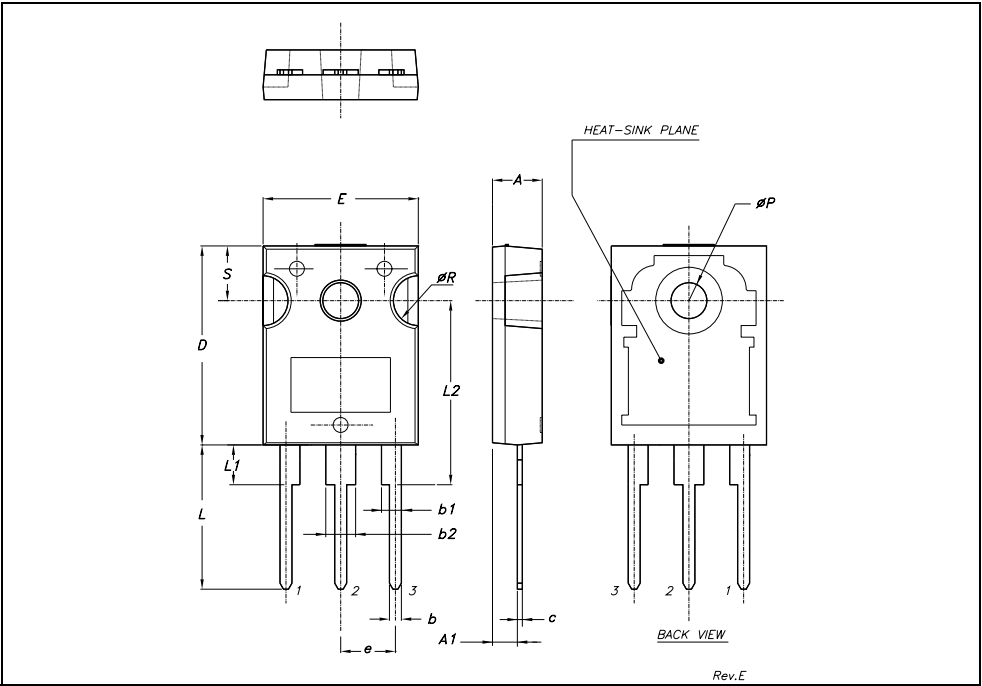


4 **Package mechanical data**

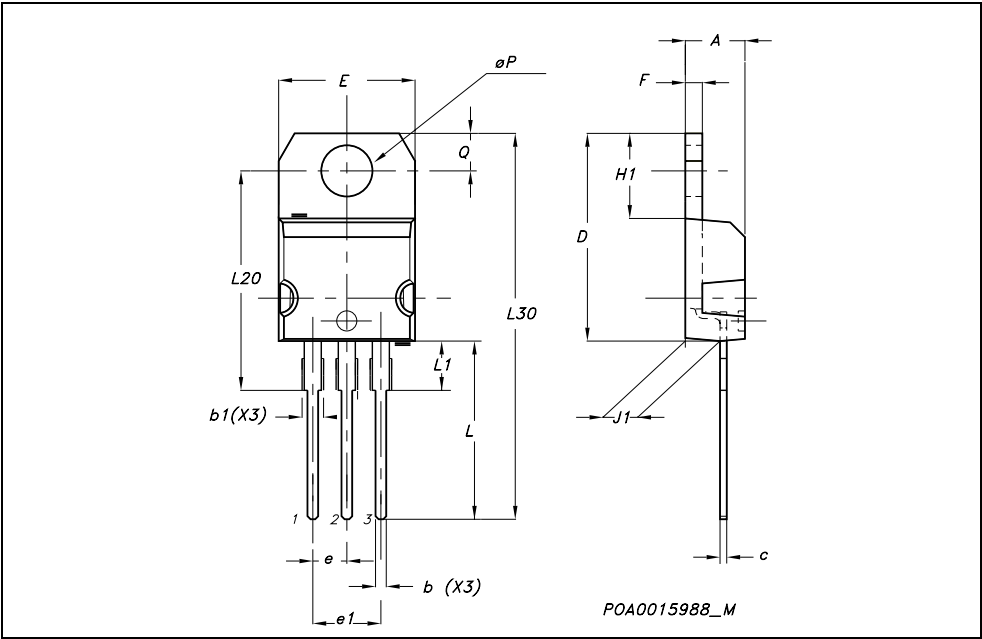
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



TO-220 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision history

Table 7. Revision history

Date	Revision	Changes
15-Sep-2005	1	Initial release.
04-Jan-2006	2	Inserted TO-220. Complete version
18-Dec-2006	3	The document has been reformatted

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