TIMER1 MODULE

Timer1 Module Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device data sheets listed below, the following clarifications and corrections should be noted. Any silicon issues related to the Timer1 Module will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

Device	Data Sheet	Device	Data Sheet	Device	Data Sheet	Device	Data Sheet
PIC12F609	DS41302	PIC16F716	DS41206	PIC18F2321	DS39689	PIC18F6585	DS30491
PIC12HV609		PIC16F737	DS30498	PIC18F4321		PIC18F6680	
PIC12F615		PIC16F747		PIC18F2331	DS39616	PIC18F8585	
PIC12HV615		PIC16F767		PIC18F2431		PIC18F8680	
PIC12F629	DS41190	PIC16F777		PIC18F4331		PIC18F24J10	DS39682
PIC12F675		PIC16F785	DS41249	PIC18F4431		PIC18F25J10	
PIC12F635	DS41232	PIC16HV785		PIC18F2439	DS30485	PIC18F44J10	
PIC16F636		PIC16F818	DS39598	PIC18F2539		PIC18F45J10	
PIC16F639		PIC16F819		PIC18F4439		PIC18F63J11	DS39774
PIC12F683	DS41211	PIC16F870	DS30569	PIC18F4539		PIC18F64J11	
PIC14000	DS40122	PIC16F871		PIC18F2455	DS39632	PIC18F65J11	
PIC16C62A	DS30234	PIC16F872	DS30221	PIC18F2550		PIC18F83J11	
PIC16C63		PIC16F873	DS30292	PIC18F4455		PIC18F84J11	
PIC16C64A		PIC16F874		PIC18F4550		PIC18F85J11	
PIC16C65A		PIC16F876		PIC18F2480	DS39637	PIC18F63J90	DS39770
PIC16C66		PIC16F877		PIC18F4480		PIC18F64J90	
PIC16C67		PIC16F873A	DS39582	PIC18F4580		PIC18F65J90	
PIC16C62B	DS35008	PIC16F874A		PIC18F2510	DS39636	PIC18F83J90	
PIC16C72A		PIC16F876A		PIC18F2610		PIC18F84J90	
PIC16C63A	DS30605	PIC16F877A		PIC18F4510		PIC18F85J90	
PIC16C65B		PIC16F882	DS41291	PIC18F4610		PIC18F65J10	DS39663
PIC16C73B		PIC16F883		PIC18F2520	DS39631	PIC18F65J15	
PIC16C74B		PIC16F884		PIC18F4520		PIC18F66J10	
PIC16C72	DS30390	PIC16F886		PIC18F2585	DS39625	PIC18F66J15	
PIC16C73A		PIC16F887		PIC18F2680		PIC18F67J10	
PIC16C74A		PIC16F913	DS41250	PIC18F4585		PIC18F85J10	
PIC16C76		PIC16F914		PIC18F4680		PIC18F85J15	
PIC16C77		PIC16F916		PIC18F2620	DS39626	PIC18F86J10	
PIC16C745	DS41124	PIC16F917		PIC18F4620		PIC18F85J15	
PIC16C765		PIC16F946				PIC18F87J10	

TIMER1 MODULE

Device	Data Sheet	Device	Data Sheet	Device	Data Sheet	Device	Data Sheet
PIC16C773	DS30275	PIC17C42A	DS30412	PIC18F4685	DS39761	PIC18F65J50	DS39775
PIC16C774		PIC17C43		PIC18F6390	DS39629	PIC18F66J50	
PIC16C923	DS30444	PIC17C44		PIC18F6490		PIC18F66J55	
PIC16C924		PIC17C752	DS30289	PIC18F8390		PIC18F67J50	
PIC16C925	DS39544	PIC17C756A		PIC18F8490		PIC18F85J50	
PIC16C926		PIC17C762		PIC18F6520	DS39609	PIC18F85J55	
PIC16F72	DS39597	PIC17C766		PIC18F6620		PIC18F87J50	
PIC16F73	DS30325	PIC18C242	DS39026	PIC18F6720		PIC18F66J11	DS39778
PIC16F74		PIC18C252		PIC18F8520		PIC18F66J16	
PIC16F76		PIC18C442		PIC18F8620		PIC18F67J11	
PIC16F77		PIC18C452		PIC18F8720		PIC18F86J11	
PIC16F87	DS30487	PIC18C601	DS39541	PIC18F6525	DS39612	PIC18F86J16	
PIC16F88		PIC18C801		PIC18F6621		PIC18F87J11	
PIC16F610	DS41288	PIC18C658	DS30475	PIC18F8525		PIC18F66J60	DS39762
PIC16HV610		PIC18C858		PIC18F8621		PIC18F66J65	
PIC16F616		PIC18F242	DS39564	PIC18F6527	DS39646	PIC18F67J60	
PIC16HV616		PIC18F252		PIC18F6622		PIC18F86J60	
PIC16F627A	DS40044	PIC18F442		PIC18F6627		PIC18F86J65	
PIC16F628A		PIC18F452		PIC18F6722		PIC18F87J60	
PIC16F648A		PIC18F248	DS41159	PIC18F8527		PIC18F96J60	
PIC16F630	DS40039	PIC18F258		PIC18F8622		PIC18F96J65	
PICF676		PIC18F458		PIC18F8627		PIC18F97J60	
PIC16F631	DS41262	PIC18F1220	DS39605	PIC18F8722			
PIC16F677		PIC18F1320					
PIC16F685		PIC18F1230	DS39758				
PIC16F687		PIC18F1330					
PIC16F689		PIC18F2220	DS39599				
PIC16F690		PIC18F2330					
PIC16F684	DS41202	PIC18F4220					
PIC16F688	DS41203	PIC18F4320					

1. Asynchronous Counter

When Timer1 is started or updated, the timer needs to see a falling edge from the external clock source before a rising edge can increment the counter. If writes to TMR1H and TMR1L are not completed while the external clock pulse is still high, Timer1 will miss counting the first clock pulse after the update.

One half of a 32.768 kHz external clock crystal period yields a 15.25 μs window to complete all writes to TMR1H and TMR1L (50% duty cycle). The number of instructions that can be executed within this window is dependent on FOSC, as shown in Table 1.

TABLE 1: FREQUENCY DEPENDENT INSTRUCTION EXECUTION AMOUNTS

FOSC	TCY (μs)	TCY within 15.25 μs
1 MHz	4	3
2 MHz	2	7
4 MHz	1	15
8 MHz	0.5	30
16 MHz	0.25	61
20 MHz	0.2	76
40 MHz (PIC18)	0.1	152

One of the following methods can be used to update Timer1 depending on whether all writes to TMR1H and TMR1L can or cannot be reliably completed before the clock pulse falling edge:

- If Timer1 *can* be reliably updated before the clock pulse falling edge occurs:

  Update TMR1H and TMR1L as needed.
- If Timer1 updates can *not* be reliably completed before the clock pulse falling edge occurs:
  1. Wait for TMR1L to increment.
  2. When an increment is detected, immediately update TMR1H and TMR1L as needed.

     Include the code between `RTCisr` and `Update`.

Code examples are given for the affected devices:

- PIC12/PIC14/PIC16 devices – Example 1
- PIC18 devices – Example 2

Both examples include code to wait for Timer1 to increment twice between the `RTCisr` and `Update` labels.

In PIC18 devices, it is not possible to reliably update Timer1 in a *low-priority* interrupt. A high-priority interrupt could occur at any time and unexpectedly delay the TMR1 update.

PIC18 devices also include Timer3 which is functionally identical to Timer1.

EXAMPLE 1: PIC12/PIC14/PIC16 INTERRUPT SERVICE ROUTINE

```
IntVector   code 0x004      ;   (3-4Tcy) fixed interrupt latency
    movwf   W_temp          ;   (1tcy) save W register contents
    movf    STATUS,W        ;   (1tcy) save STATUS register contents
    movwf   Status_temp     ;   (1tcy)
    BANKSEL PIR1            ;   (2tcy) select correct SFR bank
    btfss   PIR1,TMR1IF     ;   (2tcy) did a Timer1 overflow occur?
    goto    NextISR         ;   (2tcy) no, check another interrupt source

; Insert the next 4 lines of code when TMR1 can not
; be reliably updated before clock pulse goes low
RTCisr:
    btfsc   TMR1L,0         ;   wait for TMR1L<0> to become clear
    goto    $-1             ;   may already be clear (loops for 0 to 30.5us)
    btfss   TMR1L,0         ;   wait for TMR1L<0> to become set
    goto    $-1             ;   (loops for 30.5us)

; If TMR1 update can be completed before clock pulse
; goes low, start update here
Update:
    bsf     TMR1H,7         ;   reload for a 1 second overflow
    bcf     PIR1,TMR1IF     ;   clear flag
    incf    Seconds,F       ;   record second
    goto    Exit            ;   return from interrupt

NextISR:    ; Another interrupt source...
    ....                    ;   code for other interrupts, if needed
    goto    Exit            ;   return from interrupt

Exit:
    movf    status_temp,w   ;   retrieve copy of status register
    movwf   status          ;   restore pre-isr status register contents
    swapf   w_temp,f
    swapf   w_temp,w        ;   restore pre-isr w register contents
    retfie
```

EXAMPLE 2: PIC18 HIGH-PRIORITY INTERRUPT SERVICE ROUTINE

```
HIntVector  code 0x0008     ;   (3-4Tcy), fixed interrupt latency
    goto    HighISR         ;   (3Tcy) jump to high priority ISR code

            code            ;   unprotected code space
HighISR:
    btfss   PIR1,TMR1IF     ;   (1Tcy) TMR1 overflow?
    goto    NextISR         ;   (2Tcy) No, check another interrupt source

;   Insert the next 4 lines of code when TMR1 can not
;   be reliably updated before clock pulse goes low
RTCisr:
    btfsc   TMR1L,0         ;   wait for TMR1L<0> to become clear
    bra     $-2             ;   may already be clear (loops for 0 to 30.5us)
    btfss   TMR1L,0         ;   wait for TMR1L<0> to become set
    bra     $-2             ;   (loops for 30.5us)

; If TMR1 update can be completed before clock pulse
; goes low, start update here
Update:
    bsf     TMR1H,7         ;   reload for next 1 second overflow
    bcf     PIR1,TMR1IF     ;   clear flag
    incf    Seconds,F       ;   record second
    retfie  FAST

NextISR:                    ;   Another interrupt source...
    ....                    ;   code for other interrupts, if needed
    retfie  FAST
```

REVISION HISTORY

Rev A Document (7/2007)
Initial release of this errata.

NOTES:

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