## 1.5-GHZ PRESCALER FOR FREQUENCY METERS

Most simple and inexpensive frequency meters have a maximum input frequency of 10 MHz or 100 MHz. Decimal prescalers that enable frequencies in the gigahertz ranges to be measured are expensive and usually require a special type of RF preamplifier. Not so with the SDA4212 from Siemens, which offers new ways of building a compact, low-cost 1.5-GHz divide-by-100 prescaler.

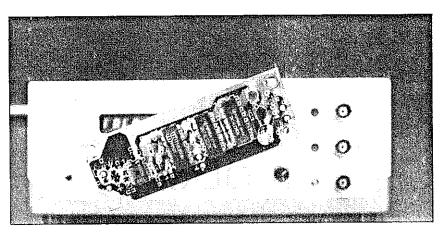
## R. Bönsch

The SDA4212 features a high input sensitivity and excellent large-signal behaviour Unlike many other prescalers, the SDA4212 does not require its input signal to be kept within certain limits for correct operation of the internal divider. Over the frequency range of 70 MHz to 1200 MHz, the SDA4212 accepts input signal levels between 5 mV and 400 mV (typical values) The prototype circuit constructed on the printed-circuit board shown here has a frequency range of 20 MHz to 1,600 MHz

The internal structure of the SDA4212 is shown in Fig 1. The input circuit is formed by a difference amplifier. Next, a high-speed divider divides the signal either by 64 (pin 5 high') or 256 (pin 5 'low'). The ECL-level output signal (1 Vpp) is supplied at pin 6 or 7 by a symmetrical driver stage.

## Circuit description

The circuit diagram of the prescaler is given in Fig 2 The two Schottky diodes at the input protect the SDA4212 against ex-



cessive input voltages. The M (mode) input of the chip is tied to the positive supply line to achieve division by 64. The ECL-to-TTL level converter at the output of the SDA4212 is formed by LS-TTL gates N1, N2 and N3. The first gate, N1, is an AC-coupled linear amplifier. Its gain is set to about 10 times with the aid of feedback resistors R1 and R2. Gate N2 provides fur-

ther amplification and a well-defined TIL signal. The ECL-to-TIL level convertor used here is easily reproduced, requires no adjustment and is hardly affected by changes in the ambient temperature.

The 74LS390 that follows the SDA4212 contains two divide-by-5 counters. The first QD output (pin 9) goes high on the fifth input pulse. At the same time, the input signal of the 74LS390 appears inverted at the output of N5. This means that gate N6 is blocked for one-fifth of the time and allows the signal to pass for four-fifths of the time. In other words: four of every five input pulses arrive at the input of the second divide-by-5 counter.

The above divide operation is duplicated in the second counter. Gates N5 and N7 are required to compensate signal delays in the dividers and to ensure that the 74LS390 can reach its maximum input frequency.

The output of the prescaler supplies a TTL signal whose frequency is

 $1/64 \times 4/5 \times 4/5 = 16/1600 = 1/100$ 

times the frequency of the input signal. It should be noted that a dual-rate counter such as the one applied here supplies an output signal whose mark-space ratio is irregular. Fortunately, this is not a problem for most frequency meters. The out-

ig 1 Block diagram of the SDA4212 from Siemens

ELEKTOR ELECTRONICS SEPTEMBER 1990

Fig

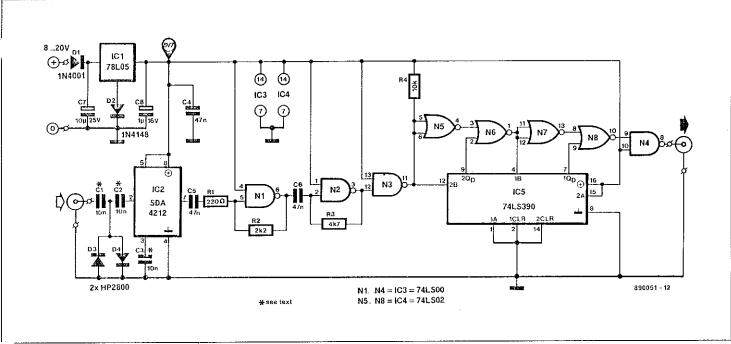
teg the volt inpi matect volt

Cc A i (SM prib

of 3

pon

shor inpu



2. Circuit diagram of the 1.5-GHz prescaler. Note the absence of an RF preamplifier ahead of the divider chip, IC2.

1 220Ω	
	R1
1 2k2	R2
1 4k7	R3 ::
1 10k	R4
Capacitors:	
3 10nF SMA	C1;C2;C3
1 47nF SMA	C4
2 47nF ceramic	C5;C6
1 10μF 25V radial	C7
1 1μF 16V radial	C8
Semiconductors:	
1 1N4001	D1
1 1N4148	D2
2 HP2800	D3;D4
78L05	IC <sub>1</sub>
1 SDA4212	IC2
1 74LS00	IC3

put signal may not be suitable for PLL-based circuits, however.

The prescaler is powered by a 5-V regulator Type 78L05 (IC1) Diode D2 at the common terminal ruises the output voltage to about 5.7 V to push the highest input frequency of the SDA4212 to the maximum specification Diode D1 protects the circuit against reverse supply voltages. The relatively low consumption of 30 to 50 mA enables the prescaler to be powered by a battery

## Construction

number of surface-mount assembly (5MA) parts are accommodated on the printed-circuit board (Fig. 3) to ensure the shortest possible connection between the input of the circuit and the SDA4212 The

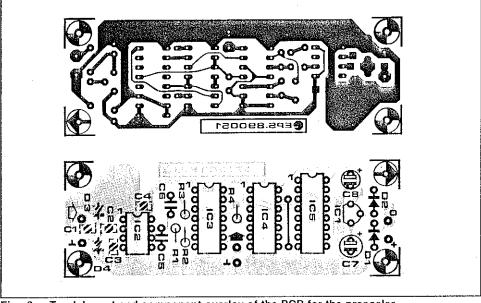


Fig. 3. Track layout and component overlay of the PCB for the prescaler.

SMA parts are fitted at the track side of the board

The board is single-sided with a relatively large unetched copper area around the SDA4212 to ensure adequate screening and decoupling of the high-frequency input signals. The SDA4212 must be soldered directly on to the PCB

Fit the completed circuit board in a small metal enclosure. The prescaler may be coupled to the circuit under test either

capacitively by means of a short wire, or inductively (at a low impedance) by means of a wire loop. Both methods require the prescaler to be located fairly near the circuit under test, but avoid the risk of signal attenuation by the capacitance of long (coaxial) test cables

